EE 323002

Lab 2 : Simulation with the Analog Design Environment

Version 1.0 (Sept 2023)

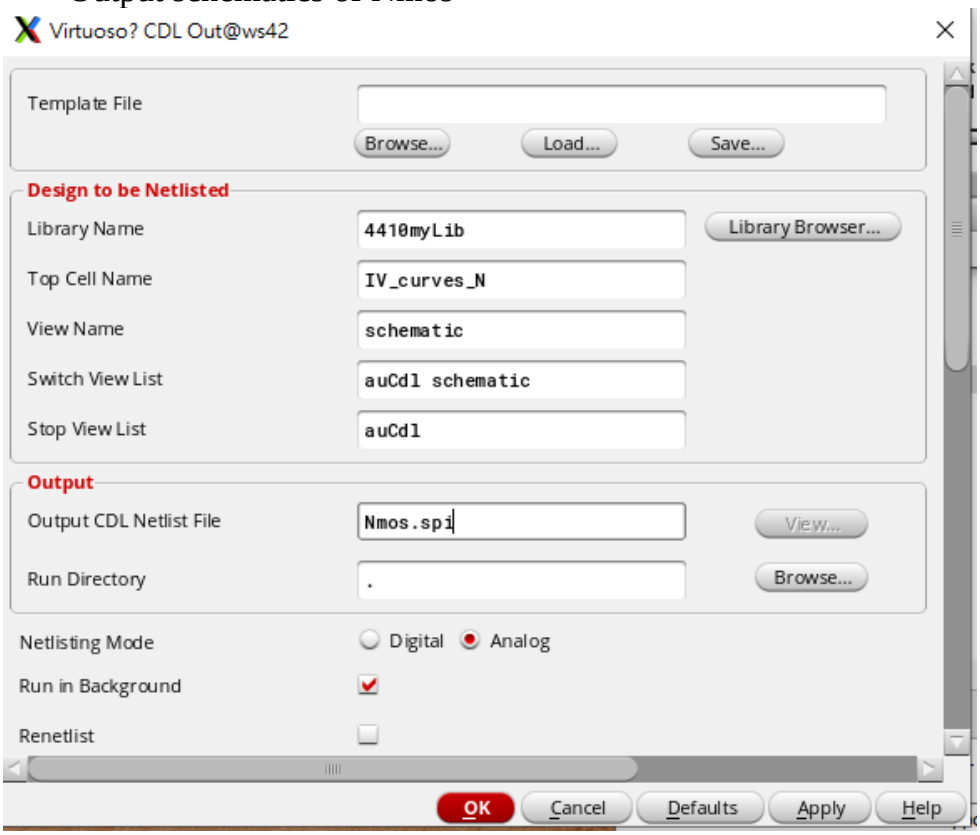
Hspice Circuit Simulator

I. Pmos and Nmos

In lab1-b,we draw schematics of Pmos and Nmos.

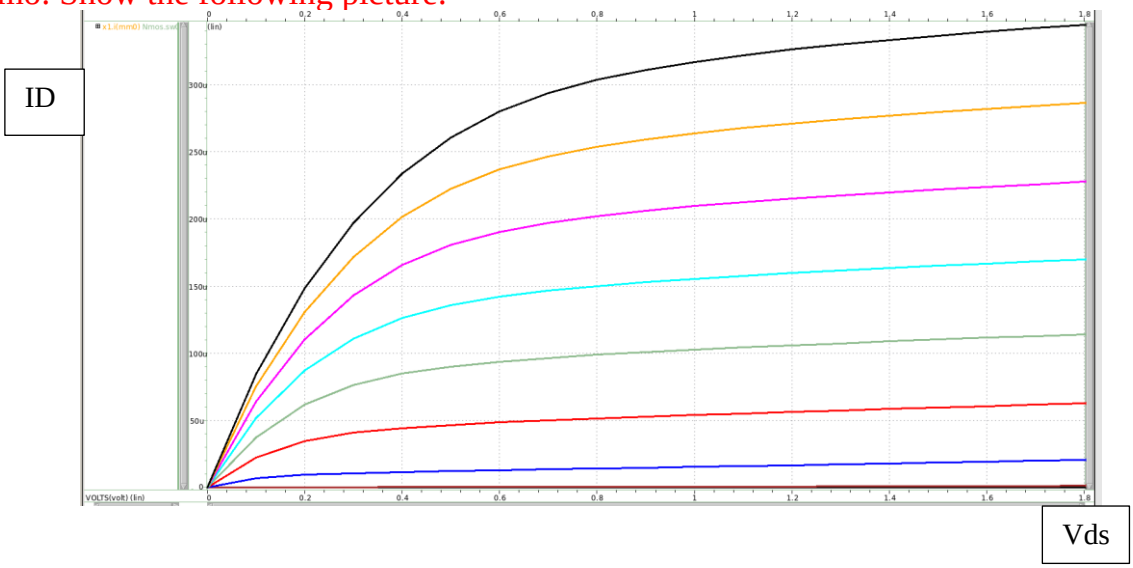
For NMOS:

- Output schematics of Nmos



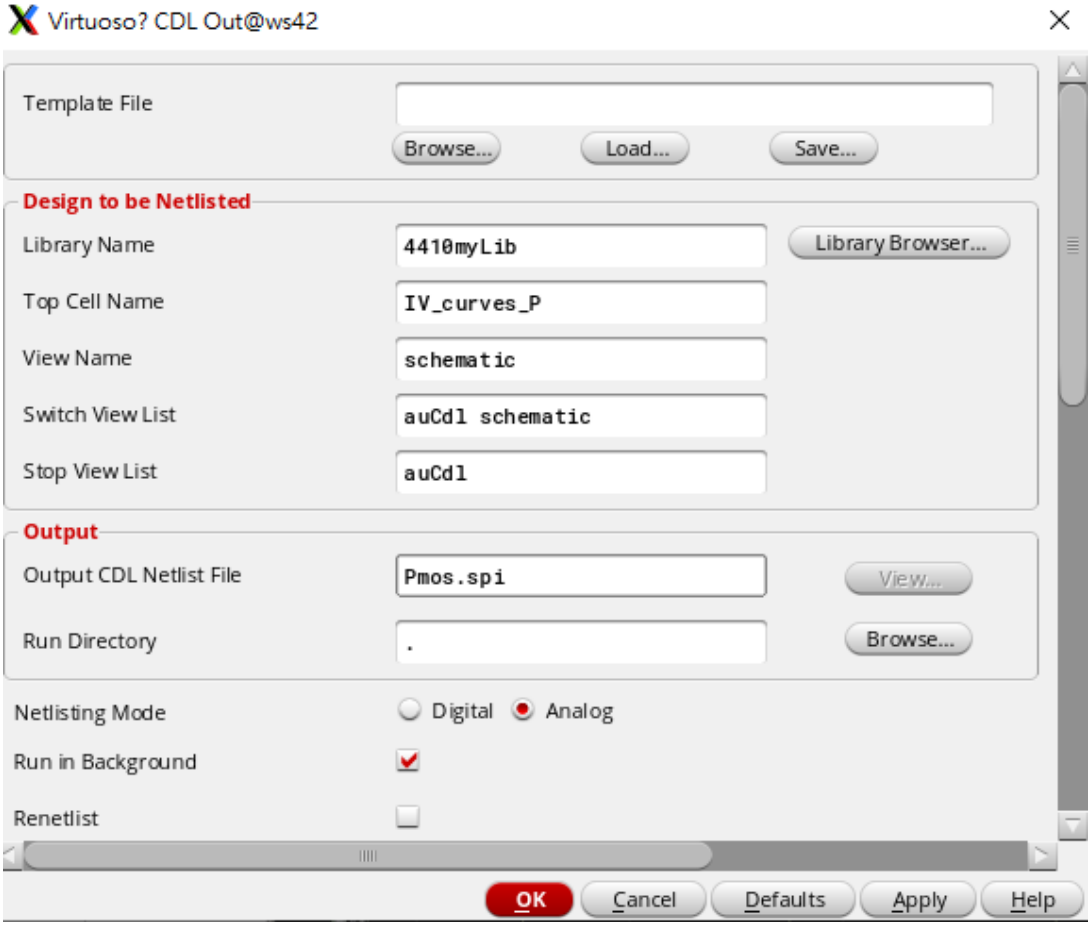
- Run simulation
  Vds from 0 to 1.8 sweep Vgs from 0 to 1.8 step is 0.2.

Demo: Show the following picture.

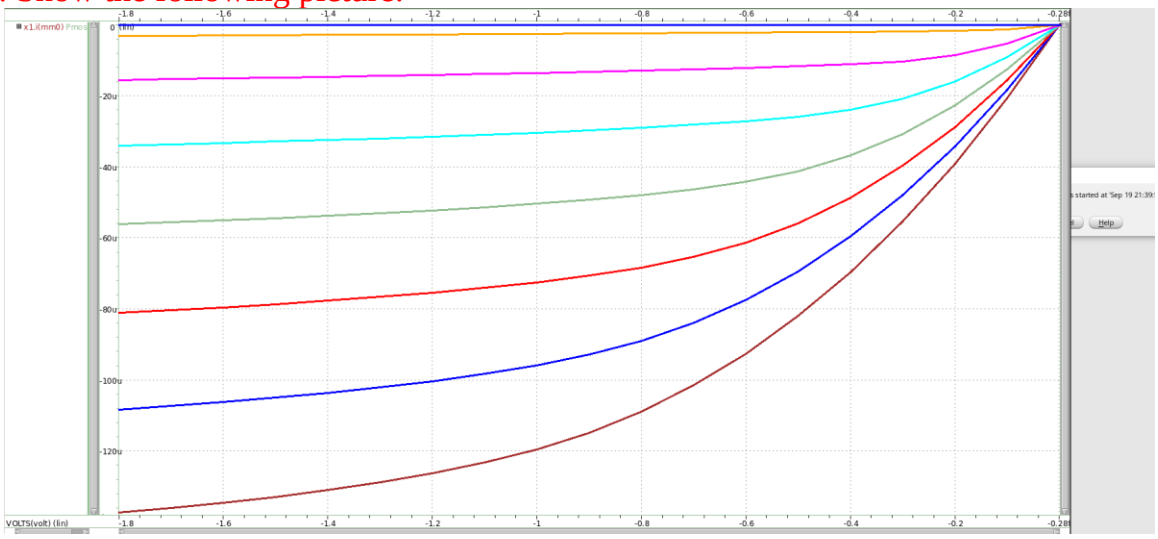


For PMOS:

- Output schematics of Pmos



- Run simulation
  Vds from -1.8to 0 sweep Vgs from -1.8 to 0 step is 0.2.
  Demo: Show the following picture.



Demo: Compare the amplitudes and directions of the active currents that are produced by NMOS and PMOS transistors that experience. Report your simulation results and conclusion to your TA, try to explain it.

II. Is MOSFEET an ideal switch ?

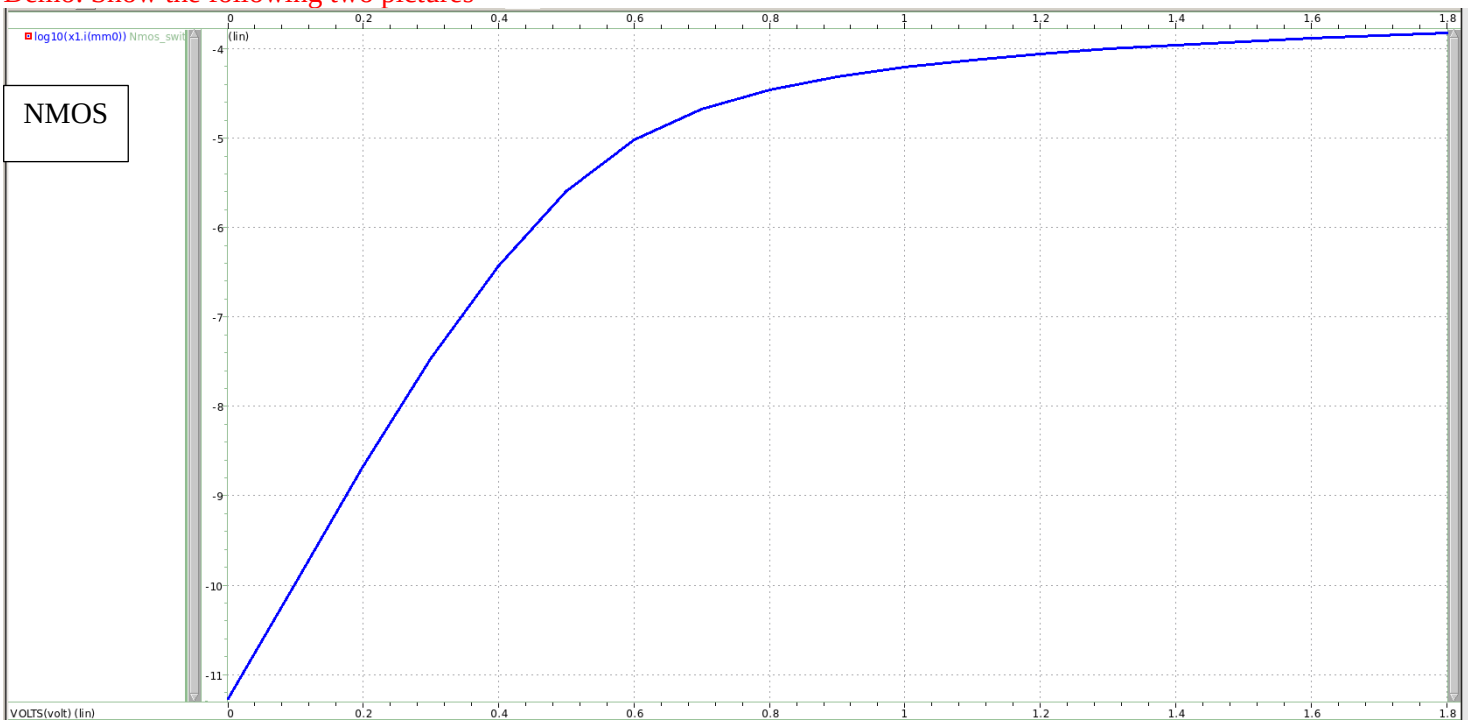
- Set vds = 200mV for NMOS transistor and vds = -200mV for PMOS transistor. DC sweep vgsfrom 0 to 1.8V for NMOS transistor and from 0 to -1.8V for PMOS transistor. You should choose the right port of transistors to measure positive current, because we will set it to log scale later.

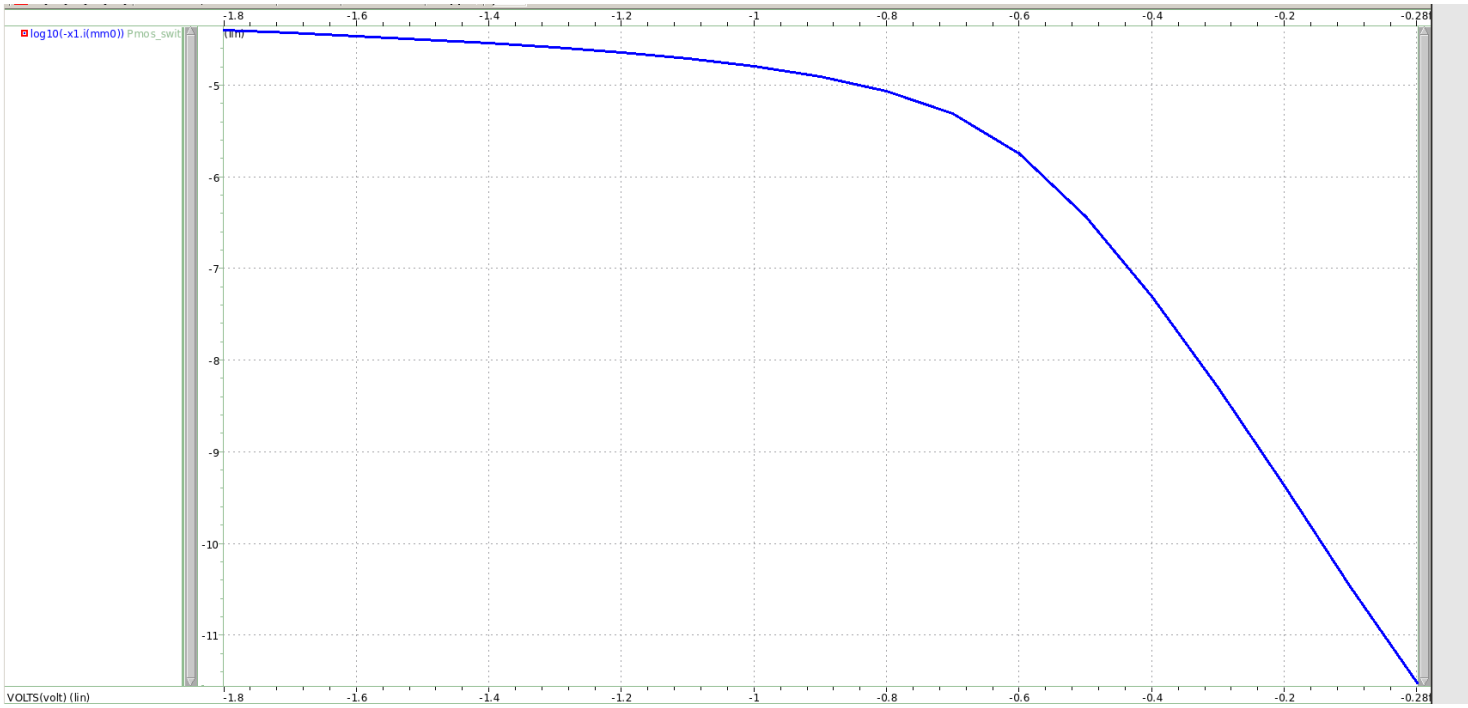
- Use equation builder to change y-axis to log scale. Display results of NMOS and PMOS transistors should be similar to the second and third figures, respectively.

	Name	Equation (click here to edit min/max)	Target		Result	
☐		log10('x1.i(mm0)')	D0/Nmos_switch.sw0			

Demo: Show the following two pictures

NMOS



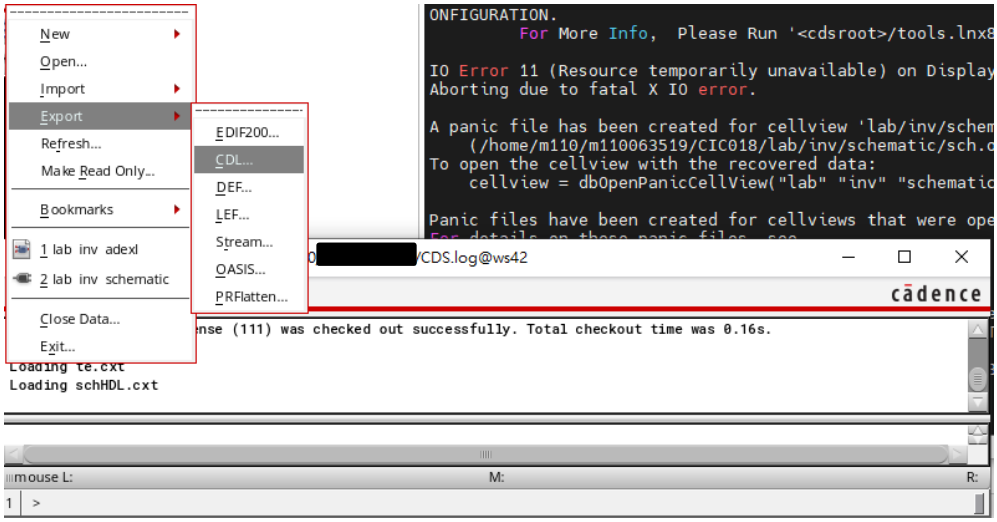


- Demo: Observe the currents produced by NMOS and PMOS transistors for subthreshold gate-to- source voltage differences. Compare the amplitudes and directions of the subthreshold leakage currents that are produced by cut-off NMOS and PMOS transistors that experienceidentical |VDS| and |VGS|. Report your conclusion to your TA.

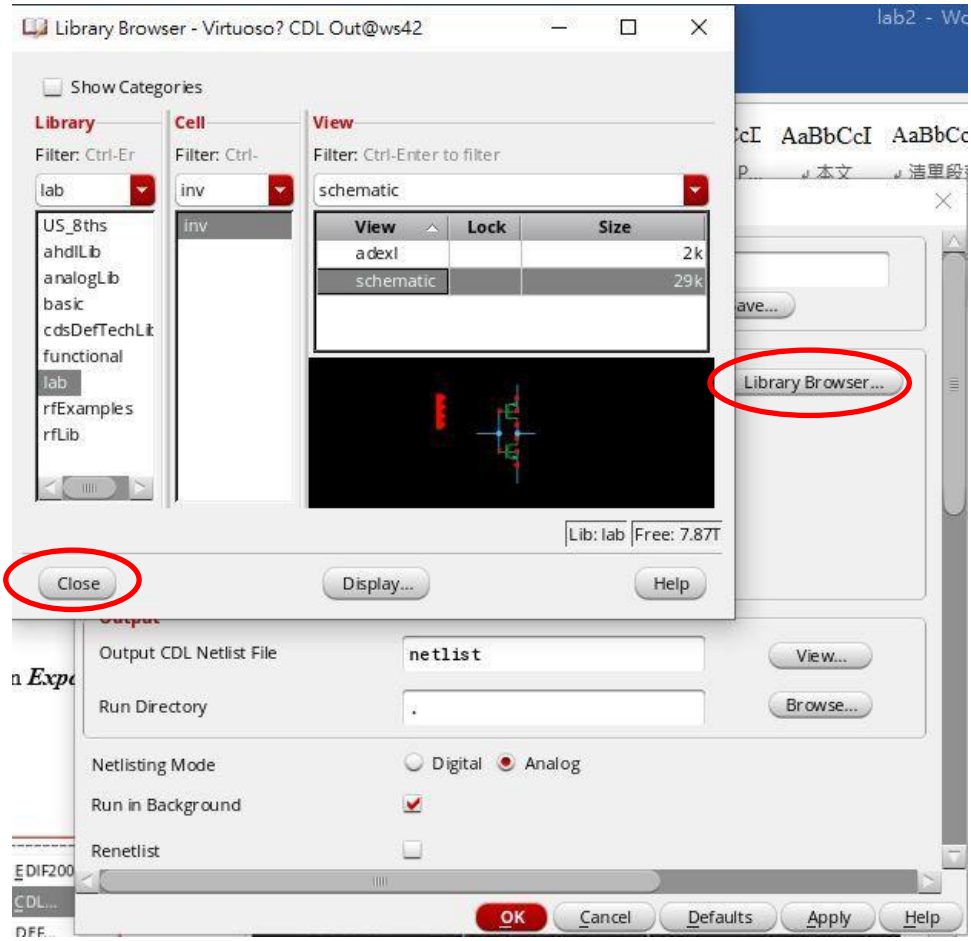
  Comment on the effect of drain voltage on the subthreshold leakage currents that are produced by ideally cut-off NMOS and PMOS transistors. Report your comment to your TA.

III.Export file

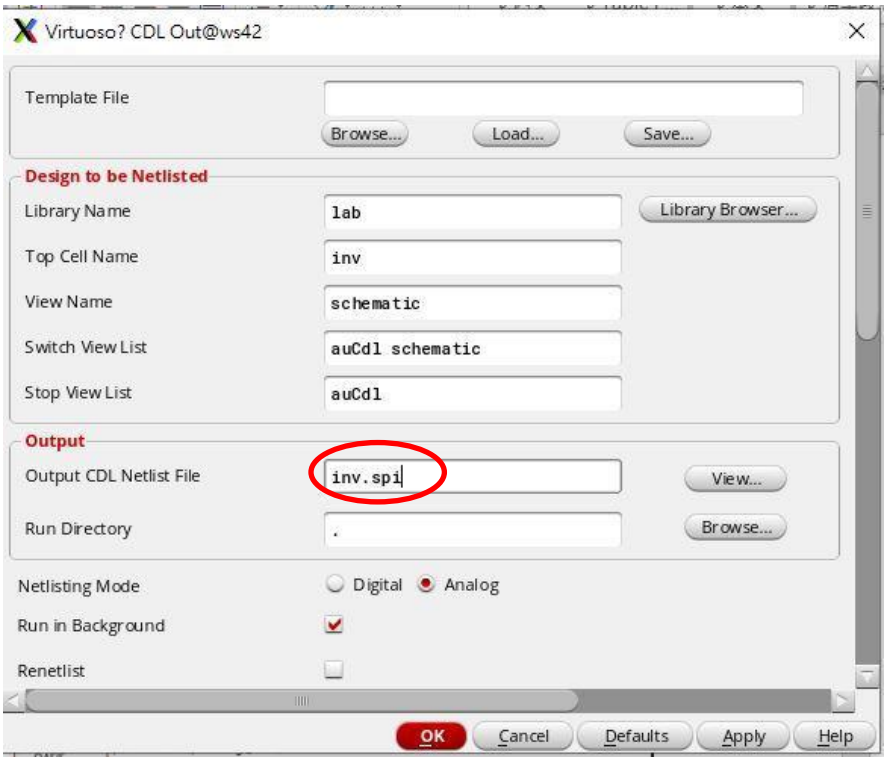
- Just click on ***File →Export→ CDL***, then change to the desired design in the pop-up window .

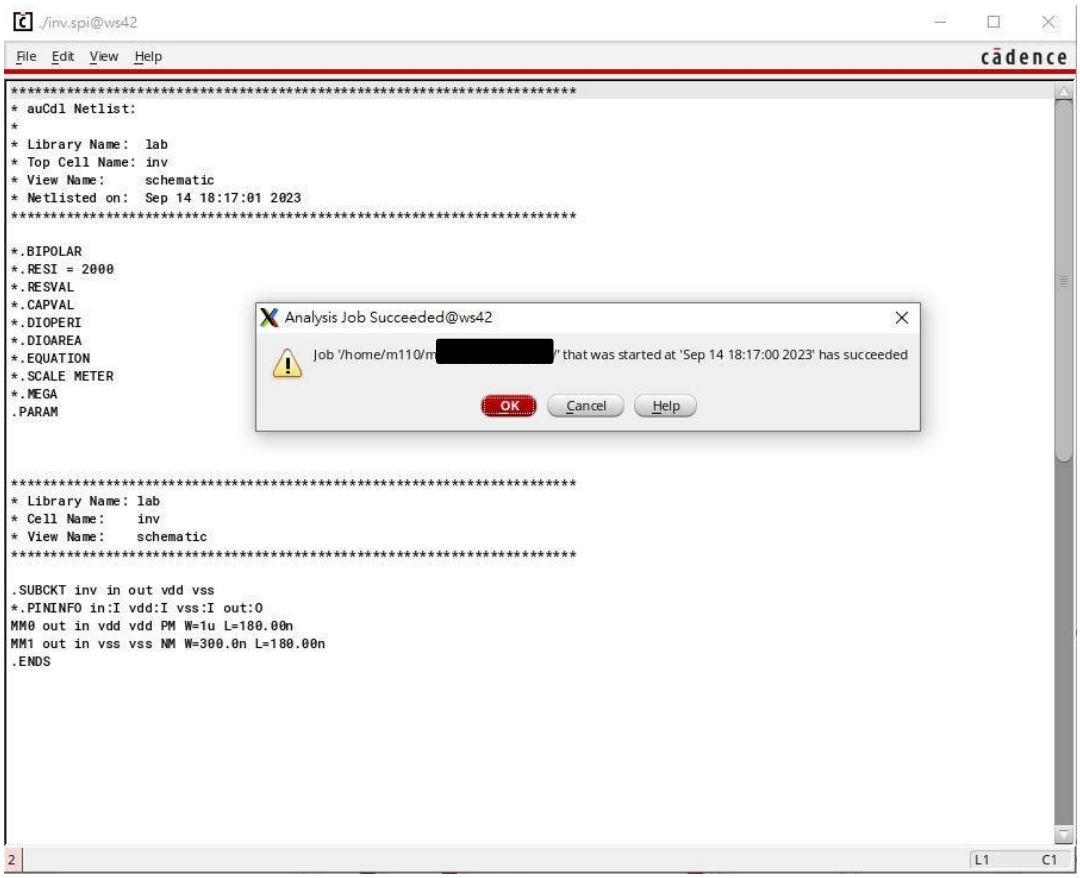


- In the window, click on ***Library Browser***, find the cell in your library, click ***schematic*** and then close window,



- Name your netlist file (.spi). If the file exported succeeded, your netlist file will pop-up.





IV. Before run Hspice simulation

Before carrying out the simulation, you have to set up the simulation environment properly;

1. Check your netlist file.
2. specify the **test bench** (the test.input file).
3. specify the **model file** used.

- In the terminal window, enter the command of texting file ***'gedit file_name.spi &'***, then below window pops up,

  - Name model name of mos and save. i.e. p_18 for pmos, n_18 for nmos (according to 0.18μm CMOS process).

```
********************************************************************************
* Library Name: lab
* Cell Name:    inv
* View Name:    schematic
********************************************************************************

.SUBCKT inv in out vdd vss
*.PININFO in:I vdd:I vss:I out:O
MM0 out in vdd vdd PM W=1u L=180.00n
MM1 out in vss vss NM W=300.0n L=180.00n
.ENDS
```

To specify the test bench (test.input file)

- To define "test.input" as a simulation file; in the terminal window, create new file ***'testbench_name.sp'*** .

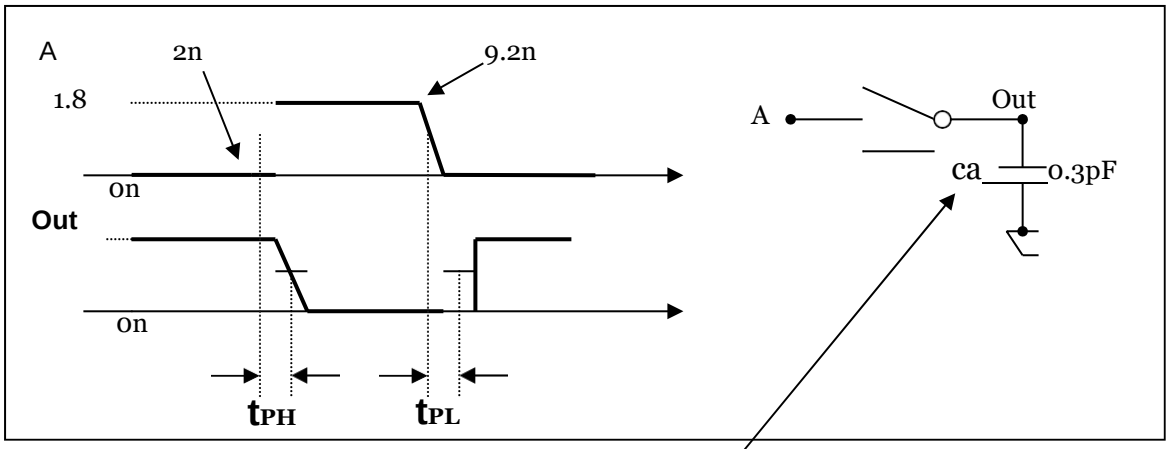
Model file →

```
.protect
.lib 'cic018.l' TT
.unprotect
.temp 25
.option
+unwrap
+ post                    $output waveform to user
+ acout=0 runlvl=6        $increase simulation accuracy
+ captable
.param y=4.15u
```

Include netlist → `.include "inv.spi"`

More about the test.input file:

The input voltage waveform at pin A from the test.input file looks like below and the expected output waveform at the pin 'Out' is drawn underneath. The actual waveform Out will be obtained after the simulation, and then we can check for the delay times t_{PHL} and t_{PLH} of the inverter.



Connect a loading capacitor, named 'ca', of 0.3pF between the output pin *Out* and *gnd.*(pin names are defined in the schematic view and are case sensitive)

- Make sure your model file and testbench file in the same files. (If you don't have model file, please contact your TA)

V. Run the simulation

You are about to run the simulation.

- In terminal window, enter the command of hspice simulation ***'hspice testbench_name.sp -o simulation_name.lis &'*** ,If simulation succeeded, the terminal will display 'concluded'.

```
hspice inv.sp -o inv.lis &
[7] 7730
[6]    Exit 255                      hspice inv.sp -o inv.lis
[m]        @ws42 ~/CIC018]$ Using: /usr/cadtool/cad/synopsys/hspice/2020.12-sp2/hspice/linux64/hsp
ice  'inv.sp' -o inv.lis

>info:         ***** hspice job concluded
```

- You can confirm simulated information in .lis file.

inv.spi | inv.sp | inv.lis

```
****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
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  This software and the associated documentation are proprietary
  to Synopsys, Inc. This software may only be used in accordance
  with the terms and conditions of a written license agreement with
  Synopsys, Inc. All other use, reproduction, or distribution of
  this software is strictly prohibited.
  Input File: inv.sp
  Command line options: /usr/cadtool/cad/synopsys/hspice/2020.12-sp2/hspice/linux64/hspice inv.sp -o
inv.lis
  Start time: Thu Sep 14 20:28:22 2023
 lic:
 lic: FLEXlm: SDK_12.9.5
 lic: USER:   m[redacted]          HOSTNAME: ws42
 lic: HOSTID: "5cf3fcb5e35c"       PID:      8948
 lic: Using FLEXlm license file:
 lic: 26585@lstn
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 31-mar-2024/2023.03
 lic: 73(in_use)/450(total) FLOATING license(s) on SERVER 26585@lstn
 lic:
  **info**  the obsolete option acout is ignored
  **info**  the obsolete option acout is ignored
  **warning** (inv.spi:18) Parameter name is not defined in .param. Please enter parameter variable with
their respective value/expression.
  **error** (inv.sp:14) Number of nodes mismatch between instance "x1" and subcircuit "inv". Subcircuit
definition has    4 node(s) whereas subckt instance has    5 node(s). Please specify same number of
nodes.
```
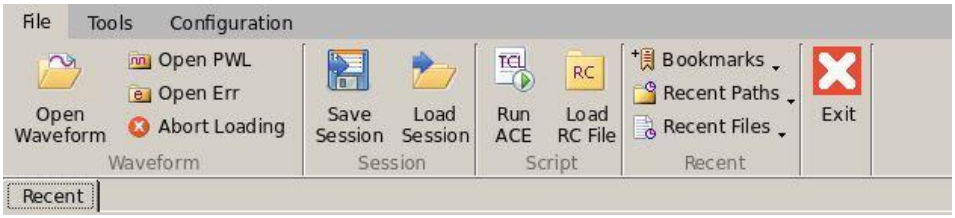
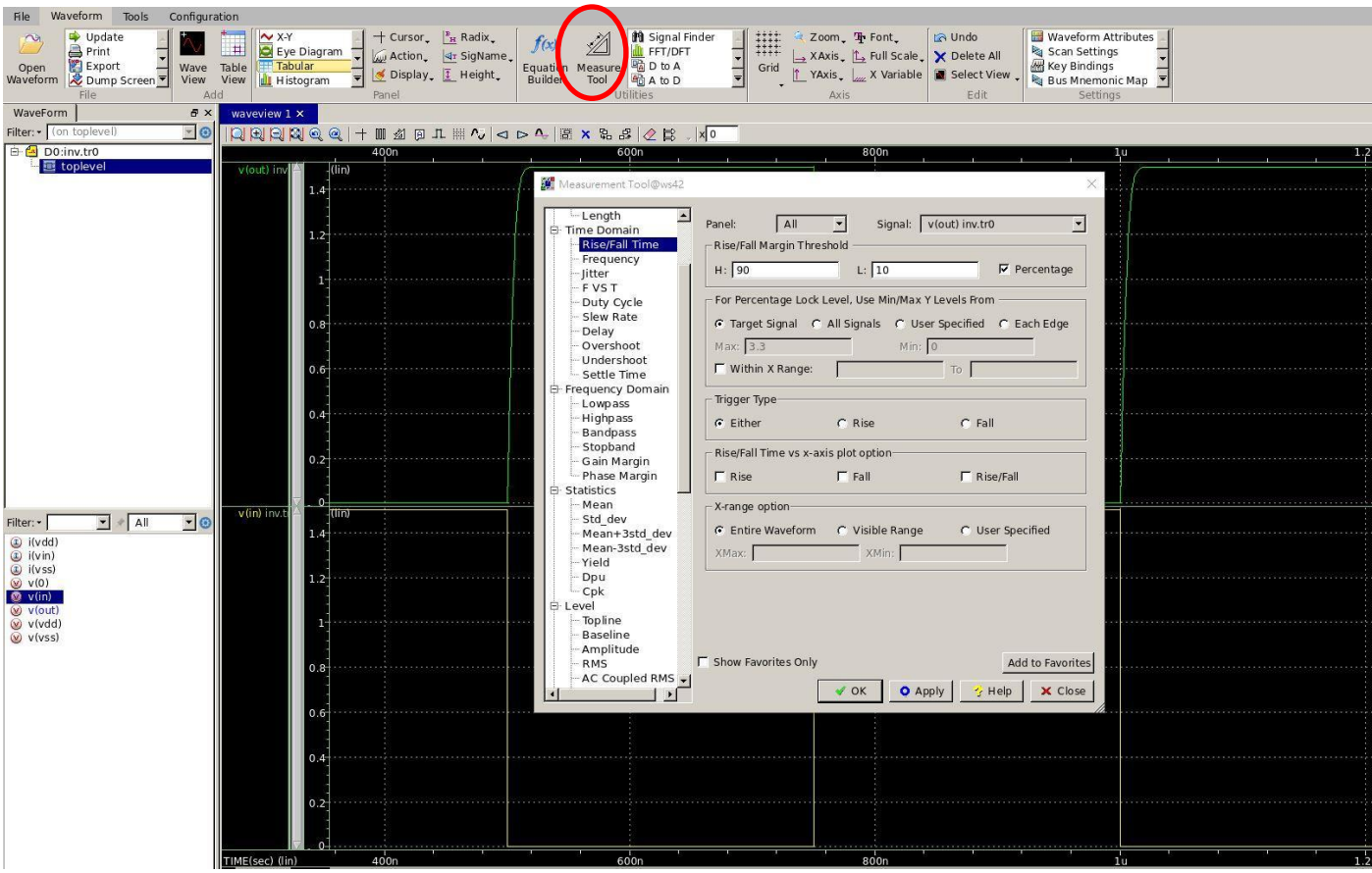

VI. Use the Waveform tool

The simulation is done now, to show the simulation waveform, in the terminal, Enter the command of waveform ***'wv &'***,then the window pop-up. Click on ***Open waveform→ Simulation_name.tr***, the Result Browser window appears. To show the files of the waveforms, double click on "tran-tran", then a list of waveform files display.



Here is the plot.

- click on ***Measure***, and measure what you want.



- Report the delay times, tp_{HL} is defined for output wave Fall from Logic High to Logic Low while tp_{LH} is defined for output wave change from Logic Low to Logic High.

  Both output H ~> L (10% ~> 90%) or L ~> H (90% ~>10%) are stimulated by input Logic change read at **50% point**; example for above waveform
  tp_{HL} = 0.9ns – 1.1ns ~ 0.16 ns ; tp_{LH} = 2.55ns – 2.75ns ~ 0.18 ns
  for VDD = 1.8V
  Report your own reading to TA.

The End of Lab2