

# EE 323002

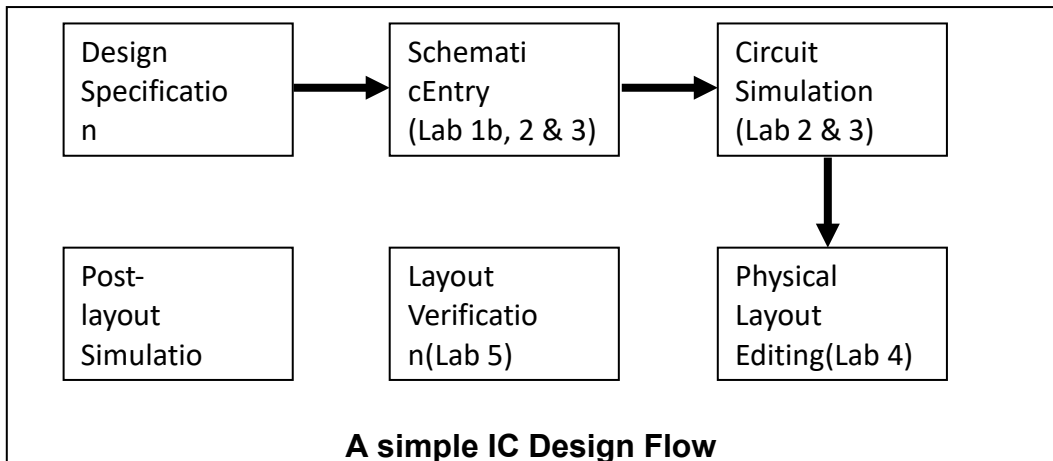
## Lab 1 - Part b: Schematic Entry

Version 1.0 (Sept 2023)

### Introduction

In this lab, you will learn to use the Cadence suit of IC design tools. Cadence tools are very popular in industry and can be used for schematic entry, circuit simulation, layout design, all the way up to a complete chip design.

In the coming labs, the basic of Cadence design framework and schematic capture of simple circuits (in transistor level) will be covered. You will learn how to build a chip through our lab exercises.



### I. Starting Cadence

Step 1. Enter to the Cadence working directory (working directory is the directory where you open Cadence and directory ~/ is your home directory). All your cadence-related files will be stored there from now onwards

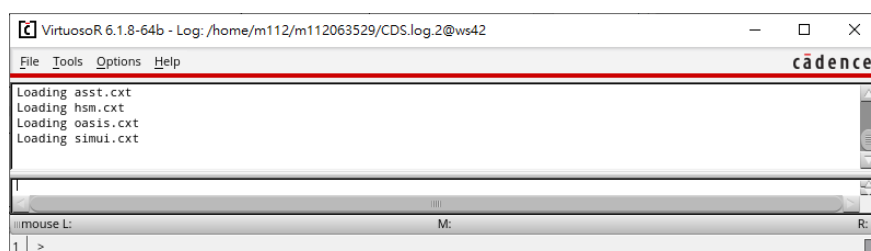
```
cd ~/323002cadence
```

1. Always start Cadence software under this working directory (~/323002cadence).
2. Add source /usr/cadtool/user\_setup/03-spectre.csh in .tcshrc file.
3. Put technology file under (~/323002cadence)
4. And to activate the Cadence tool, under this working directory, **type in the following command lines**,

```
virtuoso &
```

It will take a few seconds to execute. The main Cadence window, Command Interpreter Window (CIW) will appear as below.

Command Interpreter Window (CIW)



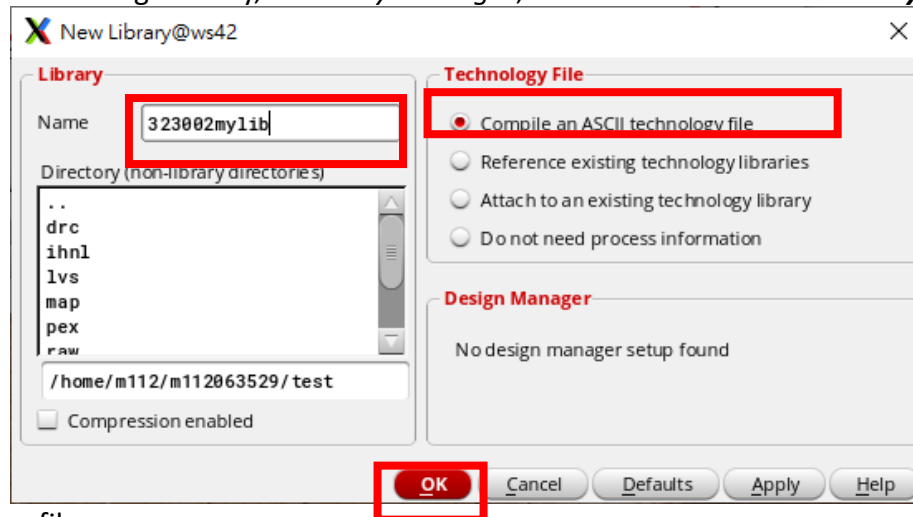
You should **frequently and carefully read** the messages shown in CIW because most of the information, warnings and error messages from the system are shown there.

5. To quit Cadence, click on the CIW's menu bar **File → Exit**, then click on the “Yes” button in the pop-up menu to confirm.

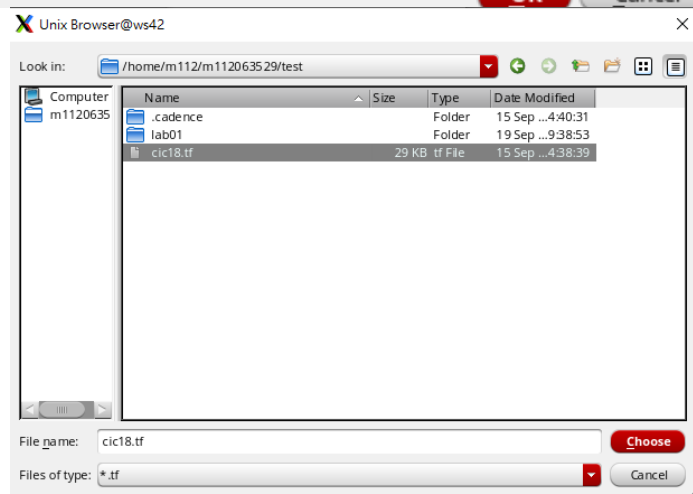
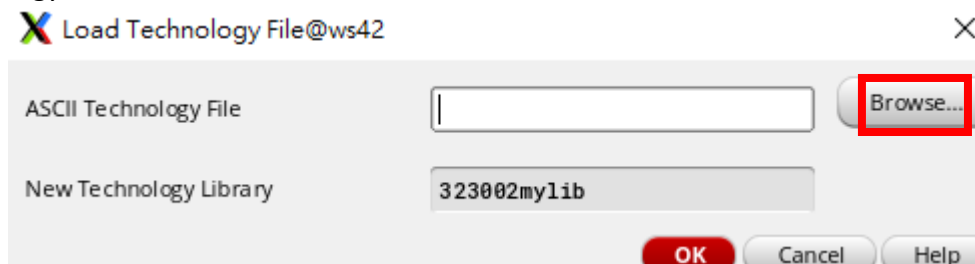
## II. Creating Cadence Library and Specifying the technology library used

Now, you are going to create an empty Library. Later, you will have all your designs stored inside this library: “323002mylib”.

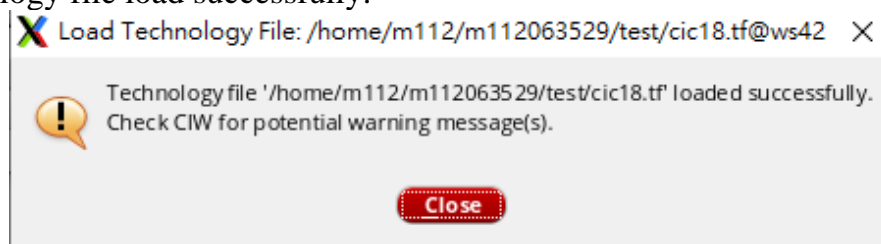
To create you're the design library, in *Library Manager*, click on **File → New → Library**



Load technology file



Make sure technology file load successfully.



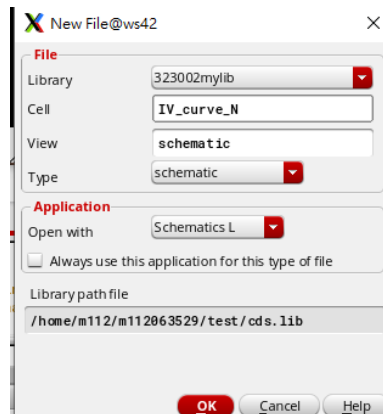
Well done! You have now set up the required design environment for your 323002myLib design library. You can start designing your own circuits now! **Note that whenever you create a new design library, you must specify which technology library to be used.**

### III. Active MOSFET current-voltage characteristics

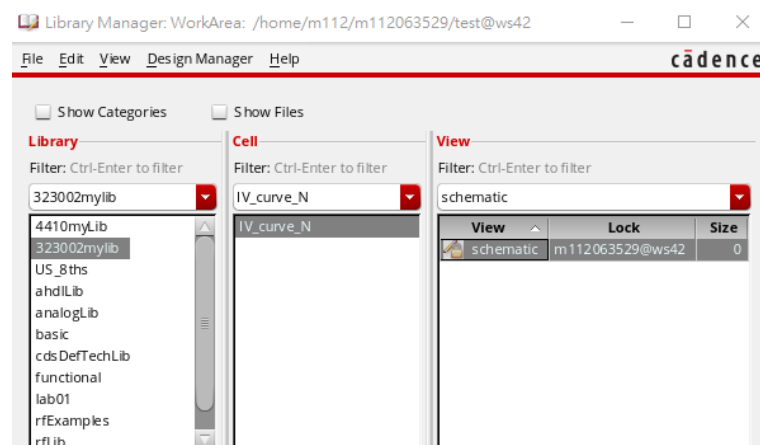
You are going to inspect the I-V characteristics of MOSFETs in this experiment.

#### 1. File → New → Cellview


Input Cell Name as **IV\_curves\_N**.



Click OK. A blank schematic window will appear. Note that the newly created IV\_curves\_N schematic cell view appears in the *Library Manager* as shown below:



#### 2. Create schematic in *Schematic Editor*.

- Click **Create** in the menu bar and choose **Instance** (or just press i) as shown below, or just click this button  in the tool bar.
- Input Library as "*analogLib*" and Cell name as "*nmos4*" and input "symbol" in View field. You can flip and rotate the instance using buttons on this window. You can change model name and physical parameters by modifying the contents of the input box.

Press Q to see instance properties

Apply To

only currentinstance

Show

system

user

CDF

Browse

Reset Instance Labels Display

Property	Value	Display
Library Name	analogLib	off
Cell Name	nmos4	off
View Name	symbol	off
Instance Name	M0	off

Add

Delete

Modify

CDF Parameter	Value	Display
Model name	n_18	off
Width	1u M	off
Length	180.00n M	off
Source diffusion area		off
Drain diffusion area		off

Or you can click Browse button to choose them in *Library Browser*, as shown below:

Library Manager: Directory ...ome/m112/m112063529/test/lab01@ws42

File Edit View Design Manager Help

cadence

Show Categories

Show Files

Library

Filter: Ctrl-Enter to filter

analogLib

4410myLib  
US\_8ths  
ahdlLib  
analogLib  
basic  
cdsDefTechLib  
functional  
rfExamples  
rfLib

Cell

Filter: Ctrl-Enter to filter

nmos4

n3port  
n4port  
nbsim  
nbsim4  
njfet  
nmes  
nmes4  
nmos  
nmos4  
nodeQuantity  
npn

View

Filter: Ctrl-Enter to filter

Select or Filter


View	Lock	Size
auCdl		19k
auLvs		19k
hspiceD		19k
spectre		19k
symbol		19k
symbol_xform		13k

Messages

Log file is "/home/m112/m112063529/test/lab01/libManager.log".

Lib: analogLib

Free: 437.72G


- Now you can close the Browser window (selected library, cell, and view will be automatically filled into the *Add Instance* window) and click **Hide** button in the *Add Instance window* so that you can place an NMOS transistor in the *Schematic Editing* window. Left Click to place one selected instance, press Esc to finish placing (you can press Esc a few times more to insure there no function active).
- Adding Wires to the Schematic
  - . Select the fixed menu **Wire (narrow)** button . You can also press “w” to select wire.
  - Then move the mouse cursor back into the schematic window. Note that two cursors (one in diamond shape and the other in square shape) move with your mouse pointer. These cursors can help you to connect the wires accurately from point to point.
  - Point at a starting point (overlap the square cursor with the diamond one) and click the left mouse button to start drawing the wire.
  - You can also use the keyboard key ‘s’ to snap the square cursor into the diamond one.
  - Connect all the components with wires (refer to the first figure in the next page)
  - To end the wire, double click the left mouse button. The finished schematic should look like the following figure.

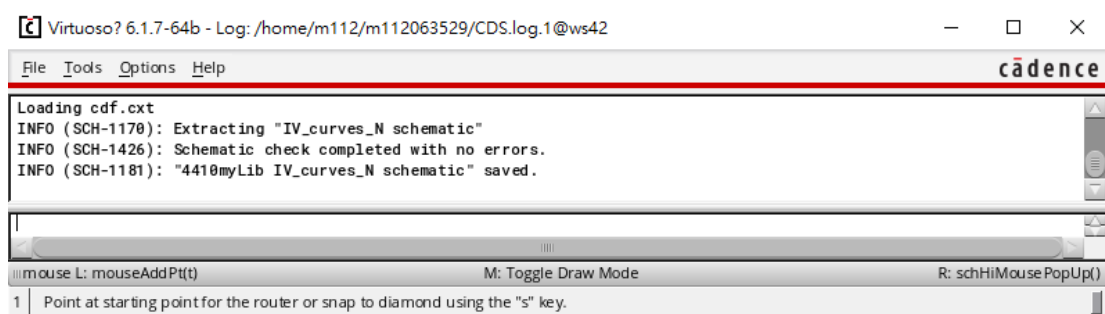
Note: When this **Wire** command is activated, press "F3" on the keyboard to bring up an option form. This form can also help you to draw wires, try it out yourself.
- Add Pin to input and output
 

Press “p” to add pin



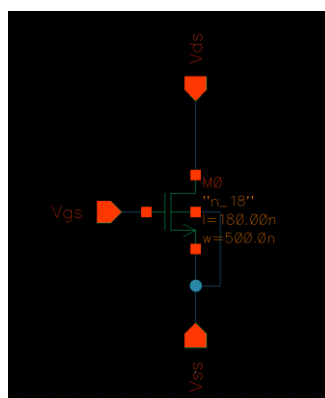
- Don't forget to check and save every time you finish editing a component:

click on **File** → **Check and save** (or this button ). If any errors and warnings occur, go to **check** → **find marker**, and correct the errors and warnings. If everything works well, the CIW window would look like this:

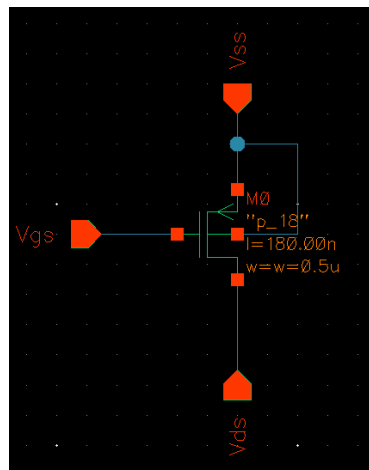


## Goal is to make schematic of NMOS and PMOS

Nmos(Name:IV\_curves\_N): W=0.5u L=0.18u M=1



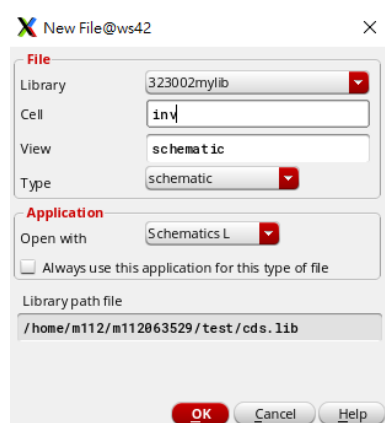
Pmos(Name:IV\_curves\_P): W=0.5u L=0.18u M=1



#### IV. Creating a new cellview – the schematic view of an inverter

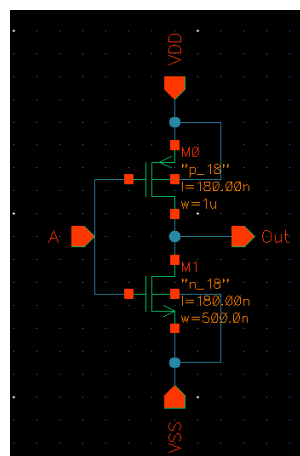
You are going to create an inverter design in schematic view, it is called “inv”. The corresponding schematic tool used is called Composer.

1. In Library Manager, click on **File** → **New** → **Cellview** → **inv** → **ok**



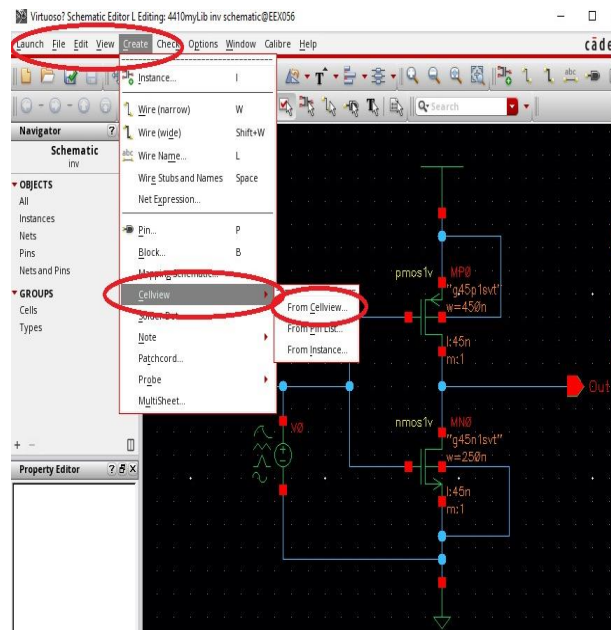
2. Create **inverter schematics**

You need to modify transistor size and also make sure there is no errors.

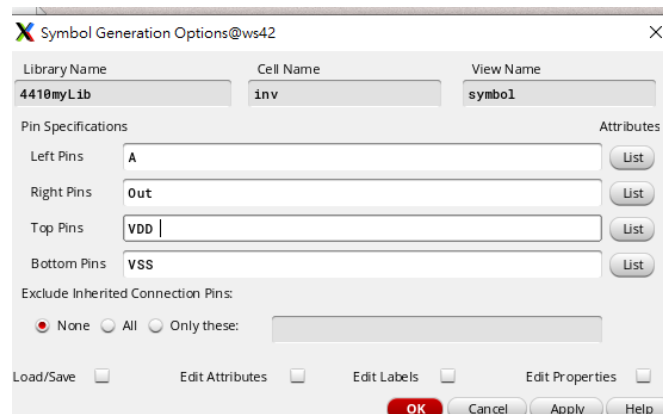


3. Creating a Symbol view

- In schematic editing window, click on **Design** → **Create Cellview** → **From Cellview**. This form appears. If there is no error, press **OK**.



- Then the Symbol Generation Options form appears. Double check the pin names. If there is no error, press **OK**.



- The symbol view is then created automatically and will look as follows. Always remember to **'check and save'** the cellview so that the system

[@instanceName]



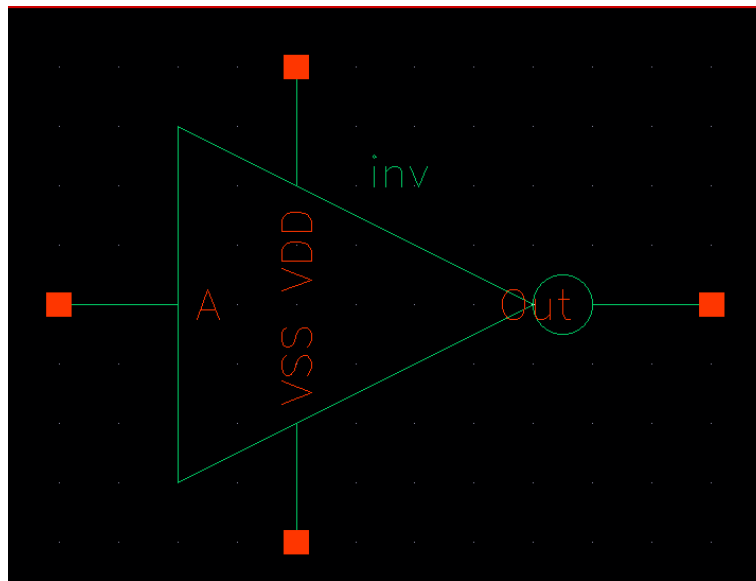
can cross-check the pin names and pin types among the symbol view and the schematic view.

**Note:** You can add lines/circles on the symbol view to make it more recognizable.

To add lines/circles, at the pull down menu of the symbol view editing window, click on **Add** → **Shape** → **Line**, or **Add** → **Shape** → **Circle** to



draw. You can create a symbol like this.



**The End of Lab1 (Part b)**