EE 323002
Lab 3: Hierarchical Schematic Design

Version: Fall 2023

Objective

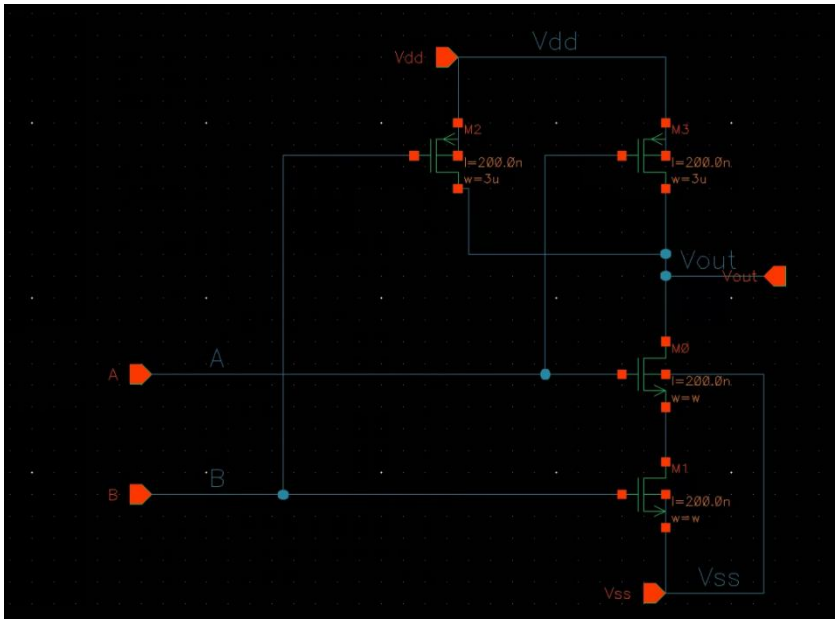
- To build the schematic and symbol views of a 2 input **NAND** gate.
- To design a **ring oscillator** with **NAND** and **NOT** gates.
- To introduce the concept of design **hierarchy** using a ring oscillator design as an example.

I. Building a 2-input NAND gate

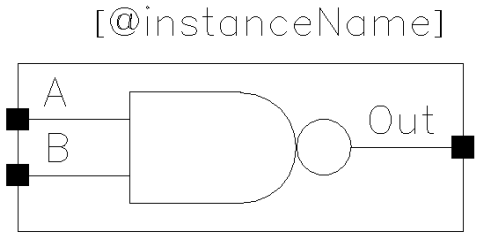
You have finished the schematic design of inverter, now you are going to finish the NAND gate design by your own.

Step 1. Create the **schematic** and **symbol** views of a new cell called ***nand2*** (a 2 inputs NAND gate) as shown below.

- Fill in the truth table by yourself



Schematic view of nand2 cell



Symbol view of nand2 cell

A	B	Out
0	0	
1	0	
0	1	
1	1	

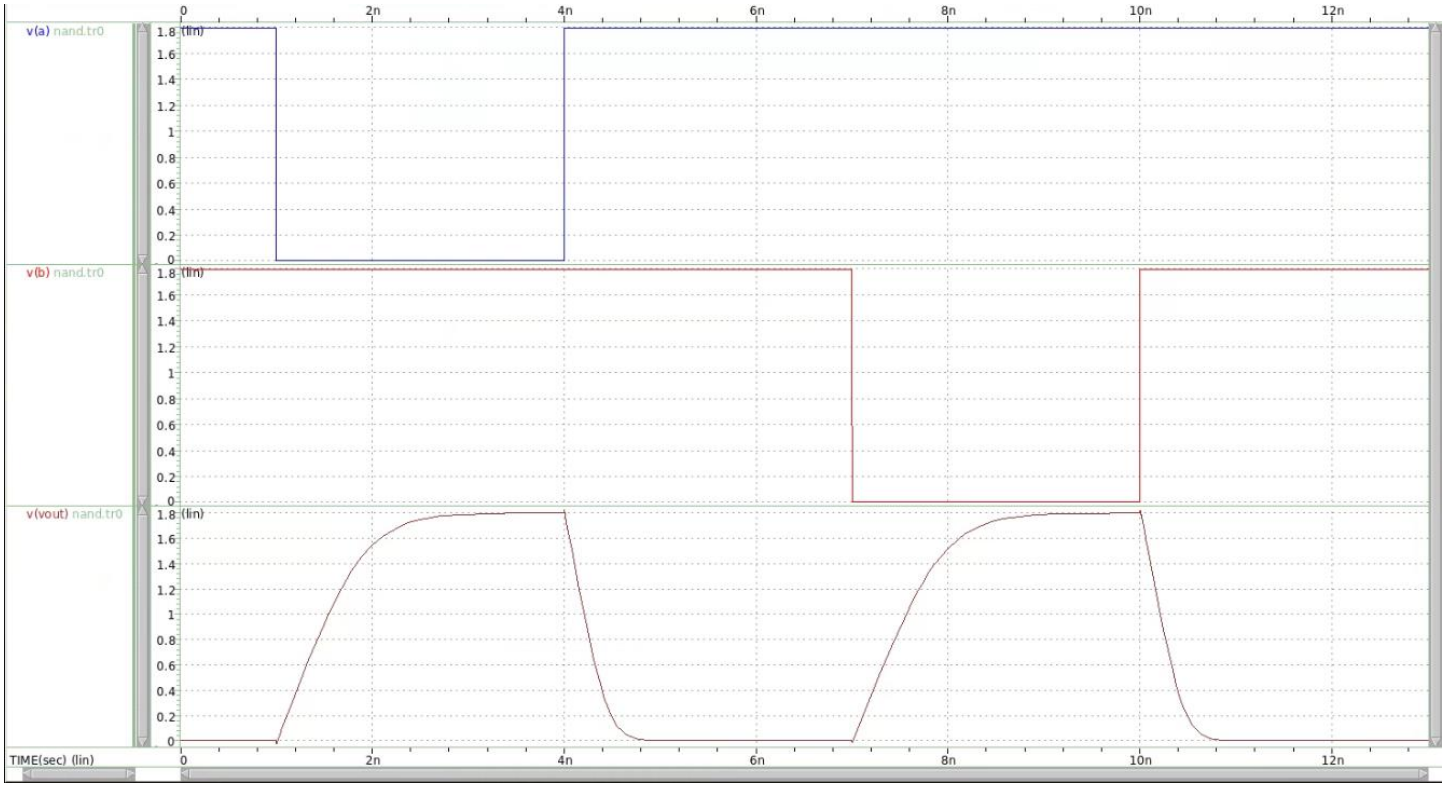
The truth table of the NAND2 gate

Step 2. To check the functionality of the nand2 design, simulate the design in its schematic view.

- Use 'nand2-ADE.run1' as your simulation run directory's name.
- Remember to perform ***File → Check and Save*** on **schematic** and **symbol** views before runningthe simulation.
- Modify/create the necessary files for your simulation, refer to above steps if necessary. The value of the output capacitive load, ca, is 0.3pF. Set the input signals A and B yourself.
- Record **all values** of $\mathbf{t_{PLH}}$ and $\mathbf{t_{PHL}}$ and report and show the results to your TA.

- What is the delay time of this gate?

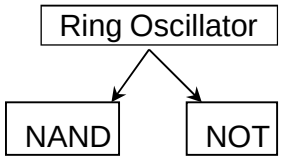
The resulting waveforms of A, B & Out should look like these.



II. Designing a Ring Oscillator

The Use of Hierarchy

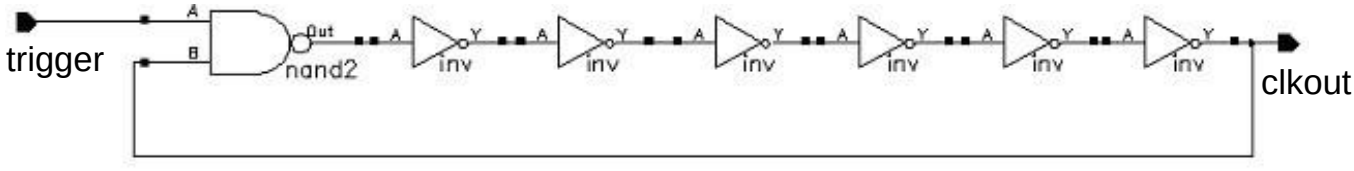
The principle of hierarchy is dividing a complex system into a set of sub-modules and then repeating this operation on each of the sub-modules until the complexity of the sub-modules become manageable (this is also called a 'divide and conquer' technique). As a simple hierarchy design example, the ring oscillator (a module) may be decomposed structurally into individual logic gates (sub-modules) as shown below.



A hierarchy for the ring oscillator

The Ring Oscillator – Schematic View

From the structural hierarchy above, the ring oscillator (7 stages) consists of NAND and NOT gates, and their connections are shown below.



Schematic view of the ring oscillator

Step 1. Create a **schematic** view of a new cell called ***clkgen*** for the ring oscillator.

- In your 323002myLib design library, use the ***nand2*** cell and ***inv*** cell to build the ***clkgen*** cell; Put ***inv*** and ***nand2*** (their **symbol** views) in the ***clkgen*** schematic by clicking on
  Add → Instance.
- Create pins and make the connection as above.

Step 2. In the schematic-editing window, you can look into the nand2 and inv symbols (go down one level to transistor level) by clicking ***Edit → Hierarchy → Descend read ,*** at '***view name***' selects ***'schematic'***.

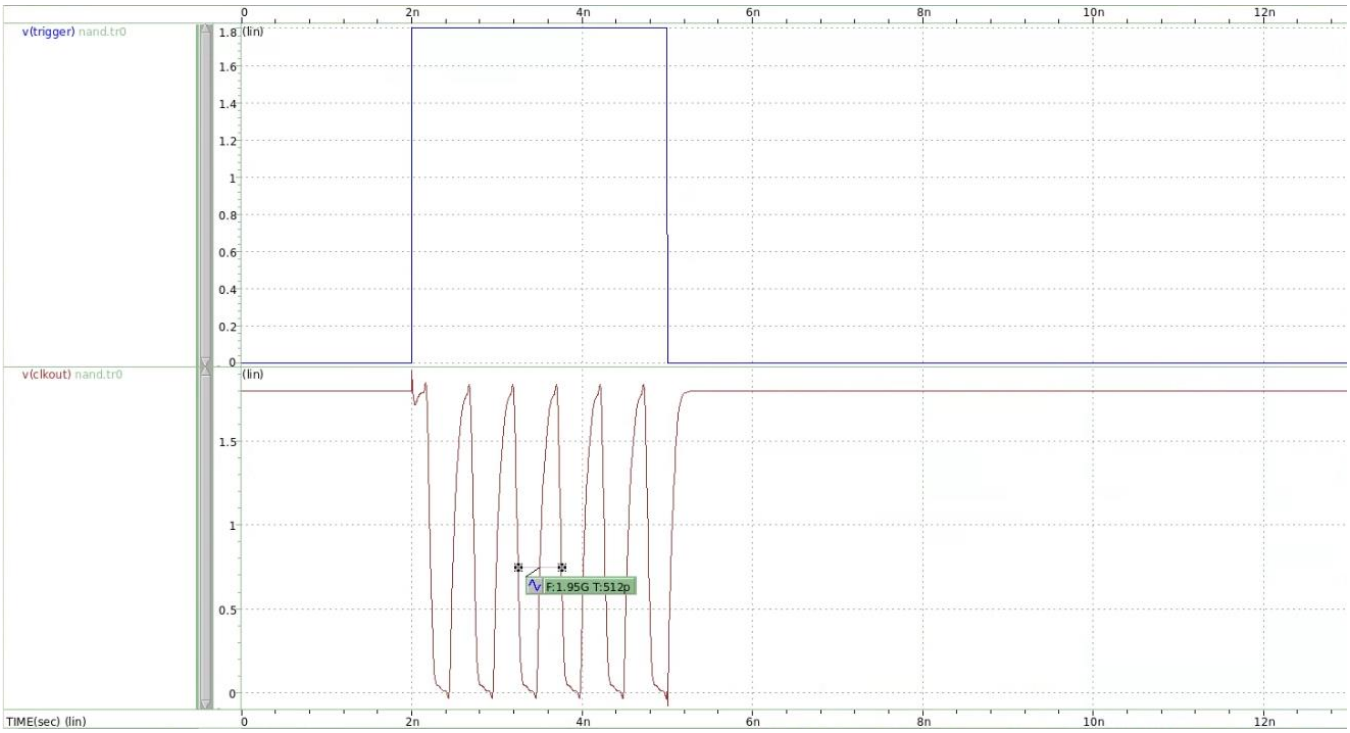
- The schematic view of inv cell shows. If you want to go back to the original display,
  Edit → Hierarchy→ Return.
- You use the ***inv*** cell in ***clkgen*** schematic view from now onwards, any change in the ***inv*** cell will be updated automatically in the ***clkgen*** cell. OR, if necessary, you can edit ***inv*** cell inside the ***clkgen*** schematic, to open up the ***inv*** cell and make changes, select the ***inv*** instance and then click on
  Edit → Hierarchy → Descend Edit

Circuit Simulation on the Ring Oscillator

Step 3. To check the functionality of the ring oscillator, simulate your design in its schematic view.

- Use 'clkgen-ADE.run1' as your simulation run directory's name.
- Remember to perform ***File → Check and Save*** on its **schematic** and **symbol** views before running any simulations otherwise the simulations would fail!
- Prepare the necessary files for your simulation. Present the output waveform and report the **frequency** of the oscillation to TA.

The resulting waveforms should look like these:



The End of the Lab3

Appendix

Add the library of AnalogLib in the Library Manager

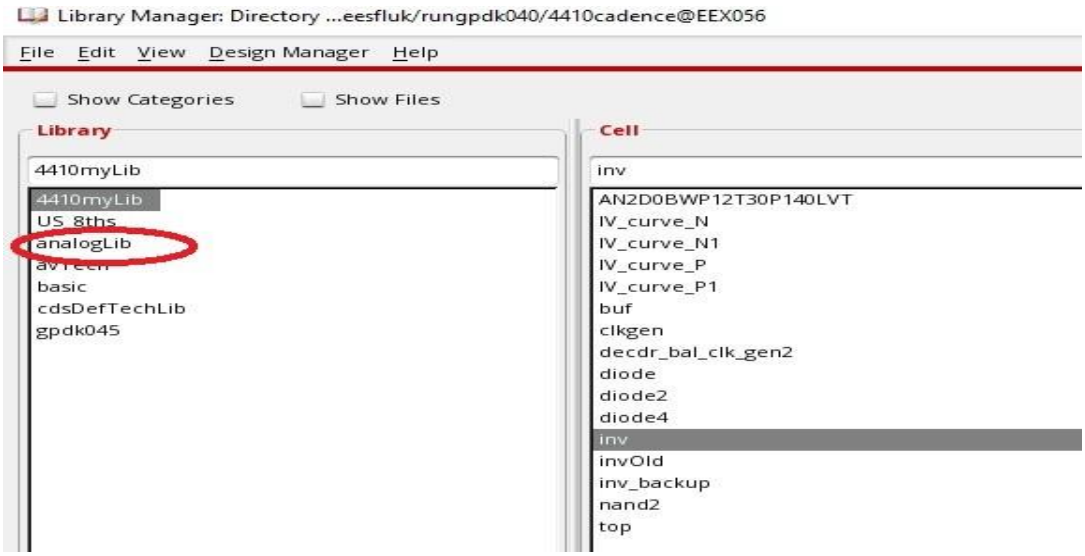
There are many functions in the ADE, for advance use, you may need to include a library called AnalogLib. But now we do not need it for our course.

The **cds.lib** file contains the information of the location of design libraries. The Library Manager looks up the **cds.lib** file (under ~/323002cadence) and display the design libraries in the Library Manager display window. To include Analoglib in Library Manager, we need to modify the cds.lib file,

- open the cds.lib file, ~/323002cadence/cds.lib (use the text editor, /usr/dt/bin/dtpad)
- in this file, key in the following line (**in one single line**) at the end of this file,

DEFINE analogLib
/usr/eelocal/cadence/ic617hf/tools.sun4v/dfII/etc/cdslib/artist/analogLib

- **re-open** the Library Manager, the analogLib is then shown.



Useful Hint - The pulse voltage source

- Instead of using PWL voltage source, you can use pulse voltage source to be your input voltage waveform. The pulse voltage source can repeat itself periodically. Here is an example,

v1 (A 0) vsource type=pulse val0=0 val1=1.2 delay=5n rise=3n fall=2n width=7n period=20n