# Final project

Teamwork: two people a team

## Introduction

In this project, we will learn how to design 8*8 array read-out circuit (clock generators), including frequency divider and decoder. The following picture is the block diagram of the project. You need to finish pre-sim, layout, and post-sim. Moreover, try to optimize the design to reach a higher score.

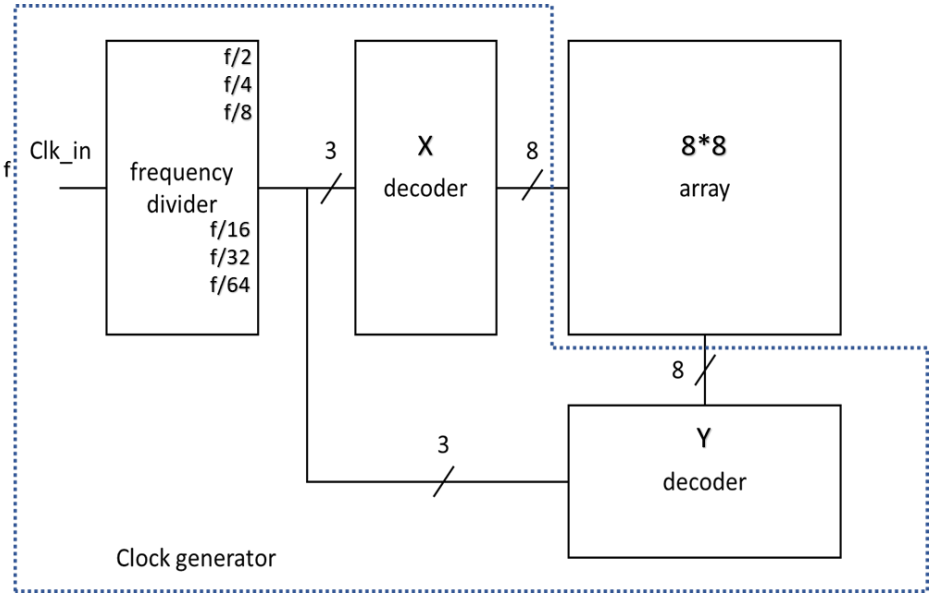



fig1. System block diagram

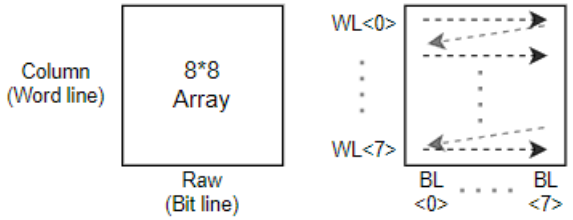



fig2. Array reading order

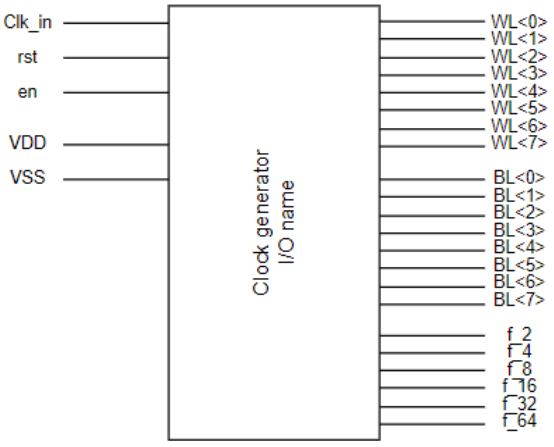



fig3. System I/O name

## Design

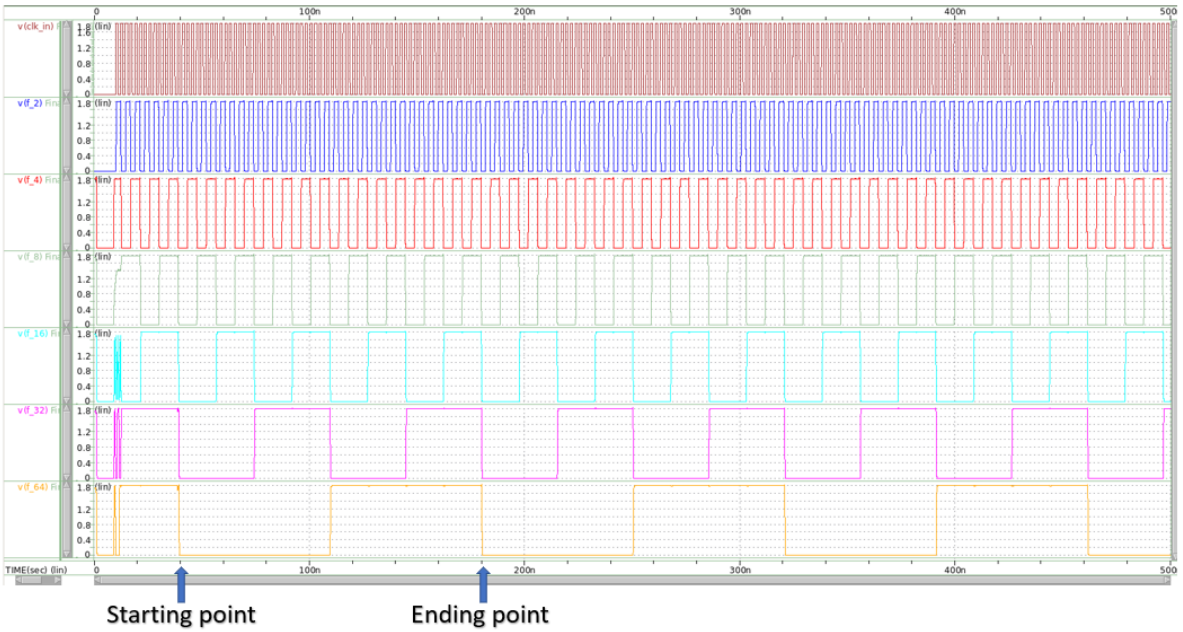
1. Design an inverter.
2. Design a nand.
3. Design two 3 to 8 decoder (X and Y).
4. Design a D flip-flop.
5. Design a frequency divider (6 mode frequency).

## Design Constraints

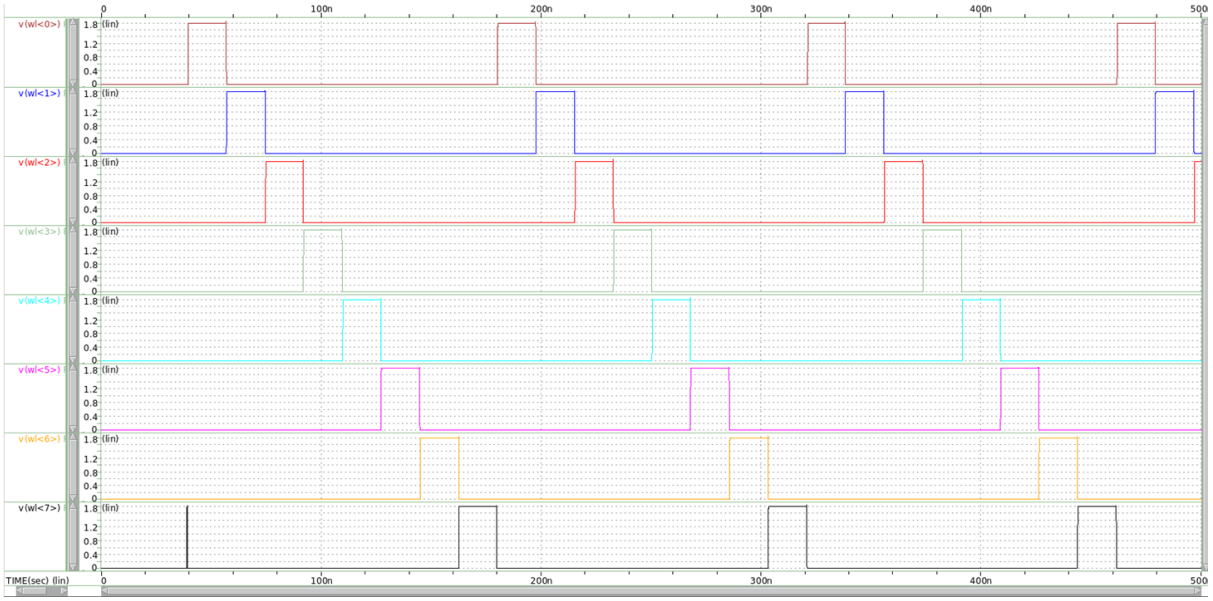
1. Power supply:1.8V
2. Clk_in: the input clock with frequency defined by yourself. (rising / falling time **0.1ns**)
3. With temperature 25˚C for all 5 corners simulation.
4. Layout total area is not limited.
5. .tran simulation time resolution:(1/1000)*(1/fmax), fmax is the maximum frequency of CLK_in.
6. WL<0:7>, BL<0:7> output loading = **0.1pF**
7. .option accurate=1 runlvl=6
8. Frequency divider need to reset at first

## Waveview (TT for example)

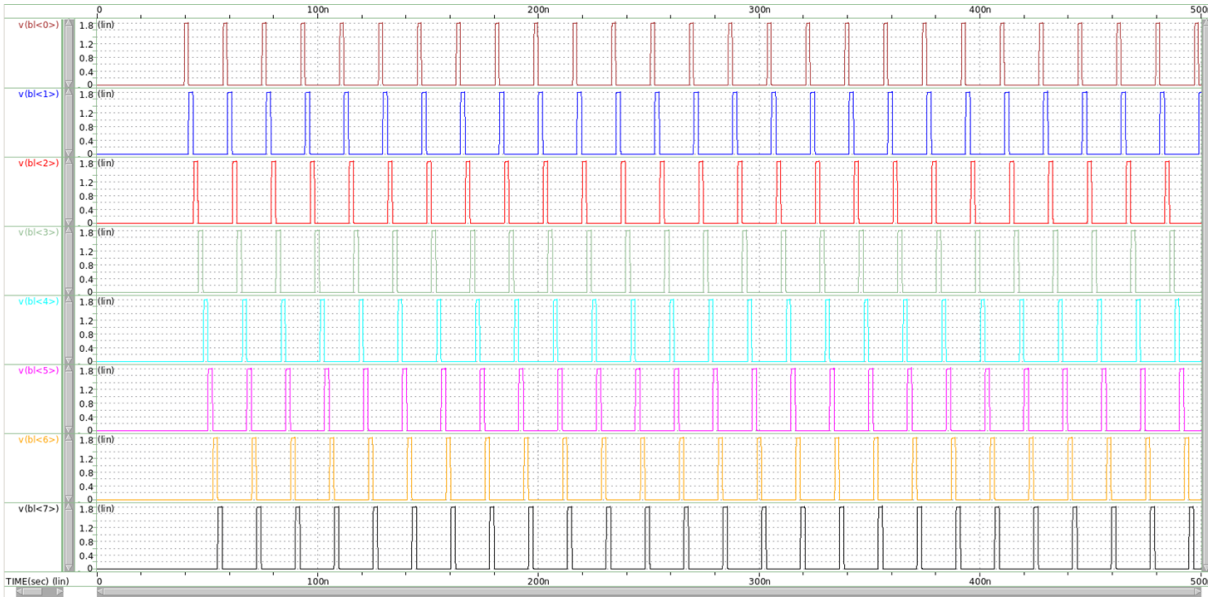
**Frequency divider (f_2 ~ f_64)**



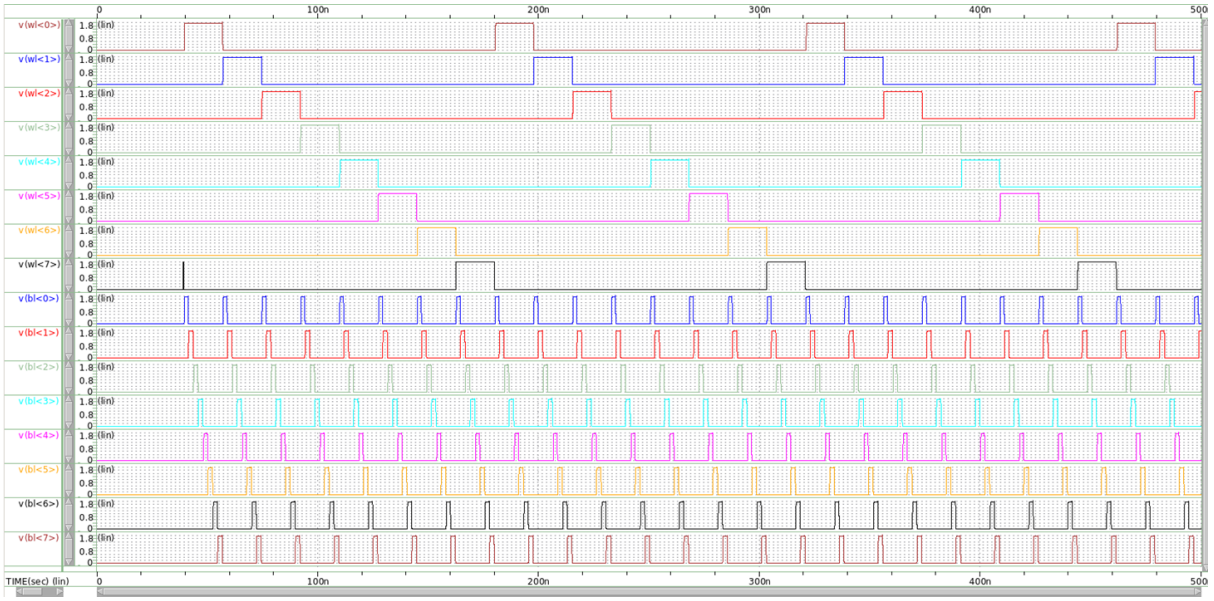

**X decoder (Word line) (WL<0:7>)**



## Y decoder (Bit line) (BL<0:7>)

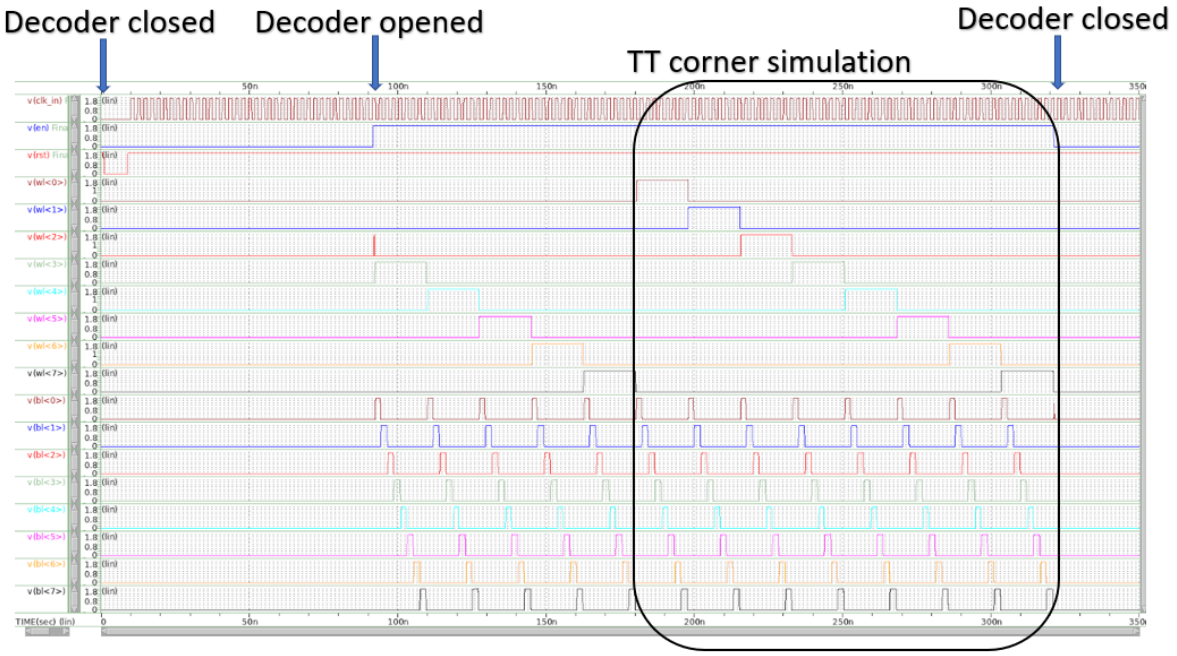


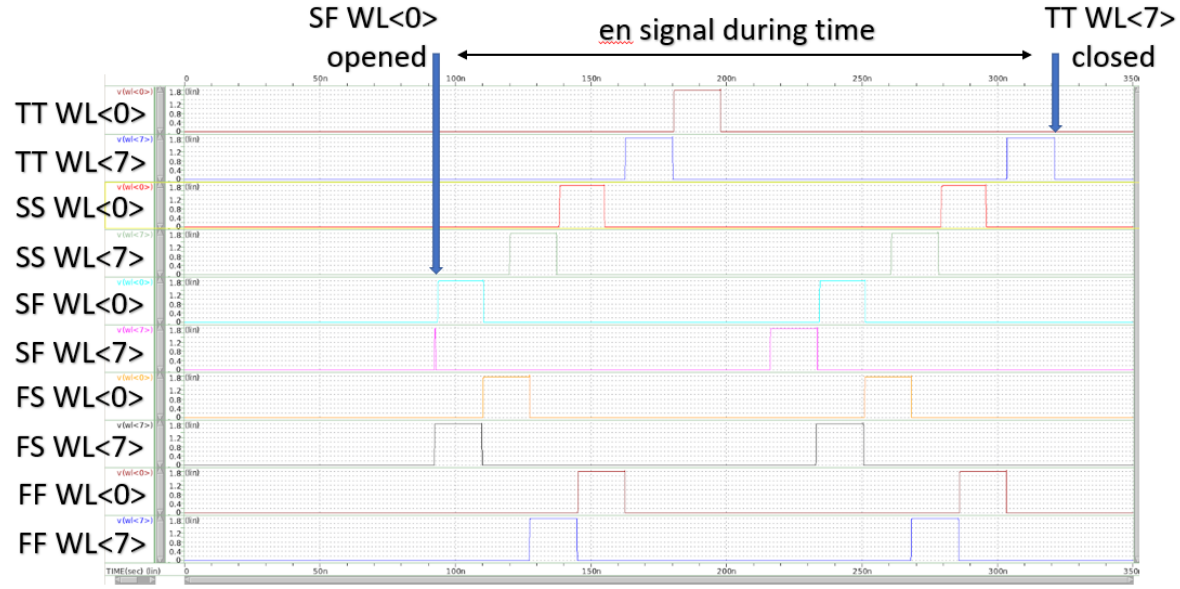

## Read-out diagram




<Note> When WL<n> turns on, BL<0:7> needs to be turned on successively. We need to see that WL<0:7> with its BL<0:7> are all operating successfully in all corners.

**Timing control (rst/en signal are designed by yourself)**

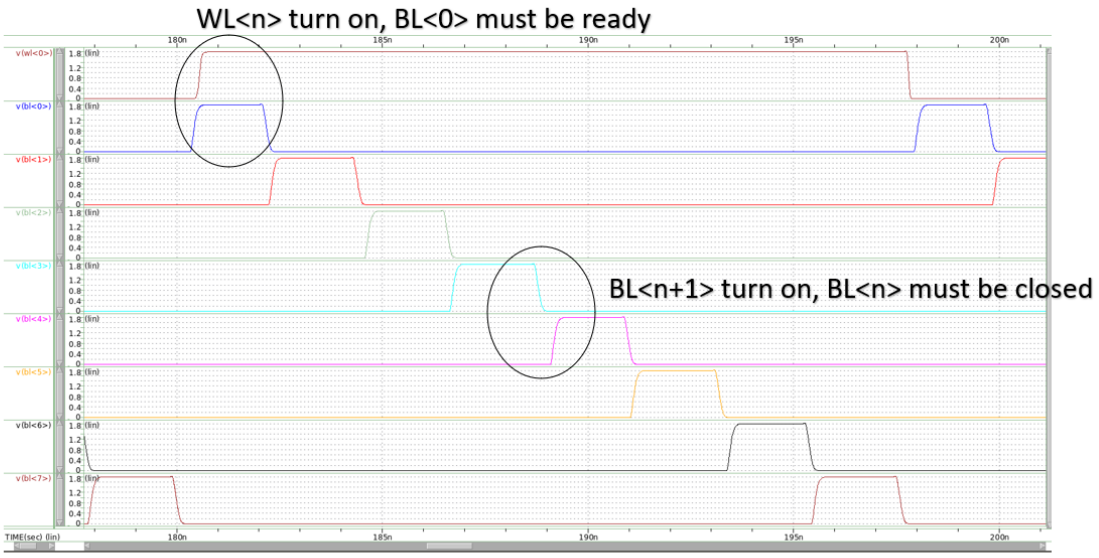



<Note> Your timing control needs to be the same in all corners simulations. After you run the all corners simulations, find out what is the maximum time that en signal should be holded.

<Note> Everyone's design will not be the same including timing and corners simulation results. So, find your own timing control, do not copy TA's timing!

**Some details**




No any glitches on the waveview (overshot are allowed)

## Report (Deadline 1/12)

1. **Design**
   (1) How do you design the circuit?
   (2) Draw the block diagram, circuit schematic of your design.
   (3) Explain the operation of the sub-circuit you used.
   (4) Design constraints.

2. **Layout**
   (1) Print-screen the whole design (measure the area) and sub-circuit
   (2) Print-screen DRC summary with no error
   (3) Print-screen LVS result

3. **Simulation**
   (1) Pre-sim and post-sim results. Mark the delay time and measured data
   (2) Explain the difference between pre-sim and post-sim

## Demo (Pre-sim Deadline 12/1～12/8, Final Deadline 12/29)

1. Demo will be held at DSP lab
2. Show DRC/LVS result
3. Show pre-sim and post-sim waveform
4. Explain how you design it and write down the max frequency your design can operate and your area.

## Score

Report:30%
Functionality: 40%
Performance(you need to finish post-sim ): 30%
For performance,
get 30% for the first place
get 29% for the second place
get 20% for the eleventh place
get 15% for 12~19 place
get 10% for 20~26 place
Get 5% for 27~32 place

$$Performance = Max\ operation\ frequency^2 \div area^2 \div power$$