EE 323002
Lab 4: Cadence Layout Tutorial

Version 1.0 (Sept 2023)

Objective

- To create the mask layout of the inverter defined in lab 2 by using the layout editor **Virtuoso**.
- To use **DRC** (Design Rule Checker) for detecting any layout design rule violations.

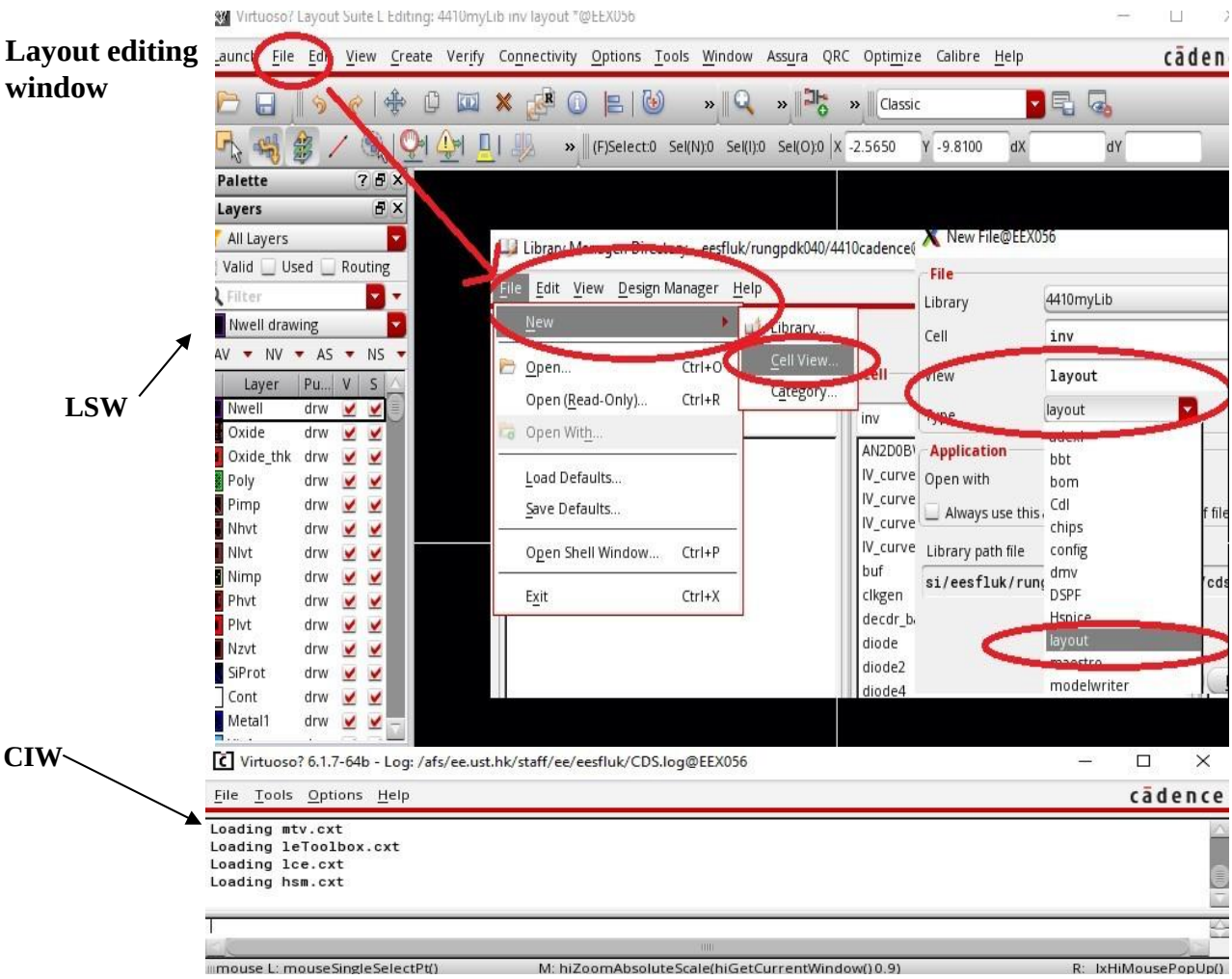
I. Creating a layout view for the inverter design

You created the schematic view and symbol view of your inverter in lab 2. You are going to create the corresponding layout view.

1.1. By using the **Library Manager**, under your design library **323002myLib,** create the ***layout*** view of the ***inv*** cell.

- In **the <u>File ->New-> CellView</u>** <u>Form</u>, remember to select "**Layout**" as the tool to be used.

1.2 With the help of the **Layout Selection Window** (***LSW***), you can draw and edit the mask layout. You should always check for messages shown in the **CIW**.

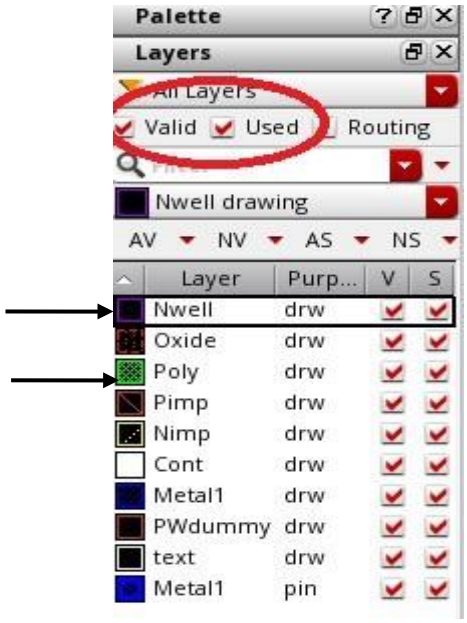


II. Use of the Layer Selection Window (LSW)

The **Layer Selection Window (LSW)** shows you which layout layer is being selected for drawing. For example, if you want to draw **poly gate**, you have to highlight the "**Poly (drw)**" field in the LSW, hence, what you draw then is for the poly mask.

It shows that **Nwell (drw)** becomes the current entry layer

If click on **Poly(drw)** becomes the current entry layer



Important Notes:

You have to know the design rules before drawing anything.
Here is the reference video for you to learn how to draw an inverter. But there are some differences between 'laker' and 'virtuoso'. Please study online by yourself, and you are welcome to ask questions on eeclass discussion area.
https://www.youtube.com/watch?v=O0Z1ELxZV1E

This table describes the layers used to create devices.

Comment Table

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
Bondpad	36	0	Bondpad	Bondpad	drawing	95	252	Bonding Pad
CapMetal	14	0	CapMetal	CapMetal	drawing	97	252	MiM capacitor metal
Nburied	19	0	Nburied	Nburied	drawing	18	252	N+ Buried Layer
Nhvt	18	0	Nhvt	Nhvt	drawing	11	252	NMOS High Vt
Nlvt	26	0	Nlvt	Nlvt	drawing	26	252	NMOS Low Vt
Nimp	4	0	Nimp	Nimp	drawing	12	252	N+ Implant
Nwell	2	0	Nwell	Nwell	drawing	6	252	Nwell
Nzvt	52	0	Nzvt	Nzvt	drawing	15	252	NMOS Zero Vt
Oxide	1	0	Oxide	Oxide	drawing	2	252	Active Area
Oxide_thk	24	0	Oxide_thk	Oxide_thk	drawing	4	252	1.8V Active Area
Phvt	23	0	Phvt	Phvt	drawing	13	252	PMOS High Vt
Plvt	27	0	Plvt	Plvt	drawing	27	252	PMOS Low Vt
Pimp	5	0	Pimp	Pimp	drawing	14	252	P+ Implant
Poly	3	0	Poly	Poly	drawing	10	252	Poly
SiProt	72	0	SiProt	SiProt	drawing	16	252	Salicide Block

Table 1: Device Layers

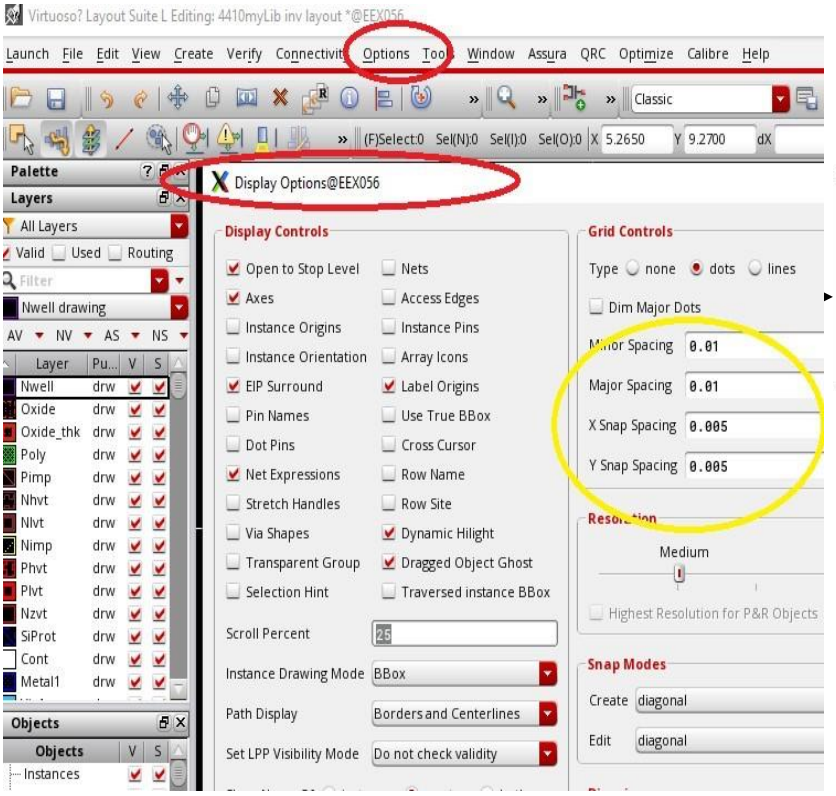
III. The Virtuoso Layout Editing Window

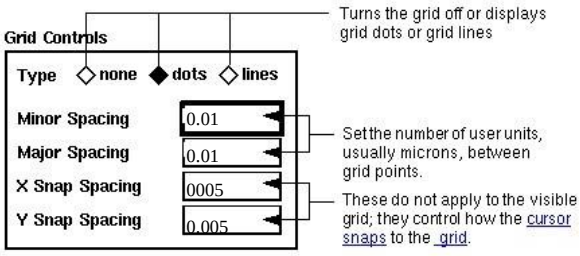
Very important things on layout drawing,

1. We are using 180nm technology, the description is 'TSRI 0.18um 1.8V/3.3V 1P6M Virtual Mixed Mode CMOS Process'.
2. Default unit for layout drawing dimension is micro-meter, μm.
3. The design rules (design rules file at the given link on page 2) and the lambda rule use the value of lambda $\lambda = 0.01\mu m$ for the given technology.
4. The resolution for mask making, i.e. the smallest dimension achievable, is 0.005μm.

Before drawing the first block in the editing window, you have to set the display options **properly** by using the above information!!

- Check the display option and see whether they are appropriate or not. Click on **Options → Display**
- The X and Y snap spacing should **not be smaller** than the smallest dimension which is 0.005 (i.e. the resolution for mask making).



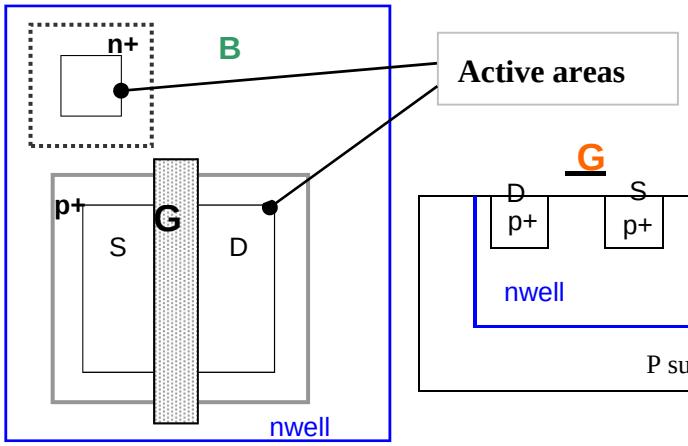


These values are very important to your layout drawing. If you fail to set the correct values above, you may need to redraw everything again.

Note: we have set above values for you in the system. These are now the default values.

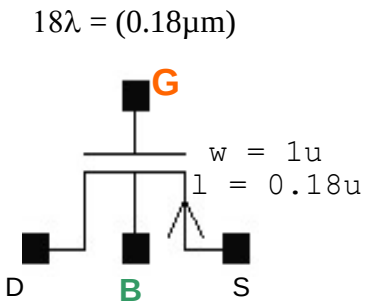
IV. Creating PMOS Transistor Layout

We will guide you how to draw the layout of a PMOS transistor step by step below. In layout view we use polygons to represent transistors and all device elements. The minimum allowable geometry dimensions are all listed in Design Rules file. The value of lambda (λ) is **0.01μm**, and the smallest dimension you can draw is 0.005μm. (Note: the following figures are not drawn to scale)



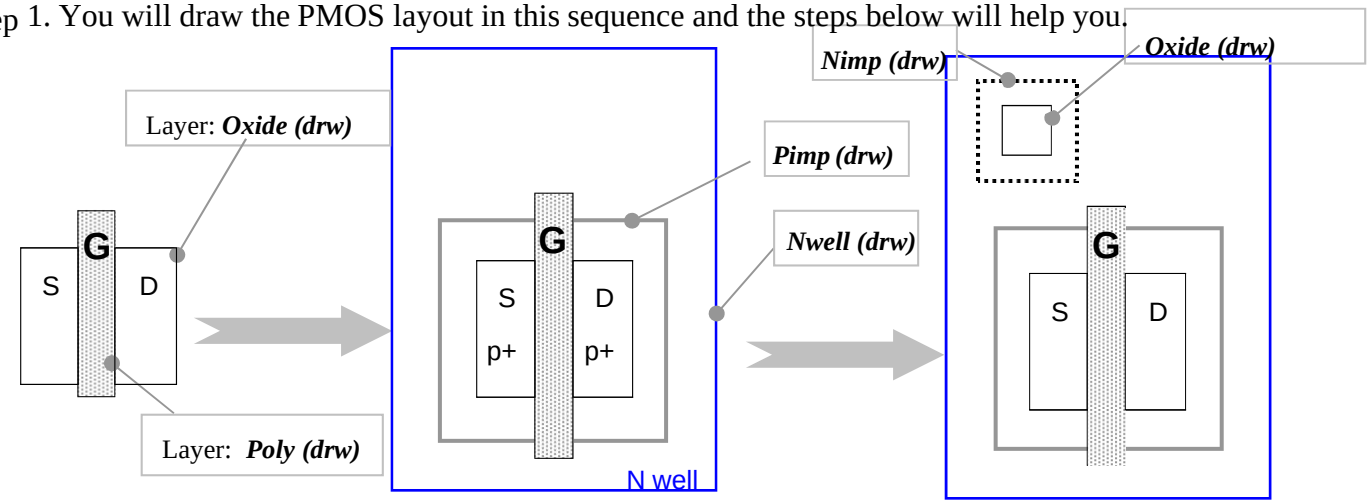
Layout view

PMOS cross-section



Schematic view

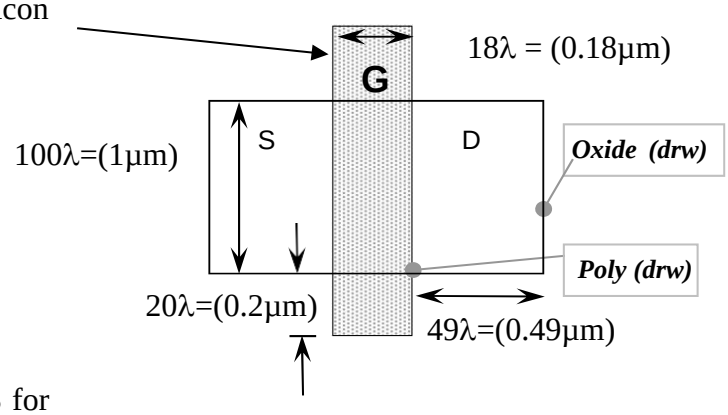
Step 1. You will draw the PMOS layout in this sequence and the steps below will help you.



1.1. The first thing to draw is the polysilicon block; click on the '***Poly (drw)'*** box in the **LSW** first.

- Hence any geometry being drawn is on the polysilicon layer then.

1.2. Click on ***Create*** → ***Rectangle*** to draw the polysilicon gate in the layout editing window.

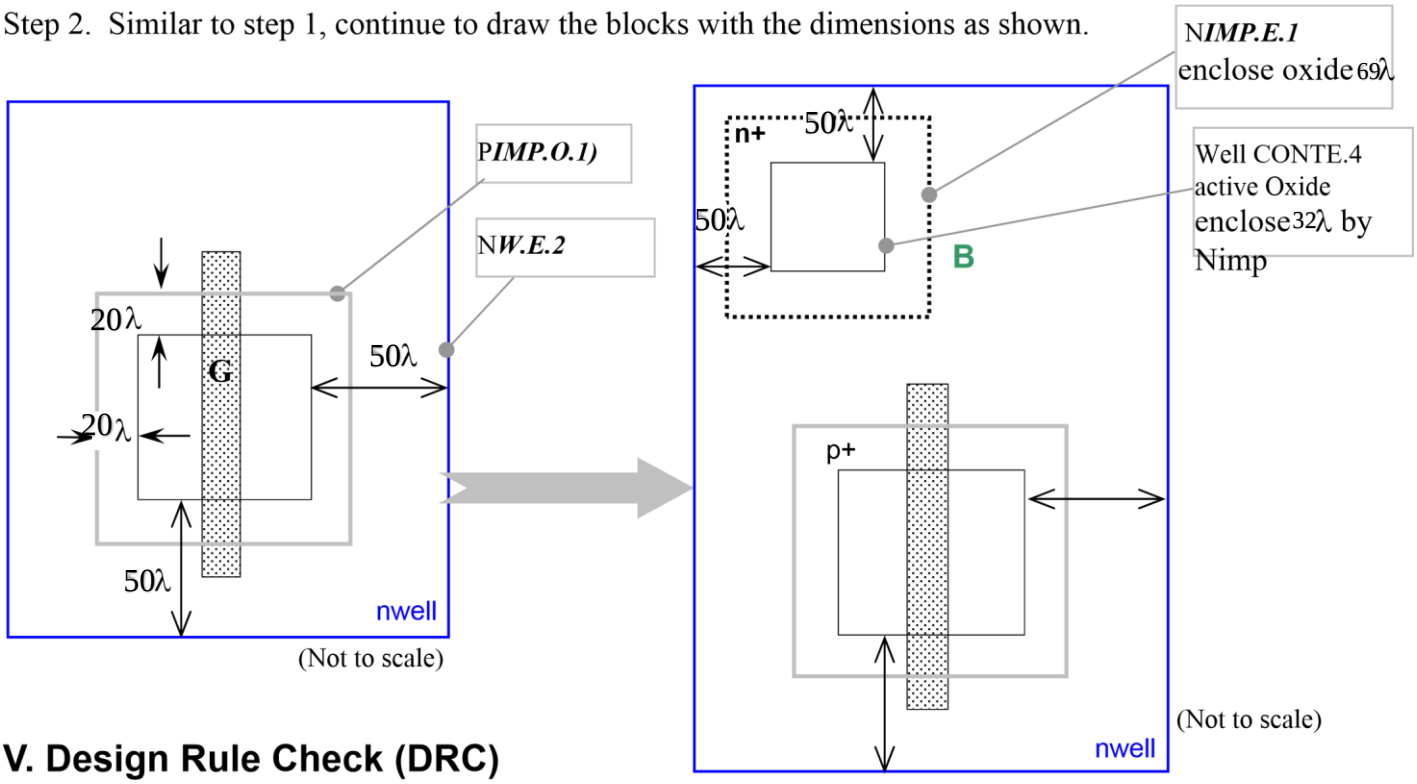


1.3 You are going to draw the active area (the ***Oxide*** layer),
click on '***Oxide (drw)'*** in the **LSW first.**

1.4. Draw the blocks with the dimensions as shown in right

- You can use the **Ruler** to measure the dimension; Click on ***Window*** → ***Create Ruler*** then press **F3** for options.
- To remove the Ruler by ***Window*** → ***Delete All Rulers***
- You can also use '**Stretch**' to help you to extend blocks in all directions by ***Edit*** → ***Stretch***
- You can **check**/**change** the properties (the size, place & layer) of rectangles by ***Edit*** → ***Properties.*** (this is a very useful command for drawing or editing shapes, try it out yourself!)

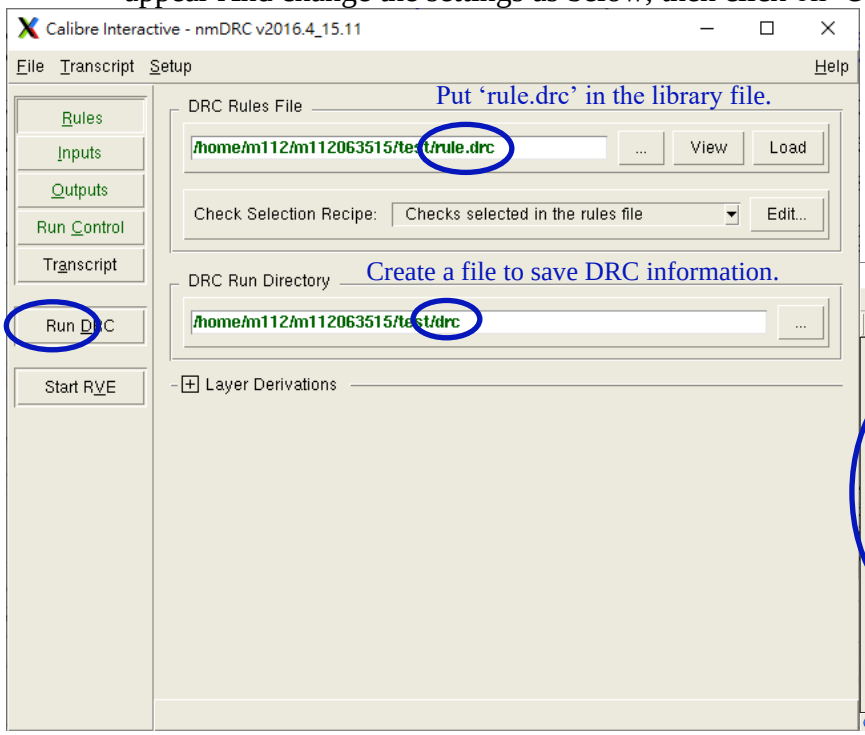
Step 2. Similar to step 1, continue to draw the blocks with the dimensions as shown.

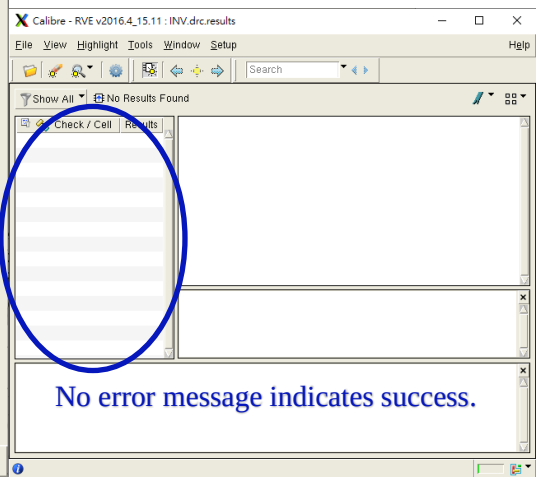


V. Design Rule Check (DRC)

In order to lower the probability of fabrication defects, the mask layout must conform to a set of design rules. You should perform **DRC** frequently while you are drawing the layout. The tool called Design Rule Checker, which is built into the layout editor, is used to detect design rule violations.

Step 3. Use your current layout to run a DRC, ***Calibre → Run nmDRC,*** and the DRC form will appear And change the settings as below, then click on '***OK***' to start the checking.



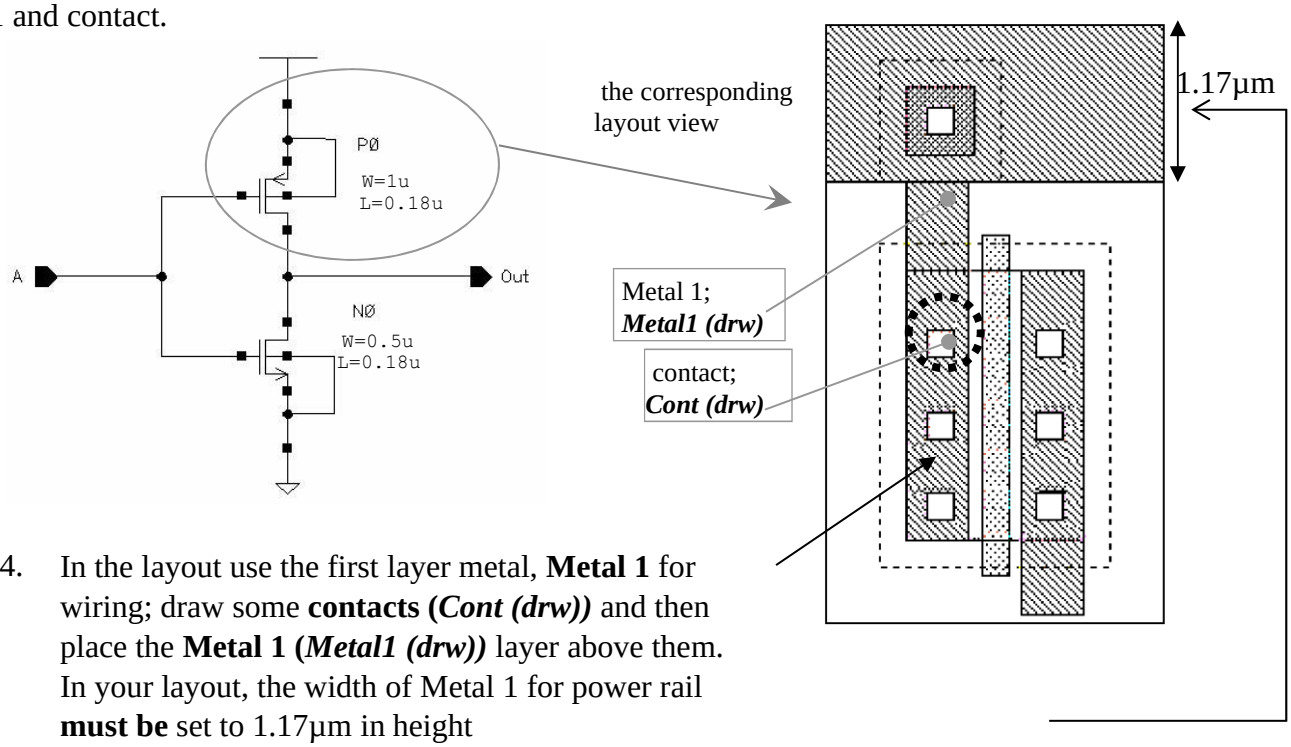


3.1 It may take some time to finish the checking. As it finished, windows will prompt out automatically, then click on 'Yes' to see the result. If there is error, you have to correct it at once, and then do the DRC again to verify. The DRC checker (the Error Layer Window) will tell you what the errors are, and can help you to locate them. Please ask TA for help if necessary.

3.2 If there is no error or you have fixed all the errors, you can proceed to the next part - wiring the transistor.

VI. Wiring the Transistor

You now have a PMOS transistor layout, which has passed ***DRC***. Then we will wire the transistor with Metal 1 and contact.



Step 4. In the layout use the first layer metal, **Metal 1** for wiring; draw some **contacts (*Cont (drw)*)** and then place the **Metal 1 (*Metal1 (drw)*)** layer above them. In your layout, the width of Metal 1 for power rail **must be** set to 1.17µm in height

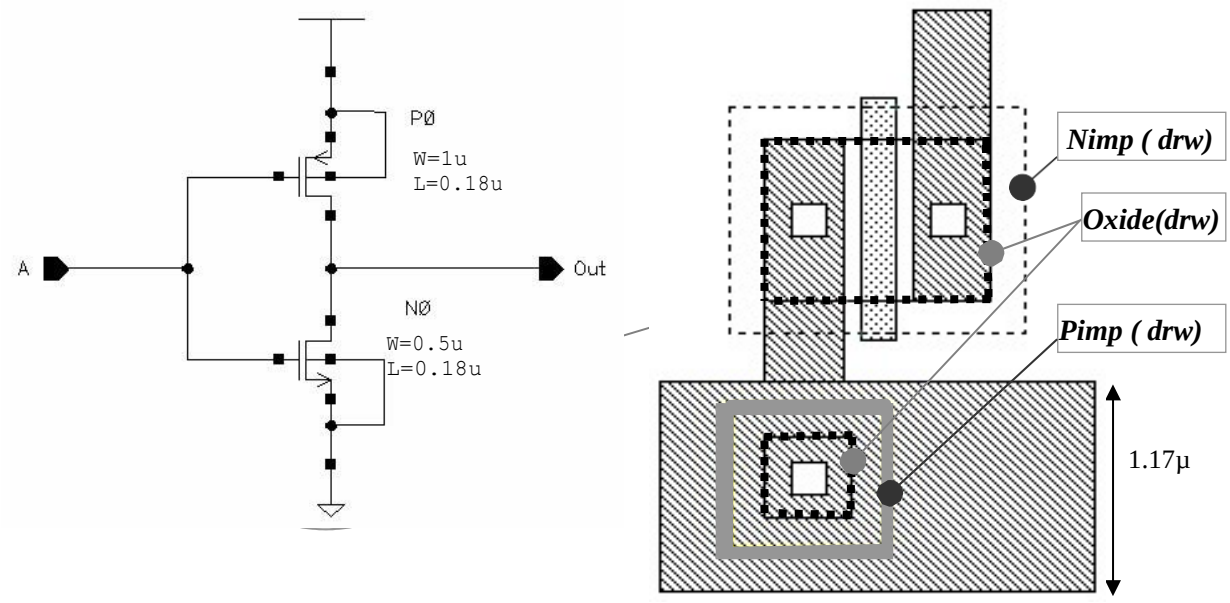
To draw the contacts and metal 1 wires as above, you have to determine their dimension/spacing constraints by checking the design rules of contact layer and metal 1 layer yourself, then undergo DRC to check for any errors, fix them for any. (The design rules of CONT.E.1/2 METAL1.E.1 may help) page 44/109, page 49/109.

VII. Creating NMOS Transistor Layout

You are going to draw the NMOS layout.

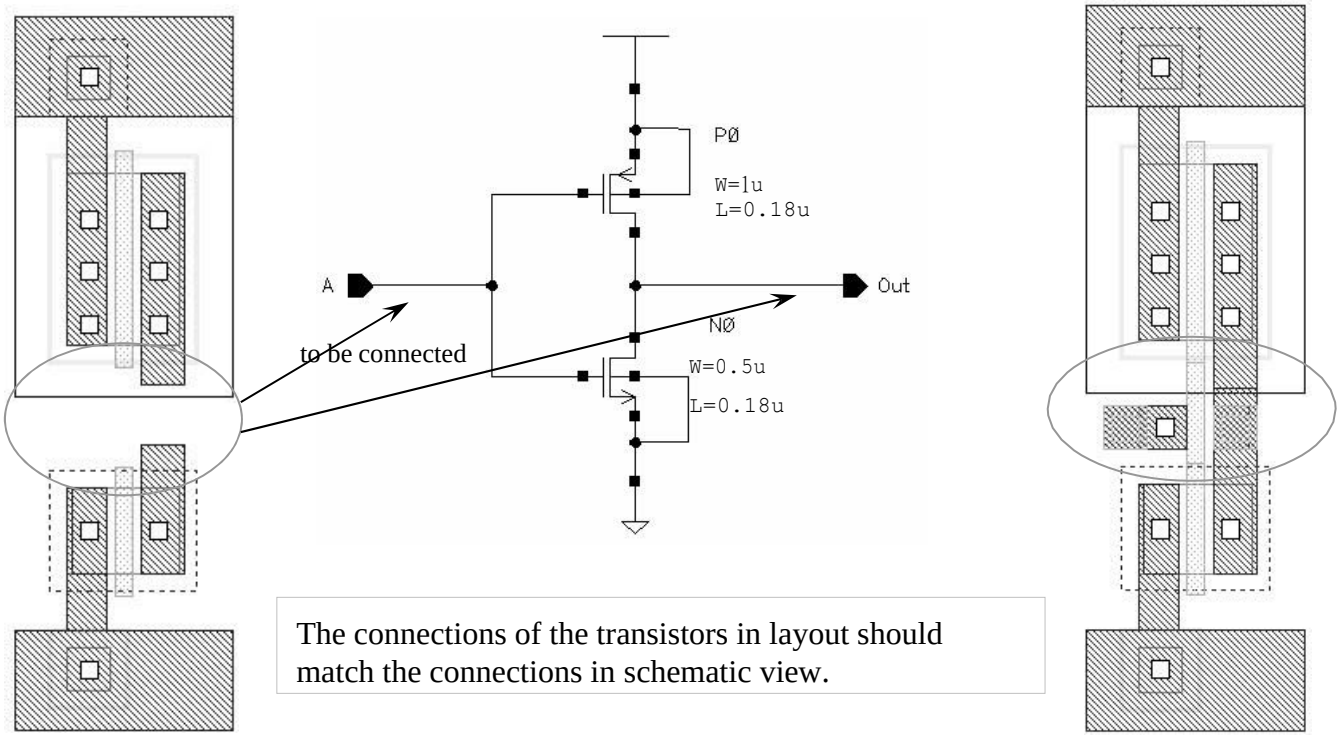
Step 5. Using the similar procedure as drawing PMOS, draw the NMOS transistor as shown below and place it below the PMOS transistor. The gate width of PMOS 100λ NMOS should be 50λ.

- Run the DRC, and fix errors if there is any.



VIII. Connecting NMOS and PMOS Transistors Together

You have finished the NMOS and PMOS transistors of the ***inv*** cell. Make sure they pass the design rules check (DRC). The next step is to make the internal and the external connection for the ***inv layout view***.

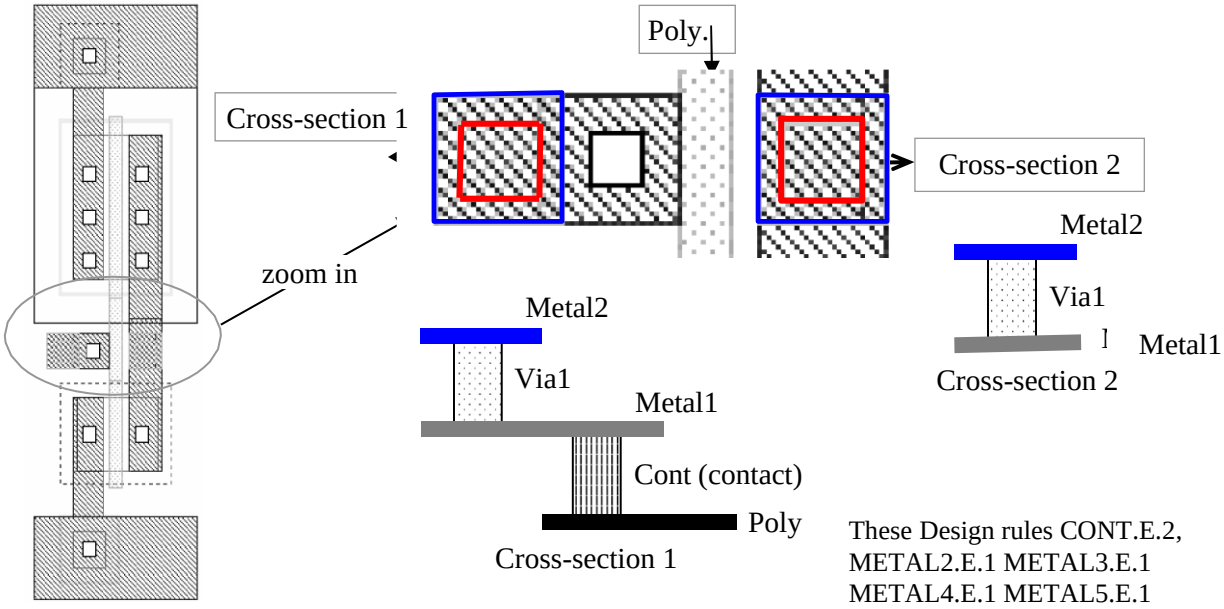


The connections of the transistors in layout should match the connections in schematic view.

Step 6. As above pictures, connect the two transistors' **Poly** rectangles together (i.e. their Gate terminals), and connect the two transistors' **Metal1** rectangles together (i.e. their Drain terminals).

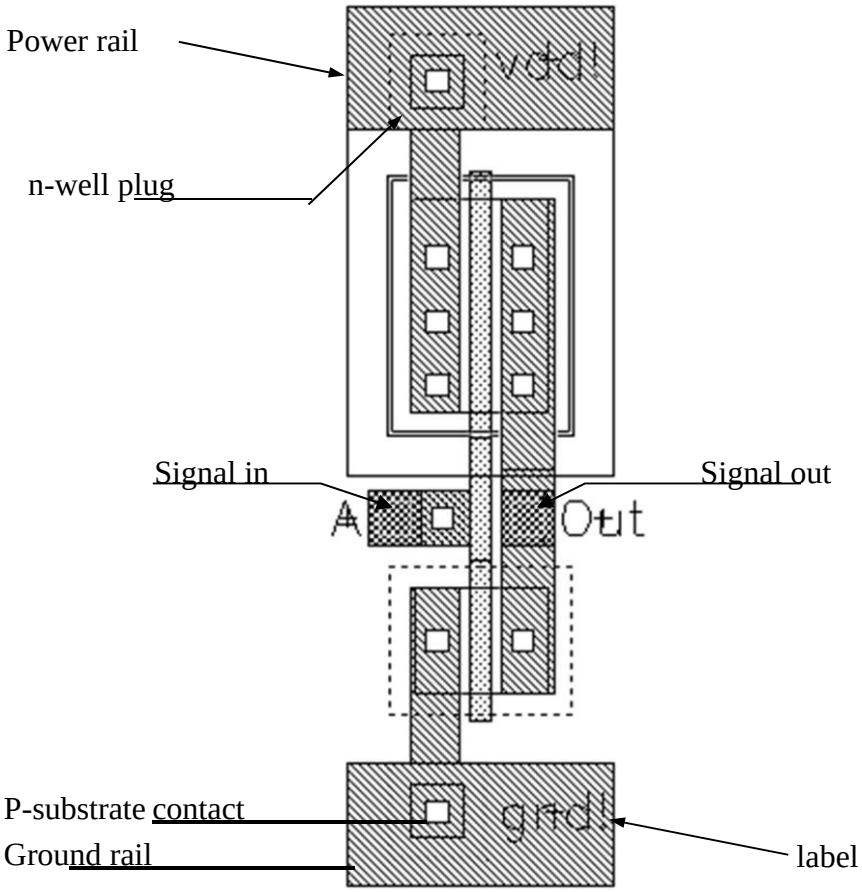
- To do so, we can use the ***Edit → Stretch*** to help.
  Refer to the above pictures for correct connections.

6.1. To make connections for external circuit (for input pin A and output pin Out):
Make the interconnection as shown below, determine the dimensions by checking the design rules of contact, via1, metal 1 and metal 2 layers yourself, then undergo DRC to check for any errors.



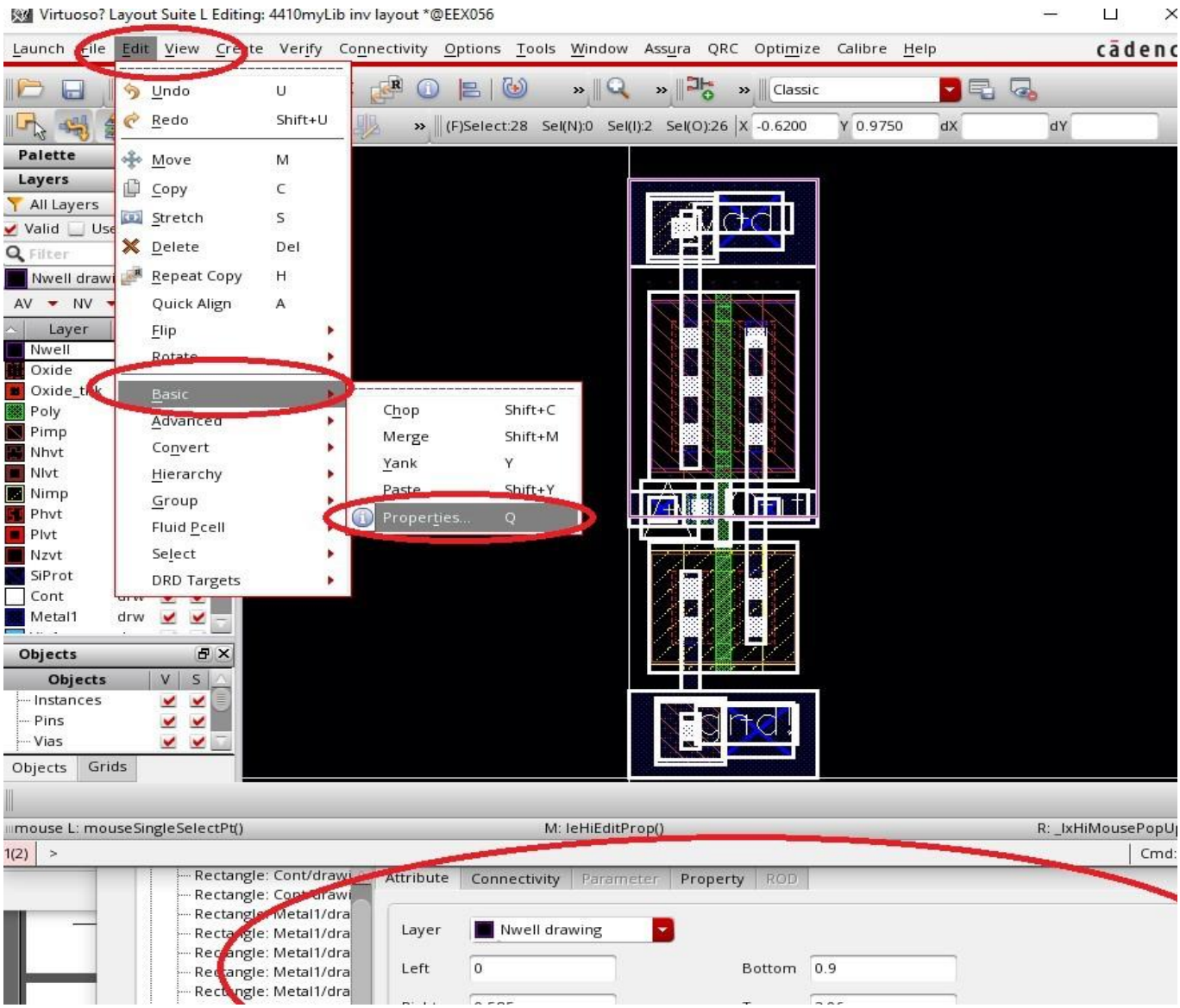
These Design rules CONT.E.2, METAL2.E.1 METAL3.E.1 METAL4.E.1 METAL5.E.1 METAL6E.1 ... etc page 52/109

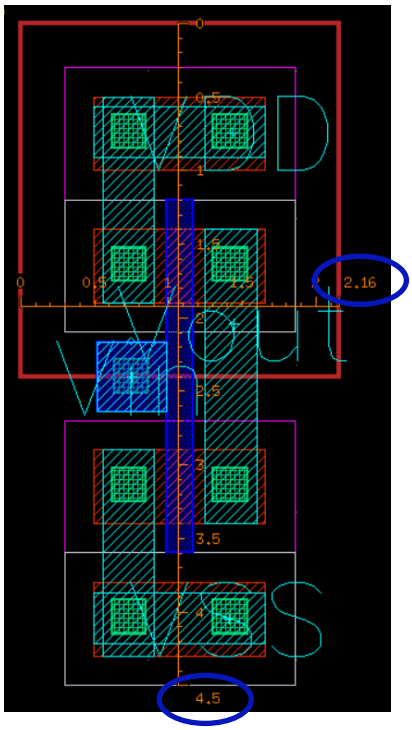
Step 7. Run DRC again and check for any error, and correct them if there is any.



Area of the Layout : have to select the Layout structure so it is highlighted

To find the area of the layout, select all layouts, click on ***Design → Properties,*** the coordinates of the boundary boxof your layout will be shown. For example, in this case, the area of the layout is x*y = z μm^2. It needs your own reading and calculate the area..??





Or, you can press ‘k’ to measure the length and width of the layout. The area is equal to maximum width * maximum length.

For example, the right hand side inverter layout area is 2.16*4.5=9.72um^2.

IX.Setting Layer Visibility and Selectivity using the LSW

You have basically finished the ***inv*** layout. However, you may want to check/look into the transistor design layer by layer. The Layer Selection Window (**LSW**) allows you to set particular layers selectable and visible.

Step 9. To make the layers invisible, click on the '***Metal1 (drw)'*** in the LSW. Then click on '**NV**' button at the top, then ***'Window'*** → ***'Redraw'*** in the layout editing window to refresh the screen.

- Note that except the Metal1 layer all other layers are hidden. To show the hidden layers, click on '**AV**' button and click on ***'Window'*** → ***'Redraw'***.
  (**AV**: all visible; **NV**: Not visible)

Step 10. To make the layer unselectable (inactive), move the cursor over the '***Metal1 (drw)'*** in the LSW then click the right mouse button. The function is very useful if there are too many layers overlapping each other.

- The right mouse button toggles layer selectivity, try it out! If '***Metal1 (drw)'*** field's background color becomes grey, it means that the layer has been made unselectable (inactive) in the layout window. If you right click on it one more time, it will become active again. These functions can also be applied by clicking on the '**NS**' and '**AS**' buttons (AS: All selectable, NS: Not selectable).

Step 11. Well done!! Show your layout and DRC results to TA!

The END of Lab4