EE 323002
Lab 5: Layout Versus Schematic (LVS)

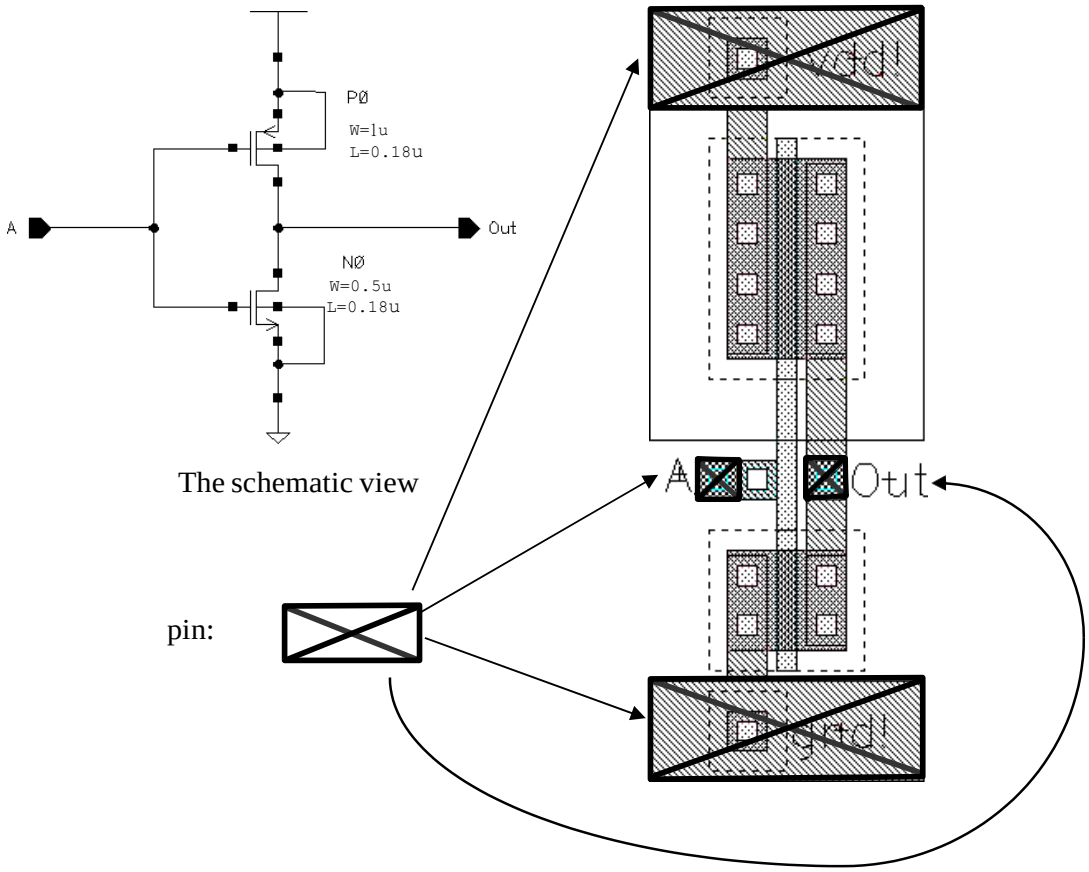
Version 1.0 (Sept 2023)

Objective

- To complete the inverter's layout by establishing inverter's external connections (vdd!, gnd!, A & Out) using **Pins**.
- To check any inconsistency between the inverter's layout and its schematic views by **LVS** (Layout versus Schematic Check).
- To create the layout view of your **nand2** cell and perform **DRC** and **LVS**.
- To design a buffer, create its schematic, symbol, layout, and perform **LVS**.

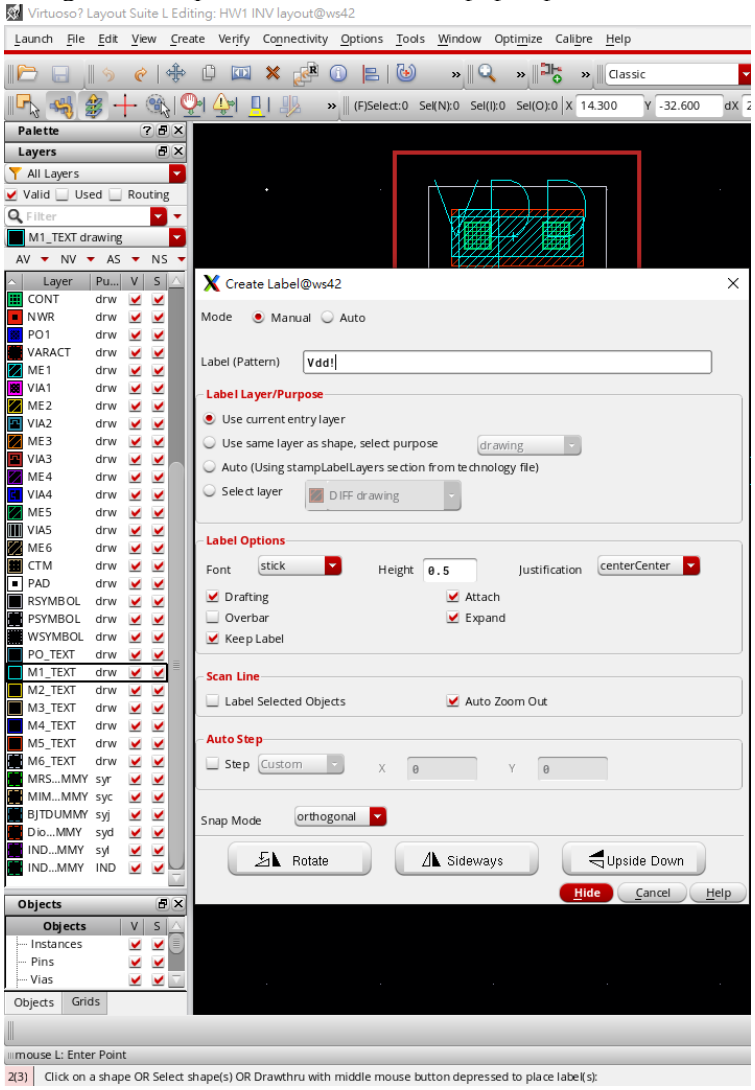
I. Creating Pins in Layout View

You finished most of the layout drawing in lab4. In this part, pins will be defined and drawn, after which the layout design will be complete. Pins locate <u>where</u> to connect from a cell/instance/block to the 'outside world' (external connections), and different names are given for pins of different purposes. There are total 4 pins in our inverter, i.e. on the **inv schematic view**, they are **vdd!**, **gnd!**, **A** and **Out**.



To create pins, open the layout view of the ***inv*** cell,

- In LSW, select the layer '**M1_text**' (this is a key step!)**.** '**M1_text**' stands for pin text defining on Metal 1 layer.
- In the layout editing window, press '**l**' and this form pops up,



- In the Create Label form, type in the pin's name '**vdd!'**, then draw on the layout as shown on page 1.
- To create pin for **gnd!, A, and Out** in the same way.

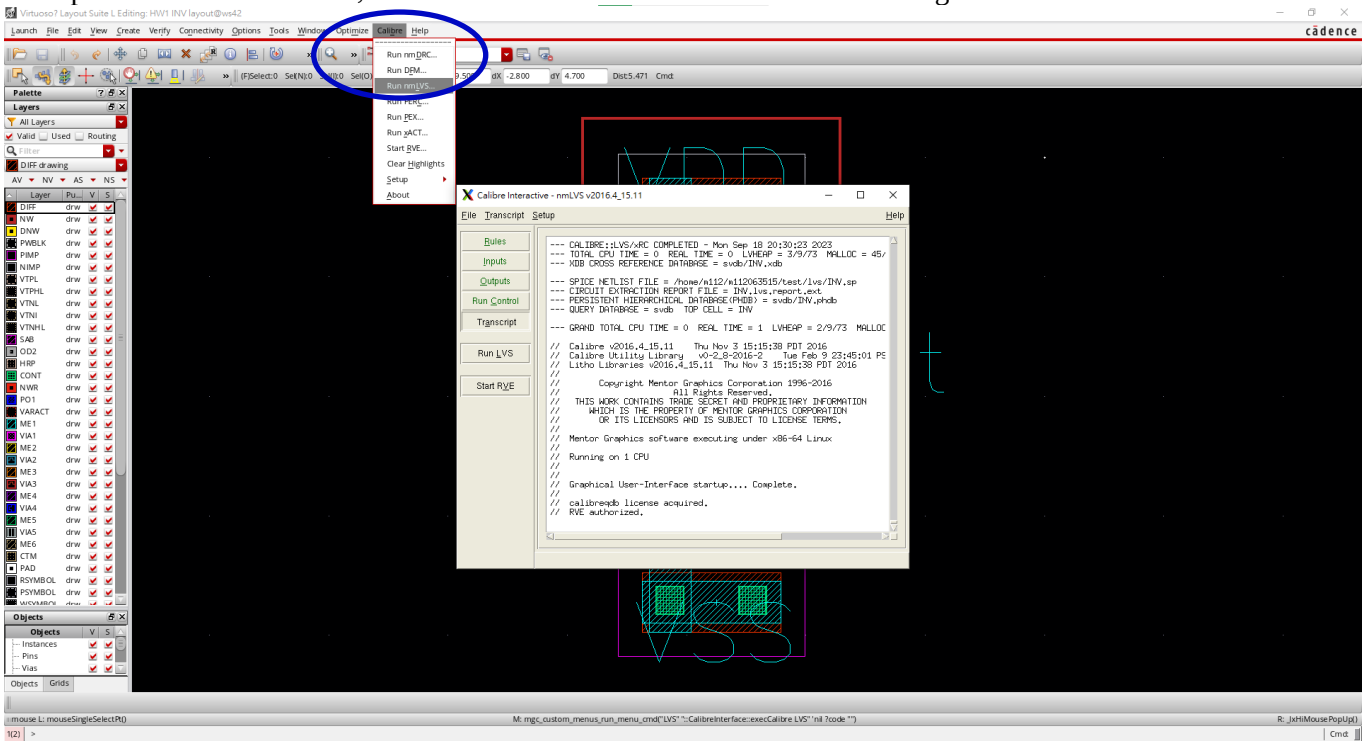
Well done!! You have finished the inverter layout design. You have to run the DRC again to ensure it passes the DRC.

II. Layout versus Schematic Check (LVS Check)

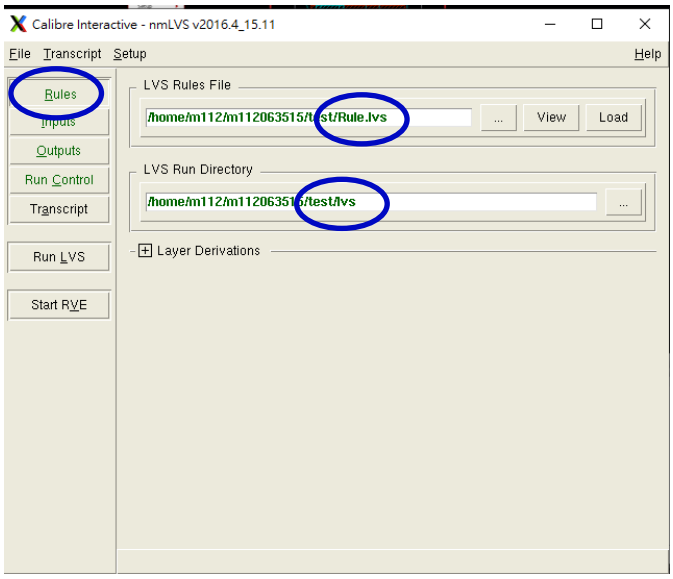
You are ready to carry out the Layout versus Schematic Check (LVS). It is an important step because the layout drawing is based on its schematic, the devices' dimensions and connection in the layout should be consistent with that in the schematic. In order to ensure the layout design is matched with its schematic view totally, the layout versus schematic check (**LVS**) must be performed.

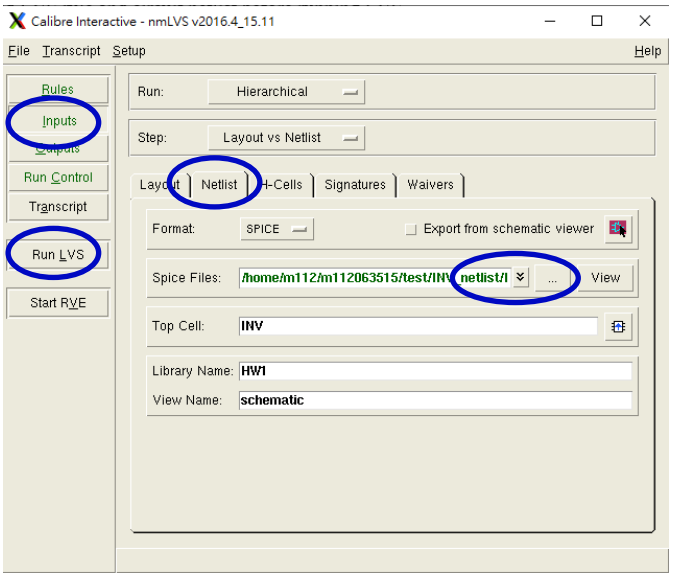
The layout view represents the circuit topology, which consists of layers of rectangles only! How can the system recognise devices and their connectivity in the layout view? While LVS is running, Cadence will look for the technology file which contains the electrical rules. These rules define structures, for example if overlapping poly layer, Nimp layer and Oxide layer are present, that will be considered as a NMOS transistor. Therefore, gates and electrical connections are traced out and identified from their layout view. Only then the layout and schematic views can be compared.

Step 3. To start the LVS, click on ***Calibre*** → *Run nmLVS.* Use the settings as below.

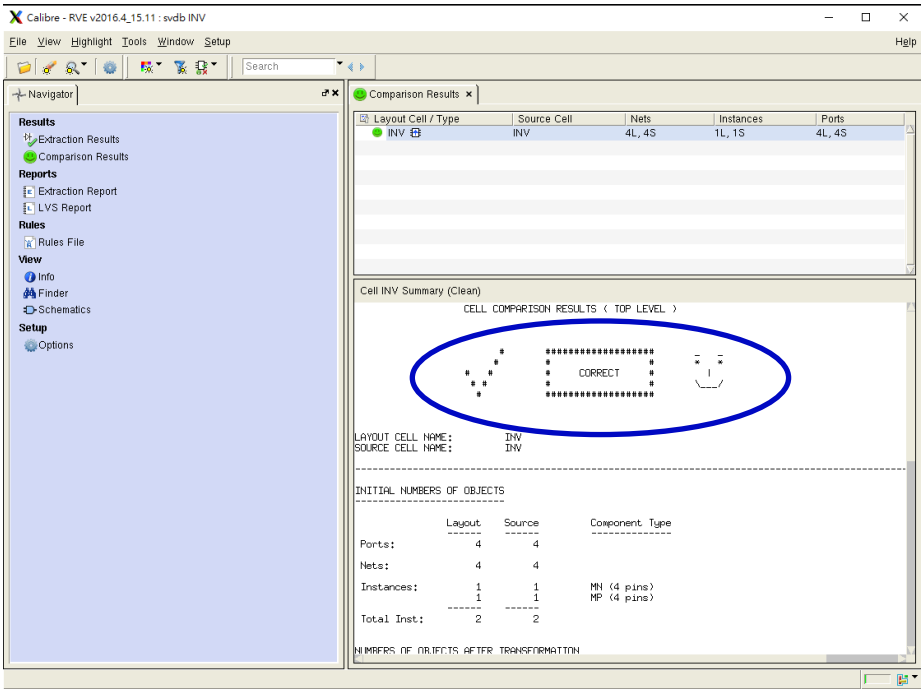


Step 4. Add LVS rule and circuit netlist before running LVS.



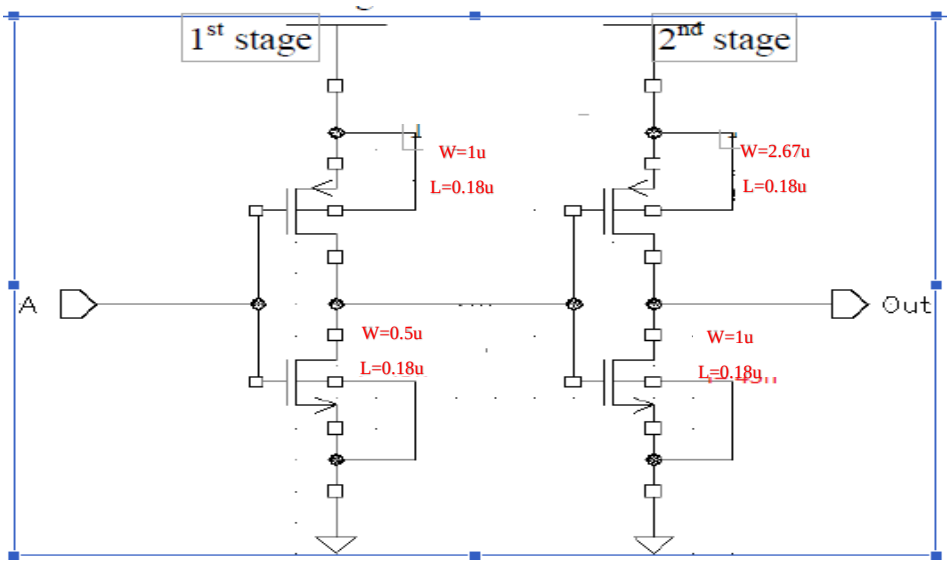


- A "Progress" window will prompt out automatically as the LVS check finished. As the schematic view matched its "layout view", the message “Smiling face” would showed, otherwise, mismatches would be listed out.
- Else debug window would pop up guide you to debug schematic and layout views. Ask for help if necessary.



III. Designing a buffer

You are required to design a two-stage buffer (cell's name: ***buf***). A two-stage buffer is made of 2 inverters cascaded together. The width and length of the transistors are given below. Your buffer design has to include its schematic view, symbol view and layout view. Moreover, the layout view has to be DRC and LVS passed. What is the scaling factor of this buffer?



Read below messages carefully,

1. Create the schematic view of the buffer.
2. Create the layout view, it must be DRC passed. The ground and power rails **must be** set to 1.17μmin height (same as your ***nand2*** design on page 6). You have to use ***metal 1*** for ground and power rails, and ***metal 2*** for connecting external circuit at Pins A and Out. The height of your design should be the same everywhere.
3. Perform LVS, the layout view should match its schematic view.

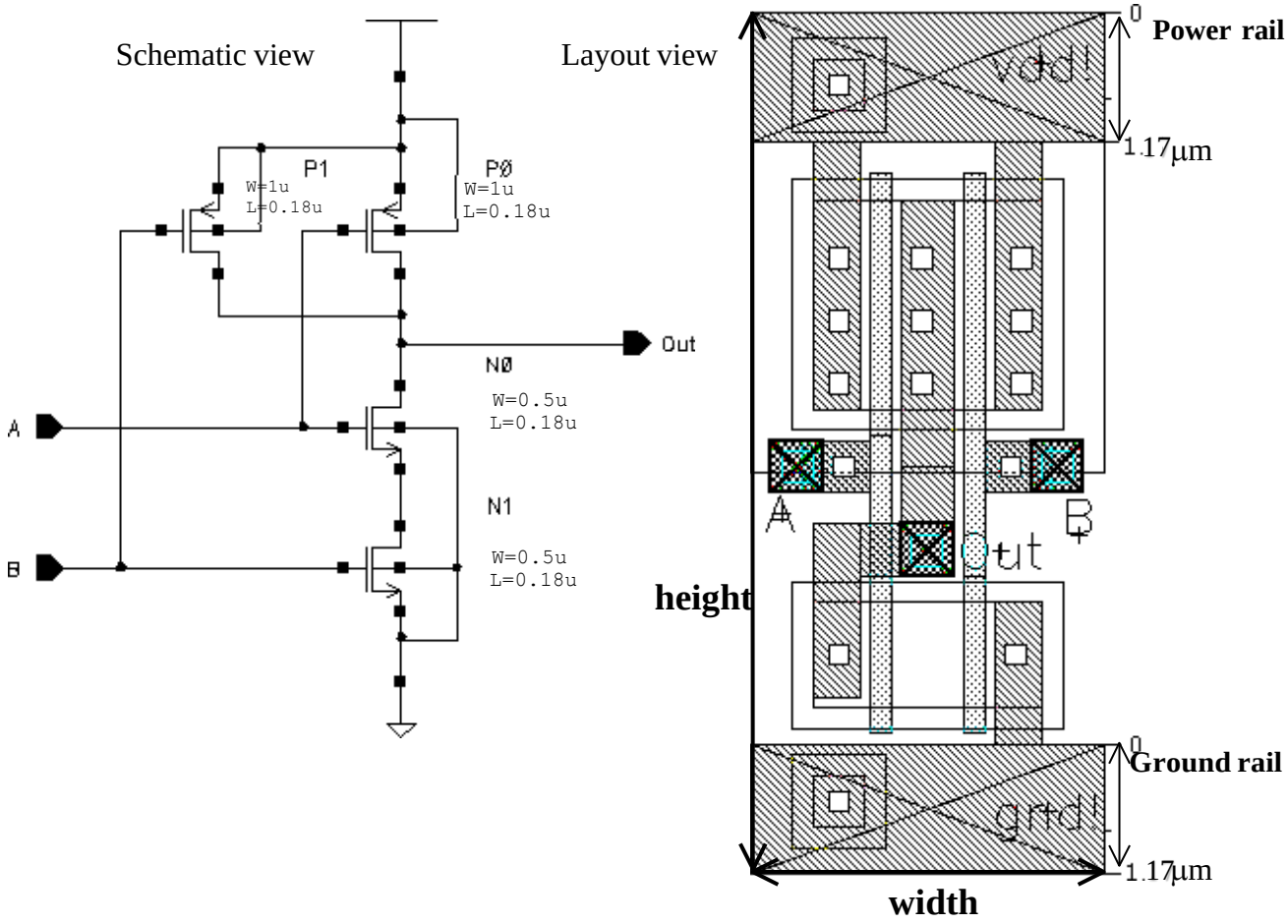
Hint: - you have finished an inverter design before, modify that inv design to build the ***buf***'s schematic and layout views.

IV. Creating the Layout of the 2-input NAND gate

You built the schematic view of the ***nand2*** cell in lab 3. You can start drawing the **nand2** layout view; refer to lab 4 if necessary. The **nand2** layout may look like below (for your reference only!!).
Hint: you have finished a DRC passed inverter's layout, **modify** that layout for ***nand2***'s layout.

Read the messages below carefully,

1. In your layout, the ground and power rails **must be** set to 1.17μm in height.(as shown in the picture below).
2. You have to use ***Metal 1*** for ground and power rails, and ***Metal 2*** for connecting external circuit at Pins A, B and Out.



Target: Perform LVS. Correct mismatches if there are any. The nand2's layout must match its schematic view. Ask for help if necessary.

V. Standard-cells based design

We have developed some commonly used logic cells; inverter, buffer and nand gate in our **323002myLib** library. All the cells' layouts should be designed with a **fixed height** so that they can be abutted side by side to forms rows for sharing a common power and ground bus. Moreover, these fixed height cells can enable automated placement and routing of cells.

Step 1. **Readjust** the **layouts** of **inv** cell, **nand2** cell and **buf** cell to the **same height**.

- Re-run DRC and LVS checks to make sure all views are correct and updated.

The End of Lab5

Appendix I: More about LVS

If the LVS checker reports that the schematic and layout do not match each other, you have to find, check and correct the errors.

To know what is unmatched, you have to understand the terms used in the debug window:

Instance - The instance of devices in 'layout' and in 'schematic'.

Unmatched instances - The instance of devices in 'layout' and in 'schematic' do not match with each other.

Rewired instances - LVS recognizes that a better match can be made by switching the terminal connection of an instance from one net to another. This is referred to as a rewired terminal. For this to occur, many of the instances and nets in the local region must have already matched. This kind of error occurs when two nets are cross-wired. The LVS program interchanges the connection and continues processing.

Size errors – Size Difference in W & L values**,** LVS compares transistors' W & L values only when the instances are matched with each other in its schematic and layout. Any unmatched instances will not be compared.

Pruned instances - You may ignore this error.

Nets – interconnection node.

Merged nets - A second class of unmatched nets is the merged nets. In some cases, LVS recognizes that two nets need to be "shorted" together to improve the comparison. This occurs when many of the instances attached to the nets have already matched. When two nets need to be merged in the extracted representation, it indicates the possibility of an open. When two nets are merged in the schematic representation, it indicates the possibility of a short in the layout.

Pruned nets - You may ignore this error.

Terminals – pins for input, output and power.

Unmatched terminals - Terminals (Pins) that failed to match in layout as compared to those in schematic.