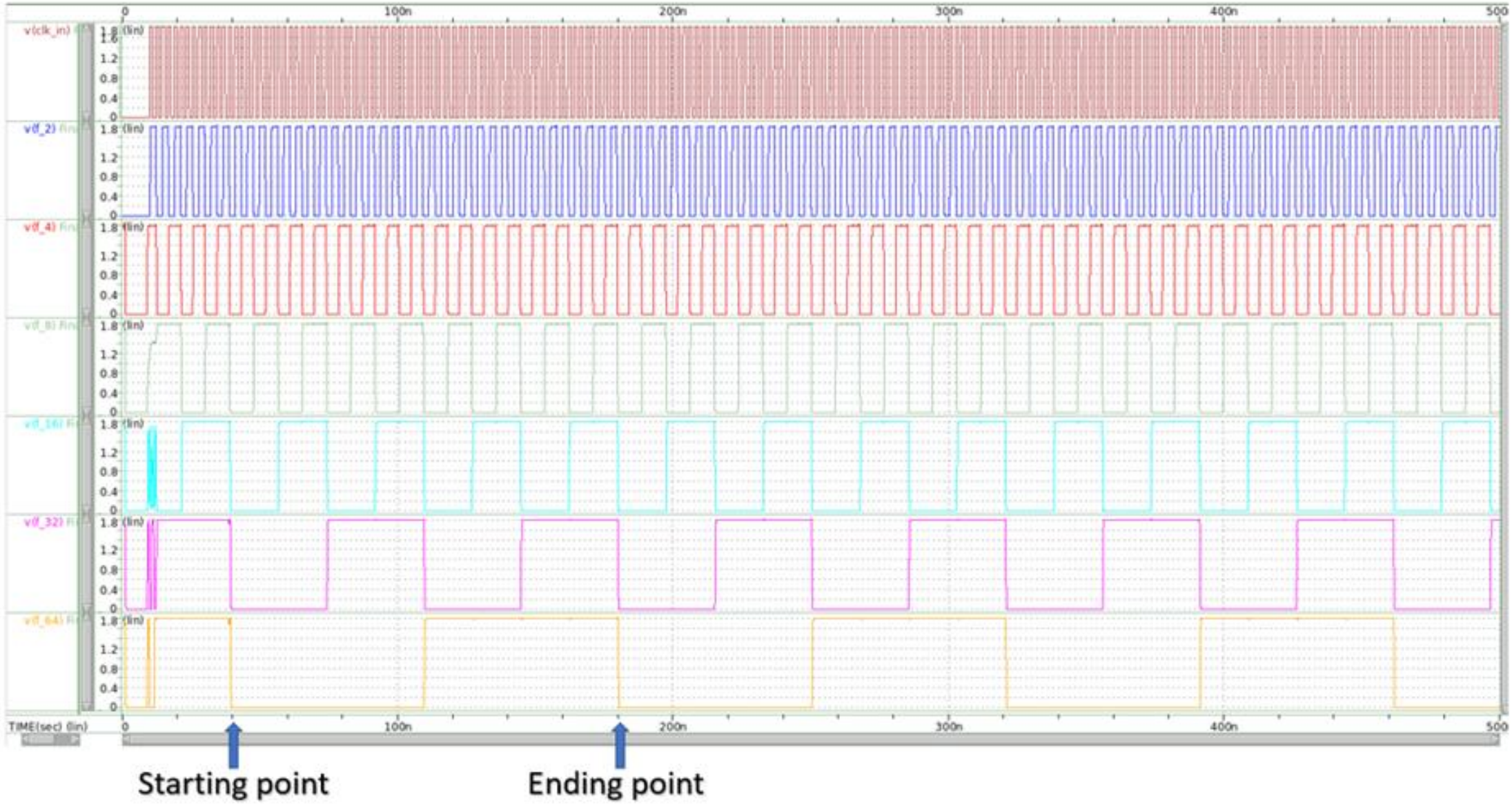
Final project

Demo standard

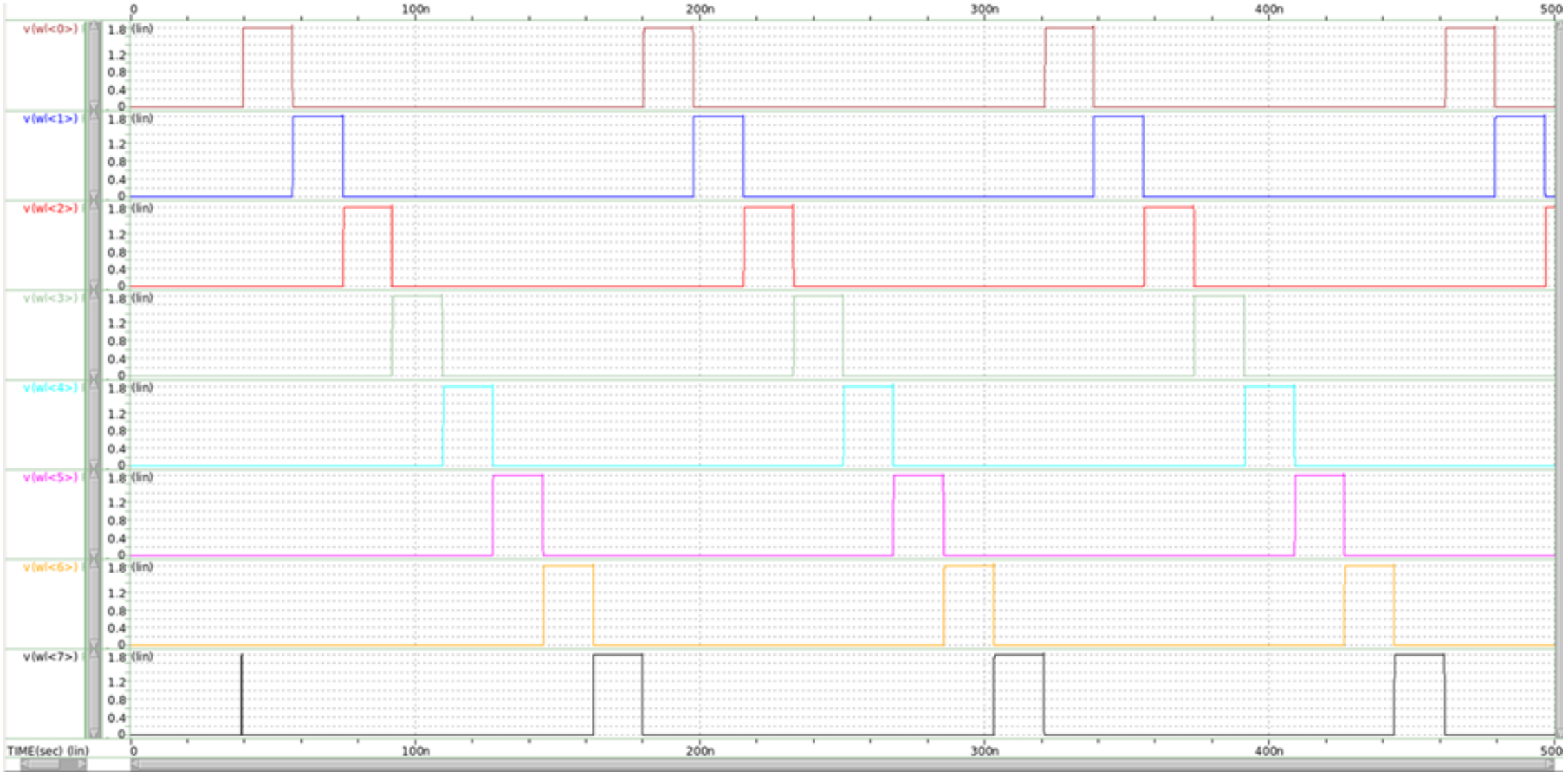
Design Constraints

- 1. Power Supply:1.8V
- 2. Clk_in: the input clock with frequency defined by yourself.
  rising / falling time 10% x pw(s)
- 3. With temperature 25˚C for all 5 corners simulation.
- 4. Layout total area is not limited.
- 5. .tran simulation time resolution:(1/1000)*(1/fmax), fmax is the maximum frequency of CLK_in.
- 6. WL<0:7>, BL<0:7> output loading = 0.1pF
- 7. .option accurate=1 runlvl=6
- 8. Frequency divider need to reset at first

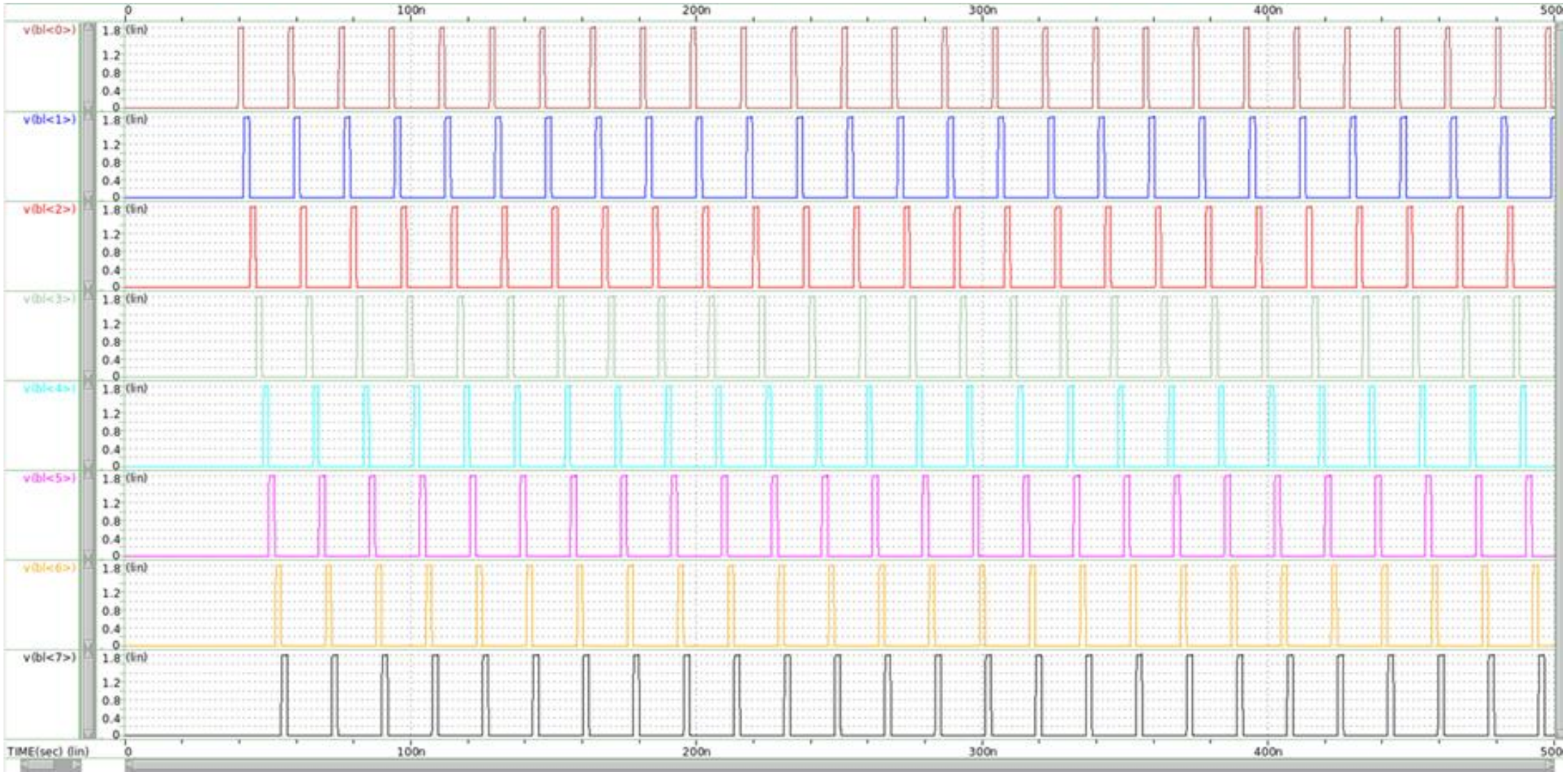
Waveview (TT for example)-Frequency divider (f_2 ~ f_64)



Waveview (TT for example)-X decoder (Word line)(WL<0:7>)

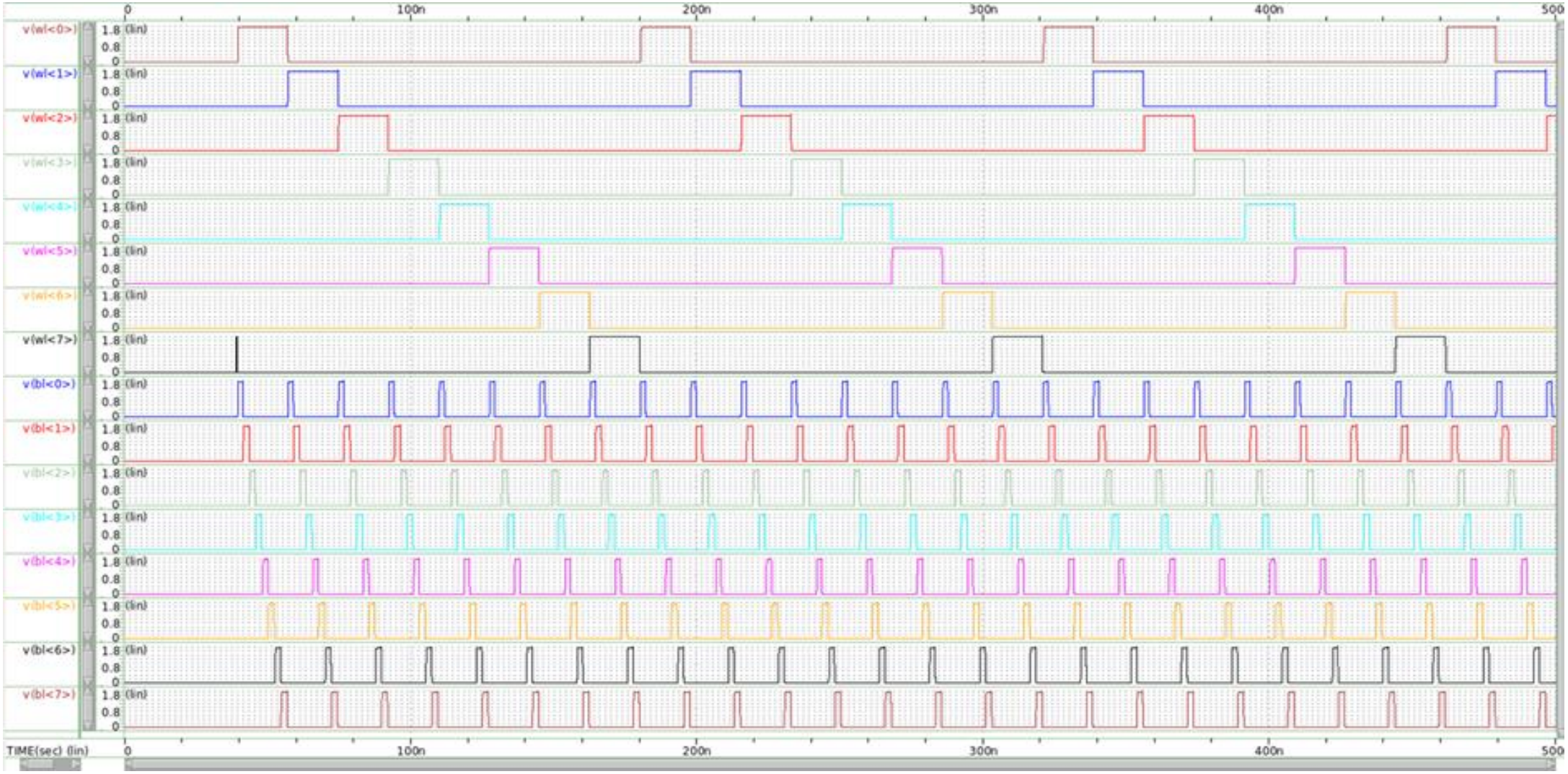


Waveview (TT for example)-Y decoder (Bit line) (BL<0:7>)



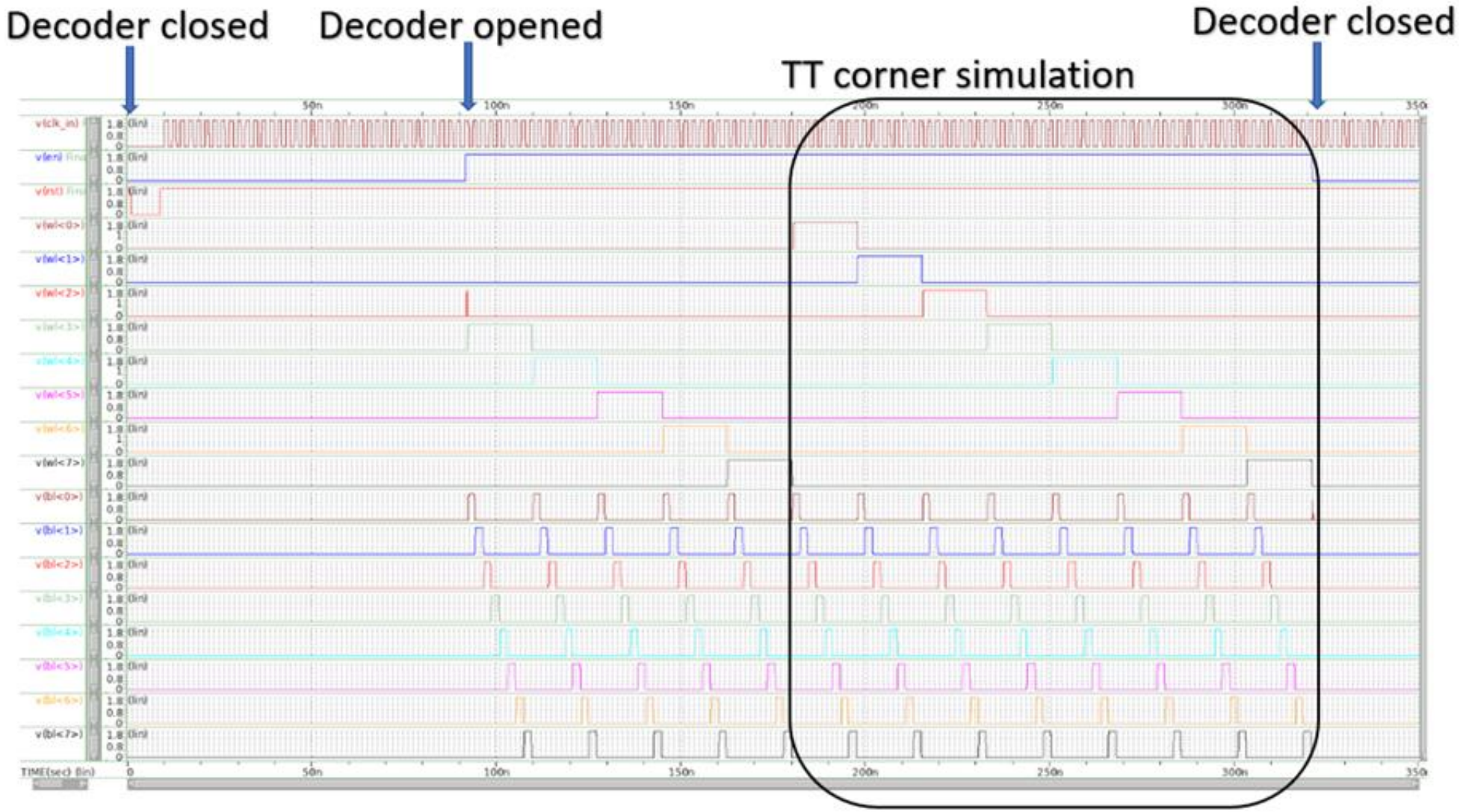
Waveview (TT for example)-Read_out diagram

<Note> When WL<n> turns on, BL<0:7> needs to be turned on successively.We need to see that WL<0:7> with its BL<0:7> are all operating successfully in all corners.



Waveview (TT for example)-Timing control

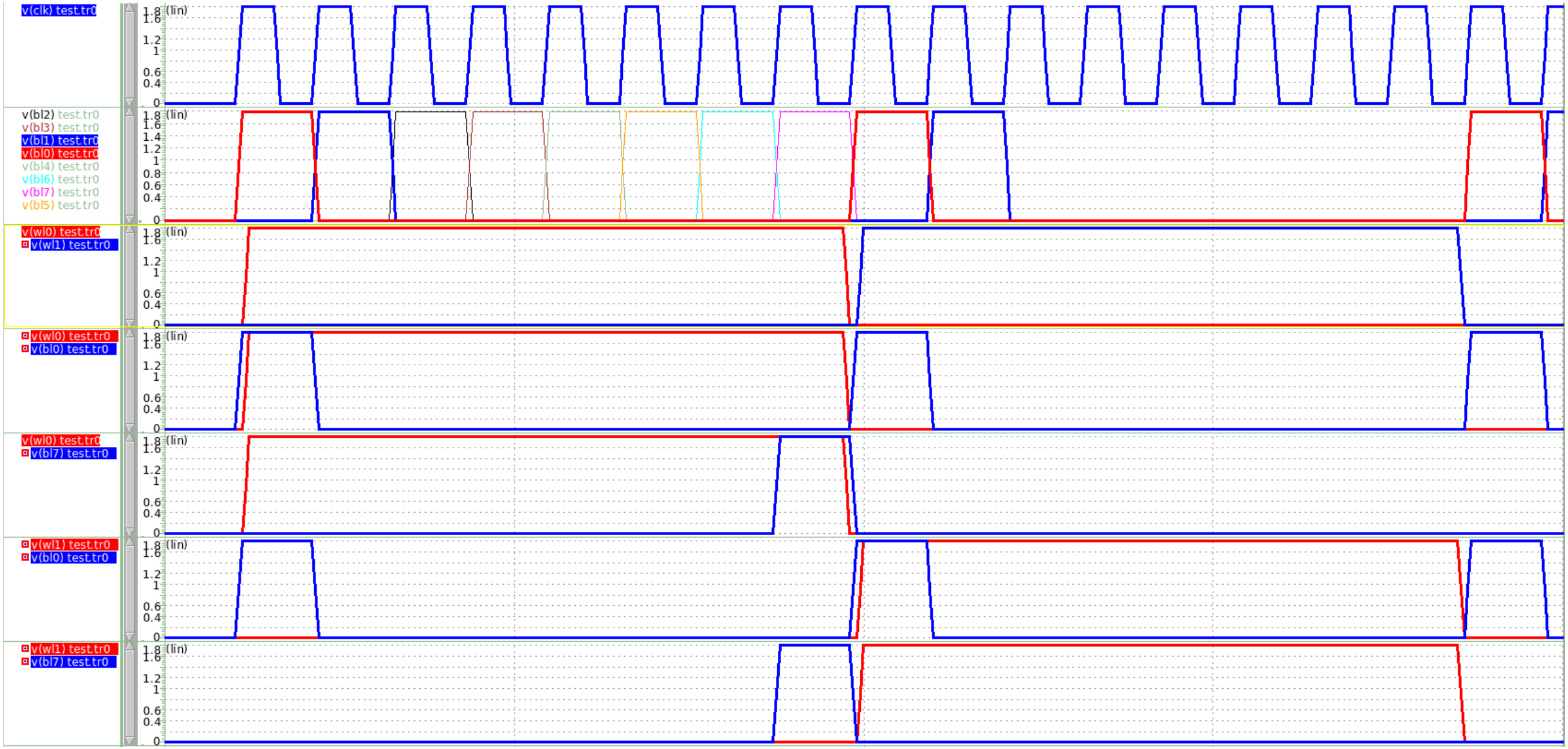
(rst/en signal are designed by yourself)



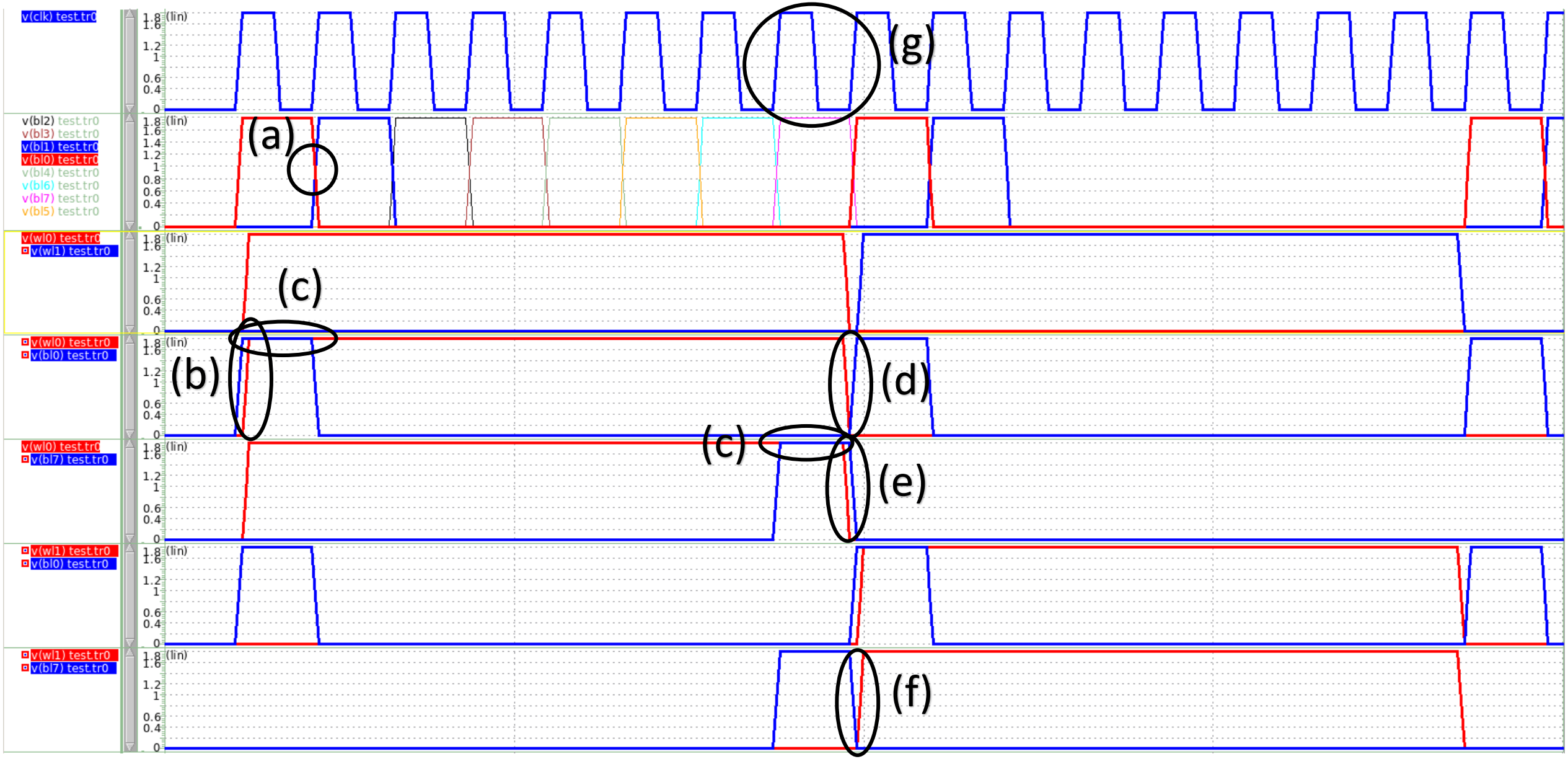
<Note> Your timing control needs to be the same in all corners simulations. After you run the all corners simulations, find out what is the maximum time that en signal should be holded.

<Note> Everyone's design will not be the same including timing and corners simulation results. So, find your own timing control, do not copy TA's timing!

Demo standard



Demo standard



Demo standard

- (a) When BL<n+1> turn on , BL<n> must turn off , $intersection\ of\ two\ lines\ "V \leq 0.9(V)"$
- (b) When WL<n> turn on , BL<0> must be ready. (1.8(V))
- (c) Each BL must overlap with WL for more than 0.1(nsec) *note : Both are 1.8 (V)
- (d) When BL<0> turn on , WL <n-1> must turn off , $intersection\ of\ two\ lines\ "V \leq 0.1(V)"$
- (e) We recommend that WL<n> be designed to shut down earlier than BL<7>
- (f) When WL<n+1> turn on , BL<7> must turn off , $intersection\ of\ two\ lines\ "V \leq 0.1(V)"$
- (g) The duty cycle of CLK_in must be 50 %
- (h) Glitch must be smaller than 0.9(V)
- (i) The changing rate of BL must be determined by f_2

Report (Deadline 1/12)

1. Design

- (1) How do you design the circuit?
- (2) Draw the block diagram, circuit schematic of your design.
- (3) Explain the operation of the sub-circuit you used.
- (4) Design constraints.

2. Layout

- (1) Print-screen the whole design (measure the area) and sub-circuit
- (2) Print-screen DRC summary with no error
- (3) Print-screen LVS result

3. Simulation

- (1) Pre-sim and post-sim results. Mark the delay time and measured data
- (2) Explain the difference between pre-sim and post-sim Demo

(Pre-sim Deadline 12/1～12/8, Final Deadline 12/29)

SCORE

- Report:30%
- Functionality: 40%
- Performance(you need to finish post-sim): 30%

  For performance
- get 30% for the first place
- get 29% for the second place
- get 20% for the eleventh place
- get 15% for 12~19 place
- get 10% for 20~26 place
- Get 5% for 27~32 place

$$Performance = Max\ operation\ frequency^2 \div area^2 \div power$$