RK3568 CORE BOARD BLOCK DIAGRAM

CPU ROCKCHIP
Quad Core A55
GPU MALI G52

DDR4
2GB/4GB

EMMC 5.1
8GB-128GB

UART x10

UART0 - CONNECTOR
UART1 - ETHERNET
UART2 - DEBUG
UART3 - CONNECTOR
UART4 - CONNECTOR
UART5 - SD CARD
UART6 - SD CARD
UART7 - CONNECTOR
UART8 - BLUETOOT
UART9 - CONNECTOR

PWM x15

PWM1 - CONNECTOR
PWM2 - CONNECTOR
PWM3 - EDP HPD
PWM4 - LCD
PWM5 - LCD
PWM6 - CONNECTOR
PWM7 - CONNECTOR
PWM8 - UART4
PWM9 - UART4
PWM10 - GPIO
PWM11 - GPIO
PWM12 - UART3
PWM13 - UART3
PWM14 - UART7
PWM15 - UART7

VIDEO OUTPUT

Dual MIPI DSI x1
LVDS x1
HDMI x1
eDP x1
RGB888 x1

VIDEO INPUT

Dual MIPI CSI x1
CAMERA DVP 16bit x1
BT1120 OUT x1

AUDIO

I2S 8CH x1
I2S 2CH x1
SPDIF OUT x1
MIC x2
SPK x1
headset x1

SDIO x3

SDIO0 - TF
SDIO1 - ETHERNET
SDIO2 - SDIO WIFI

SPI x3

SPI0 - CONNECTOR
SPI1 - CONNECTOR
SPI2 - GPIO
SPI3 - ETHERNET

I2C x4

I2C1 or TOUCH
I2C2 or SPI0
I2C3 or CONNECTOR
I2C4 or CAMERA
I2C5 or RTC

ADC x8

ADC0 - RECOVERY
ADC1 - CONNECTOR
ADC2 - CONNECTOR
ADC3 - CONNECTOR
ADC4 - CONNECTOR
ADC5 - CONNECTOR
ADC6 - CONNECTOR
ADC7 - CONNECTOR

IR RX x1

IR RX x1

GPIO x130

GPIO REPEAT x130

GMAC PHY

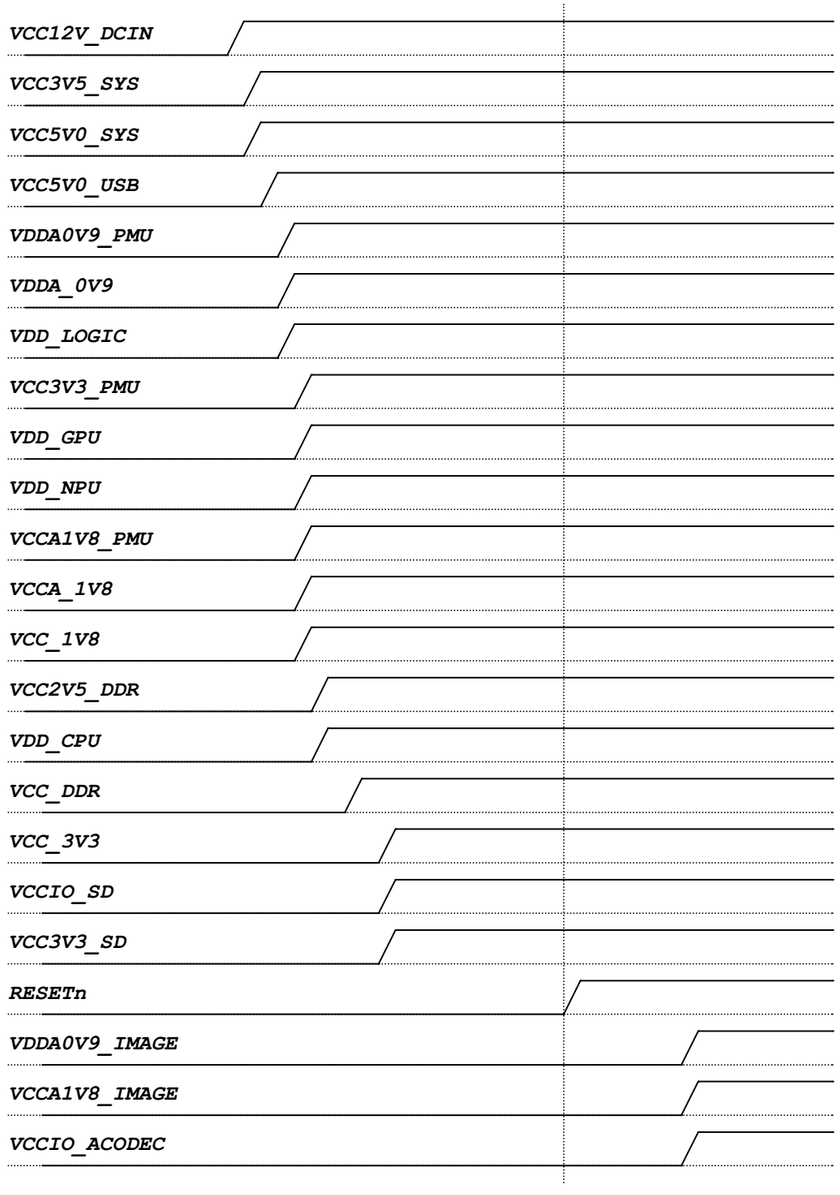
GMAC ETHERNET x2

USB x4

HOST 2.0 x3
OTG 2.0 x1
HOST3.0 x1
SATA2.0 x3
SATA3.0 x2
PCIE3.0 x1
PCIE2.0 x2

	Design Name: **FYSETC_K7_Panel**	
	Rev 1.0 / Page Name: **00.BLOCK**	Size A3
Date: Monday, May 05, 2025	Sheet 1 of 1	

Power Sequence



	Design Name: **FYSETC_K7_Panel**	
	Rev 1.0	Page Name: **01.POWER MAP** / Size B
Date: Monday, May 05, 2025	Sheet 2 of 1	

J1
AXK5F80337YG
J2
AXK5F80337YG
J3
AXK5F80337YG
J4
AXK5F80337YG
J5
CON10
VCCIO5-IN
VCCIO4-IN
VCCIO6-IN
VCCIO7-IN
ETHERNET IO=3V3
ETHERNET IO=1V8
VCCIO5 IO=3V3
VCCIO5 IO=1V8
VCCIO6 IO=3V3
VCCIO6 IO=1V8
VCCIO7 IO=3V3
VCCIO7 IO=1V8
I2C5_SCL_M0
I2C5_SDA_M0
I2C4_SDA_M0
I2C4_SCL_M0
Design Name:
FYSETC_K7_Panel
Rev
1.0
Page Name:
02.CORE
Size
Custom
Date:
Monday, May 05, 2025
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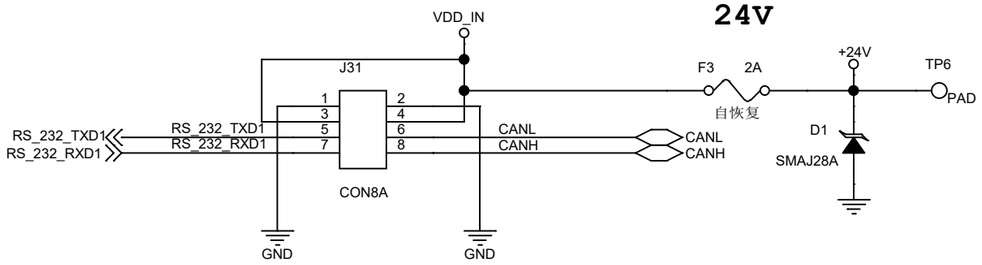
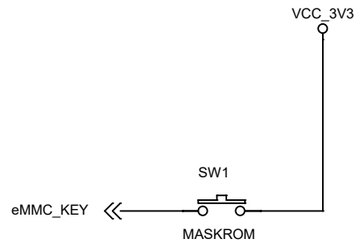
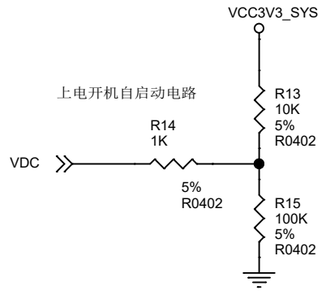
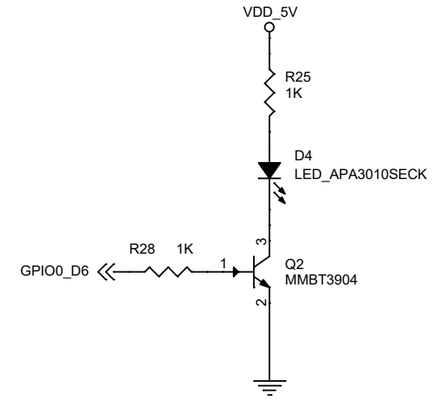
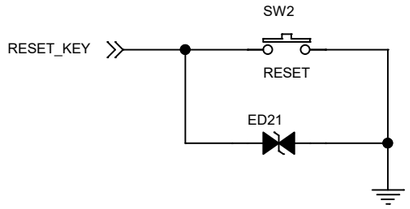
3
of
1

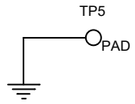


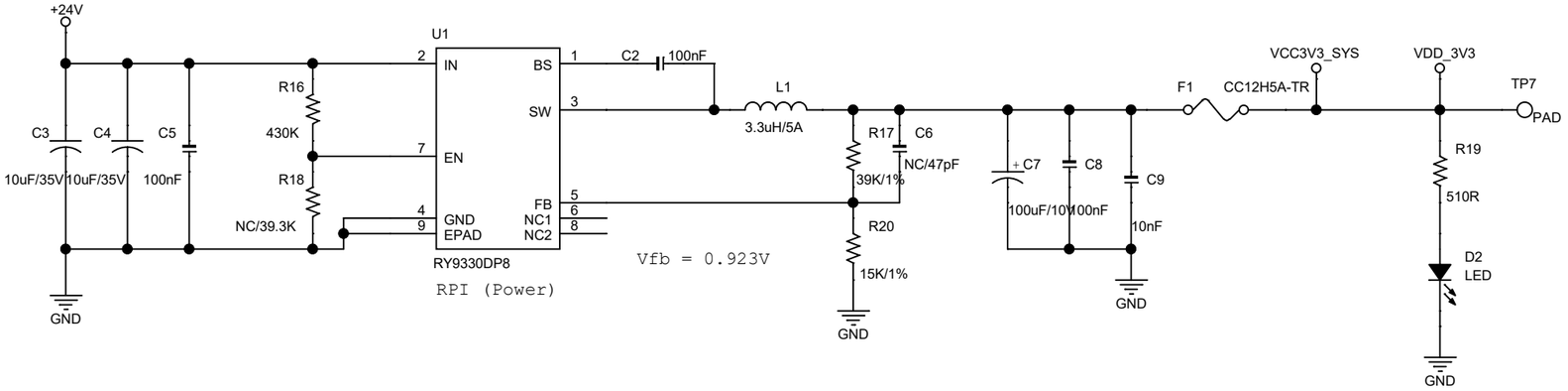


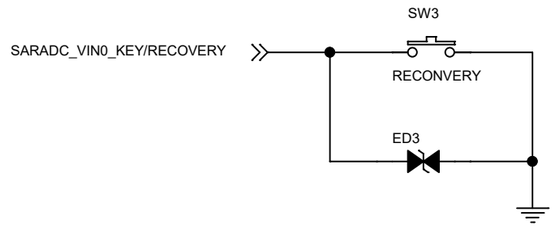


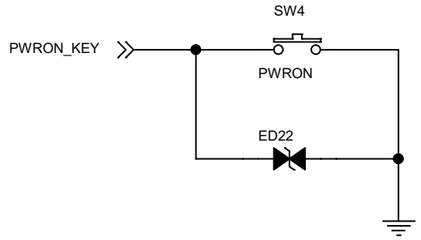


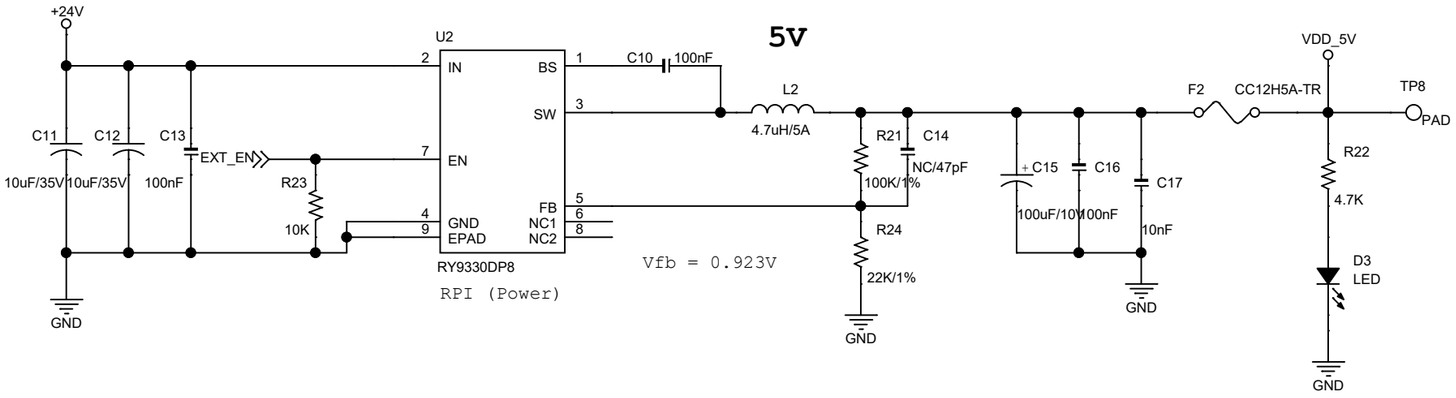


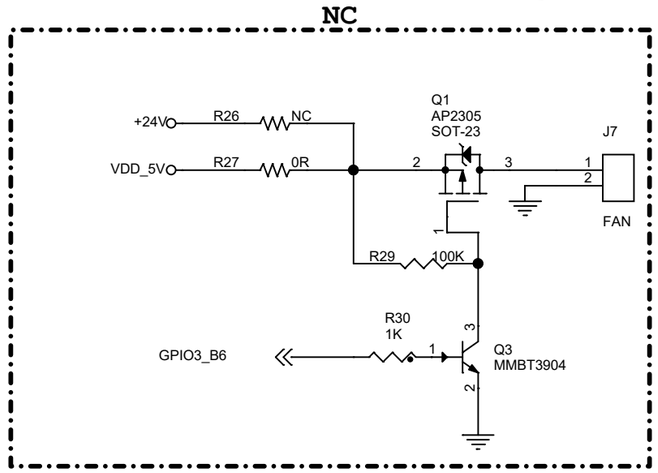








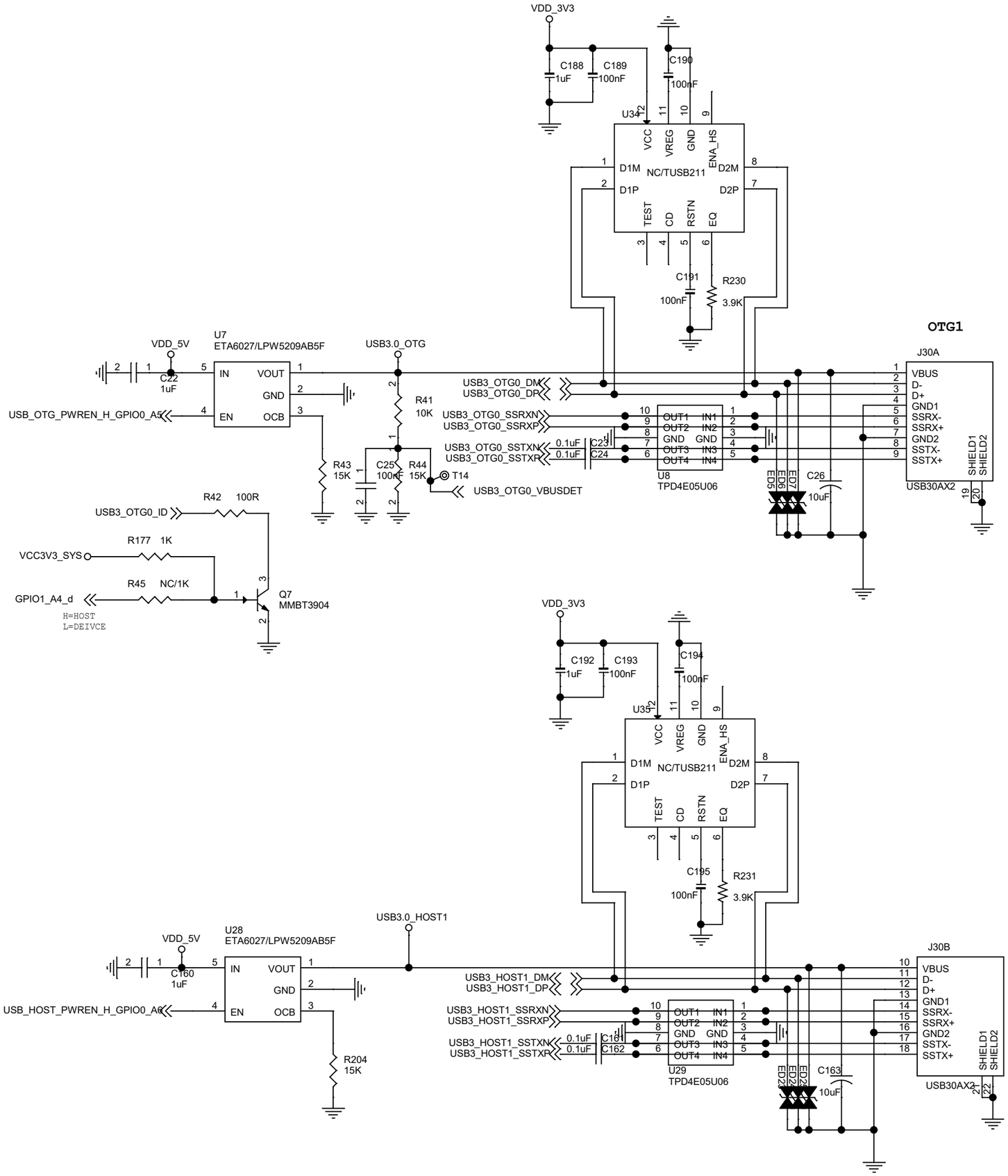




MARK

M1
M2
M3
M4

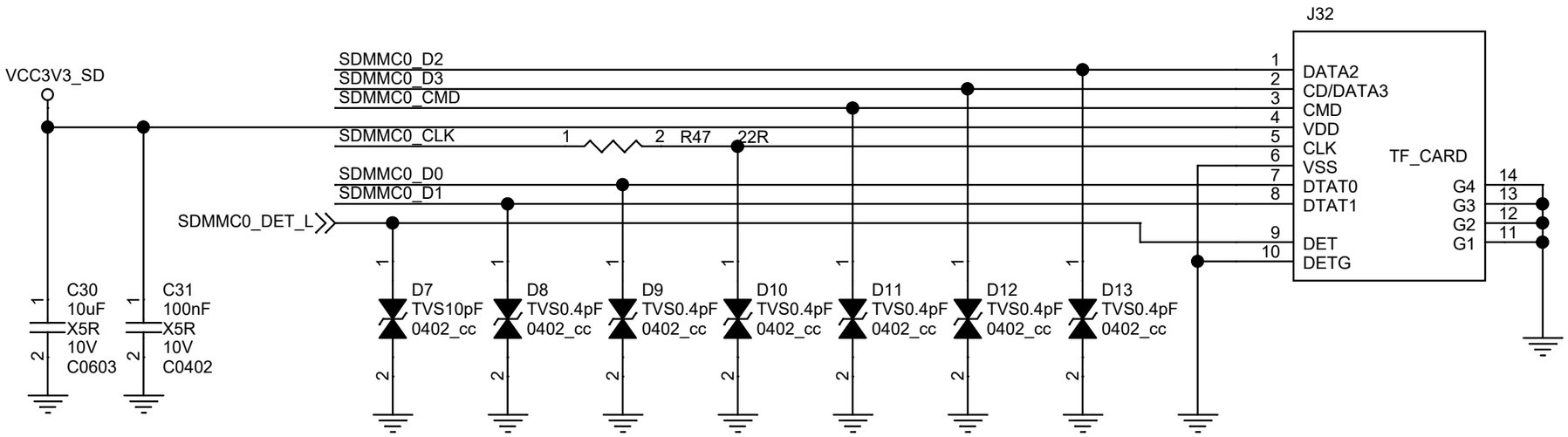
	Design Name: **FYSETC_K7_Panel**	
	Rev 1.0 / Page Name: **03.POWER**	Size A3
Date: Monday, May 05, 2025	Sheet 4 of 1	



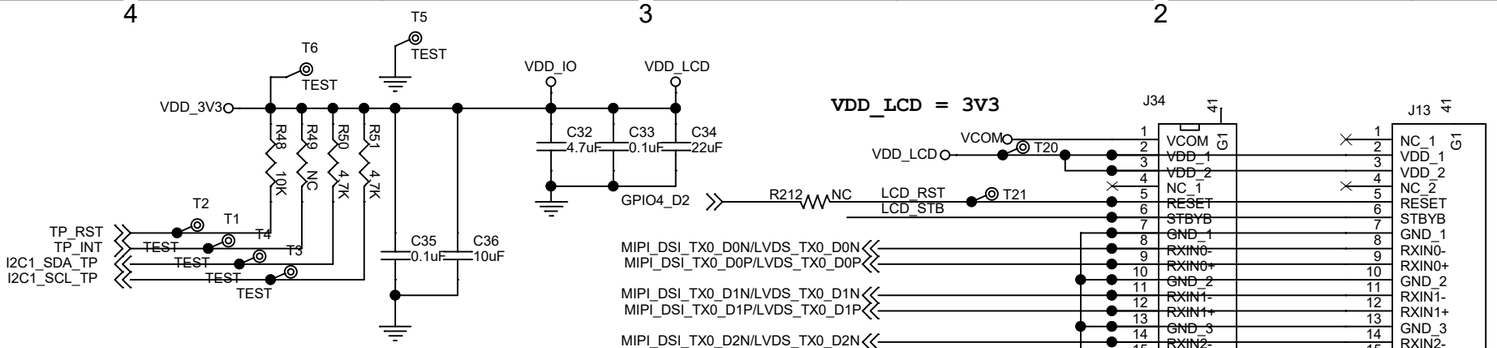
	Design Name: **FYSETC_K7_Panel**	
Rev 1.0	Page Name: **04.USB**	Size A3
Date: Monday, May 05, 2025	Sheet 5 of 1	

SDMMC0_D0
SDMMC0_D1
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDMMC0_CLK

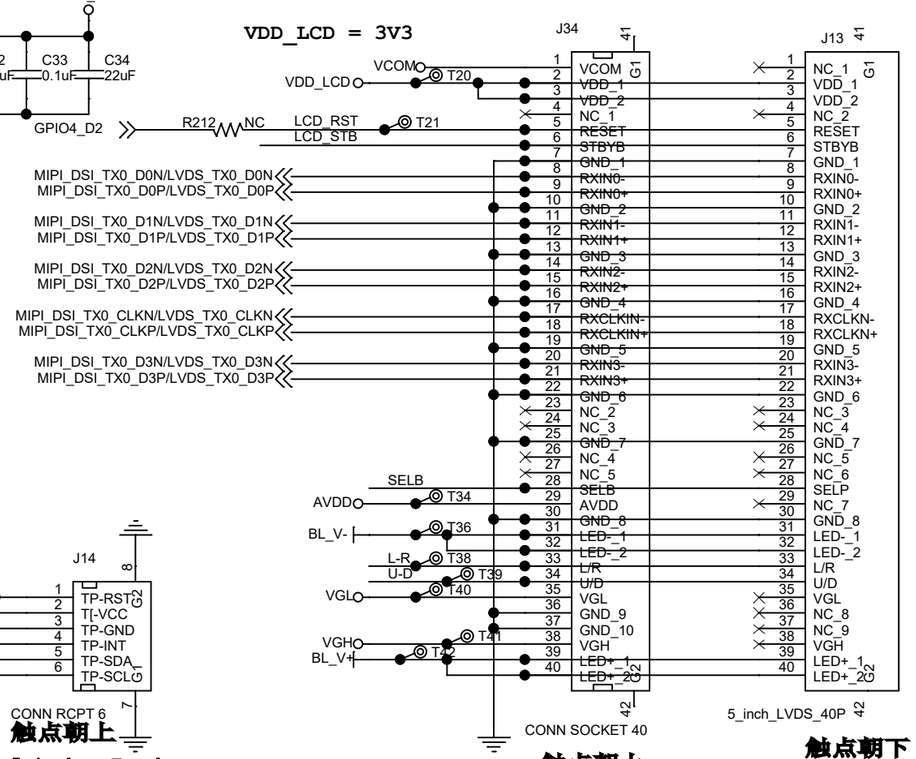
SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1
SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1
SDMMC0_D2/ARMJTAG_TCK
SDMMC0_D3/ARMJTAG_TMS
SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1
SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1

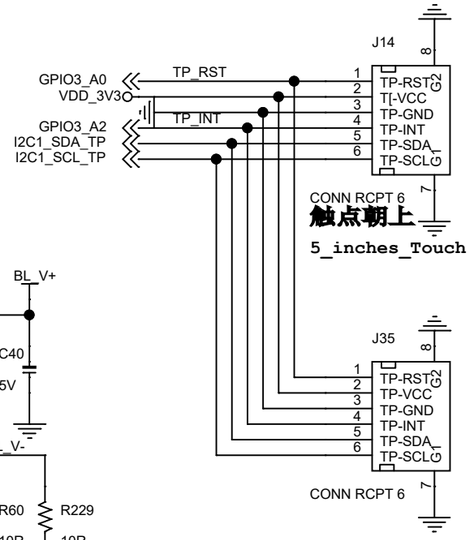


	Design Name: **FYSETC_K7_Panel**		
	Rev 1.0	Page Name: **05.TF**	Size A4
Date: Monday, May 05, 2025		Sheet 6 of 1	



VDD_LCD = 3V3

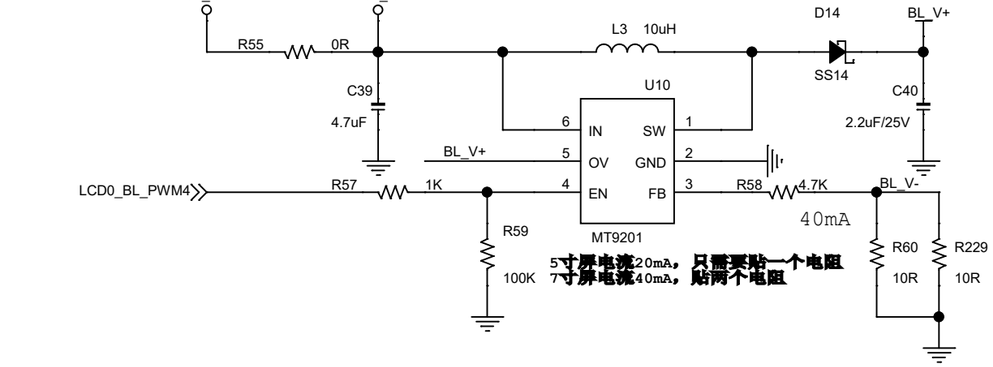


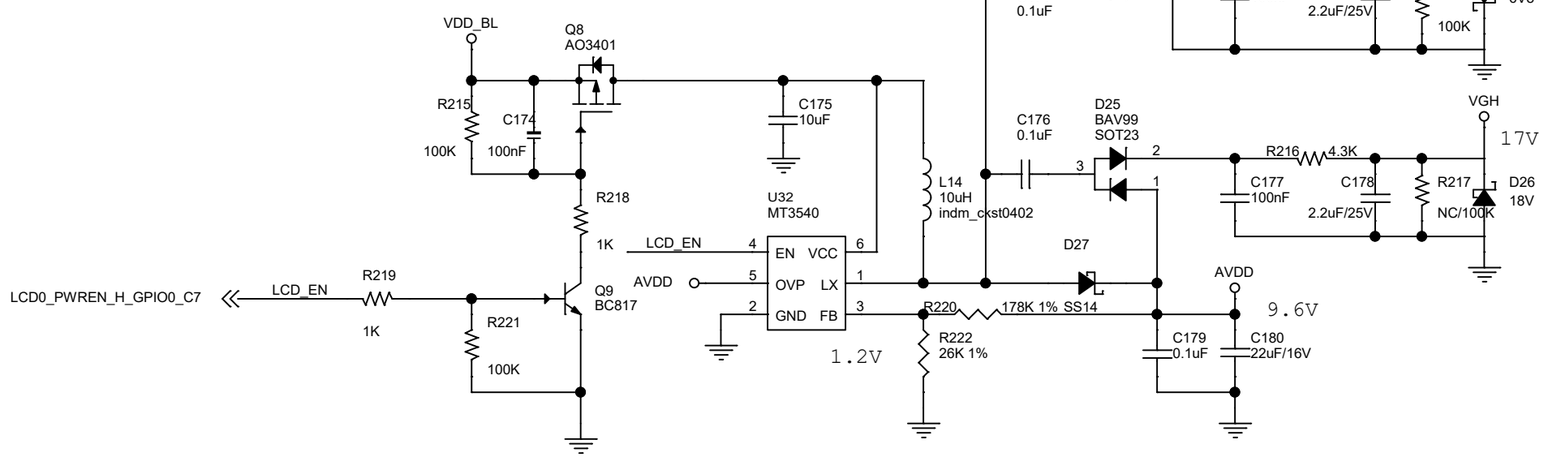


LVDS

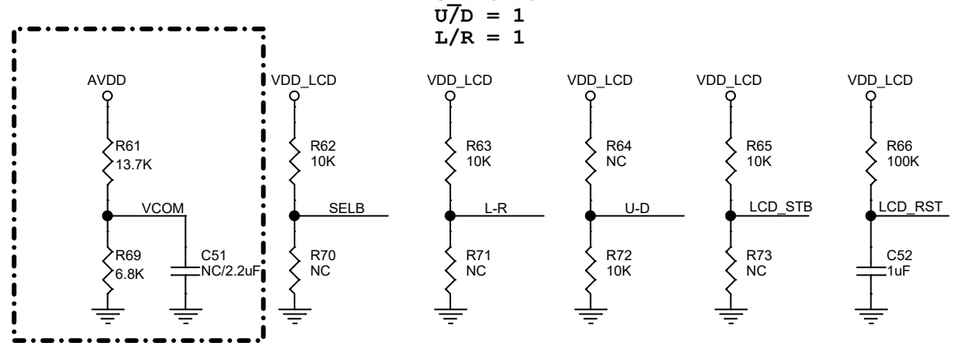
If LVDS input data is 6 bits, SELB must be set to High;
If LVDS input data is 8 bits, SELB must be set to Low.

When L/R= 0, set right to left scan direction.
When L/R= 1, set left to right scan direction.
When U/D= 0, set top to bottom scan direction.
When U/D= 1, set bottom to top scan direction.



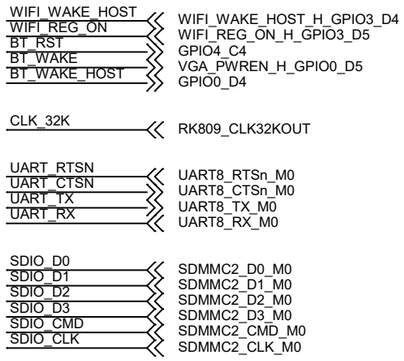


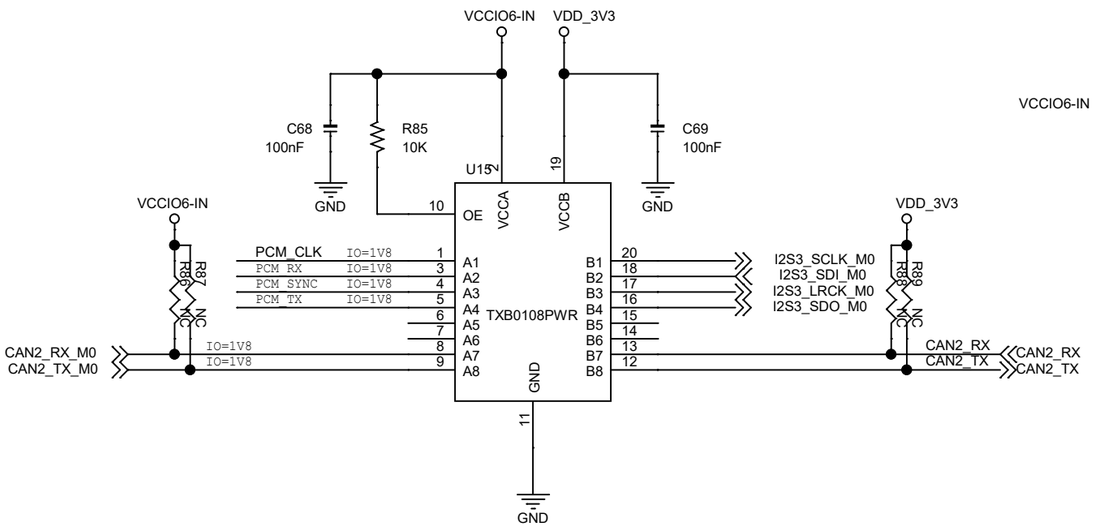
VCOM电压待确认

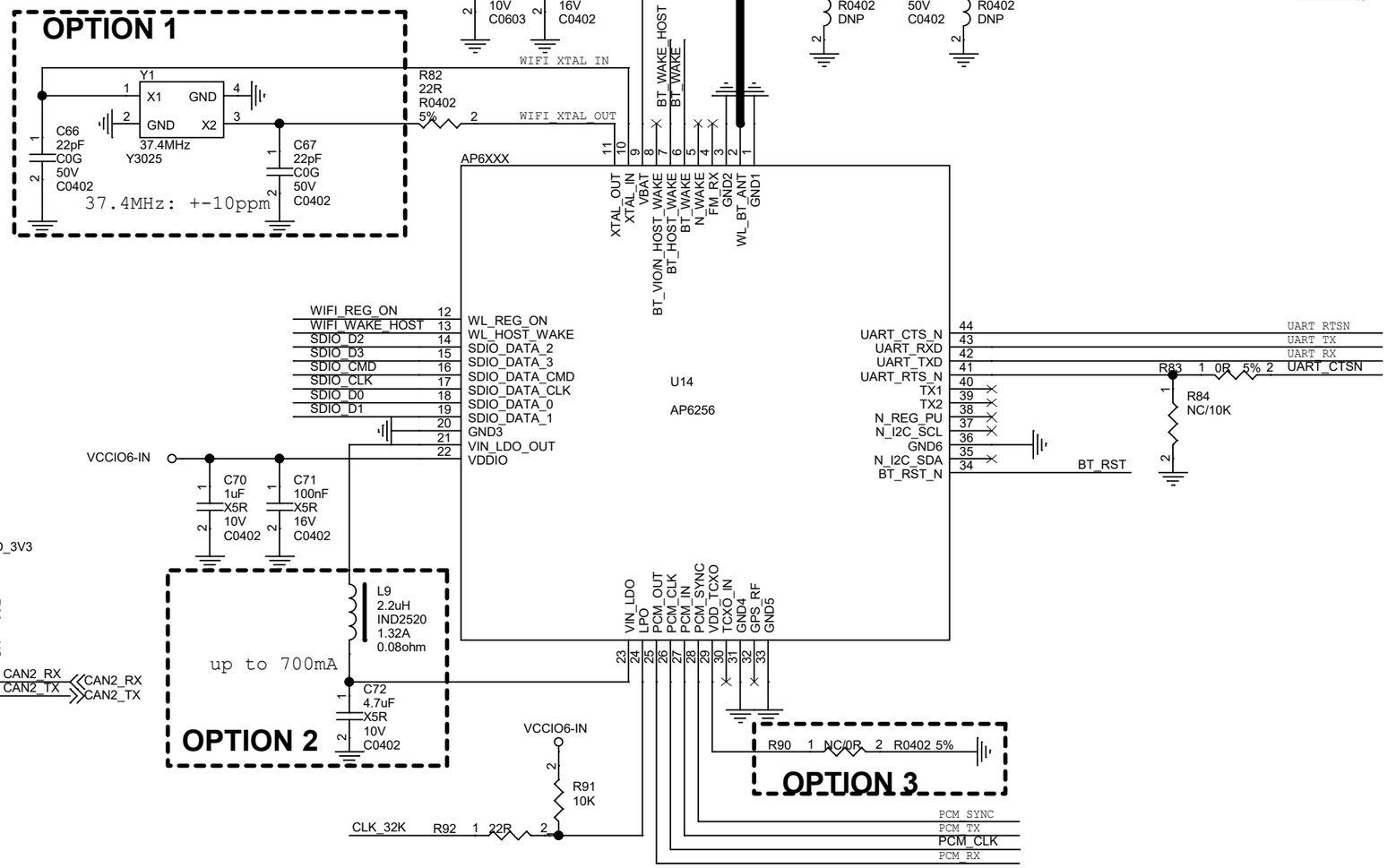


	Design Name: FYSETC_K7_Panel	
	Rev 1.0 / Page Name: 06.LCD	Size A3
Date: Monday, May 05, 2025	Sheet 7 of 1	

WIFI/BT Module





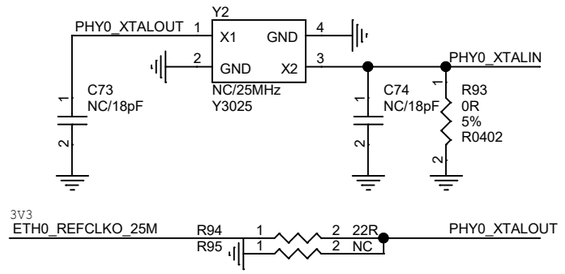


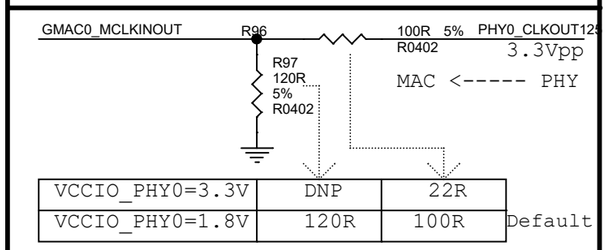
WIFI module		
Pin	AP6255	UWE5622
6	BT_WAKE	CHIP EN
7	BT_HOST_WAKE	AP_INT
12	WL_REG_ON	RST_N
13	WL_HOST_WAKE	SD_INT

OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3
	a	b/g/n	ac	5GHz						
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No
UWE5622	Yes	Yes	Yes	Yes	5.0	Module Integrated	1.62-1.98V	No	No	No

	Design Name: FYSETC_K7_Panel	
Rev 1.0	Page Name: 07.WIFI	Size A3
Date: Monday, May 05, 2025	Sheet 8 of 1	

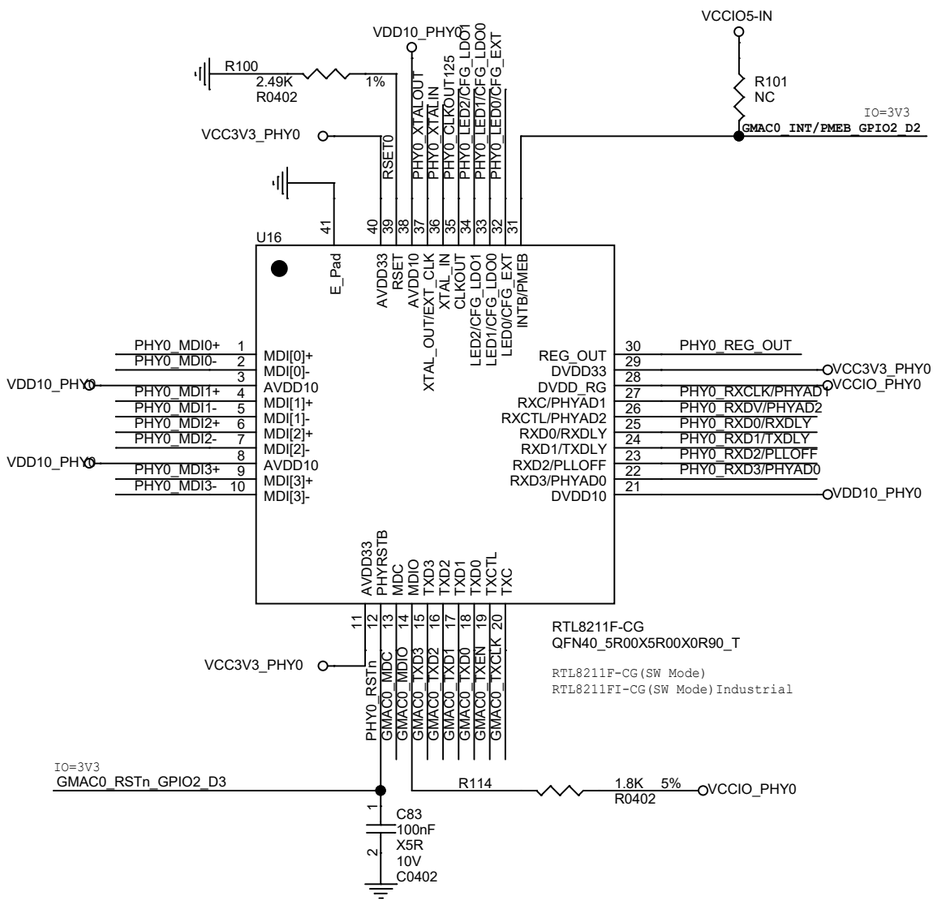
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
ETH0_REFCLKO_25M
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO2_D3
GMAC0_INT/PMEB_GPIO2_D2



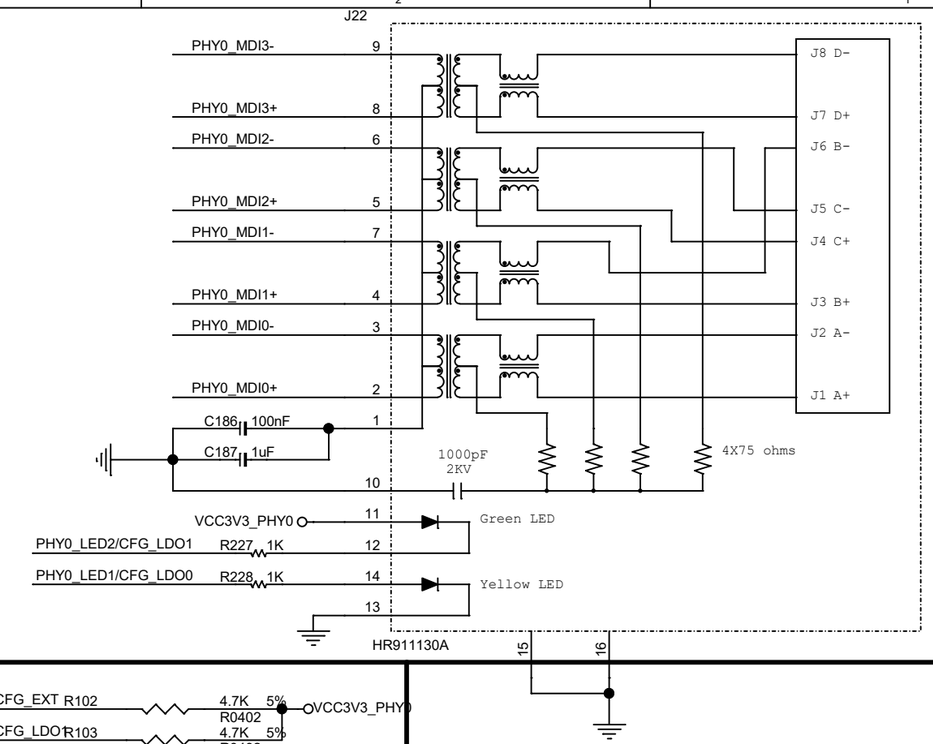


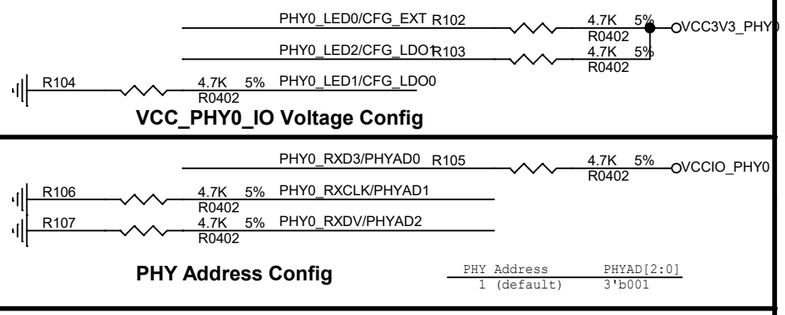
VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default



PHY0_RXD0/RXDLY	GMAC0_RXD0
PHY0_RXD1/TXDLY	GMAC0_RXD1
PHY0_RXD2/PLLOFF	GMAC0_RXD2
PHY0_RXD3/PHYAD0	GMAC0_RXD3
PHY0_RXCLK/PHYAD1	GMAC0_RXCLK
PHY0_RXDV/PHYAD2	GMAC0_RXDV_CRS

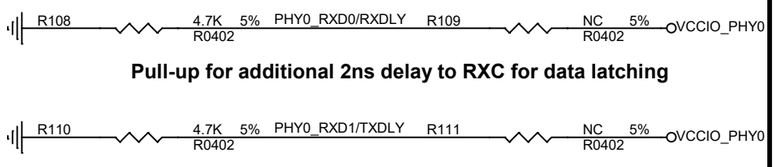




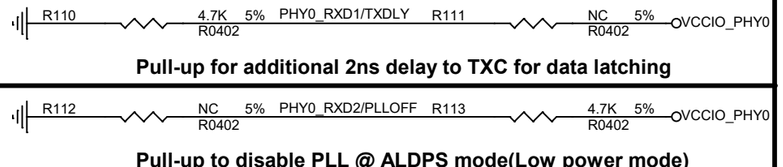
VCC_PHY0_IO Voltage Config

PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

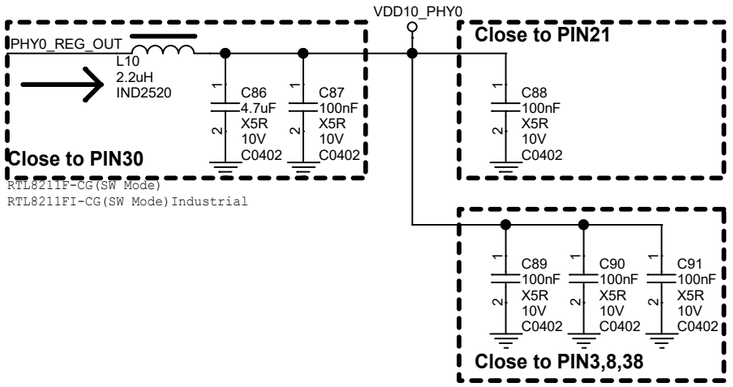


Pull-up for additional 2ns delay to RXC for data latching

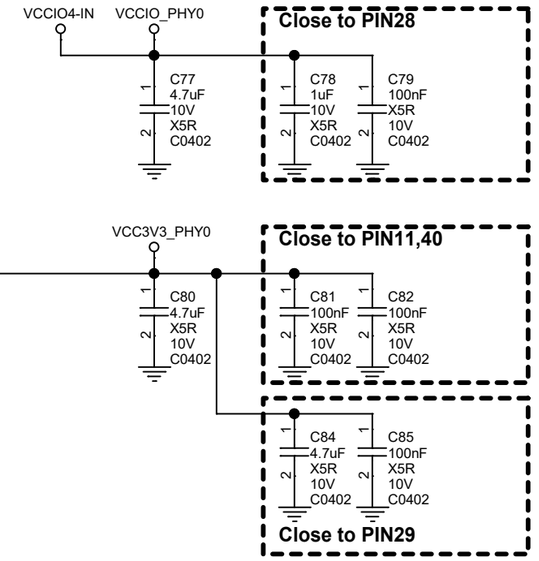


Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)



RGMII Power Source	CFG EXT	CFG LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V (default)	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	



	Design Name: FYSETC_K7_Panel	
Rev 1.0	Page Name: 08.RTL8211F/ETH0	Size A3
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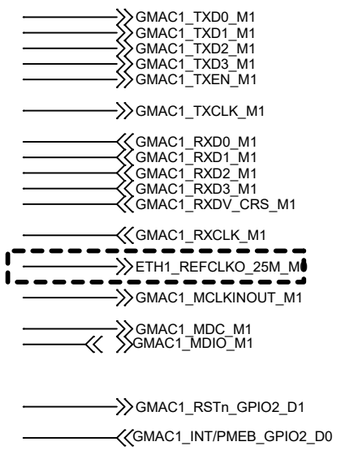
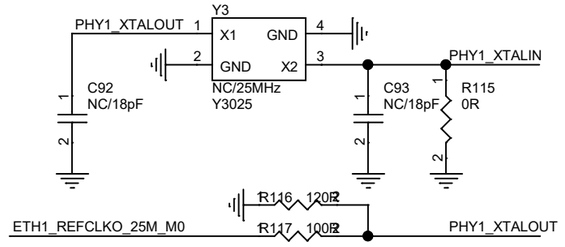
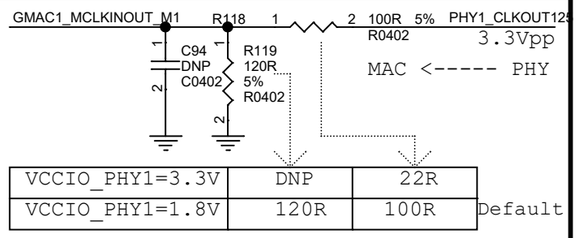
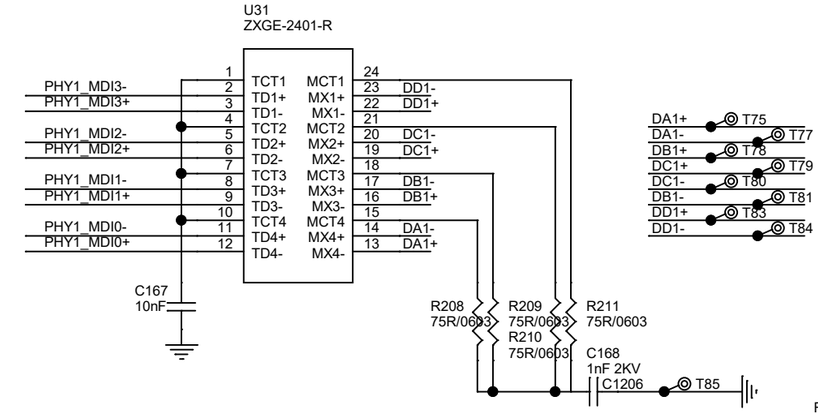


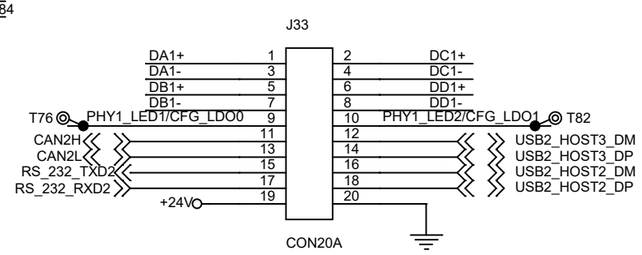




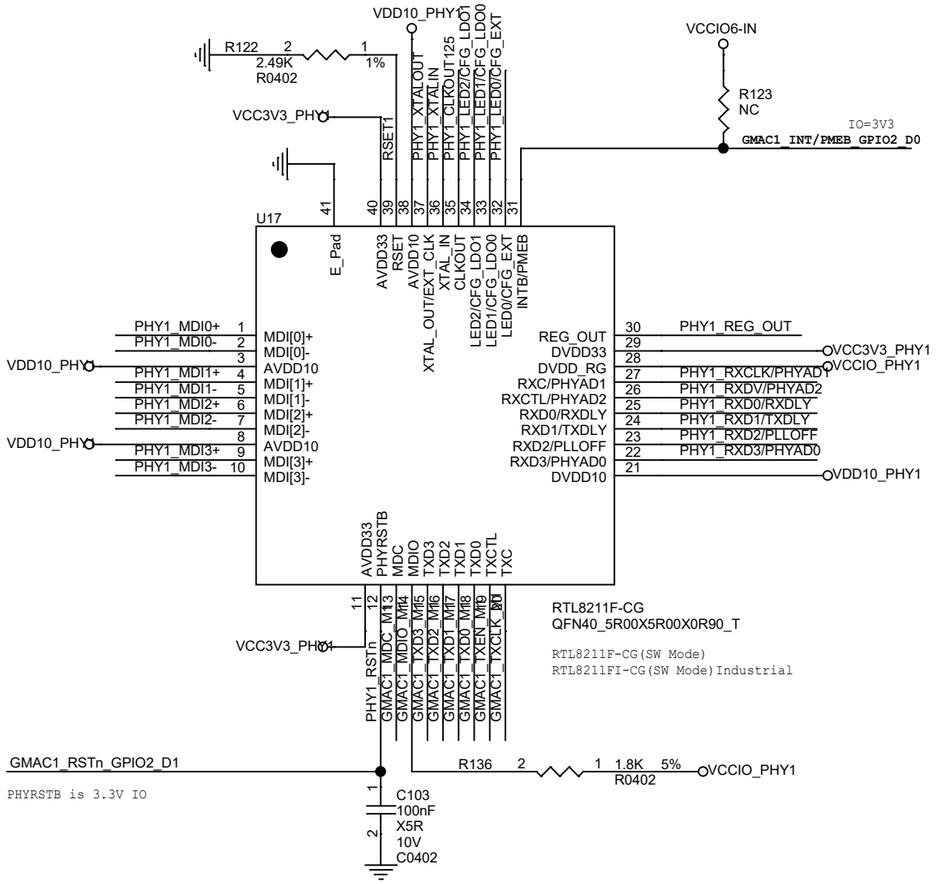
VCCIO_PHY1=3.3V	DNP	22R
VCCIO_PHY1=1.8V	120R	100R

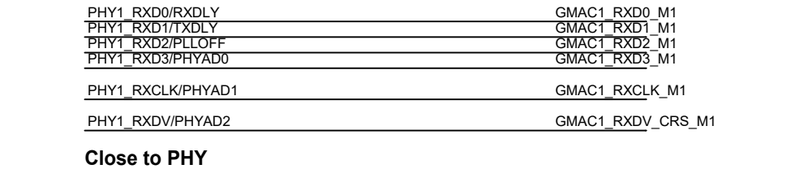
Default



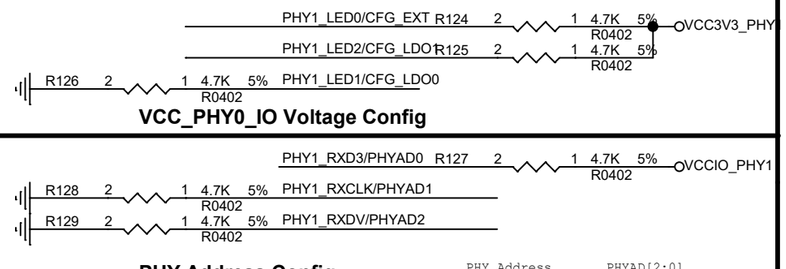


LED0 /High=Link Up at 10Mbps
LED1 /Low=Link Up at 100Mbps
LED2 /High=Link Up at 1000Mbps





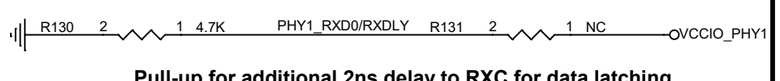
Close to PHY



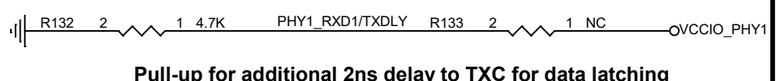
VCC_PHY0_IO Voltage Config

PHY Address Config

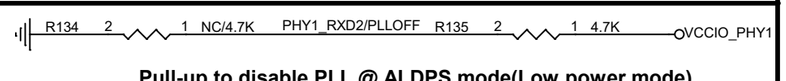
PHY Address	PHYAD[2:0]
1 (default)	3'b001



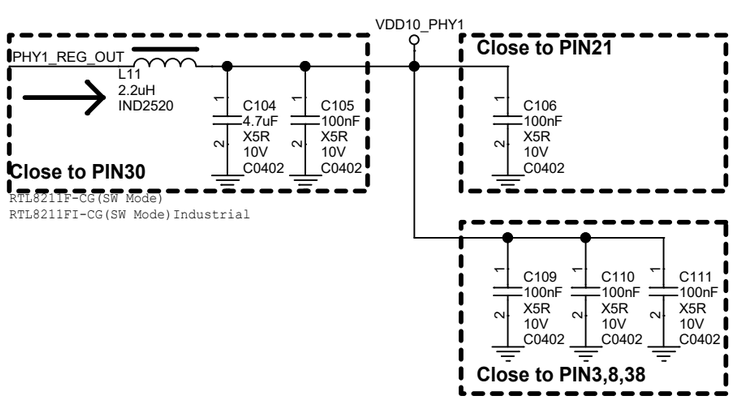
Pull-up for additional 2ns delay to RXC for data latching



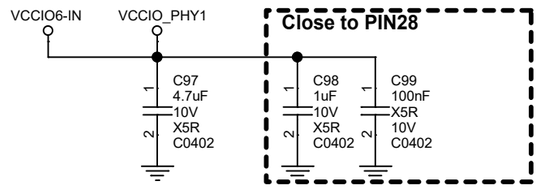
Pull-up for additional 2ns delay to TXC for data latching

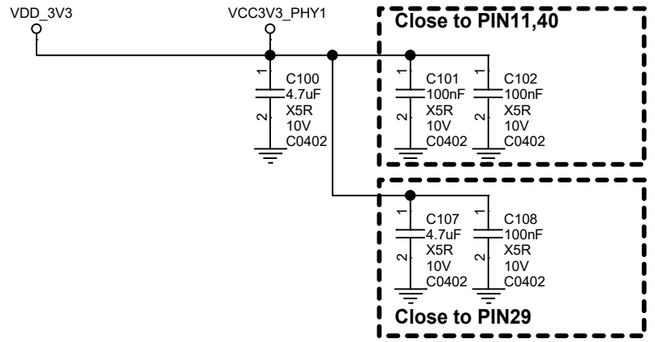


Pull-up to disable PLL @ ALDPS mode(Low power mode)



RGMII Power Source	CFG EXT	CFG LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V (default)	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	





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	Design Name: FYSETC_K7_Panel	
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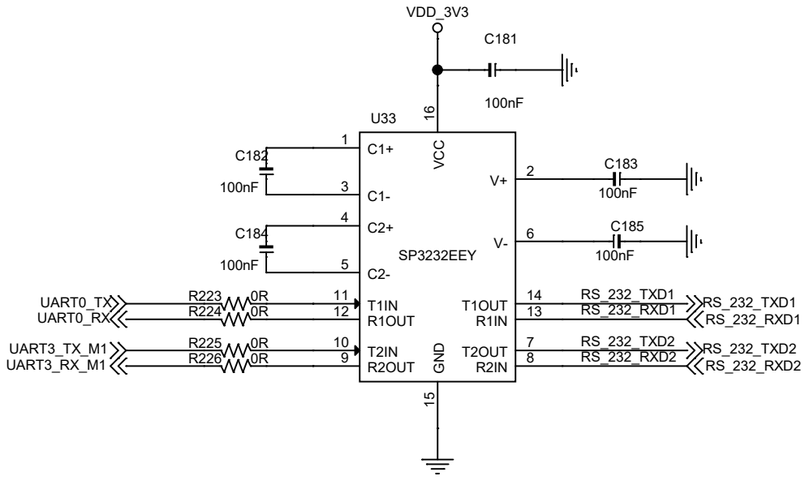
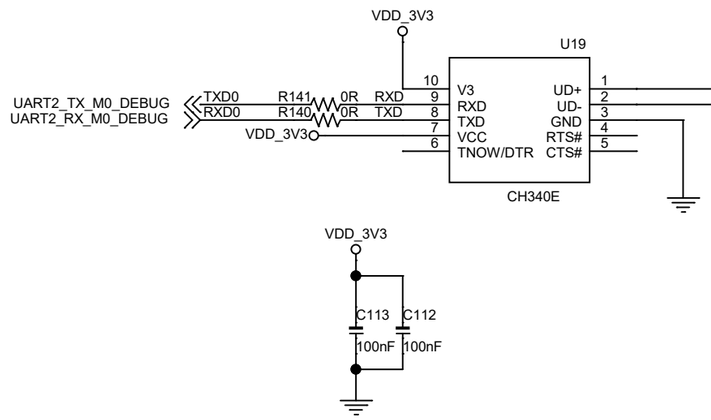
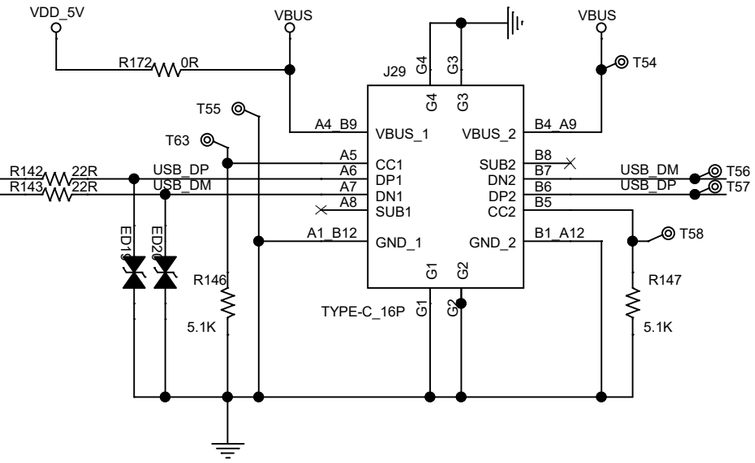
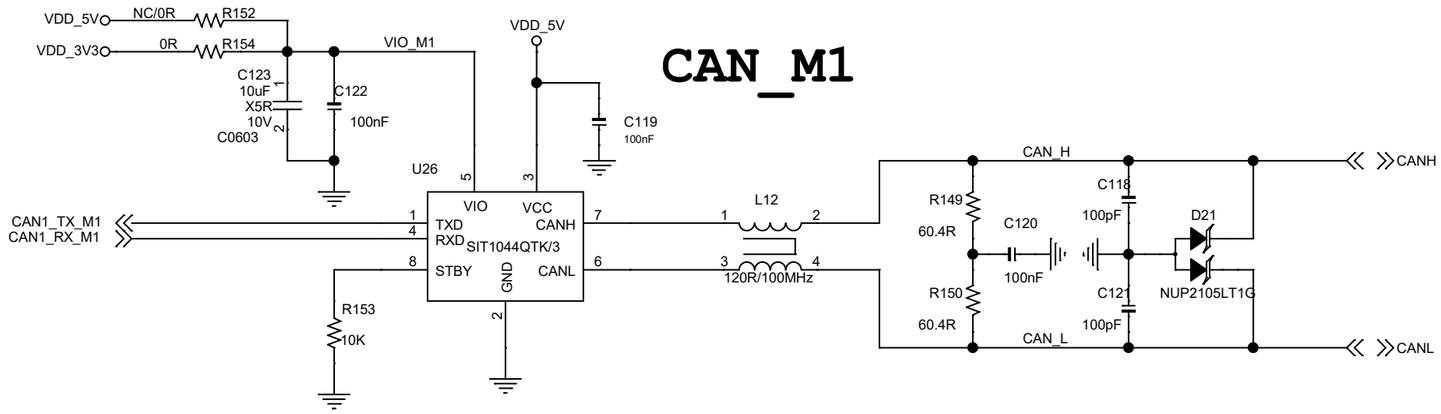


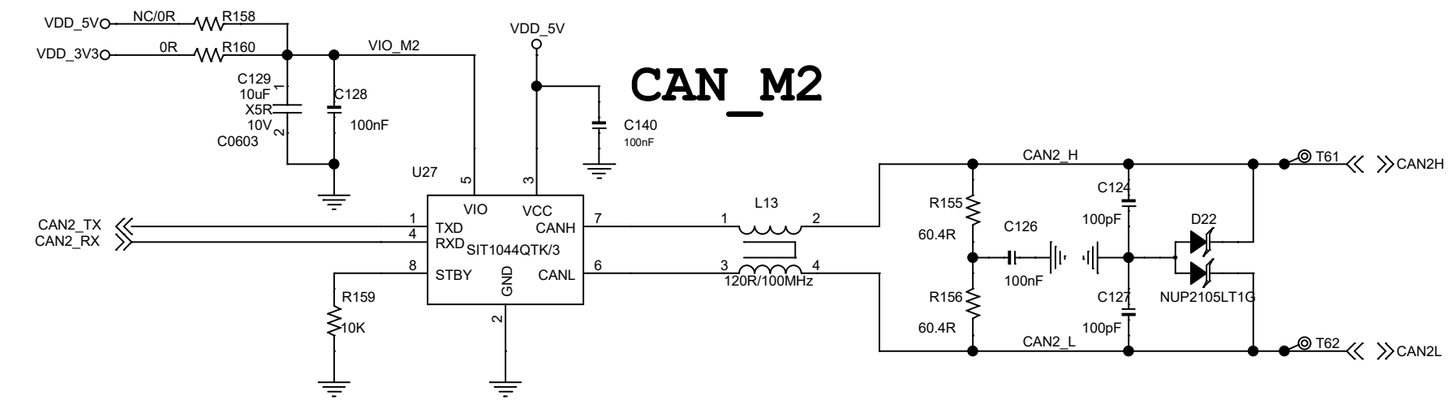




CAN_M1



CAN_M2



	Design Name: **FYSETC_K7_Panel**	
	Rev 1.0 / Page Name: **10.CAN/UART/GPIO**	Size A3
Date: Monday, May 05, 2025	Sheet 11 of 1	