DISTRIBUTED GPU PROGRAMMING FOR EXASCALE

ISC22 TUTORIAL *SESSION 1*

29 May 2022 | Andreas Herten | Jülich Supercomputing Centre, Forschungszentrum Jülich

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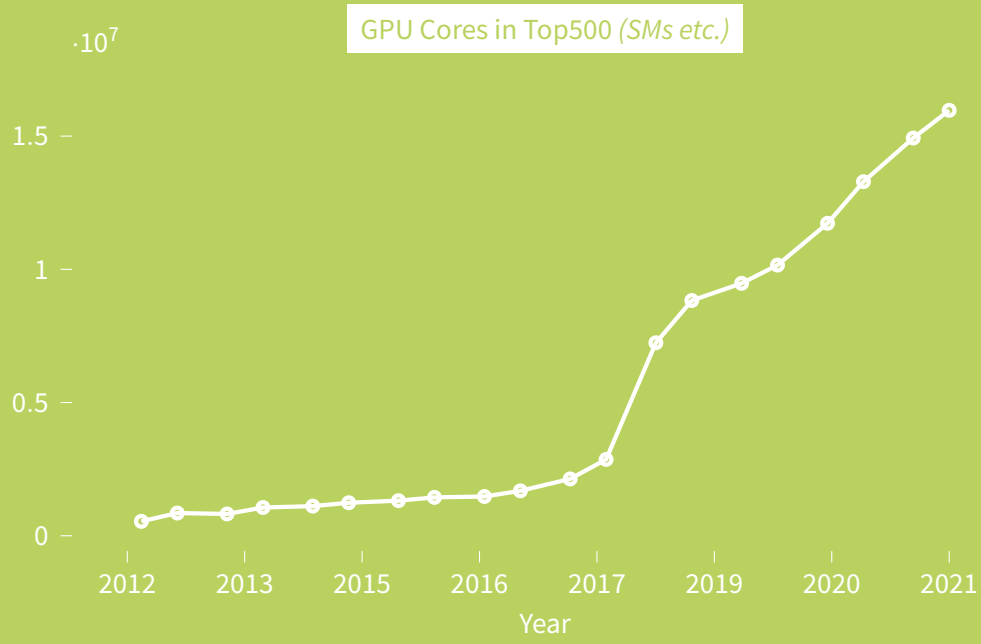
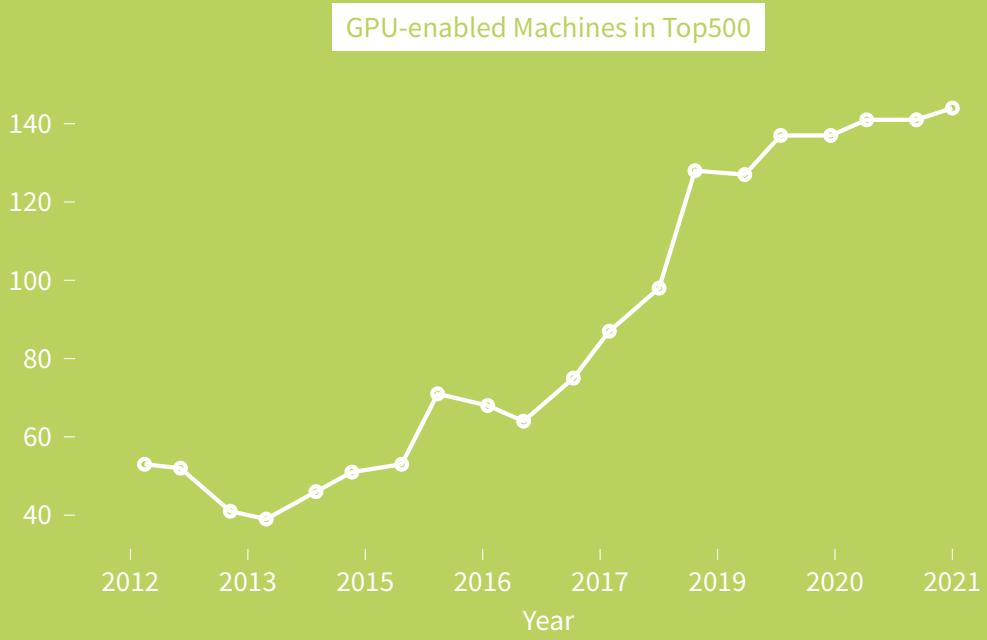
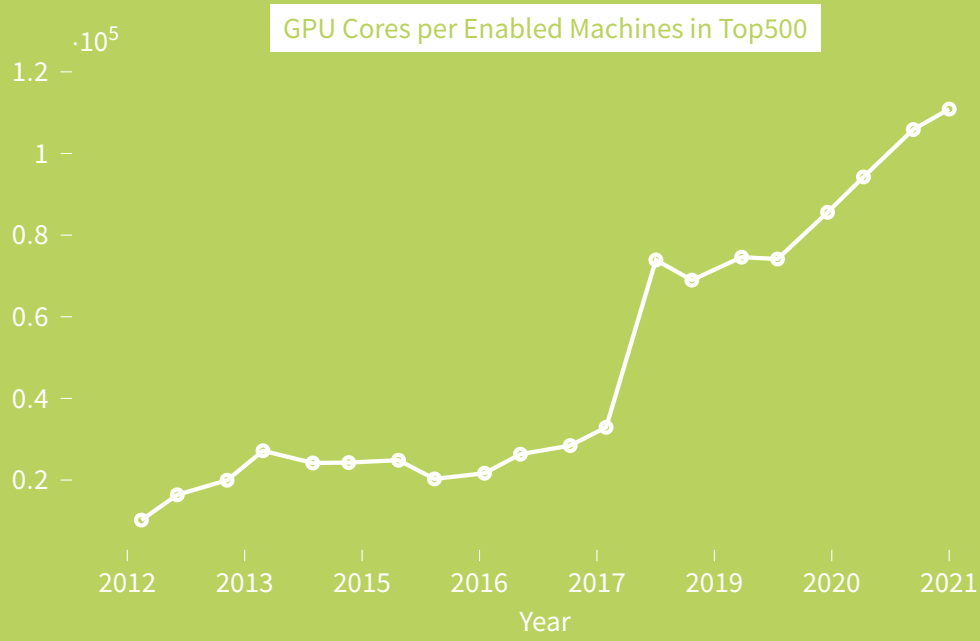
Welcome to

Efficient Distributed GPU Programming for Exascale,

an *ISC22 Tutorial*


GPU Cores in Top500 (SMs etc.)
·10^7
1.5
1
0.5
0
2012
2013
2015
2016
2017
2019
2020
2021
Year


GPU-enabled Machines in Top500
140
120
100
80
60
40
2012
2013
2015
2016
2017
2019
2020
2021
Year


GPU Cores per Enabled Machines in Top500
·10^5
1.2
1
0.8
0.6
0.4
0.2
2012
2013
2015
2016
2017
2019
2020
2021
Year

State of the GPUnion

Landscape Overview

- Last 10 years
  - More and more GPUs installed in HPC machines
  - More and more HPC machines with GPUs
  - More and more GPUs in each machine

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- Future
  - GPUs selected as technology for enabling Exascale

  → Even larger GPU machines with larger GPUs

  - Pre-Exascale systems: LUMI[A], Leonardo[N]; JUWELS Booster[N], Perlmutter[N]
  - Exascale systems: Frontier[A], El Capitan[A], Aurora[I]

ORNL's Frontier: > 35 000 GPUs, 1.5 EFLOP/s, 2022; rendering by ORNL

A: AMD, I: Intel, N: NVIDIA

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  - GPUs
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We help to Tame the Beasts!

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[A]: AMD, [I]: Intel, [N]: NVIDIA

About Tutorial

Goals

- Prepare for large-scale GPU systems
- Learn GPU+MPI basics
- Apply optimization, analysis techniques
- Study CPU-less GPU+MPI
- Use advanced libraries to improve scaling efficiency

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Non-Goals

- Optimize your GPU application; we teach tools and techniques, you need to apply!
- Learn MPI; we expect base-level knowledge of MPI, you don't need more.
- Discuss general scalability; GPU-independent features (like load balancing) are too broad a topic
- Learn CUDA; we expect principle knowledge of GPU programming
- Showcase all GPU platforms; we use an NVIDIA system and teach NVIDIA libraries and tools, other platforms follow along (see last lecture)

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Curriculum

1L	Lecture	Tutorial Overview, Introduction to System
	Onboarding	*Accessing JUWELS Booster*
2L	Lecture	Introduction to MPI-Distributed Computing with GPUs
3H	Hands-On	Multi-GPU Parallelization
		Coffee Break
4L	Lecture	Performance and Debugging Tools
5L	Lecture	Optimization Techniques for Multi-GPU Applications
6H	Hands-On	Overlap Communication and Computation with MPI
		Lunch Break
7L	Lecture	Overview of NCCL and NVSHMEM in MPI Programs
8H	Hands-On	Using NCCL and NVSHMEM
		Coffee Break
9L	Lecture	Device-initiated Communication with NVSHMEM
10H	Hands-On	Device-initiated Communication with NVSHMEM
11L	Lecture	Outline of Advanced Topics and Conclusion

Tutorial Team

Hello from Europe

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Barcelona Supercomputing Center

Andreas Herten
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Jülich Supercomputing Centre

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DevTech Compute
NVIDIA

Jiri Kraus
DevTech Compute
NVIDIA

Lena Oden
Prof. for Computer Engineering
University Hagen

System: JUWELS Booster

JUWELS Overall Architecture

JUWELS Cluster (2018)

- 2511 compute nodes (2× Skylake)
- 48 GPU nodes (4× V100 w/ NVLink2)
- Mellanox EDR 100 Gbit/s network, fat-tree topology (1:2@L1)
- 12 PFLOP/s

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JUWELS Booster (2020)

- 936 compute nodes (2× AMD Rome, 4× A100 w/ NVLink3)
- Mellanox HDR 200 Gbit/s network, DragonFly+ topology
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JUWELS Overall Architecture

JUWELS Cluster (2018)

- 251 ke)
- 48 nk2)
- Me rk,
  fat-
- 12

TOP 500 The List.

Top500 Jun-2021:

- #1 Europe
- #8 World
- #4* GreenTop500

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JUWELS Booster Overview

Node Configuration

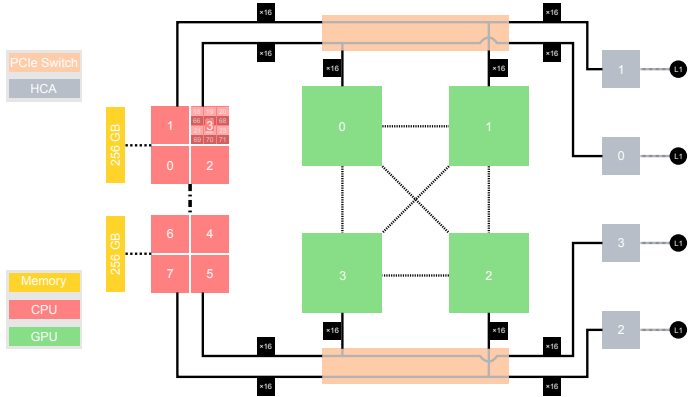
Arch Atos Bull Sequana XH2000

CPU 2 × AMD EPYC 7402:
$2_{\text{Socket}} \times 24_{\text{Core}} \times 2_{\text{SMT}}$,
2 × 256 GB DDR4-3200 RAM;
NPS-4

GPU 4 × NVIDIA A100 40 GB, NVLink3

HCA 4 × Mellanox HDR200
(200 Gbit/s) InfiniBand
ConnectX 6

etc 2 × PCIe Gen 4 switch



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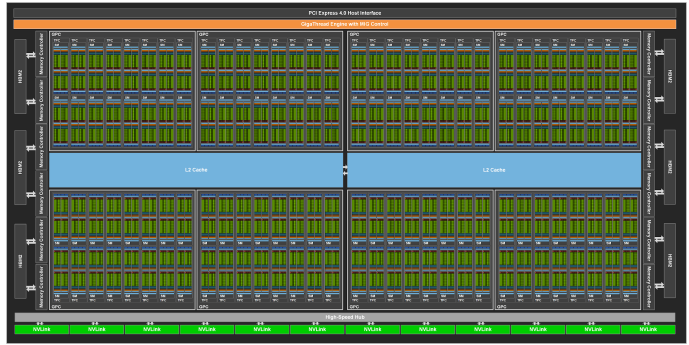
NVIDIA A100 Tensor Core GPU

- JUWELS Booster: 3744 A100 GPUs
- Vs. V100: More SMs, larger/faster L1, larger/faster L2, faster memory, faster NVLink, faster PCIe, …
- New features: MIG, async copy to/barrier in shared mem



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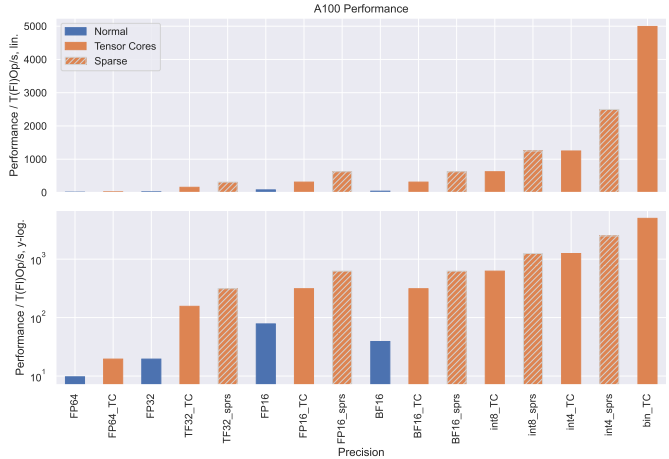
- New features: MIG, async copy to/barrier in shared mem
- New Tensor Cores, new performances:
  73 PFLOP/s_{FP64TC} 584 PFLOP/s_{FP32TC}
  1.16 EFLOP/s_{FP16TC} 18.7 EOP/s_{BinTC}



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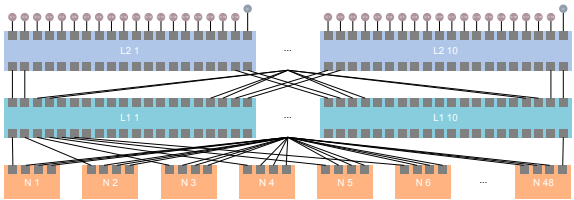
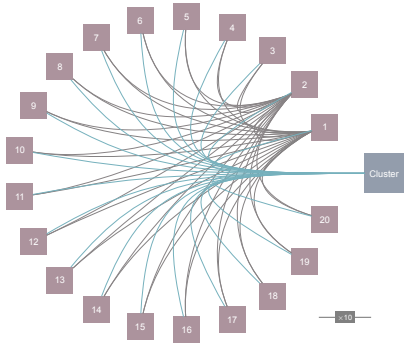
JUWELS Booster Overview

Network Configuration: DragonFly+ Network





In-Cell (48 nodes): Full fat-tree in 2 levels

Inter-Cell (20 cells): 10 links between each pair of cells

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JUWELS

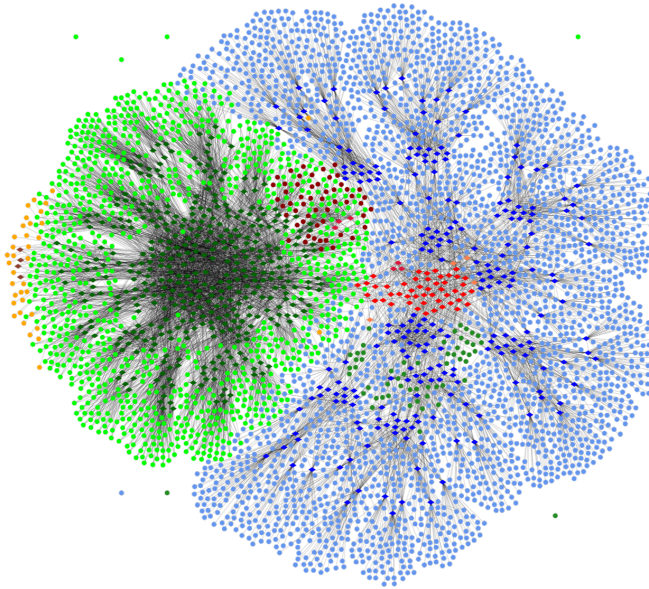
Cluster Booster Integration

Fully integrated system: **JUWELS** with Cluster and Booster modules

- File system: GPFS
- Network: InfiniBand
- Workload management: Slurm
- Resource management: ParaStation / ParaStation Slurm

Picture legend:

- Cluster CPU node
- Cluster GPU node
- Cluster switch
- Cluster gateway
- Top-level switch
- Booster node
- Booster switch
- Booster gateway
- JUST
- Service node



Graphic provided by D. Alvarez

AMD EPYC Rome

Some Processor Basics

- JUWELS Booster: AMD EPYC Rome 7402 (24 core (SMT-2) $\times$ 2 sockets)
- EPYC processor: Built as Multi-Chip Module
  $\rightarrow$ Many building blocks, hierarchies

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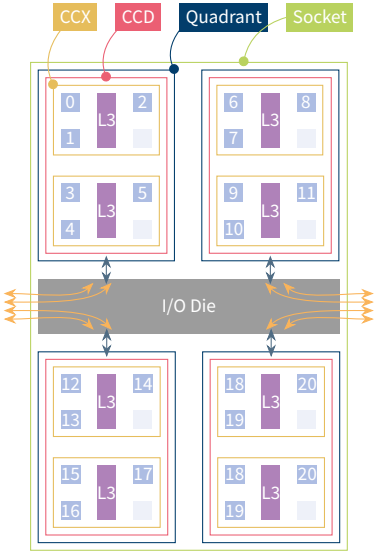
3 cores	Core-Complex (CCX), shared L3 *(max 4 cores)*
2 CCXs	Core Complex Die (CCD)
1 CCD	1 quadrant *(max 2 CCDs per quadrant)*
4 quadrants	1 socket; NPS-4: 4 NUMA domains per socket
2 sockets	1 node *(only 1 shown)*
I/O Die	Connections between quadrants and outside
RAM	8 memory channels, 2 per quadrant



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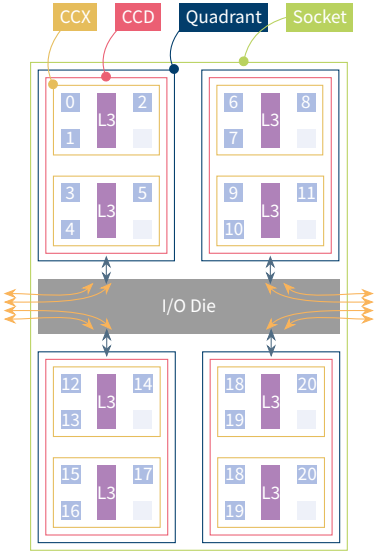
$\Rightarrow$ **Complex topology!**



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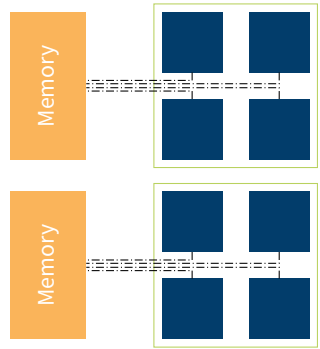
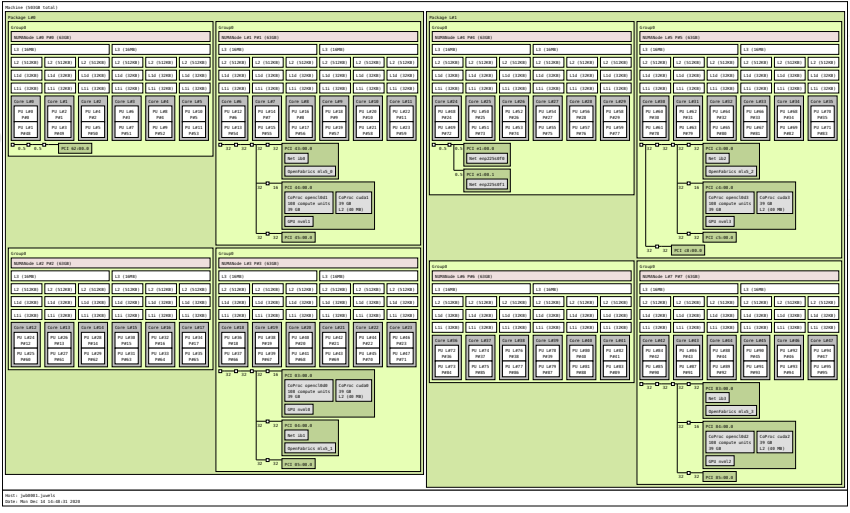
PCIe Affinity

- PCIe via I/O die → also hierarchy
- GPUs connected via PCIe (through PCIe switch)



PCIe Affinity

- PCIe via
- GPUs co



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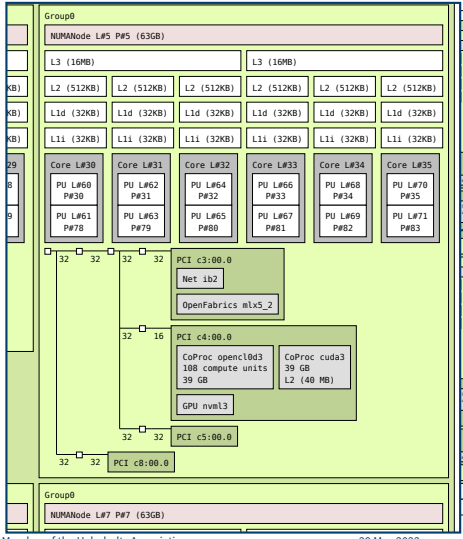
PCIe Affinity



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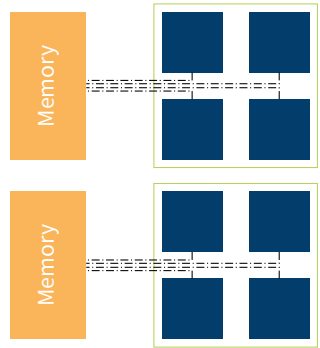
- PCIe 4.0 lanes: 2×16, each 16 connected to 1 quadrant



PCIe Affinity

3 C | 2 CCX | 1 CCD | 4 Q | 2 S

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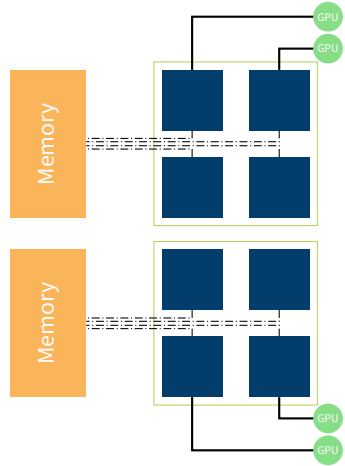
→ *True* GPU affinity only by half of chiplets

But impact application-dependent and possibly quite low



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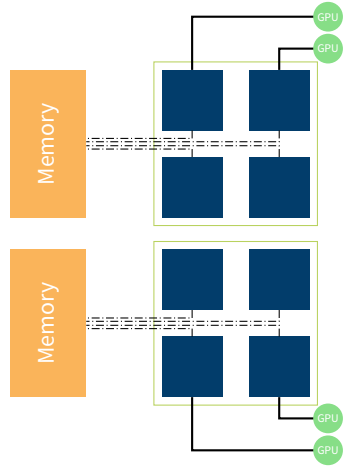
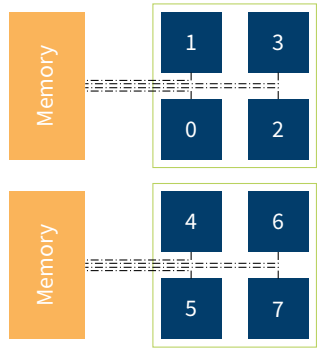
- InfiniBand HCA adapters also via PCIe switch
  - Same affinity considerations
  - 1:1 relation between HCA and GPU



NUMA Numbering

- NUMA domains (= quadrants) are numbered



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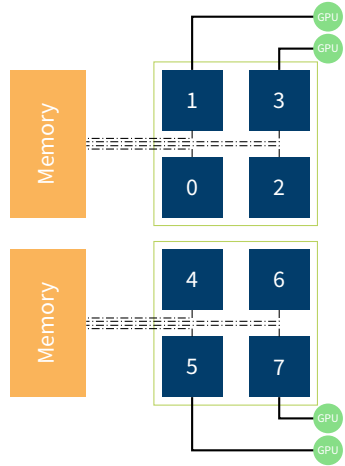

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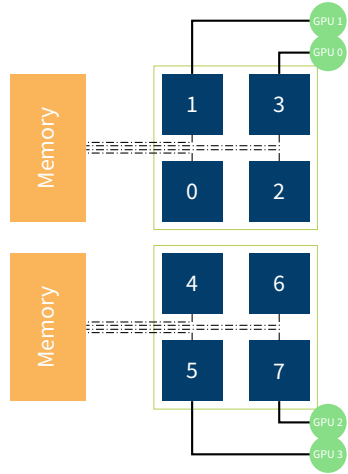

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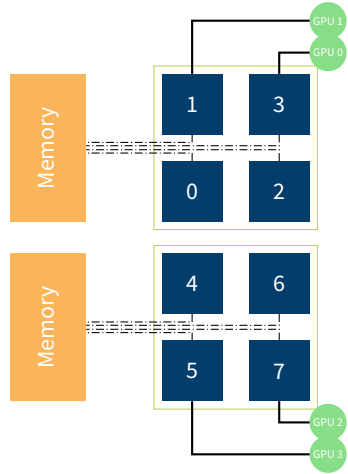
- Complete affinity table

Rank	NUMA Domain	GPU ID	HCA ID
0	3	0	0
1	1	1	1
2	7	2	2
3	5	3	3



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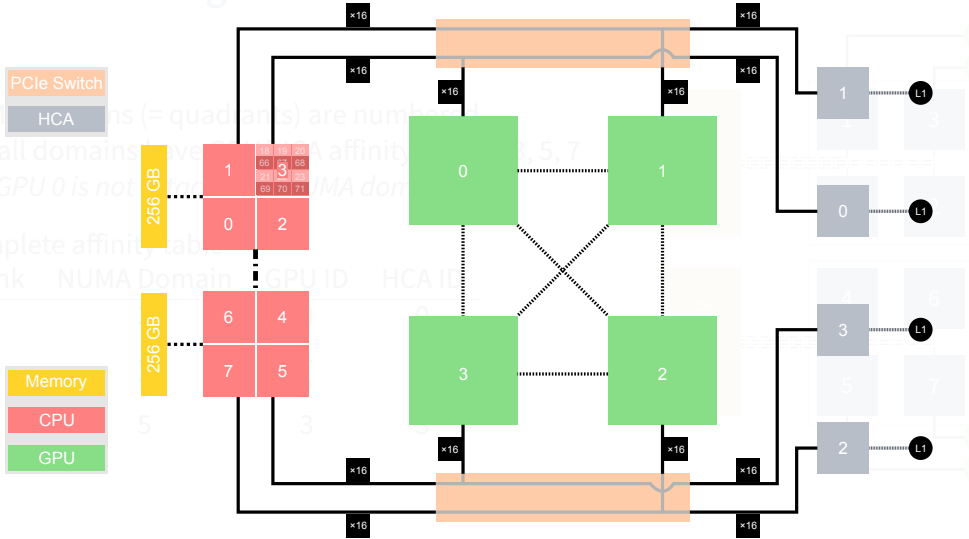

Affinity in Practice

CPU and GPU Affinity

- We configured *PS*Slurm to use best topology **as default**

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CPU and GPU Affinity

- We configured *PS*Slurm to use best topology **as default**
- *PS*Slurm sets CPU affinity masks with *GPU-first-approach*: Fill cores with GPU affinity first
- *PS*Slurm sets `$CUDA_VISIBLE_DEVICES` to associated GPU
- Example GPU affinity for 2 tasks:

```
$ srun -n 2 --cpu-bind=verbose env | grep 'PMI_RANK\|CUDA_VIS'
cpu_bind=THREADS - jwb0001, task  0  0 [18307]: mask 0x40000 set
cpu_bind=THREADS - jwb0001, task  1  1 [18309]: mask 0x40 set
PMI_RANK=0
CUDA_VISIBLE_DEVICES=0
PMI_RANK=1
CUDA_VISIBLE_DEVICES=1
```

DragonFly+ Topology

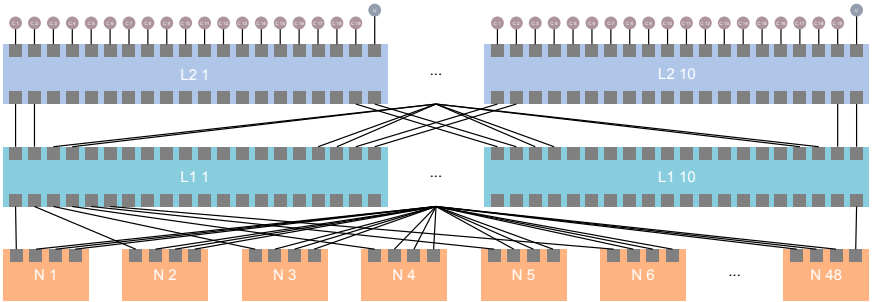
Overview

- 3744 end points; adaptive routing
- HDR200: 200 Gbit/s per link per direction
- Dragonfly+ Topology selected as good way to balance factors (space, investment, performance)
- Two-level topology: local (in-cell), non-local (inter-cell)
- Still learning practical implications of topology

DragonFly+ Topology

In-Cell Topology

- In-cell: full fat-tree in 2 levels
  - 48 nodes, each 4 links *(strided to 4 L1 switches)*
  - 10 L1 switches, 48 port *(each L1 switch: 2 links to L2, strided to 10 L2 switches)*
  - 10 L2 switches, 48 port *(each L2 switch: 1 link to L2 switch of all other cells, 1 link to cluster)*

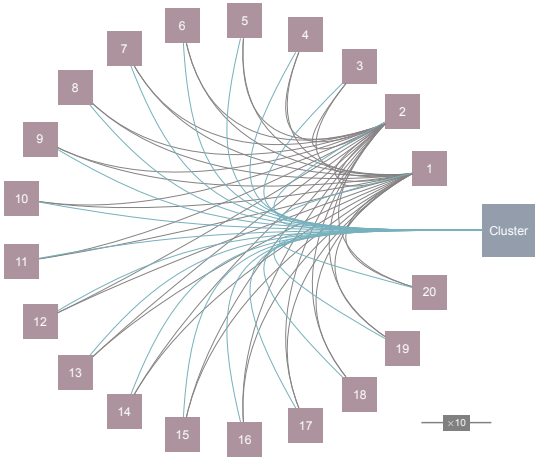


DragonFly+ Topology

Intra-Cell Topology

- Inter-cell: 20 cells
  - 10 links between each pair of cells
  - 10 links per cell to JUWELS Cluster
  - Filesystem access via cell 20
  - Bi-section bandwidth between N cells:

$$\mathcal{B}(N) = \lfloor (N/2)^2 \rfloor \times (10 \times \mathrm{bw}_1)$$

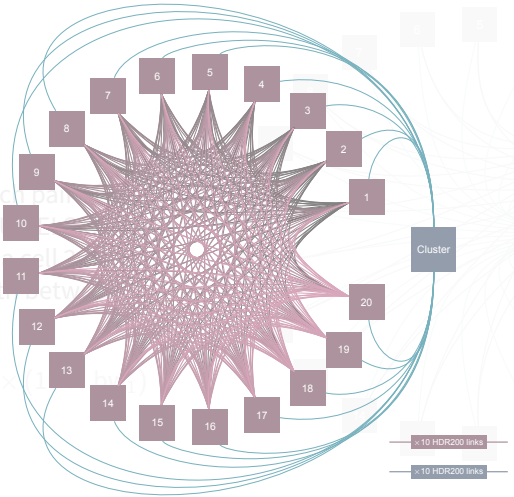


DragonFly+ Topology

Intra-Cell Topology

- Inter-cell: 20 cells
  - 10 links between each pa
  - 10 links per cell to J
  - Filesystem access via all
  - Bi-section bandwid
    cells:

$$B(N) = \lfloor (N/2)^2 \rfloor$$



Summary and Conclusions

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Thank you for your attention!

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