به نام خدا

پروژه اول

طراحی کامپیوتری

سیستم های دیجیتال

پاییز 1401

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فایل های وریلاگ:

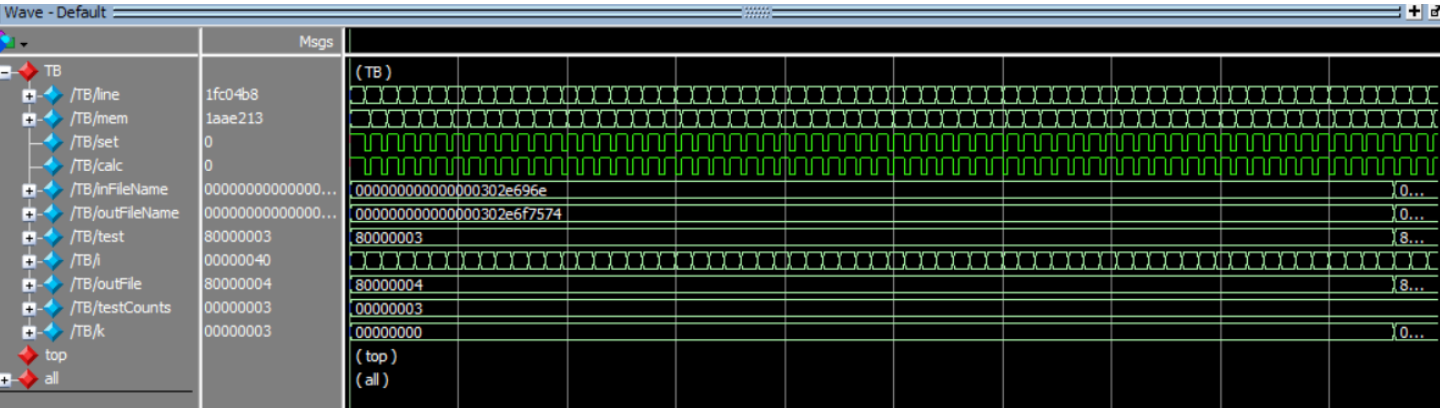
```
`timescale 1ns/1ns
module Controller (
    set,
    calc
);
    input set;
    output reg calc;
    always@(set)begin
    calc = 1'b0;
    if(set == 1'b1)
       calc = 1'b1;
    end

endmodule
```

```
`timescale 1ns/1ns
module DataPath (
    in,
    out,
    calc,
    set
);
    parameter memsize = 25;

    input calc, set;
    input [memsize-1:0]in;
    output [memsize-1:0]out;

    Reg25 permutation_reg(in, out, calc, set);
endmodule
```

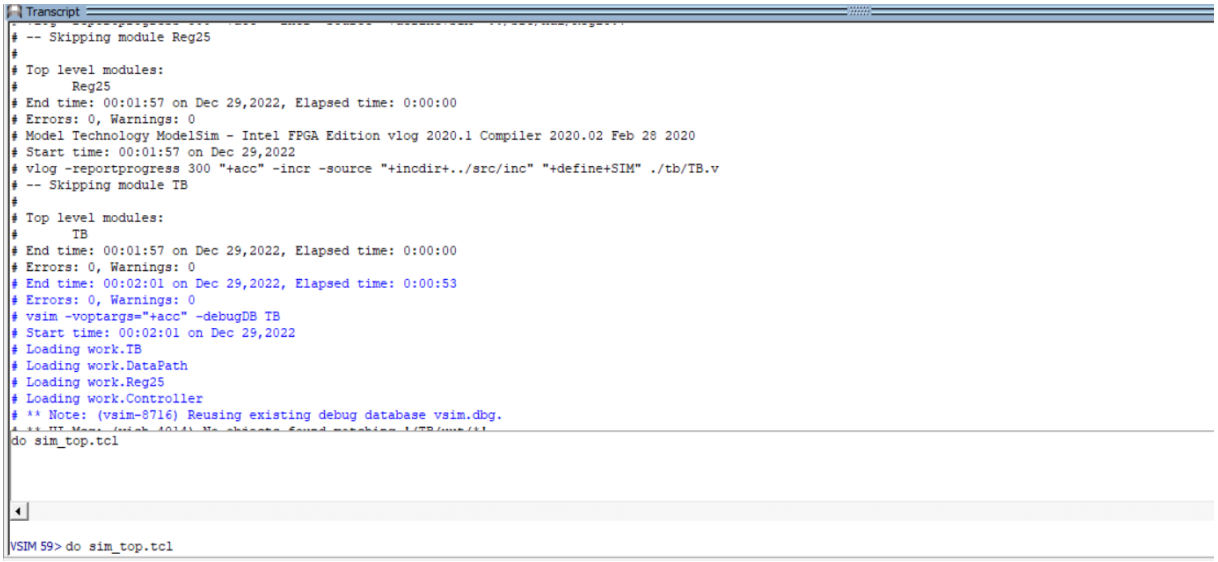
```
`timescale 1ns/1ns
`define EOF 32'hFFFF_FFFF

module TB ();

    reg [24:0] Mem [0:63];
    reg [24:0]line;
    wire [24:0]mem;

    reg set = 1'b1;
    wire calc;

    reg [8*11:0]inFileName = "0.in";
    reg [8*12:0]outFileName = "0.out";

    integer test, i, outFile, testCounts=3, k;

    DataPath db(line, mem, calc, set);
    Controller cu(set, calc);

    initial begin
        for (k = 0; k < testCounts ; k = k+1) begin
            $sformat(inFileName, "%0d.in", k);
            $sformat(outFileName, "%0d.out", k);
            $readmemb(inFileName,Mem);
            test = $fopen(inFileName, "r");
            outFile = $fopen(outFileName, "w");

            for(i = 0; i < 64; i= i+1) begin
                line = Mem[i];
        #5 set = 1'b1;
                #5;
                $fwriteb(outFile, mem);
                $fdisplay(outFile, "");
        #5 set = 1'b0;
            end
            $fclose(test);
            $fclose(outFile);
        end
        #1000;
        $stop;
    end

endmodule
```

```
`timescale 1ns/1ns
module Reg25 (
    in,
    out,
    calc,
    set
);
    parameter memsize = 25;

    input calc, set;
    input [memsize-1:0]in;
    output [memsize-1:0]out;

    reg [memsize-1:0]mem;

    always @(posedge set)
    mem = in;

    always @(posedge calc) begin
        mem[10] <= mem[0];
        mem[11] <= mem[6];
        mem[12] <= mem[12];
        mem[13] <= mem[18];
        mem[14] <= mem[24];
        mem[20] <= mem[1];
        mem[21] <= mem[7];
        mem[22] <= mem[13];
        mem[23] <= mem[19];
        mem[5] <= mem[2];
        mem[6] <= mem[8];
        mem[7] <= mem[14];
        mem[24] <= mem[20];
        mem[15] <= mem[3];
        mem[16] <= mem[9];
        mem[8] <= mem[15];
        mem[9] <= mem[21];
        mem[0] <= mem[4];
        mem[17] <= mem[10];
        mem[18] <= mem[16];
        mem[19] <= mem[22];
        mem[1] <= mem[5];
        mem[2] <= mem[11];
        mem[3] <= mem[17];
        mem[4] <= mem[23];
    end
```

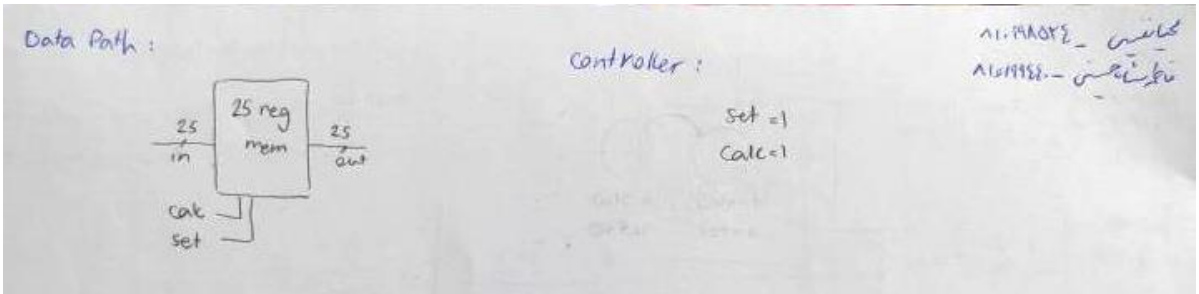
:Waveform



: Run in Modelsim

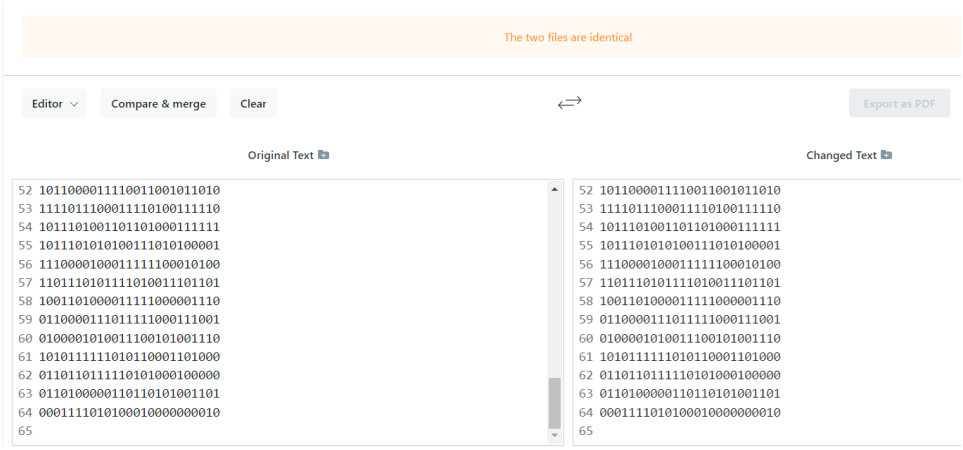


Data Path and Controller

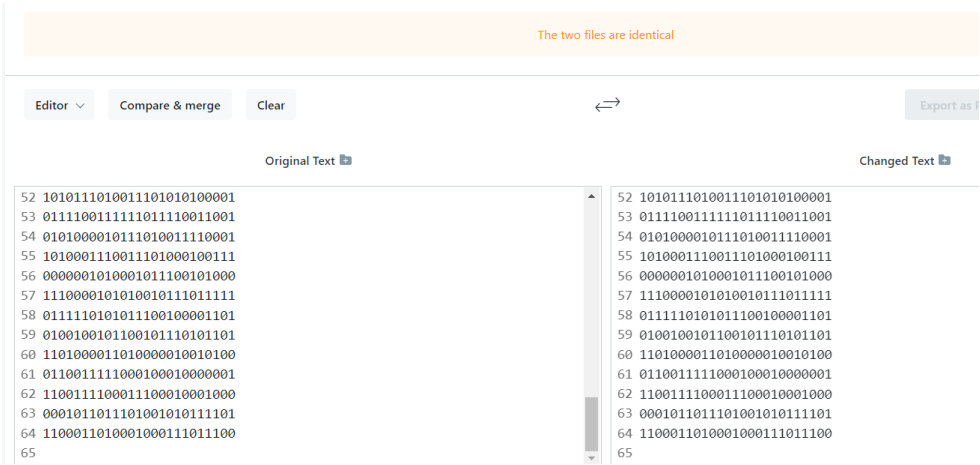


Test cases

0.out<<



1.out<<



2.out <<