SSP0700A1-800480 Series SSP0700A2-1024600 Series SPI TFT LCD Module USER MANUAL

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Shenzhen Surenoo Technology Co.,Ltd.

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Reference Controller Datasheet

SPI TFT LCD Module Selection Guide

LT7686

FT5426

Model No.: SSP0700A2-1024600

Model No.: SSP0700A1-800480

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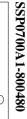
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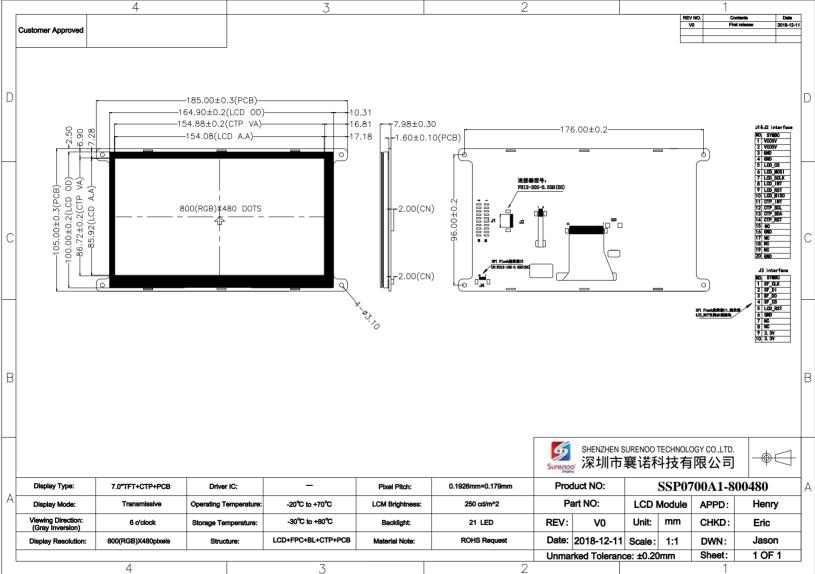
1, GENERAL INFORMATION

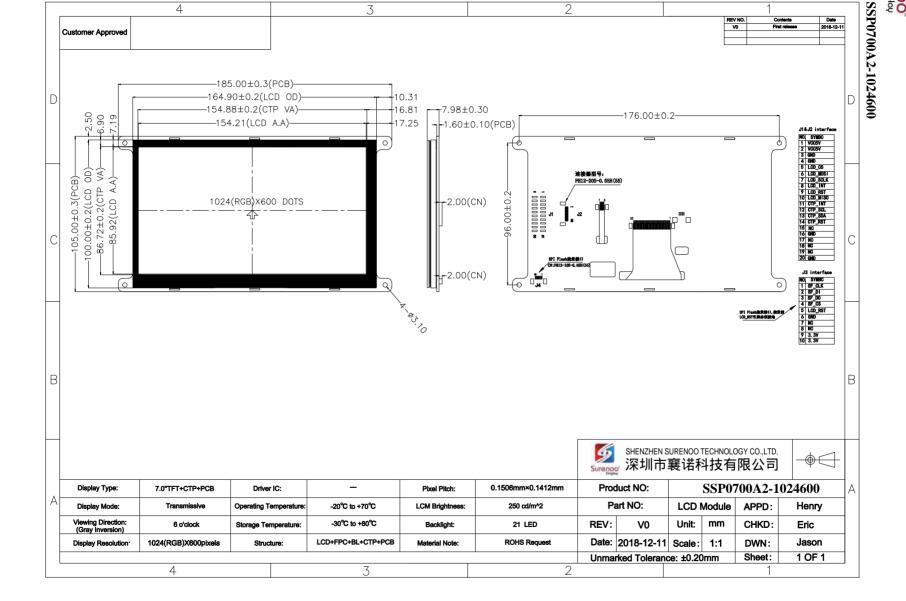
Item of general information		Con	tents	Unit
LCD Display Size (Diagonal)		7.0		inch
Module Structure	LCD .	Display + C	CTP Touch + PCB	-
LCD Display Type		TFT/TRAN	NSMISSIVE	-
LCD Display Mode		Normal	lly White	-
Recommended Viewing Direction		Î	12	o'clock
Gray inversion Direction			6	o'clock
$Module\ size\ (W{ imes}H{ imes}T)$	185.00×105.00×7.98		mm	
Active area (W×H)	154.21×85.92		154.08×85.92	mm
Number of pixels (Resolution)	1024R	<i>PGB</i> ×600	800RGB×480	pixel
Pixel pitch (W×H)	0.1500	6×0.1432	0.1926×0.1790	mm
LCD Driver IC			-	-
	LCD	LCD SPI interface (LT7686)		-
Module Interface Type	СТР	I2C interface (FT5426)		-
Module Input voltage	5.0V		V	
Module Power consumption	-		mW	
Color Numbers		16.	.7M	-
Backlight Type		White	e LED	-



2, EXTERNAL DIMENSIONS







3, ABSOLUTE MAXIMUM RATINGS

Parameter of absolute maximum ratings	Symbol	Min	Max	Unit
Operating temperature	Тор	-20	70	$^{\circ}C$
Storage temperature	Tst	-30	80	$^{\circ}C$
Humidity	RH	-	90%(Max 60°C)	RH

Note: Absolute maximum ratings means the product can withstand short-term, not more than 120 hours. If the product is a long time to withstand these conditions, the life time would be shorter.

4. ELECTRICAL CHARACTERISTICS(DC CHARACTERISTICS)

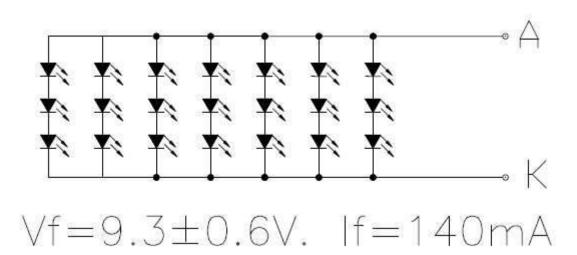
Parameter of DC characteristics	Symbol	Min.	Тур.	Max.	Unit
PCB operating voltage	VCC5V	-	5.0	-	V
LCD I/O operating voltage	VDD	3.0	3.3	3.6	V
Input voltage 'H' level	VIH	2	-	3.6	V
Input voltage 'L' level	VIL	-0.3	-	0.8	V
Output voltage 'H' level	VOH	2.4	-	-	V
Output voltage 'L' level	VOL	-	-	0.4	V

5 SACKLIGHT CHARACTERISTICS

Item of backlight characteristics	Symbol	Min.	Тур.	Max.	Unit	Remark
Forward Voltage	Vf	8.7	9.3	9.9	V	Note1
Forward Current	If	-	140	-	mA	-
Number of LED	_	-	3*7=21	-	Piece	-
LED Connection mode	P/S	-	Serial/Parallel	-	-	-
Lifetime of LED	-	-	10000	-	hour	Note2

Note:

- Note1: The LED Supply Voltage is defined by the number of LED at Ta=25°C and If=140mA.
- Note2: The LED lifetime define as the estimated time to 50% degradation of initial luminous. The LED lifetime could be decreased if operating If is larger than 140mA.
- Backlight circuit:



6, CTP CHARACTERISTICS

Item of CTP characteristics	Specification	Unit	Remark
Panel Type	Glass Cover + Glass Sensor	-	-
Resolution	800*480/1024*600	pixel	-
Surface Hardness	<i>≥6H</i>	-	-
Transparency	>82%	-	-
Driver IC	FT5426	-	-
Interface Type	I2C	-	-
Support Points	5	-	-
Sampling Rate	20~100	Hz	-
Supply voltage	3.3	V	-

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7、ELECTRO-OPTICAL CHARACTERISTICS

Item o electro-op character	otical	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark	Note
Response	time	Tr+Tf	$\theta = 0$	-	25	40	ms	FIG 1.	4
Contrast I	Ratio	CR	$\theta = 0$ $\emptyset = 0$	-	320	-	-	<i>FIG 2</i> .	1
Luminance un	iformity	<i>SWHITE</i>	Ta=25°C	-	80	-	%	<i>FIG 2</i> .	3
Surface Lum	inance	Lv		-	250	-	cd/m2	<i>FIG 2</i> .	2
	White	White x	$\theta=0$ $\varnothing=0$ $Ta=25^{\circ}C$	_	0.302	-		FIG 2.	
	White	White y		_	0.338	-			5
	Red	Red x		_	0.606	-			
CIE(x, y)	кеа	Red y		_	0.325	_			
chromaticity	C	Green x		-	0.303	-			
	Green	Green y	14 25 C	-	0.567	-			
	D.I.	Blue x		-	0.147	-			
	Blue	Blue y		-	0.161	-			
	Ø=90(1	2 o'clock)		-	60	-	deg		
Viewing angle range	Ø=270((6 o'clock)	CD > 10	-	70	-	deg deg deg	EIC 2	6
	Ø=0(3 d	o'clock)	<i>CR</i> ≥ 10	-	60	-		FIG 3.	
	Ø=180 ₀	9 o'clock)		-	60	-			
NTSC ratio		-	-	-	50		%		

Note 1. Contrast Ratio(CR) is defined mathematically by the following formula. For more information see FIG 2.:

 $Contrast\ Ratio(CR) = \frac{Average\ Surface\ Luminance\ with\ all\ white\ pixels(P1,P2,P3,P4,P5,P6,P7,P8,P9)}{Average\ Surface\ Luminance\ with\ all\ black\ pixels(P1,P2,P3,P4,P5,P6,P7,P8,P9)}$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see FIG 2.

Lv=Average Surface Luminance with all white pixels (P1,P2,P3,P4,P5,P6,P7,P8,P9)

Note 3. The uniformity in surface luminance $(\delta WHITE)$ is determined by measuring

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luminance at each test position 1 through 9, and then dividing the maximum luminance of 9 points luminance by minimum luminance of 9 points luminance. For more information see FIG 2.

$$\delta \text{WHITE} = \frac{Minimum \, Surface \, Luminance \, with \, all \, white \, pixels \, (P1, P2, P3, P4, P5, P6, P7, P8, P9)}{Maximum \, Surface \, Luminance \, with \, all \, white \, pixels \, (P1, P2, P3, P4, P5, P6, P7, P8, P9)}$$

Note 4. Response time is the time required for the display to transition from White to black(Rise Time, Tr) and from black to white(Decay Time, Tf). For additional information see FIG 1.

Note 5. CIE (x, y) chromaticity, The x,y value is determined by screen active area position 5. For more information see FIG 2.

Note 6. Viewing angle is the angle at which the contrast ratio is greater than a specific value. For TFT module, the specific value of contrast ratio is 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

Note 7. For Viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope. Series Instruments. For contrast ratio, Surface Luminance, Luminance uniformity and CIE, the testing data is base on BM-7 photo detector.

Note 8. For TN type TFT transmissive module, Gray scale reverse occurs in the direction of panel viewing angle.

FIG.1. The definition of Response Time

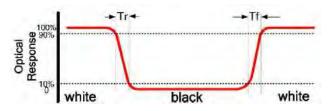


FIG.2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE(x, y) chromaticity

A: H/6; B: V/6;

H,V: Active Area(AA) size

Measurement instrument: BM-7; Light spot size=5mm, 350mm distance from the LCD surface to detector lens.

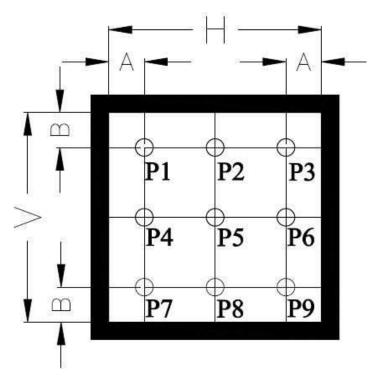
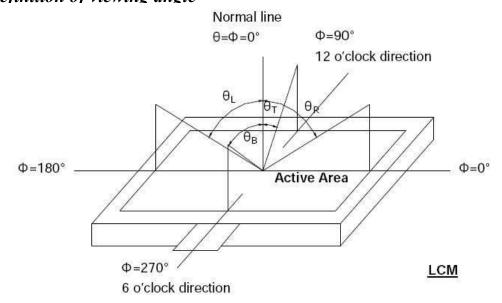


FIG.3. The definition of viewing angle



8. INTERFACE DESCRIPTION

8.1, J1 J2 Interface Description (SPI interface)

NO.	Symbol	I/O	DESCRIPTION
1~2	VCC5V	Power supply	Module Power supply (5V Typ.)
3~4	GND	Power supply	Power ground
5	LCD_CS	I	Chip Select pin for 3-wire or 4-wire serial I/F.
6	LCD_MOSI	I	Data input pin of 4-wire SPI I/F.
7	LCD_SCLK	I	Clock of 3-wire or 4-wire serial I/F.
8	LCD_INT	0	The interrupt output for host to indicate the status.
9	LCD_RST	I	This is an active low Reset pin for LCD.
10	LCD_MISO	0	Data output pin of 4-wire SPI I/F. Bi-direction data pin of 3-wire SPI I/F.
11	CTP_INT	0	CTP External interrupt to the host
12	CTP_SCL	I	CTP I2C clock input
13	CTP_SDA	I/O	CTP I2C data input and output
14	CTP_RST	I	CTP external reset signal, Low is active
15	NC	-	No connection
16	GND	Power supply	Power ground
17	NC	-	No connection
18	NC	-	No connection
19	NC	-	No connection
20	GND	Power supply	Power ground

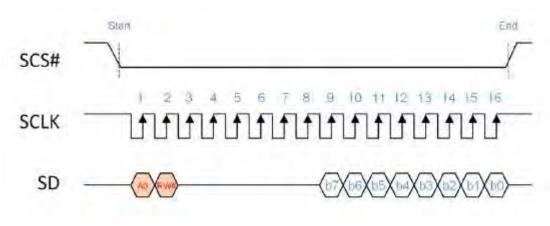


8.2, J3 Interface Description (SPI Flash burning interface)

NO.	Symbol	I/O	DESCRIPTION
1	SF_CLK	I	Serial Clock Input
2	SF_DI	I	Data Input
3	SF_DO	0	Data output
4	SF_CS	I	Chip Select Input
5	LCD_RST	I	LCD RESET signal. This pin must be pull low
6	GND	Power supply	Power ground
7	NC	-	No connection
8	NC	-	No connection
9~10	3.3V	Power supply	Power supply for the SPI Flash (3.3V Typ.)

9, INPUT TIMING

9.1 , 3-wire SPI Interface



Status Register Read:

- 1. Host drive SCS#(Low) and SCLK (SPI Clock).
- 2. Host drive A0(Low), then drive RW#(High).
- 3. The Driver IC will drive the Data of Status Register ($b7 \sim b0$) at 9th ~ 16 th Clock. Then Host will get the content of Status Register.

Write Register's Address:

- 1. Host drive SCS#(Low) and SCLK.
- 2. Host drive A0(Low), then drive RW#(Low).
- 3. Host drive the Register's Address ($b0 \sim b7$) at 9th ~ 16 th Clock to The Driver IC.

Write Data to Register or Memory:

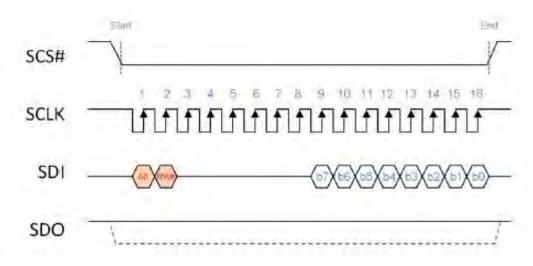
- 1. Host drive SCS#(Low) and SCLK.
- 2. Host drive A0(High), then drive RW#(Low).
- 3. Host drive the Data at 9th ~ 16th Clock to The Driver IC. i.e. Data will be stored in Register or Memory.

Read Register's Data:

- 1. Host drive SCS#(Low) and SCLK.
- 2. Host drive A0(High), then drive RW#(High).
- 3. The Driver IC will drive the Data of Register at 9th \sim 16th Clock. Then Host will get the content of Register.

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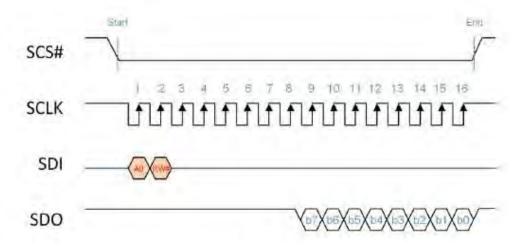
9.2, 4-wire SPI Interface



4-Wire SPI Interface Write Timing

When Host drive A0(Low) and RW#(Low), that's means Host write Register's Address. When Host drive A0(High), then RW#(Low) that's means Host write data to Register or Display RAM.

The following Timing diagram is the Read Cycle of 4-Wires SPI. When Host drive A0(Low) and RW#(High), that's means Host want to read the data of Status Register. The Driver IC will drive the Data of Status Register ($b7 \sim b0$) at $9th \sim 16th$ Clock. Then Host will get the data of Status Register. When Host drive A0(High), then RW#(High) that's means Host want to read the data of Command Register. The Driver IC will drive the Data of Command Register ($b7 \sim b0$) at $9th \sim 16th$ Clock for Host. Of course, Host will get the content of Command Register.



4-Wire SPI Interface Read Timing

10.	RELIABILITY	YTEST	CONDITIONS
101			CULIDITION

No.	Test Item	Test Condition
1	High Temperature Storage	80°C/120 hours
2	Low Temperature Storage	-30°C/120 hours
3	High Temperature Operating	70°C/120 hours
4	Low Temperature Operating	-20°C/120 hours
5	Temperature Cycle Storage	-20°C(30min.)~25(5min.)~70°C(30min.)×10cycles

A. Inspection after test:

Inspection after 2~4 hours storage at room temperature, the sample shall be free from defects:

- *Air bubble in the LCD;*
- Sealleak;
- Non-display;
- Missing segments;
- Glass crack;
- Current is twice higher than initial value.

B, Remark:

- The test samples should be applied to only one test item.
- Sample size for each test item is 5~10pcs.
- Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11 SINSPECTION CRITERION

This specification is made to be used as the standard of acceptance/rejection criteria for TFT-LCD/IPS TFT-LCD module product, and this specification is applicable only in the case that the size of module equal to or exceed than 3.5 inch.

11.1 Sample plan

Sampling plan according to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993,normal level 2 and based on:

Major defect: AQL 0.65

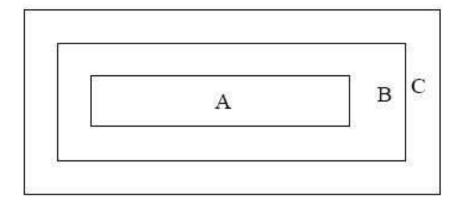
Minor defect: AQL 1.5

11.2 Inspection condition

Viewing distance for cosmetic inspection is about 30cm with bare eyes, and under an environment of $20\sim40W$ light intensity, all directions for inspecting the sample should be within 45° against perpendicular line. (Normal temperature $20\sim25$ ° Cand normal humidity 60 $\pm15\%$ RH)

11.3 Definition of Inspection Item.

A Definition of inspection zone in LCD.



Zone A: character/Digit area

Zone B: viewing area except Zone A (Zone $A + Zone B=minimum \ Viewing \ area)$

Zone C: Outside viewing area (invisible area after assembly in customer's product)

Fig. 1 Inspection zones in an LCD

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

B. Definition of some visual defect

	Because of losing all or part function, bad pixel dots appear bright and the
Bright dot	size is more than 50% of one dot in which LCD panel is displaying under
	black pattern.
Dowl La	Dots appear dark and unchanged in size in which LCD panel is displaying
Dark dot	under pure red, green, blue picture, or pure whiter picture.

11.4 Major Defect

Item No.	Items to be inspected	Inspection standard	Classification of defects
1	Functional defects	 No display Display abnormally Missing vertical, horizontal segment Short circuit Excess power consumption Backlight no lighting, flickering and abnormal lighting 	major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	



Surenco[®] 11.5 Minor Defect

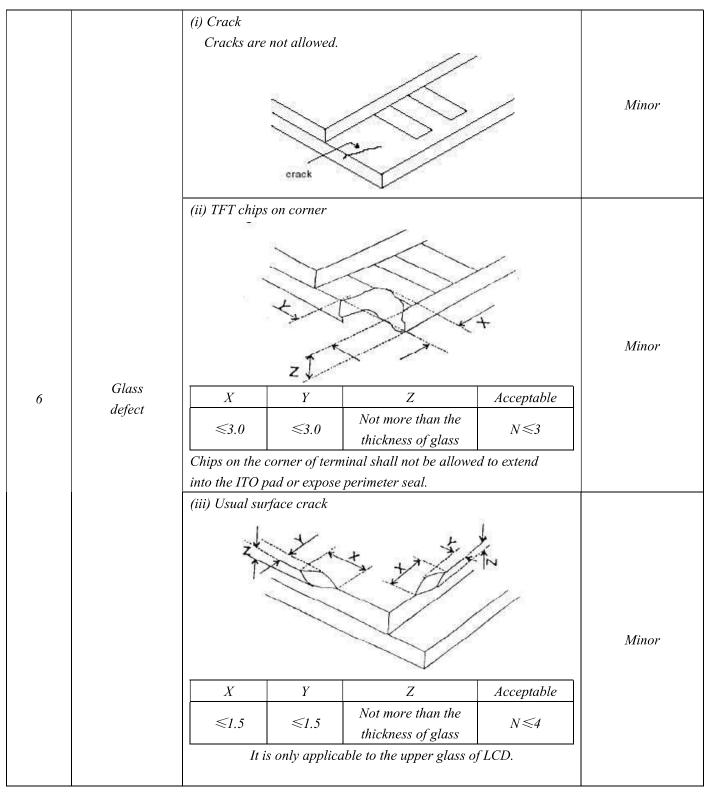
Item No.	Items to be	Inspection standard						Classification of defects	
		Zone		Acceptable Qty A+B					
				3.5" ∼ 7"	7~10.1	>10.1"	С		
		Bright pixel do	rt .	1	2	3			
	Bright dot	Dark pixel do		4	4	4	A		
1	/dark dot defect	2bright dots adjo		0	0	0	Acceptable	Minor	
		2dark dots adja		0	0	0	ptal		
		Total bright and dots		5	6	7	ble		
		Note: Minimum distance between defective dots is more than 5mm; Pixel dots' function is normal, but bright dots caused by foreign material and other reasons are judged by the dot defect of 5.2.							
	Dot defect	Zone Acceptable Qty							
			A+B						
		Size(mm)	3.5"~	7~7" 7~10.1" >10.1"		>10.1"	c		
		<i>Φ</i> ≤0.2	Accepto	able Ac	cceptable	Acceptable	Acc		
2		$0.2 < \Phi \leqslant 0.5$	4	4	5	6	Acceptable	Minor	
2		Φ>0.5	0		0	0	ible	Millor	
		Note: 1. Minimum distance between defective dots is more than 5 mm; 2. The quantity of defect is zero in operating condition.							
	Linear defect	Zone Acceptable Qty							
3		Size (mm)	A+B						
		Length Width	3.5"~	7" 7	<i>'~10.1</i> "	>10.1"	С	Minor	
		defect	Ignore W≤0.05	Accepta	able Ac	ceptable	Acceptable	Ac	Minor
		$ \begin{array}{ c c c } \hline L \leqslant 5.0 & 0.05 < \\ \hline W \le 0.1 \end{array} $	4		5	6	Acceptable		
		L>5.0 W>0.1	0		0	0	le		

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Display	<u> </u>							
		5.4.1 Pola						
		(i) Shiftin						
		dimension						
		(ii) Incor						
		allowed.						
		5.4.2 Dirt						
		Dirt which						
		5.4.3 Pola						
		Zone Acceptable Qty						
				A+B				
		Size(mm)		3.5"~7" 7~10.1" >10.1"			С	
			<u>≤0.2</u>	Acceptable	Acceptable	Acceptable		
			10.2		, and a primary	TICO OF THIS IS	Acc	
		0.2 <	<i>Φ</i> ≤0.5	4	5	6	ept	
	Polarizer	Φ	>0.5	0	0	0	Acceptable	
4	defect					, and the second		Minor
	иејесі	5.4.4 Pol	larizer scr	atch				
		(i) If the I						
		or in the	operating	condition, ji	idge by the li	inear defect (of 5.3.	
		(ii)If the						
		condition	or some	special angle	, judge by th	e following:		
			Zone		Acceptable	Otv		
		Size (mm)		A+B				
		Length	Width	3.5"~7"	7~10.1"	>10.1"	С	
		Ignore	<i>W</i> ≤0.05	Acceptable	Acceptable	Acceptable	A	
		1.0 <l< td=""><td>0.05 <</td><td></td><td></td><td></td><td rowspan="3">Acceptable</td><td></td></l<>	0.05 <				Acceptable	
		≤5.0	<i>W</i> ≤0.20	4	5	6		
		L>5.0	W>0.2	0	0	0		
		1 2. 0.0	1	-	-	-		
	MURA	Using						
5								
			Minor					
	W/L:4 - /D1 1	17						
	White/Black	V_{i}						
	dot (MURA)	0.1.						
Ī								







11.6 Module Cosmetic Criteria

Item No.	Items to be inspected	Inspection Standard	Classification of defects
1	Difference in Spec.	Not allowable	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
	Soldering defects	No soldering missing	Major
3		No soldering bridge	Major
		No cold soldering	Minor
4	Resist flaw on PCB	Visible copper foil (Φ0.5 mm or more) on substrate pattern is not allowed	Minor
5	FPC gold finger	No dirt, breaking, oxidation lead to black	Major
6	Backlight plastic frame	No deformation, crack, breaking, backlight positioning column breaking, obvious nick.	Minor
7	Marking printing effect	No dark marking, incomplete, deformation lead to unable to judge	Minor
8	Accretion of metallic Foreign matter	No accretion of metallic foreign matter (Not exceed Φ 0.2mm)	Minor
9	Stain	No stain to spoil cosmetic badly	Minor
10	Plate discoloring	No plate fading, rusting and discoloring	Minor
	1. Lead parts	a. Soldering side of PCB Solder to form a 'Filet' all around the lead. Solder should not hide the lead form perfectly.	Minor
		b. Components side(In case of 'Through Hole PCB') Solder to reach the Components side of PCB.	Minor
11	2. Flat packages	Either 'Toe'(A) or 'Seal'(B)of the lead to be covered by "Filet". Lead form to be assume over Solder.	Minor
	3. Chips	(3/2) H ≥h ≥(1/2) H ↑ ↑ ↑ ↑ ↑ ↑ ↑ H	Minor
	4. Solder ball/Solder splash	a. The spacing between solder ball and the conductor or solder pad $h \ge 0.13$ mm. The diameter of solder ball $d \le 0.15$ mm.	Minor
		b. The quantity of solder balls or solder splashes isn't beyond 5 in 600 mm2.	Minor
		c. Solder balls/Solder splashes do not violate minimum electrical clearance.	Major