1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs

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Abstract—This paper presents bandgap reference (BGR) and sub-BGR circuits for nanowatt LSIs. The circuits consist of a nano-ampere current reference circuit, a bipolar transistor, and proportional-to-absolute-temperature (PTAT) voltage generators. The proposed circuits avoid the use of resistors and contain only MOSFETs and one bipolar transistor. Because the sub-BGR circuit divides the output voltage of the bipolar transistor without resistors, it can operate at a sub-1-V supply. The experimental results obtained in the 0.18-μm CMOS process demonstrated that the BGR circuit could generate a reference voltage of 1.09 V and the sub-BGR circuit could generate one of 0.548 V. The power dissipations of the BGR and sub-BGR circuits corresponded to 100 and 52.5 nW.

Index Terms—Bandgap reference (BGR) circuits, CMOS analog integrated circuits, low voltage, nanowatt, reference circuits.

I. INTRODUCTION

THE development of nanowatt LSIs is expected to lead to the expansion of next-generation power-aware applications such as life-log and life-assist medical devices, environmental sensors, and wireless sensor networks [1], [2]. Because they must operate for a long time with less-than-ideal energy supply from microbatteries or from surrounding natural energy, we need to design LSIs that operate with extremely low power dissipation. To develop such LSIs, we must first develop voltage reference circuits because they are one of the most fundamental analog building circuits. Here, we describe process, voltage, and temperature (PVT) variation-tolerant voltage reference circuits that can operate at several tens of nanowatts or less.

Bandgap reference (BGR) circuits are widely used in modern LSIs to generate a reference voltage on chips. The generated voltage is used for various analog signal processes. Although several BGRs have been developed, the power dissipations of most of them exceed nanowatt power [3]–[7] and have not been

significantly reduced. One reason for this is the use of resistors. The resistors in most reference circuits are used to generate current or voltage to control the temperature characteristics of the output reference voltage [3]–[9]. When we use a moderate value for resistance, sufficient current for the resistors is required and power dissipation therefore cannot be reduced. Although it can be reduced if we accept using a large value for resistance, the resistors will occupy a large area of the silicon.

Resistor-less voltage reference circuits that operate at nanowatt power have been reported [10]–[12]. However, because the output reference voltages of these circuits are based on the threshold voltage of MOSFETs, the voltages will change with process variations [10]–[12]. Therefore, they are not suitable for use as voltage reference circuits.

This paper presents a nanowatt BGR circuit that does not use resistors [13]. In contrast to Hirose *et al.* [13], we use a different 0.18-μm CMOS process to demonstrate the robustness of our BGR circuit architecture. The proposed BGR consists of a nano-ampere current reference circuit, a bipolar transistor, and proportional-to-absolute-temperature (PTAT) voltage generators. Because the circuit only consists of MOSFETs except for the bipolar transistor, it can generate a bandgap voltage without resistors. In addition, a sub-BGR circuit that generates voltage lower than 1.2 V is also presented. The proposed sub-BGR uses a voltage divider. The voltage divider accepts the base-emitter voltage of the bipolar transistor and generates a sub-1-V reference voltage in combination with the PTAT voltage generators. Therefore, the proposed sub-BGR is useful as a reference circuit in sub-1-V LSIs.

This paper is organized as follows. Section II presents the operating principles behind our proposed circuits. Section III describes the implementation of the circuits using 0.18-μm CMOS process technology with deep N-well option and presents the experimental results with a fabricated proof-of-concept chip. Extremely low power dissipation of 100 nW for the BGR and 52.5 nW for the sub-BGR were achieved. Section IV concludes the paper.

II. ARCHITECTURE

A. Characteristics of Subthreshold Current

Subthreshold operation achieves ultralow-power operation because the subthreshold current is of the order of nano-amperes. When a drain–source voltage V_{DS} of a MOSFET is
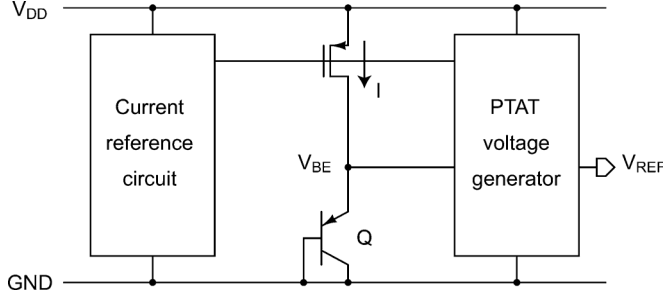
Fig. 1. Architecture of proposed BGR circuit.

higher than roughly 0.1 V, subthreshold current I is expressed as

$$I = K I_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\eta V_T}\right) \qquad (1)$$

where K is the aspect ratio ($=W/L$) of the transistor, $I_0(= \mu C_{\mathrm{OX}}(\eta-1)V_T^2)$ is a process-dependent parameter, μ is the carrier mobility, $C_{\mathrm{OX}}(= \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}})$ is the gate–oxide capacitance, $\varepsilon_{\mathrm{ox}}$ is the oxide permittivity, t_{ox} is the oxide thickness, η is the subthreshold slope factor, V_{GS} is a gate–source voltage, $V_T(= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and V_{TH} is the threshold voltage of the MOSFET [14]. We will use (1) to analyze the characteristics of a subthreshold MOSFET. Note that, in this work, we assumed that η is a constant parameter (in the process used, $\eta \sim 1.14$ and 1.40 for nMOSFETs and pMOSFETs, respectively). However, η is not constant in actual devices and depends on gate-oxide and depletion-layer capacitances [14]. This must be taken into account in high-accuracy applications.

B. BGR

Fig. 1 shows the architecture of the proposed BGR circuit. It consists of a nano-ampere current reference circuit, a bipolar transistor, and a PTAT voltage generator. The operating principles of the circuits are as follows.

PTAT voltage in conventional BGR circuits is generated by using bipolar transistors and resistors. However, as we explained in the previous section, it is not advantageous to use resistors at nano-ampere current levels. Fig. 2 shows the PTAT voltage generator we used [8], [13]. It consists of a differential pair with a current mirror. When the MOSFETs operate in the subthreshold region, gate-to-gate voltage V_{GG} in this circuit can be expressed from (1) as

$$\begin{aligned} V_{\mathrm{GG}} &= V_{\mathrm{OUT}} - V_{\mathrm{IN}} \\ &= V_{\mathrm{GS},D2} - V_{\mathrm{GS},D1} \\ &= V_{\mathrm{TH}} + \eta V_T \ln\left(\frac{I_{D2}}{K_{D2}I_0}\right) - \left(V_{\mathrm{TH}} + \eta V_T \ln\left(\frac{I_{D1}}{K_{D1}I_0}\right)\right) \\ &= \eta V_T \ln\left(\frac{K_{D1}K_{M2}}{K_{D2}K_{M1}}\right) \qquad (2) \end{aligned}$$

where K_{D1} and K_{D2} correspond to aspect ratios in the differential pair, and K_{M1} and K_{M2} correspond to aspect ratios in
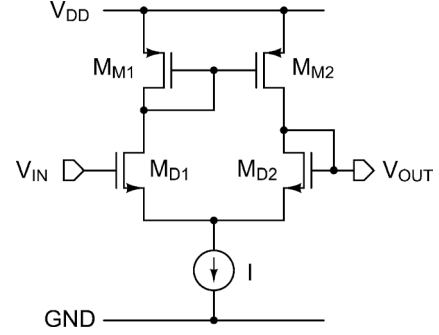

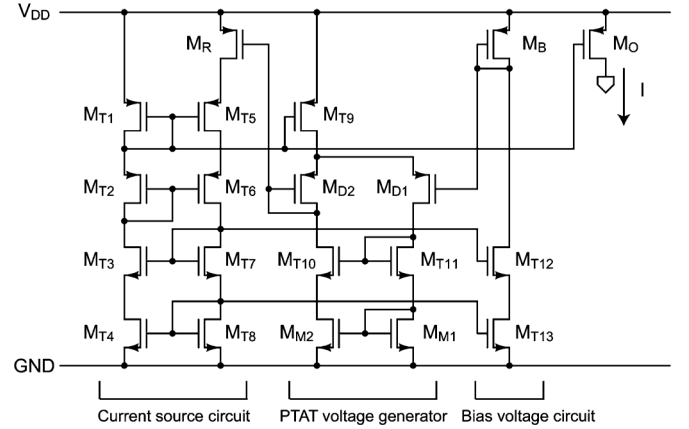Fig. 2. PTAT voltage generator consisting of differential pair circuit.

Fig. 3. Schematic of nano-ampere current reference circuit [15].

the pMOS-current mirror. Therefore, PTAT voltage can be generated by making $K_{D1}K_{M2}/K_{D2}K_{M1} > 1$.

The nano-ampere current reference circuit generates a 10-nA current [15] and supplies it to the others. Fig. 3 is a schematic of a nano-ampere a current reference circuit (no start-up circuit is shown) we used [15]. The circuit consists of a bias voltage circuit, the PTAT voltage generator, and a current source circuit. All MOSFETs operate in the subthreshold region except for the MOS resistor (M_R) that operates in the strong-inversion and deep triode regions. The gate length L and the gate width W of M_R and M_B are the same, and they are biased at the same current. The PTAT voltage generator adds a voltage to the gate–source voltage of M_B in order to increase that of M_R. The difference in their gate–source voltages forced across MOS resistor M_R, which is operating in the strong-inversion and deep triode regions. The value of the MOS resistor is defined by

$$I = \mu C_{\mathrm{OX}} K (V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}}. \qquad (3)$$

Equally sized MOSFETs M_R and M_B make their threshold voltages similar, so the value of the generated current is robust to process variations [15]. In [15], the generated current in 15 samples from one wafer exhibited a variance of 14.1%.

The bipolar transistor accepts the current through a current mirror and generates a base-emitter voltage V_{BE}, which is expressed as

$$V_{\mathrm{BE}} = V_T \ln\left(\frac{I_S + I}{I_S}\right) \approx V_T \ln\left(\frac{I}{I_S}\right) \qquad (4)$$
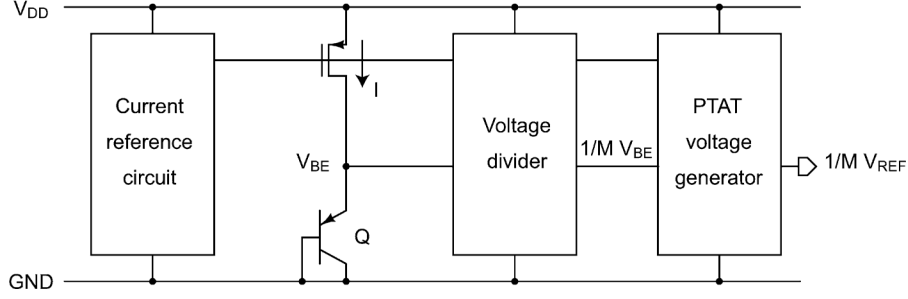
Fig. 4. Architecture of proposed sub-BGR circuit.

where I_S is the saturation current of the bipolar transistor [14]. Because V_{BE} decreases linearly with temperature, (4) can be simplified as

$$V_{BE} = V_{BGR} - \gamma T \tag{5}$$

where V_{BGR} is the bandgap voltage of the silicon (i.e., ~ 1.2 V) and γ is the temperature coefficient of V_{BE}. Because V_{BE} has a negative dependence on temperature, the PTAT voltage generator is used to cancel out this dependence. As (5) is approximated by the first order, V_{BE} has higher order dependencies on temperature. Therefore, there will be nonlinearities in the output voltage even though we cancel out the negative dependence of V_{BE} on temperature. However, the nonlinearities can be compensated for if we use a technique of curvature compensation such as that reported by Ge *et al.* [5]. The bias current of the bipolar transistor also determines the accuracy of V_{BE}. Because bias current is generated from the current reference circuit and the generated current is tolerant to threshold voltage variations, the current variations can be minimized [15]. Therefore, the effect of bias current variations can also be minimized.

The PTAT voltage generator in Fig. 2 supplies voltage which has a positive dependence on temperature as discussed previously. However, because $K_{D1}K_{M2}/K_{D2}K_{M1}$ in (2) is included in a logarithmic function, it must have a large value (~ 40 M) in order for the positive temperature coefficient of V_{GG} to cancel out the negative temperature dependence (~ -2 mV/°C) of base-emitter voltage V_{BE}. Moreover, making $K_{D1}K_{M2}$ much larger than $K_{D2}K_{M1}$ requires a large area and this cannot be made use of. We use a number of differential pairs and cascade them to obtain sufficient PTAT voltage. When the differential pairs are connected in a cascade, total gate-to-gate voltage V_{GG} can be expressed as

$$\sum_{i=1}^{N} V_{GG,i} = \sum_{i=1}^{N} \eta V_T \ln \left(\frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}} \right)$$
$$= \eta V_T \ln \left(\prod_{i=1}^{N} \frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}} \right) \tag{6}$$

where N is the number of differential pairs. Because the ratios of $K_{D2i-1}K_{M2i}/K_{D2i}K_{M2i-1}$ are multiplied, large PTAT voltage can be efficiently obtained from (6).

Output reference voltage V_{REF1} in the bandgap voltage reference circuit can be expressed from (5) and (6) as

$$V_{REF1} = V_{BE} + \sum_{i=1}^{N} V_{GG,i}$$
$$= V_{BGR} + \left(-\gamma + \eta \frac{k_B}{q} \ln \left(\prod_{i=1}^{N} \frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}} \right) \right) T. \tag{7}$$

Therefore, the condition $V_{REF1} = V_{BGR}$ can be obtained by appropriate choice of the aspect ratios of the transistors in the differential pairs and current mirrors, and of N.

C. Sub-BGR

Because the bandgap voltage of silicon is larger than 1.2 V, BGR circuits require more than 1.2 V of supply voltage. Here, we present a voltage reference circuit that operates at sub-1-V power supply.

Fig. 4 shows a block diagram of the proposed sub-BGR circuit. The circuit uses a voltage divider circuit. The voltage divider circuit divides the base-emitter voltage V_{BE}. The output voltage $V_{BE/M}$ of the voltage divider can be expressed as

$$V_{BE/M} = \frac{V_{BE}}{M} = \frac{V_{BGR}}{M} - \frac{\gamma}{M} T \tag{8}$$

where M is the division ratio of the divider. Then, the PTAT voltage generator is also used to cancel the negative dependence on temperature of $V_{BE/M}$. The reference output voltage V_{REF2} of this circuit is expressed as

$$V_{REF2} = \frac{V_{BGR}}{M} + \left(-\frac{\gamma}{M} + \eta \frac{k_B}{q} \right.$$
$$\left. \times \ln \left(\prod_{i=1}^{N'} \frac{K_{D2i-1}K_{M2i}}{K_{D2i}K_{M2i-1}} \right) \right) T \tag{9}$$

where N' is the number of differential pairs. Note that because base-emitter voltage V_{BE} is divided by M, the negative temperature coefficient γ is also divided by M. Therefore, the required PTAT voltage decreases and the number of differential pairs can be reduced. As a result, both the area and the current dissipation in the sub-BGR circuit are less than those in the BGR circuit.

A zero temperature coefficient voltage is obtained in a similar way to that of the BGR circuit by designing the aspect ratios so
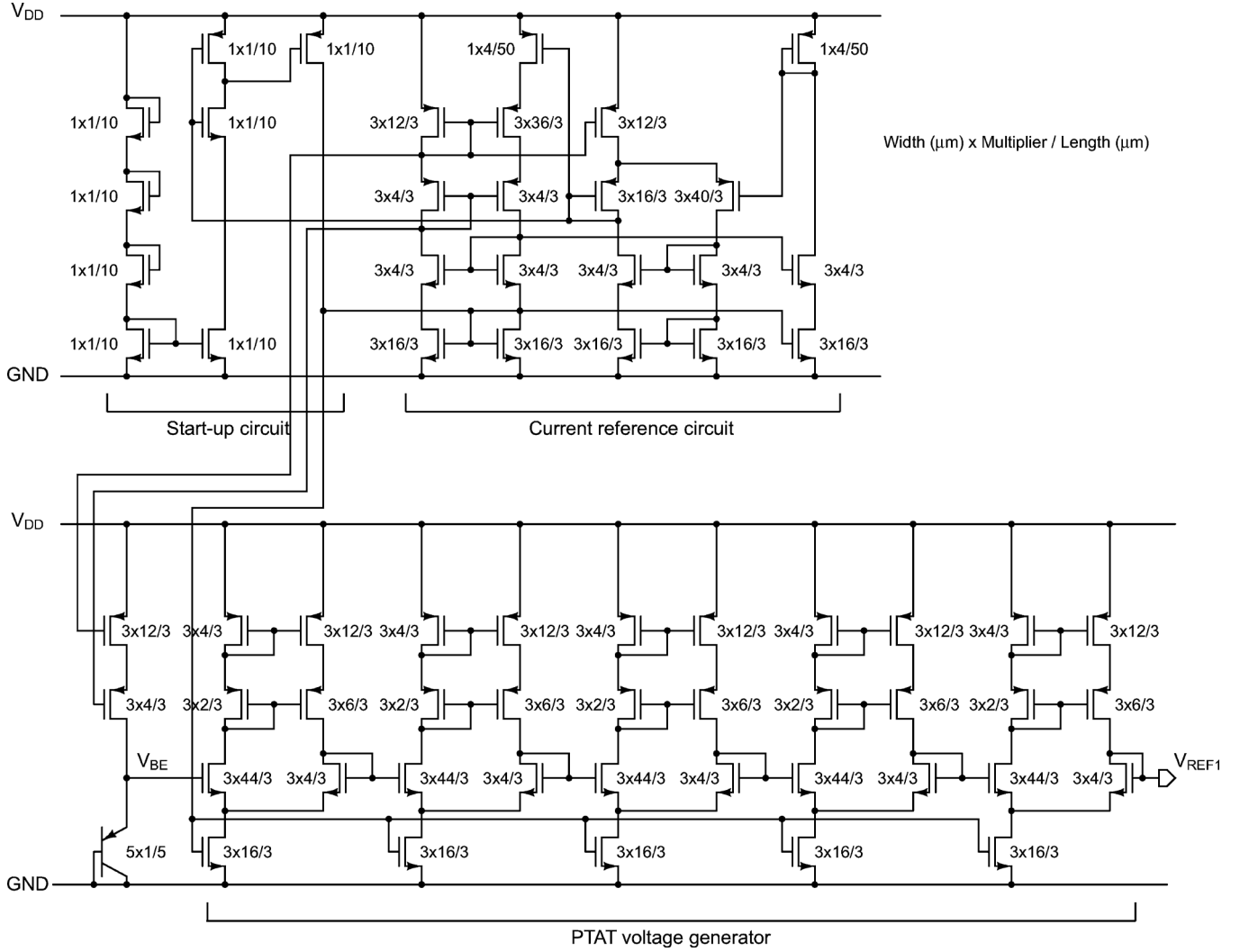
Fig. 5. Schematic of proposed BGR circuit.

that the second term in (9) becomes zero, and the voltage can be rewritten as

$$V_{\text{REF2}} = \frac{V_{\text{BGR}}}{M}. \tag{10}$$

Note that, if V_{BGR} is divided by M after it is generated, the supply voltage of the circuit requires more than 1.2 V. This is because the circuit has to generate V_{BGR} in advance. However, because the proposed sub-BGR circuit divides the base-emitter voltage and output reference voltage $V_{\text{REF}/M}$ is lower than 1.2 V, the sub-BGR circuit can operate at sub-1-V power supply.

III. EXPERIMENTAL RESULTS

A. Circuit Implementation

We fabricated a proof-of-concept chip using a 0.18-μm, 1-poly, 6-metal CMOS process with deep N-well option. Figs. 5 and 6 show the schematics for the proposed BGR and sub-BGR circuits. A cascode configuration was used in the circuits to reduce dependence on supply voltage. All transistor sizes are provided in Figs. 5 and 6. We determined the transistor sizes based on the results of Monte Carlo simulations assuming both die-to-die (D2D) and within-die (WID) variations in transistor parameters [16]–[18].

Five differential pairs were used in the BGR in this design. The reference output voltage V_{REF1} of this circuit can be expressed as

$$V_{\text{REF1}} = V_{\text{BGR}} + \left(-\gamma + \eta \frac{k_B}{q} \ln \left(\prod_{i=1}^{5} \frac{K_{D2i-1} K_{M2i}}{K_{D2i} K_{M2i-1}} \right) \right) T. \tag{11}$$

A zero temperature coefficient voltage can be obtained by designing the aspect ratios in the differential pairs and the current mirrors so that the second term in (11) becomes zero.

We used a source-follower circuit as a voltage divider circuit in the sub-BGR. The voltage divider circuit divided the base-emitter voltage V_{BE} in half. Each body terminal of the nMOS-FETs in the source-follower circuit was connected with their source terminal to avoid the body effect of the transistor. We ignored the gate and substrate leakage currents because these leakage currents were smaller than the subthreshold current in
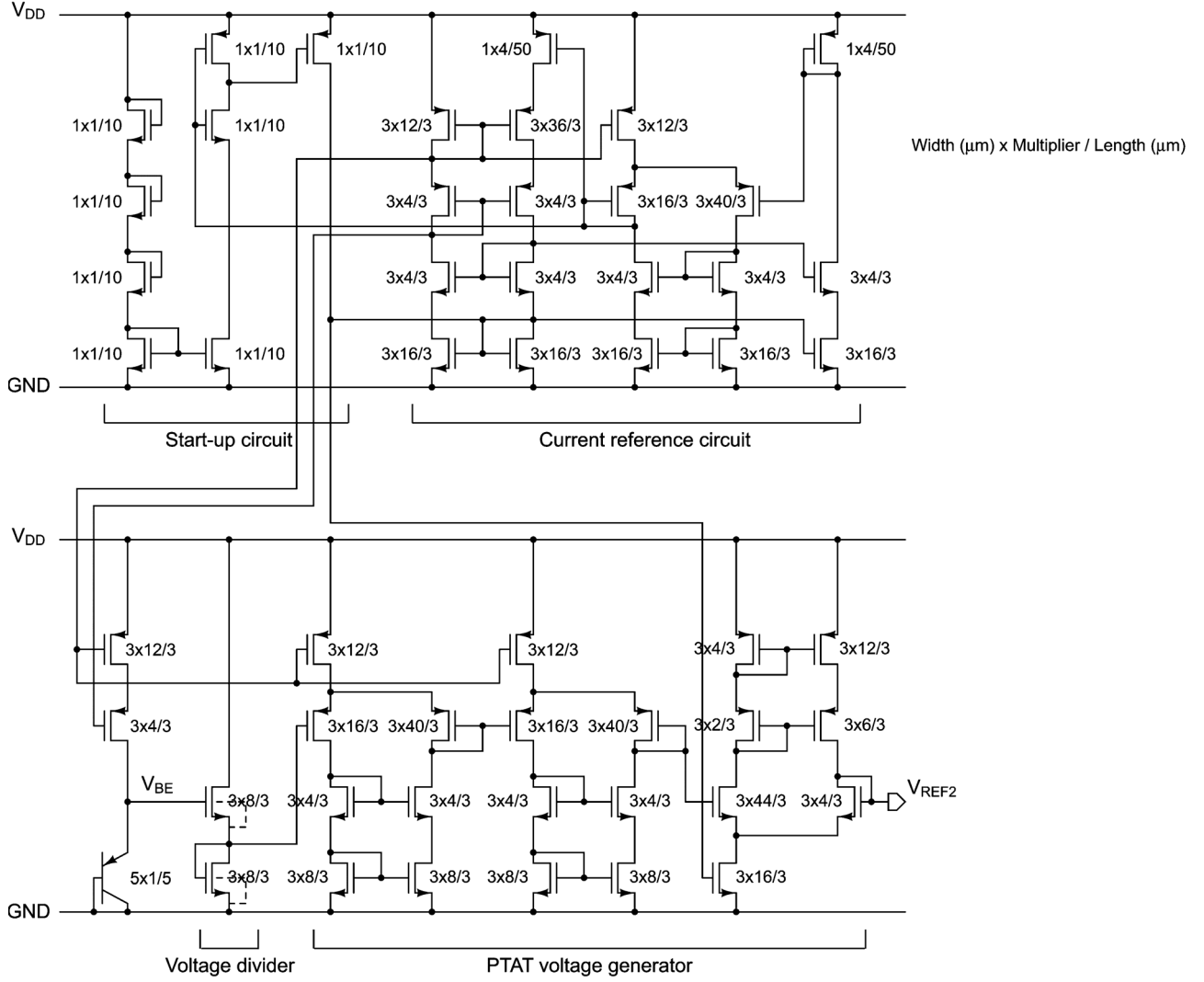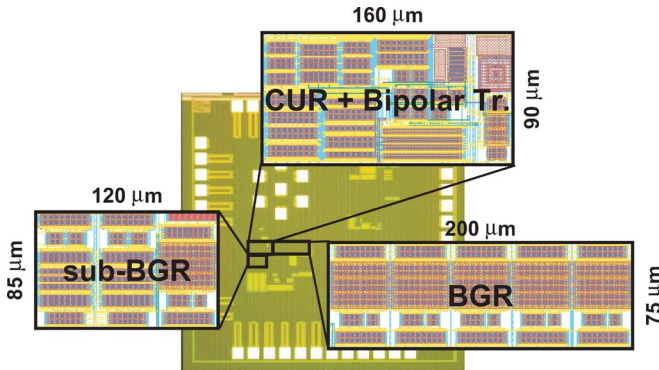
Fig. 6.   Schematic of proposed sub-BGR circuit.

Fig. 7.   Chip micrograph and layout.

the process we used. The output voltage $V_{\mathrm{BE}/2}$ of the source-follower circuit can be expressed as

$$V_{\mathrm{BE}/2} = \frac{V_{\mathrm{BE}}}{2} = \frac{V_{\mathrm{BGR}}}{2} - \frac{\gamma}{2}T. \qquad (12)$$

Then, three differential pairs were used in the sub-BGR to cancel the negative dependence on temperature of $V_{\mathrm{BE}/2}$. Note

that we used two pMOS differential pairs as first PTAT voltage generators because $V_{\mathrm{BE}/2}$ would have been too low to apply an nMOS PTAT generator. The reference output voltage V_{REF2} of this circuit can be expressed as

$$V_{\mathrm{REF2}} = \frac{V_{\mathrm{BGR}}}{2} + \left(-\frac{\gamma}{2} + \eta_P \frac{k_B}{q} \ln\left(\prod_{i=1}^{2} \frac{K_{D2i-1} K_{M2i}}{K_{D2i} K_{M2i-1}} \right) \right.$$
$$\left. + \eta_N \frac{k_B}{q} \ln\left(\frac{K_{D5} K_{M6}}{K_{D6} K_{M5}} \right) \right) T. \qquad (13)$$

Therefore, a zero temperature coefficient voltage can be obtained by designing the aspect ratios in the differential pairs and the current mirrors so that the second term in (13) becomes zero, and the voltage can be rewritten as

$$V_{\mathrm{REF2}} = \frac{V_{\mathrm{BGR}}}{2}. \qquad (14)$$

Fig. 7 shows a micrograph of the chip and the layout for each circuit. The areas that the current reference (CUR including the
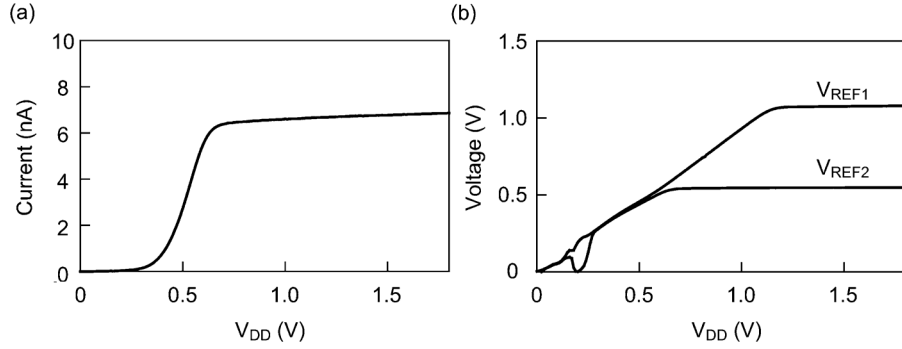
Fig. 8. (a) Measured operating current and (b) measured voltages of V_{REF1} and V_{REF2} as a function of V_{DD}.
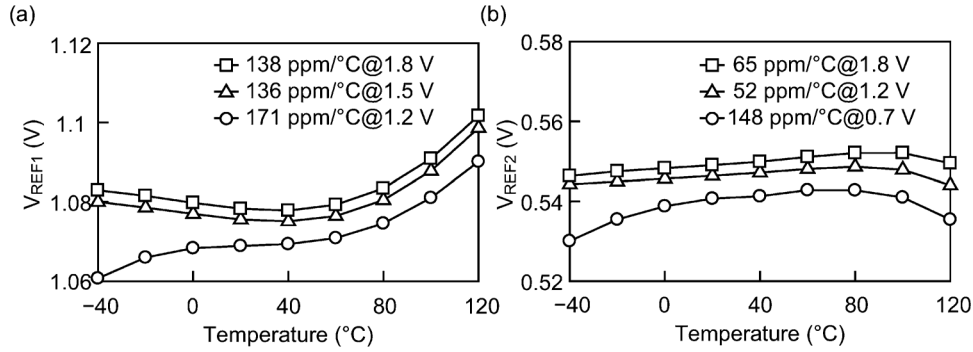

Fig. 9. (a) Measured voltage of V_{REF1} and (b) measured voltage of V_{REF2} as a function of temperature at three supply voltages.

bipolar transistor), the BGR, and the sub-BGR circuits occupy correspond to 0.0144 mm^2, 0.0150 mm^2, and 0.0102 mm^2. We measured nine sample chips.

B. Results

Fig. 8(a) plots the measured operating current I in the current reference circuit as a function of V_{DD}. The circuit operated at more than 0.7-V power supply and the current was about 6 nA. The line regulation of the current was 6.47%/V. Fig. 8(b) plots the measured voltages of V_{REF1} and V_{REF2} as a function of V_{DD}. The BGR circuit generated V_{REF1} as 1.08 V at more than 1.2-V power supply. The sub-BGR circuit could operate at sub-1-V power supply (i.e., 0.7 V) and V_{REF2} was 0.549 V.

Fig. 9(a) and (b) plots the measured voltages of V_{REF1} and V_{REF2} as a function of temperature from $-40\,^\circ$C to $120\,^\circ$C at three different supply voltages. The temperature coefficients (TCs) have similar characteristics across different supply voltages.

Fig. 10 plots measured operating current I as a function of temperature from $-40\,^\circ$C to $120\,^\circ$C in nine samples. The current reference circuit generated a nano-ampere current over a wide range of temperatures. The current increased with different dependencies on temperature at higher temperatures. We assumed that the reason for this was leakage current. However, it did not have much influence on the operation of our circuit because the increase in current was small. Fig. 11(a) and (b) plots the measured voltages of V_{REF1} and V_{REF2} as a function of temperature from $-40\,^\circ$C to $120\,^\circ$C. The average power dissipations of the BGR and sub-BGR circuits in nine samples at
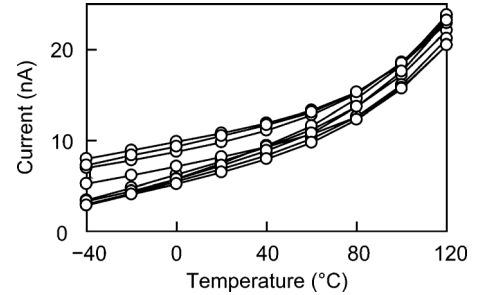

Fig. 10. Measured operating current as a function of temperature in nine samples.

room temperature were 100 and 52.5 nW, respectively. The average TCs of the BGR and the sub-BGR circuits corresponded to 147 and 114 ppm/$^\circ$C, respectively. The output voltages exhibited a nonlinear dependence on temperature as was explained in the previous section. We can reduce the dependence on temperature by using a technique of curvature compensation.

Fig. 12(a) and (b) shows the distributions of V_{REF1} and V_{REF2} in nine samples at $20\,^\circ$C with 1.5-V power supply. The output voltages were not trimmed. The coefficients of variation ($=\sigma/\mu$, where μ and σ are the mean value and the standard deviation) for V_{REF1} and V_{REF2} were 0.737% and 1.05%, respectively. The coefficients of variation were very small because the nine samples were removed from the same wafer.

Fig. 13 plots the measured PSRRs of V_{REF1} and V_{REF2}. The PSRR of V_{REF1} at 100 Hz and 1 MHz corresponded to -62 and -14 dB, respectively. The PSRR of V_{REF2} at 100 Hz and 1 MHz corresponded to -56 and -8.7 dB, respectively. The PSRR of V_{REF1} was better than that of V_{REF2} because the voltage divider
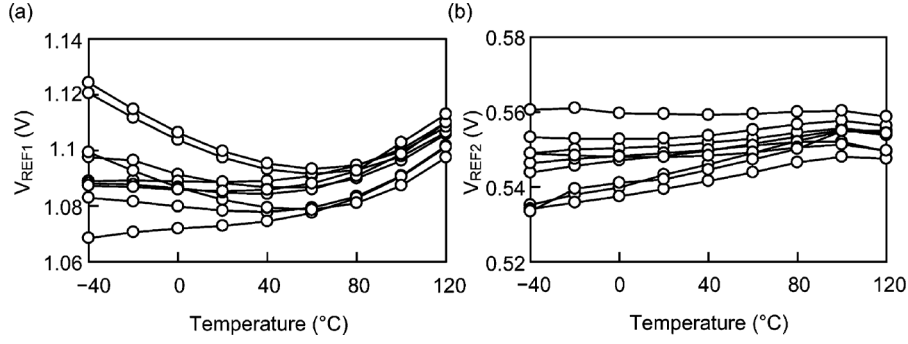
Fig. 11. (a) Measured voltage of V_{REF1} and (b) measured voltage of V_{REF2} as a function of temperature in nine samples.
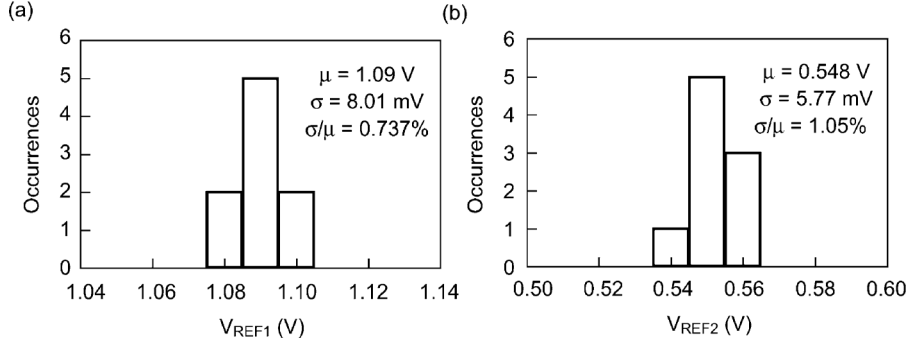

Fig. 12. Distributions of (a) V_{REF1} and (b) V_{REF2} for nine samples.
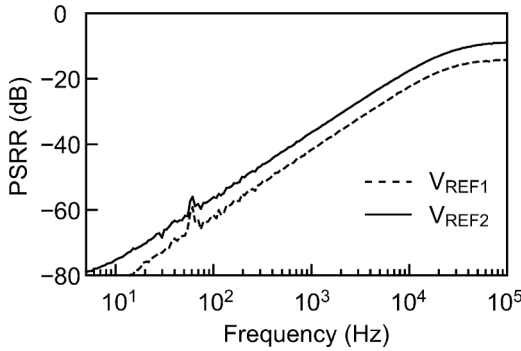

Fig. 13. Measured PSRRs of V_{REF1} and V_{REF2}.

in the sub-BGR circuit was affected by the change in the supply voltage and it degraded the PSRR of V_{REF2}.

Because our BGR and sub-BGR dissipated quite a low amount of power, they will suffer from poor noise performance, poor driving capabilities, and a slow start-up time. Note that, the simulated noise densities of V_{REF1} and V_{REF2} with 4.43-pF on-chip capacitors at 100 Hz were 1.72 and 1.90 $\mu V/\sqrt{Hz}$, respectively, and the simulated start-up time was 6 ms in our circuit. An on-chip decoupling capacitor will reduce noise. However, it may degrade start-up time. Therefore, the decoupling capacitor should be designed to satisfy the required noise accuracy and start-up time depending on applications. The circuits for driving capabilities should not be directly connected to resistive loads because of their poor driving current. Bias current in the last stage of the PTAT generators should be increased if we have to drive resistive

loads and/or large capacitive loads. However, the increase in bias current leads to high power dissipation. We have to design bias current in accordance with applications.

Table I summarizes the performance of the proposed BGR and sub-BGR circuits and compares them with other reported reference voltage circuits [3]–[13]. The proposed circuits operate with ultralow power dissipation. The minimum supply voltage of the sub-BGR is especially low at 0.7 V.

C. Discussion

The coefficients of variation in the experimental results were very small because the nine samples were obtained from the same wafer. In order to evaluate robustness to process variations, we performed Monte Carlo SPICE simulations. The results for 500 runs are depicted in Fig. 14. The coefficients of variation for V_{REF1} and V_{REF2} were 0.351% and 1.61%, respectively. It was reported to be 7% in [11]. Thus, our proposed circuit is superior in process variations. The improvement comes from the fact that our proposed circuit is based on not the threshold voltage of MOSFETs, but the bandgap voltage of the silicon.

Output voltage V_{REF1}, 1.09 V, in the experimental results was lower than the material bandgap voltage, around 1.2 V. This was because the operating current increases with temperature. Fig. 15 plots the simulated base-emitter voltages V_{BE}s as a function of temperature from −40 °C to 120 °C. The V_{BE}s were biased with constant bias currents of 10 nA and 1 μA. The measured V_{BE} biased with the current I and their linear fitting curves were also shown in the figure. When the bipolar transistor accepts the constant currents, V_{BE}s at absolute zero temperature were almost equal to the material bandgap voltage ($\sim$1.2 V). On

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work		[13]		[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]
CMOS Technology	0.18-μm		0.35-μm		0.6-μm	0.35-μm	0.16-μm	0.35-μm	0.16-μm	0.35-μm	0.6-μm	0.35-μm	0.35-μm	0.13-μm
Type	BG	Sub-BG	BG	Sub-BG	Sub-BG	BG	BG	Sub-BG	Sub-BG	V_{TH}	V_{TH}	V_{TH}	V_{TH}	V_{TH}
Supply voltage (V)	1.2 - 1.8	0.7 - 1.8	1.3 - 3.3	1.1 - 3.3	0.98 - 1.5	>1.4	1.8±10%	1.7 - 3.5	1.1 - 1.8	>0.85	1.4 - 3.0	0.9 - 4.0	1.4 - 3.0	0.5 - 3.0
Active area (mm²)	0.0294	0.0246	0.21	0.22	0.24	1.2	0.12	0.102	0.0025	0.063	0.055	0.045	0.055	0.00135
Reference voltage (V)	1.09	0.548	1.18	0.553	0.603	1.2	1.09	0.618	0.944	0.65	0.39	0.670	0.745	0.176
Temperature range (℃)	-40 - 120		-20 - 80		0 - 100	-20 - 100	-40 - 125	-50 - 150	-45 - 135	-20 - 100	0 - 100	0 - 80	-20 - 80	-20 - 80
TC (ppm/℃)	147	114	215	394	15	12.4	5 - 12	13.7	30	57.7	36.9	10	7	231
Coefficient of variation (%)	0.737	1.05	1.61	1.62	N/A	N/A	0.15 (Trimmed)	N/A	0.8	2.0	N/A	N/A	0.87	0.72
Power dissipation (μW)	0.100 @Room temp.	0.0525 @Room temp.	0.108 N/A	0.11 N/A	17.6 @100℃	162 N/A	99 N/A	65.2 @Room temp.	1.54 @Room temp.	1.02 @Room temp.	13.6 @100℃	0.036 @Room temp.	0.3 @Room temp.	0.0000022 @Room temp.
PSRR (dB)	-62@100 Hz	-56@100 Hz	N/A	N/A	-44@10 kHz -17@10 MHz	-68@100 Hz	-74@DC	N/A	N/A	N/A	-47@100 Hz -20 @10 MHz	-47@100 Hz -40@10 MHz	-45@100 Hz	-53@100 Hz -62 @10 MHz

* BG, sub-BG, and V_{TH} mean reference circuits based on bandgap voltage, sub-bandgap voltage, and threshold voltage.
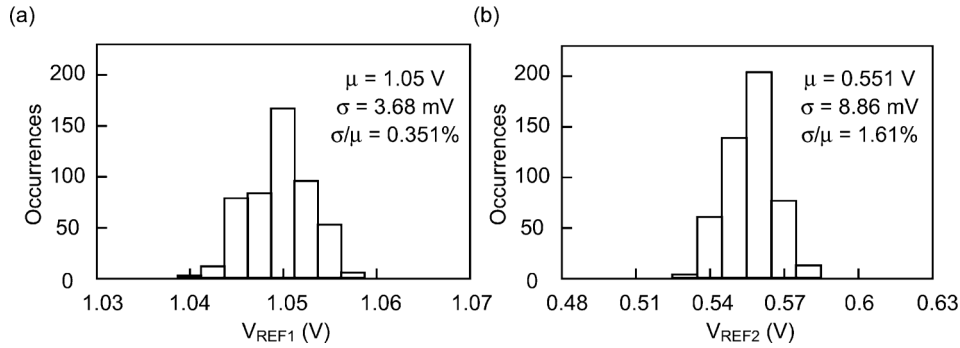
(a)　　　　　　　　　　(b)

Fig. 14. Distributions of output voltages, as obtained from Monte Carlo simulation of 500 runs.
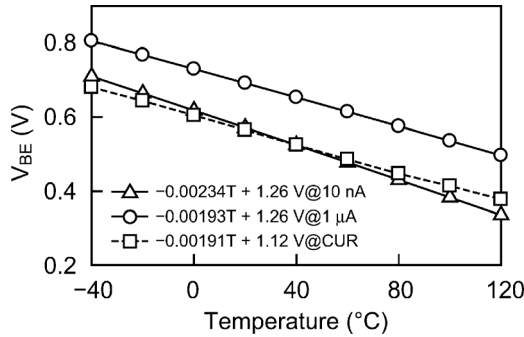

Fig. 15. V_{BE} as a function of temperature at different bias currents.

the other hand, when the bipolar transistor accepts the temperature-dependent current, V_{BE} at absolute zero temperature is not equal to the material bandgap voltage. As the operating current increased with temperature, V_{BE} increased gradually. As a result, V_{BE} at absolute zero temperature became lower than the material bandgap voltage.

IV. CONCLUSION

BGR and sub-BGR circuits for extremely low-power LSIs were presented. They consist of a nano-ampere current reference circuit, a bipolar transistor, and PTAT voltage generators. Because the circuits only consist of MOSFETs except for the bipolar transistor, they generate reference voltages without resistors. Because the sub-BGR circuit divides the output voltage of the bipolar transistor, it can operate at sub-1-V power supply. The experimental results demonstrated that the BGR circuit

could generate a reference voltage of 1.09 V and the sub-BGR circuit could generate one of 0.548 V. The power dissipation of the BGR circuit was 100 nW and that of the sub-BGR circuit was 52.5 nW.

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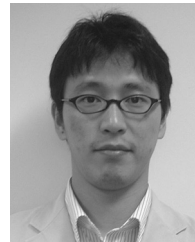
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