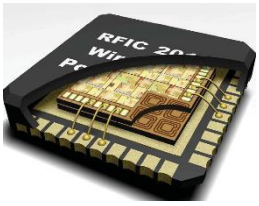
Universidad Industrial de Santander



MICROELECTRONICS – FIRST EXAM

Profesor: Javier Ardila
Deadline: **Tuesday, March 11, 2025 – 10:00PM**
Submission format: PDF document uploaded to Moodle
File name format: ***microE1_PrimerNombre_PrimerApellido.pdf***

Use the TSMC 180nm Design Kit and Simulation Tool to solve the following points as required.

1) CONCEPTS

1.1 Explain in your own words what each of the following concepts consists of:

Saturation Velocity

Drain Induced Barrier Lowering (DIBL)

Gate Leakage Current

Diffusion Leakage Current

Substrate Current Induced Body Effect (SCBE).

Halo Implantations

1.2 A figure of merit of interest in analog design is the intrinsic gain product ($g_m r_O$) and unit gain frequency (f_T),

$$GFT = g_m r_O . f_T$$

For long channel lengths, the above equation can be written, assuming operation in saturation and modeling $C_{gs} = \frac{2}{3} C_{ox} WL$, as:

$$GFT = g_m r_O . f_T = \frac{{g_m}^2}{2\pi C_{gs}} . \frac{1}{\lambda I_D} = \frac{3\mu_n}{2\pi L^2 \lambda} \propto \frac{\mu_n}{L}$$

1.3 This expression is independent of the drain current and basically depends on the channel length and the mobility of the MOSFET. However, when experimenting with a recent short-channel technology, it is observed that this expression is not entirely independent for different polarization conditions. Briefly explain what may be going on.

2) CONSOLIDATION OF CHARACTERIZATION DEVELOPED

DC simulations. For the following simulations use 3 NMOS reference transistors and 3 PMOS reference transistors with W/L=5 in all cases, but L=0.18um, L=0.4um, L=1um to differentiate each of the 3 cases within each transistor type. Using the configuration you already have for characterization developed in the course, please:

2.1) Graph the current curve I_D as a function of V_{GS} for the saturated transistor. Use the core devices (nmos2v_mac or similar).

2.2) Graph the MOS transconductance g_m vs V_{GS} using the conditions mentioned above.

2.3) Get the curve g_m/I_D vs V_{GS} using the conditions mentioned above.

2.4) Get the curve $a_0 = g_m r_o$.

2.5) Get the curves f_T vs V_{GS} y de $f_T * (g_m/I_D)$ vs V_{GS}. Taking into account these data, what is the value of V_{GS} that reaches the maximum value of $f_T * (g_m/I_D)$ for each reference transistor? Summarize these results in a table for each case.

2.6) For each reference transistor obtained in numeral 2.5 and **using the one that maximizes to $f_T * (g_m/I_D)$ vs Vgs,** extract all the parameters of each reference transistor using the OP simulation. Summarize your results in a table like the one below:

OP parameters table where the FTGMID parameter is maximized.

	NMOS W/L=5			**PMOS W/L=5**		
Parameter	L=0.18um	L=0.4um	L=1um	L=0.18um	L=0.4um	L=1um
Id						
Vgs						
Vds						
Vsb						
Vth						
Vov						
Vdsat						
Vds-Vdsat						
gm						
gmb						
ro						
gmro						
gm/Id						
Cgs						
Cgd						
ft						
FTGMID						
GFT						

3) DEVICE DESIGN

For each of the three reference transistors of each type (NMOS or PMOS) defined above, make the following designs briefly explaining the strategy used for it.

3.1) Design an NMOS transistor with **Id=100uA and ft ≥ 10 GHz** using each reference transistor with fixed L. That is, you must develop the design with each of the 3 NMOS transistor options that you have from numeral 4 (without changing the L) to reach the given specifications. In all cases compare the voltage Vds,min that it could reach and the area in each reference transistor. Comment on which transistor solves this design the most easily, why?

3.2) An NMOS transistor whose **Id=10uA and intrinsic gain (gmro) of at least 100**. That is, you must develop the design with each of the 3 NMOS transistor options that you have from numeral 4 (without changing the L) to reach the given specifications. In all cases, compare the output impedance (ro) that it could achieve and the area in each reference transistor. Comment on which transistor solves this design the most easily, why?

3.3) A PMOS transistor with **gm=0.3mS** and a **Vds,min=0.3V**. That is, you must develop the design with each of the 3 options of PMOS transistors that you have from numeral 4 (without changing the L) to reach the given specifications. In all cases compare the current Id achieved

in each reference transistor, as well as the area, what other parameters differ between the 3 designs?

4. Write Conclusions on your report.