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A 470nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter With Seamless Mode Selection for IoT Application

Wen-Liang Zeng, *Student Member, IEEE*, Yuan Ren, *Student Member, IEEE*, Chi-Seng Lam, *Senior Member, IEEE*, Sai-Weng Sin, *Senior Member, IEEE*, Weng-Keong Che, Ran Ding, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*—An ultra-low quiescent current dual-mode buck converter system is designed for IoT application, which includes a double clock time (DCT) and a pulse-width-modulation (PWM) control modes. The proposed DCT mode can reduce the conversion loss over a wide loading range from nA-to-mA and achieve seamless mode transition from DCT to PWM control. Implemented in a 0.18µm CMOS, this converter achieves a peak efficiency of 92.7%/94.7% in DCT/PWM and >80% efficiency from 10 µA to 50 mA (5000x), with a wide input voltage from 2 V to 5 V. A quiescent current of 470 nA including bandgap voltage reference and internal oscillator is achieved. The DCT-to-PWM mode selection mechanism achieves an undershoot of 80 mV at 11 µs recovery time when load current jumps from 6.67 µA to 50 mA.**

***Index Terms*—Internet of things (IoT), buck converter, ultra-low-quiescent current, double clock time (DCT) control, mode selection, pulse-width-modulation (PWM) current mode control, discontinuous conduction mode (DCM).**

I. Introduction

Low power smart devices are receiving significant growing attention in internet of things (IoT) nowadays. It is estimated that over 20 billion IoT devices would be connected through the internet in the coming future [1-2]. As an electronic device monitors and collects data from the physical environment continuously, a vast majority of them run on batteries and are expected to run for a couple of years without any replacement. A typical IoT device usually includes a power management unit, a communication unit, a microprocessor unit and a sensor unit, as shown in Fig. 1. The li-ion battery is a reliable power supply option for IoT systems whose voltage varies from 2.5 V to 4.2 V [3]. An ultra-low-power (hundreds of nA quiescent current) DC-DC converter in the power management unit plays an important role in prolonging the battery usage time. According to the load current profile of the power management unit, IoT devices can be classified into three operation modes: sleep mode (nA to µA), standby mode (µA to mA) and transmit mode (mA to hundreds mA/A). Therefore, due to the wide spread of load current range in these three operation modes, the inductor-based DC-DC converter is more popular in such IoT device applications compared with the switch-capacitor-based DC-DC converters [4-6]. In reality, the IoT devices spent most of their time in the sleep mode, in which the current consumption ranges from hundreds of nA to tens of µA. When the environmental data is collected by the sensor unit, the microprocessor unit reads and processes the data, which consumes of hundreds of µA to several mA current, that is known as the standby mode. After that, the data will be transferred to the Internet through different communication channels (Bluetooth, WIFI, NFC, and so on), which consumes of tens of mA during a short period, that is known as the transmit mode [7].

As a result, the DC-DC converter in IoT application should be able to consume an ultra-low quiescent current in sleep mode, handle a wide load current range (nA-mA) and provide a fast load transient response from nA/µA to mA (>1000x) during the transition from one mode to the other. Furthermore, the DC-DC converter should also operate properly under a wide input voltage range, due to the drop of li-ion battery voltage during the usage.

To support the aforementioned requirements for the DC-DC converter, some works apply dynamic control method with dynamic current consumption of hundreds-nA to reduce the overall control or quiescent current consumption in the sleep mode [8-10]. While in the standby mode, pulse frequency modulation (PFM) control is one of the most popular control methods, which consumes mainly dynamic current around a hundred-µA [8-12]. In the transmit mode, pulse width

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modulation (PWM) control is usually applied, which consumes less than hundreds of μA static current [9, 10, 13-15]. The works in [9] and [10] apply the triple-mode control (Asynchronous Mode (AM) [9] and Retention Mode (RM) [10] for sleep mode, PFM for standby mode and PWM for transmit mode) to keep the balance of obtaining wide operational range and ultra-low-quiescent current, but their main drawback is failed to achieve a low power and automatic mode selection function. The design in [9] achieves the mode selection function manually, while the design in [10] can switch control mode automatically, but it requires an additional analog current sensor, which consumes extra static current. In addition, the design in [8] utilizes one control mode (Single Bounded Hysteresis Control, SBHC), which does not require any mode selection circuit, however, this design is suitable to work for sleep and standby modes only, without covering the transmit mode operation in this paper.

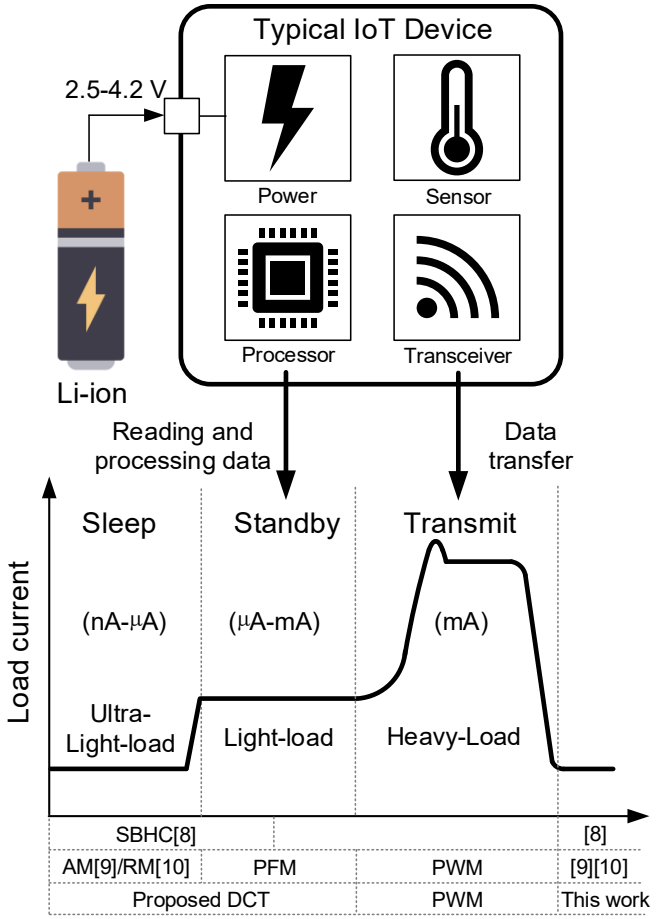


Fig. 1. Load current profile in a typical IoT device with li-ion battery supply.

TABLE I. COMPARISON WITH MODE SELECTION CHARACTERISTIC.

	Number of control mode	Automatic mode selection	Static current consumption
This work	2	Yes	17.9 nA
[10]	3	Yes	>1 μA*
[9]	3	No (Manually)	0 μA (Manually)
[8]	1	NA	NA

*: estimate from figure

As a result, a "Double Clock Time" (DCT) control technique with digital current sensor for inductive-based DC-DC converter is proposed in this paper, which consumes only hundreds of nA during sleep mode and can switch to PWM mode automatically without any static current consumption. As the switching frequency of the DCT control is changing according to the load current, it can maintain high efficiency over a wide load current range (10 μA to 10 mA) as well. The DCT control can apply for both sleep and standby modes in the IoT application as shown in Fig. 1. Combining with the PWM control, the proposed dual-mode control reduces the control circuit complexity compared with the triple-mode control design [9, 10]. Table I. compares the mode selection characteristic of this work with [8-10]. From Table I, the proposed DCT control technique, together with the proposed digital current sensor obtains very small static current consumption with automatic mode selection function. Finally, a buck converter with the proposed DCT and conventional current mode PWM control is proposed for the IoT devices application. The proposed DCT/PWM control buck converter obtains the following characteristics:

1) Ultra-low-quiescent current.
2) Wide input voltage (2-5 V) range and wide load current range (10 μA to 50 mA, 5000x) with high conversion efficiency in both light and heavy loads.
3) Seamless and stable mode transition for large load current step change automatically.

In the following, the overall system description and design consideration are provided in Section II. The low power DCT control theory and its operation principle are discussed in Section III. Section IV presents the mode selection circuit design, while Section V presents the low power bandgap reference design. Then the experimental results are provided in Section VI to verify the design. Finally, Section VII draws a conclusion of this paper.

II. PROPOSED DCT/PWM BUCK CONVERTER

In this work, a dual-mode buck converter system is designed instead of applying the triple-mode control. The proposed DCT control covers the load current range from nA to mA, while the PWM control covers it from mA to 50 mA. Fig. 2 shows the system block diagram of the proposed DCT/PWM buck converter, which includes a buck converter with power inductor L and output capacitor C_{OUT}, a DCT and a PWM control blocks, a bandgap reference buffered with low dropout regulators (LDOs) that provide clean references and supplies for the DCT and PWM control, zero current detection (ZCD) control, mode selection circuit, non-overlap circuit, level-shifter and gate drivers, and feedback resistor networks. Due to the consideration of the maximum load current (50 mA) and power inductor of 2.2 μH in this work, the dual-mode buck converter system mainly operates in discontinuous conduction mode (DCM) for sleep, standby and transmit modes. Therefore, a type II compensator is applied for the current mode PWM control [16-18] in this work. When DCT control operates during the sleep and standby mode, the PWM control is completely off to reduce the power consumption. A low power ZCD control

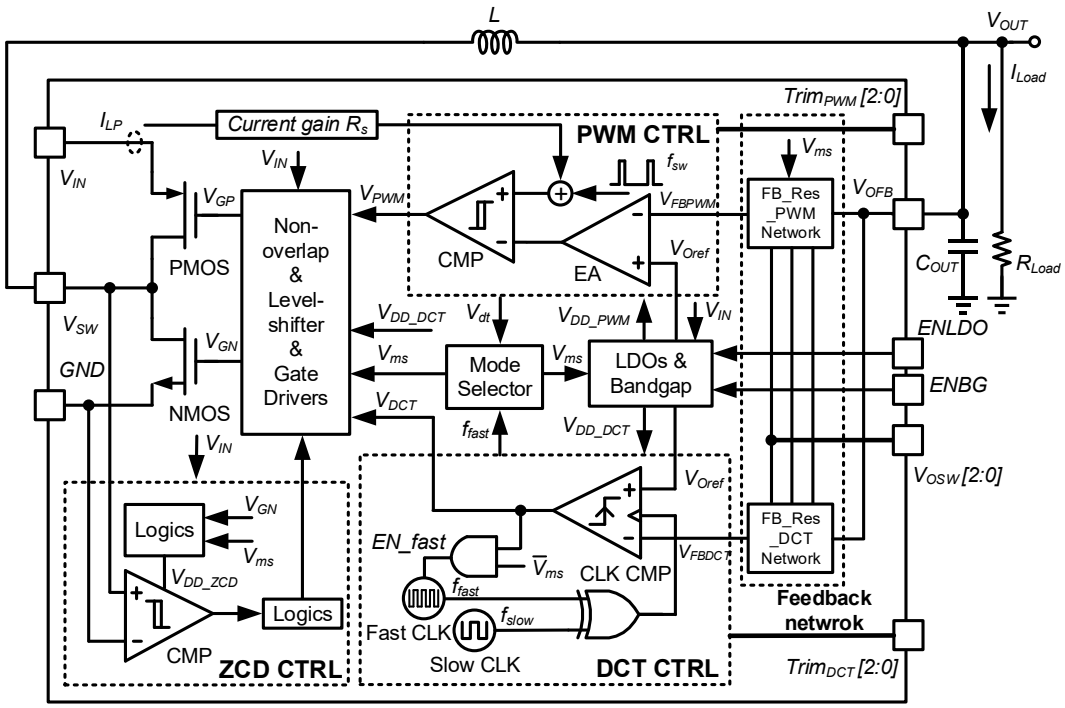


Fig. 2. System block diagram of the proposed DCT/PWM buck converter.

concept "Adaptive ZCD power supply" (AZCD) [10] is applied for this work, in which the ZCD circuit operates during the inductor demagnetize phase only in DCT control as shown in Fig. 5. With the AZCD technique, the ZCD control power consumption can be significantly lowered and is proportional to the load current, which always occupies a very short period under sleep mode situation. Furthermore, under low power consideration, there is an ultra-low-power feedback resistor network (FB_res_DCT network) designed for DCT control. The FB_res_DCT network is as large as tens of MΩ, while the feedback resistor network for PWM control (FB_res_PWM network) is as large as hundreds of kΩ. The signal $Trim_{DCT}[2:0]$ are 3-bit trimming signal for DCT slow clock frequency and the signal $Trim_{PWM}[2:0]$ are 3-bit trimming signal for PWM clock frequency. The signal $V_{OSW}[2:0]$ is used to set the different output voltages for 0.8, 1, 1.2 1.8 and 3 V in this work. ENBG is enable signal for the bandgap reference and ENLDO is enable signal for the low power LDO that works in both DCT and PWM control modes (LDO_DCT) and the buck converter. As a complete system, the designed buck converter requires only one input voltage source V_{IN} in the PCB testing environment. In this design, the input supply voltage V_{IN} is under 2 V to 5 V consideration.

A. Supply Voltage Design for DCT and PWM Control

To reduce the complexity of the control circuits under a wide range of V_{IN}, a dedicated constant voltage supply should be designed for the controller blocks. To support this, a low power bandgap and LDOs are designed based on this constant voltage as shown in

Fig. 3. As the voltage V_{DD_X} (where the subscript "x" represents PWM or DCT) should be able to turn on the 5V thick oxide NMOS completely (maximum threshold voltage V_{thmax} = 1.1 V in this process) for the logic design in the level shifter. Therefore, the voltage supplies V_{DD_X} for the DCT and PWM control are designed to be 1.2 V.

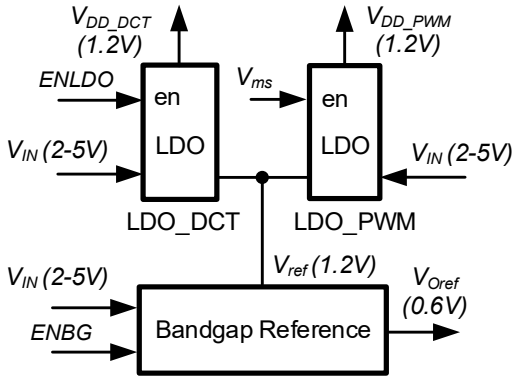


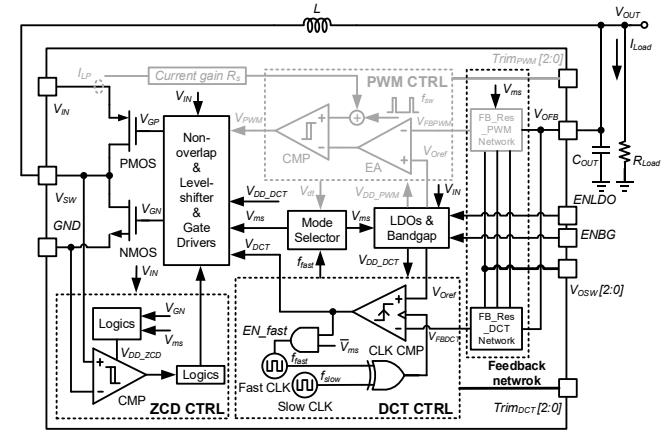
Fig. 3. Bandgap reference and LDOs schematics under a wide V_{IN} range consideration.

The bandgap reference generates a voltage reference V_{ref} = 1.2 V for the two LDOs and a half voltage divider produces an output voltage reference V_{Oref} = 0.6 V. The main purpose of applying LDOs is to fix the supply voltage of the control circuits over the wide input supply range (2-5 V), so that the corresponding controller circuit such as error amplifier, comparators, delay generator and the fast/slow clock generators are much less sensitive to the supply voltage variation. Since the bandgap reference circuit (V_{ref} = 1.2 V) cannot provide any driving capability, LDOs are required to provide driving capability for the control circuits. Specifically, the fixed 1.2 V supply will reduce the variation of the oscillation frequency of the slow clock generator, which plays a crucial role in minimizing the quiescent current of the controller. As LDOs will output a control voltage of 1.2 V for the control circuits, thin-oxide transistors can be applied instead of the thick-oxide transistors, even though the input voltage range varies from 2 V to 5 V.

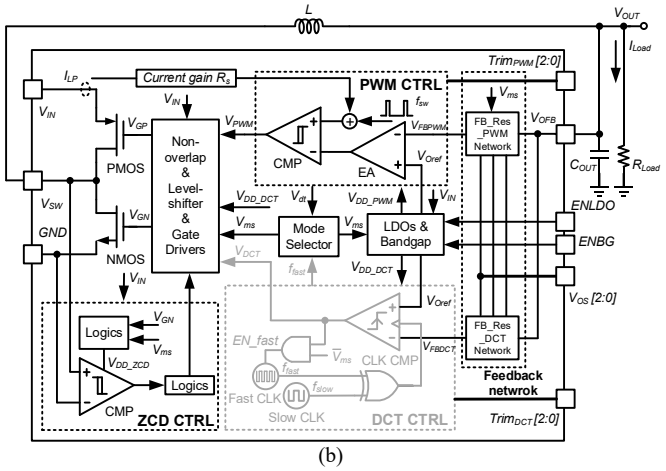
When ENBG = "1", the bandgap reference circuit starts operation. The LDO_DCT is a low-power LDO which works in both DCT and PWM control modes, and its output V_{DD_DCT} supplies the voltage/power for the DCT controller block and also part of the gate driver signals. The maximum current of LDO_DCT is 40 nA, so the power loss in this LDO is minimal even if a large dropout voltage is presented. The LDO_PWM is a normal-power LDO that works in PWM control mode only and its output V_{DD_PWM} supplies the voltage/power for the PWM controller block. The LDO_PWM is enabled by the mode selection signal V_{ms} when load current is large. When ENLDO = "1", the buck converter starts operation and regulate the output voltage to track its reference. Different output voltages can be set by controlling the feedback resistor network via the $V_{OSW}[2:0]$. We can measure the quiescent current of the buck converter by setting ENBG = "1" and ENLDO = "1" while we can measure its shutdown current by setting ENBG = "0".

B. System Operation Description

When the load current is small, the converter operates under DCT control and all the PWM control related blocks are powered off in order to achieve low quiescent current as shown in Fig. 4(a). From Figs. 3 and 4(a), the current sensing block, PWM control block, LDO_PWM and FB_Res_PWM_network turn off in DCT mode. On the other hand, when the load current is large, the converter operates under PWM control and only the DCT control block turns off as shown in Fig. 4(b).

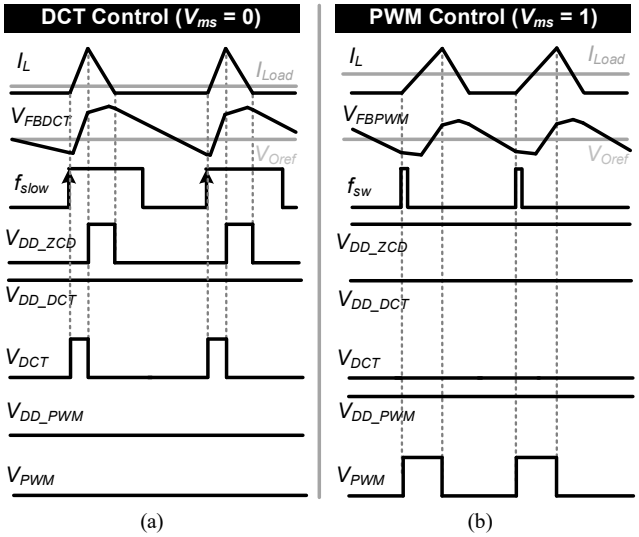


(a)



(b)

Fig. 4. Functional system block diagram of the buck converter under (a) DCT and (b) PWM control.



(a) (b)

Fig. 5. Proposed buck converter operation waveforms under (a) DCT and (b) PWM control.

Fig. 5 presents the operation waveforms under both DCT and PWM control. From Fig. 5(a), in DCT control, V_{ms} = "0", V_{DD_ZCD} = "1" in the inductor demagnetize phase, V_{DD_DCT} = "1", V_{DD_PWM} = "0", V_{DCT} triggers and V_{PWM} = "0".

From Fig. 5(b), in PWM control, V_{ms} = "1", V_{DD_ZCD} = "1", V_{DD_DCT} = "1", V_{DD_PWM} = "1", V_{DCT} = "0" and V_{PWM} triggers.

III. Low Power DCT Control

The DCT control is a dynamic clock-driven control for power saving purpose, thus the quiescent current is proportional to the control clock frequency. As shown in Fig. 6(a), there are two clocks (one fast ($f_{fast} = 1/t_{fast}$) and one slow clock frequency ($f_{slow} = 1/t_{slow}$)), one clock comparator (CLK CMP) and simple logic gates in the circuit. Notice that the slow clock frequency is the DCT control clock frequency.

A. DCT Operation Principle

In the conventional constant-on-time (COT) and adaptive-on-time (AOT) control, the control loop has been proved to be inherently stable in DCM [19], [20]. As the operation principle of the proposed DCT control is similar to the COT and AOT control, it is expected that its control loop is stable in DCM. As shown in Fig. 6(a), the slow clock is always active in DCT control. When the output feedback voltage of the DCT feedback resistor network $V_{FBDCT} < V_{Oref}$ at the rising edge of f_{slow}, V_{DCT} = "1" which represents the fast clock operation is enabled. Thus, the inductor L begins to magnetize and the output voltage V_{OUT} increases (here indirectly indicated by the output feedback voltage V_{FBDCT}). Then V_{DCT} holds "1" and the clock comparator will detect the next rising edge of the fast clock. At the second rising edge of the fast clock, once $V_{FBDCT} > V_{Oref}$, then V_{DCT} = "0" and inductor L begins to demagnetize and the fast clock is powered off. As a result, the minimum PMOS's on-time period $t_{on\_min} = t_{fast}$. After that, the V_{OUT} (V_{FBDCT}) decreases slowly until $V_{FBDCT} < V_{Oref}$, and the control cycle repeats.

The switching frequency in DCT control f_{DCT} does not equal to f_{slow}. However, their relationship can be written as:

$$f_{DCT} = \frac{f_{slow}}{m} \quad (1)$$

where $m \geq 1$ is an integer number. (1) indicates that the maximum switching frequency in DCT control is f_{slow}. When I_{Load} decreases, m increases, then f_{DCT} decreases in steps of f_{slow}. Fig. 6(b) and (c) show the conceptual operational waveforms under standby and sleep mode, respectively. In Fig. 6(b), the V_{FBDCT} is not smaller than V_{Oref} until 2 cycles of f_{slow}, hence the switching frequency of the DCT control $f_{DCT} = f_{slow}/2$. In Fig. 6(c), since I_{Load} is even smaller, V_{FBDCT} is not smaller than V_{Oref} until 5 cycles of f_{slow}, hence the switching frequency of the DCT control $f_{DCT} = f_{slow}/5$.

B. Fast Clock Period Determination

The fast clock period t_{fast} is the minimum PMOS on-time of the DCT control. When the load current is small, the magnitude of ripple V_{orp} as in Fig. 6(b) depends on the total charge sent to the output capacitor, which is equal to the total charge demagnetized from the inductor Q_L, as in Fig. 6(b). The charge Q_1 in the inductor magnetize phase is written as:

$$Q_1 = \frac{(V_{IN}-V_{OUT})t_{on}^2}{2L} \tag{2}$$

Then the total charge Q_L can be expressed as:

$$Q_L = \frac{Q_1}{M} = \frac{(V_{IN}-V_{OUT})t_{on}^2}{2ML} \tag{3}$$

where $M = V_{OUT}/V_{IN}$ is the voltage conversion gain. And the voltage ripple can be written as:

$$V_{orp} = \frac{Q_L - I_{Load}(t_{on}+t_{off})}{C_{OUT}} \tag{4}$$

Where t_{off} is the inductor demagnetize phase. Since I_{Load}, t_{on} and t_{off} are all small, so that their product I_{Load} (t_{on} + t_{off}) can be neglected here. Then, the voltage ripple can be deduced as:

$$V_{orp} = \frac{Q_L}{C_{OUT}} = \frac{V_{IN}(1-M)t_{on}^2}{2MLC_{OUT}} \tag{5}$$

With known V_{orp} and $t_{on} = t_{fast}$, solving t_{fast} from (5) yields,

$$t_{fast} = \sqrt{\frac{2V_{orp}MLC_{OUT}}{V_{IN}(1-M)}} \tag{6}$$

The maximum voltage ripple happens at the point of minimum M (that is V_{OUT} = 0.8 V and V_{IN} = 5 V). When the acceptable voltage ripple V_{orp} = 15 mV, L = 2.2 µH and C_{OUT} = 4.7 µF, t_{fast} is found to be 110 ns. In this paper, t_{fast} is designed to be 110 ns. Notice that the conventional oscillator circuit [21] is implemented for the fast clock in this work.

C. Slow Clock Frequency Determination

In DCT control, the clocked comparator monitors the output voltage at the rising edge of the slow clock and then C_{OUT} is getting charged. After that, in the DCM phase, C_{OUT} is discharged by the loading current I_{Load}. In buck converter, the voltage ripple can also be written as:

$$V_{orp} = \frac{I_{Load}t_{DCM}}{C_{OUT}} \tag{7}$$

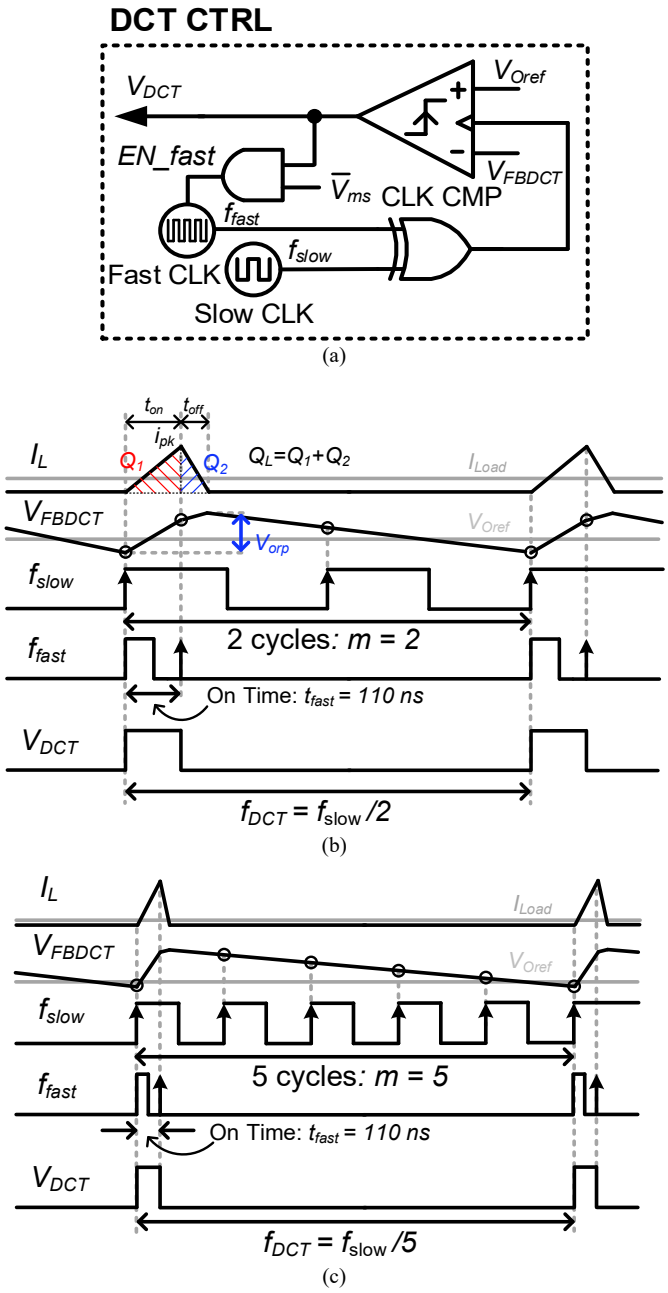


Fig. 6. (a) Block diagram of DCT control and its conceptual operation waveforms under (b) standby mode and (c) sleep mode.

Where t_{DCM} is the time duration for the DCM phase when the inductor current I_L = 0 as shown in Fig. 7. As shown in Fig. 7, when I_{Load} is sufficient large, m = 1, $f_{DCT} = f_{slow}$ as mentioned in (1), then we can assume $t_{DCM} \approx t_{slow}$, and the voltage ripple V_{orp} becomes:

$$V_{orp} = \frac{I_{Load}t_{DCM}}{C_{OUT}} \approx \frac{I_{Load}t_{slow}}{C_{OUT}} \tag{8}$$

Finally, the slow clock frequency f_{slow} can be obtained:

$$f_{slow} = \frac{I_{Load}}{C_{OUT}V_{orp}} \tag{9}$$

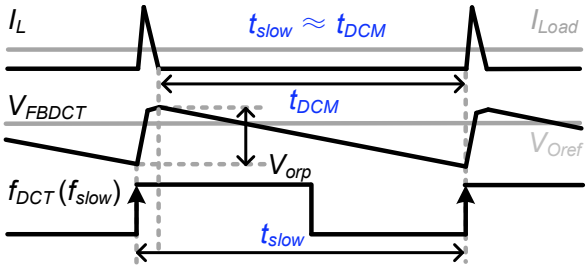


Fig. 7. DCT operation waveforms when I_{Load} is large.

When I_{Load} is 50 mA, C_{OUT} is 4.7 µF and the acceptable "voltage ripple" V_{orp} is 25 mV, f_{slow} = 424 kHz. Obviously, DCT is not designed to handle the case of maximum I_{Load} = 50 mA, however, we need to guarantee that the DCT mode can detect the sudden light-to-heavy step change, and the V_{orp} here indicates as a part of the undershoot voltage when the buck converter switches from DCT control to PWM control.

The slow clock oscillator circuit introduced in [22] is implemented in the work with designed trimming circuits as shown in Fig. 8, which achieves a very low power consumption per cycle by an additional positive feedback loop.

Finally, f_{slow} is designed to be around 400 kHz with trimming capacitor C_{a1} and the oscillator consumes 200 nA dynamic quiescent current. The signals $Trim_{DCT}[2:0]$ are designed to trim the clock frequency against process-voltage-temperature (PVT) by tuning the C_{a1} value.

D. Switching Frequency Determination

In steady state, the switching frequency f_{DCT} is related to I_{Load} and the total charge demagnetized from the inductor Q_L per cycle. Then with the help of (3), it yields:

$$f_{DCT} = \frac{1}{t_{DCT}} = \frac{I_{Load}}{Q_L} = \frac{2LMI_{Load}}{V_{IN}(1-M)(t_{fast})^2} \quad (10)$$

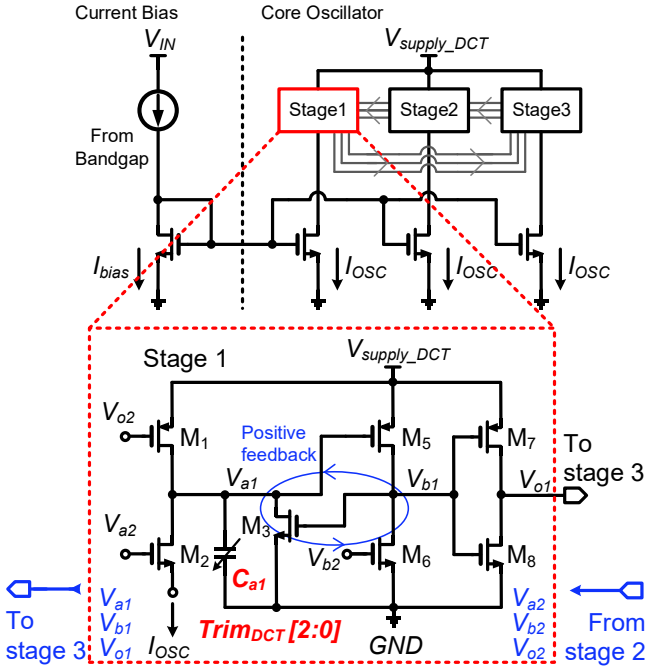


Fig. 8. Architecture of slow clock oscillator.

When V_{IN} = 2 V, V_{OUT} = 0.8 V, M = 0.4, I_{Load} = 100 nA and L = 2.2 µH, we obtain $f_{DCT} \approx$ 12 Hz. As the buck converter can operate at $f_{DCT} \approx$ 12Hz during sleep mode, the proposed DCT control can achieve an ultra-low quiescent current. When V_{IN} = 3.6 V, V_{OUT} = 1 V, M = 0.28 and I_{Load} = 10 mA, f_{DCT} = 338 kHz < f_{slow} (400 kHz), which means that the DCT control can handle a wide load current range operation. Finally, (14) proves that the switching frequency f_{DCT} is changing according to the load current I_{Load} in the DCT control. When the calculated $f_{DCT} > f_{slow}$, it means that the load current is over the DCT control range, then the design criteria for switching the converter from DCT mode into the PWM mode operation will be discussed in Section IV.

IV. Mode Selection Circuit Design

Usually, a large load current change (>1000x) will occur when the IoT devices switch from sleep or standby mode to transmit mode. In this work, it means the buck converter switches from DCT to PWM control. As discussed before, the control mode selection circuit and logic are simple in this dual- mode control system. Fig. 9 shows the schematic of the mode selection circuit schematic. The DCT-to-PWM mode selection circuit supplied by the V_{DD_DCT} is highlighted in the black block, while the PWM-to-DCT mode selection circuit supplied by the V_{DD_PWM} is highlighted in the blue block.

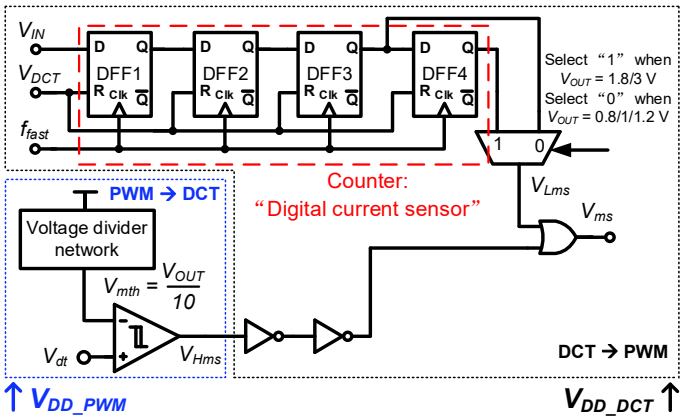


Fig. 9. Mode selector circuit schematic.

A. DCT-to-PWM Mode

A current sensor is necessary in the DCT control to accomplish the mode transition function. During the sleep mode, applying an analog current sensor consumes too much static power to detect a light load current. Hence, a digital ultra-lower power "current sensor" is proposed for the DCT control in this work. From Fig. 9, the circuit is based on a counter that is built up by cascading several D-flip-flops (DFF), which consumes almost zero static current. As mentioned before, when the load current I_{Load} is too large ($f_{DCT} > f_{slow}$ according to (10)), so that the fast clock f_{fast} may operate more than one times to handle this situation. That is, the power PMOS (in Fig. 2) on-time increases and becomes:

$$t_{on} = (N-1)t_{fast} = nt_{fast} \quad (11)$$

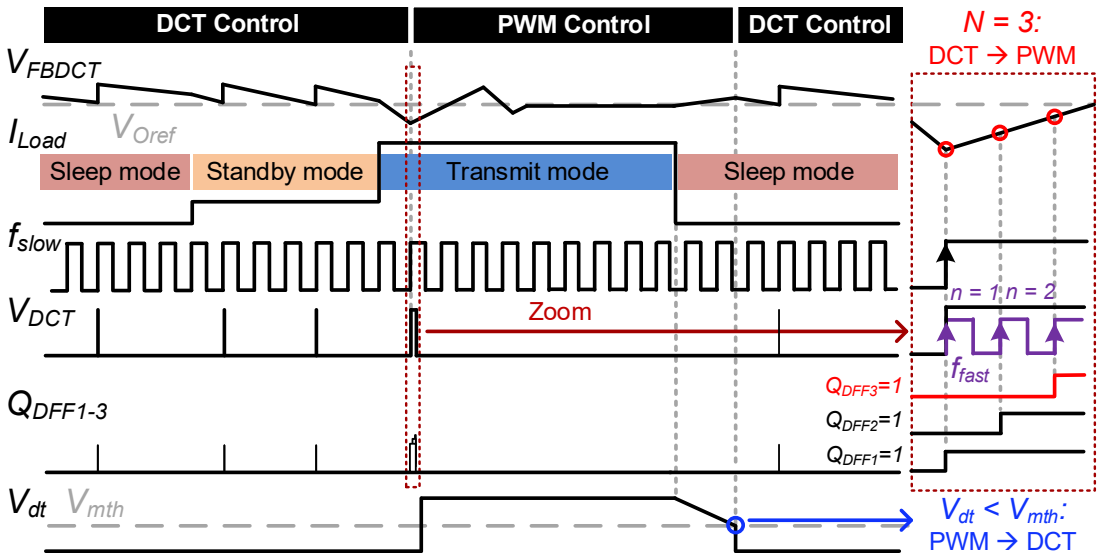


Fig. 10. Mode transition operation waveforms of the proposed DCT/PWM controlled buck converter.

where $N \geq 2$ is the number of used DFFs, $n = N - 1$ is the number of cycles for fast clock operates. Since n can be counted by using the counter as in Fig. 9, then n can reflect how large the load current is ($n \propto I_{Load}$). Thus, the number of selected DFF N can be utilized as the DCT-to-PWM mode transition design criteria. As a result, a simple counter can be functioned as a digital current sensor in the proposed DCT control.

Fig. 10 shows the detailed DCT-to-PWM mode transition operation waveforms with N = 3. When the load current changes from the standby mode to transmit mode, the feedback output voltage V_{FBDCT} will decrease rapidly. At the rising edge of the slow clock (f_{slow}), if the clock comparator detects that $V_{FBDCT} < V_{Oref}$, its output V_{DCT} = "1". Then the fast clock (f_{fast}) triggers and Q_{DFF1} = "1", and the power PMOS's on-time will be t_{fast} and charging the output capacitor C_{OUT}, V_{FBDCT} begins to rise. After that, at the rising edge of 2nd period of fast clock, Q_{DFF2} = "1", if the clock comparator detects that V_{FBDCT} is still less than V_{Oref}, the PMOS's on-time will be $2t_{fast}$. Finally, at the rising edge of 3rd period of fast clock, Q_{DFF3} = "1", if the clock comparator detects V_{FBDCT} is still smaller than V_{Oref}, V_{ms} = "1". Then the LDO_PWM turns on and the buck converter switches into PWM mode operation.

Considering different V_{IN} and V_{OUT} influence the load current upper limit in mode selection from (10), a multiplexer selects the DFF number with N = 3 for V_{OUT} = 0.8, 1, 1.2 V and N = 4 for V_{OUT} = 1.8, 3 V.

B. PWM-to-DCT Mode

In the PWM control, a conventional analog current sensing circuit with filtering capacitor [10,18] is applied for this work. As shown in Fig. 11, the power PMOS current I_{LP} *is* sensed by a current mirror I_{LPs}, and is converted into a voltage signal V_{dt} through a filtering capacitor C_s and a small DC current i_b. After that, from Fig. 9, V_{dt} will be compared with a threshold voltage V_{mth} (Different V_{mth} for different designed V_{OUT}). From Figs. 10 and 11, V_{ms} = "1" when $V_{dt} > V_{mth}$, the LDO_PWM keeps on and the converter continues working in PWM mode. However, V_{ms} = "0" when $V_{dt} < V_{mth}$, then the LDO_PWM turns off and the converter switches into DCT mode.

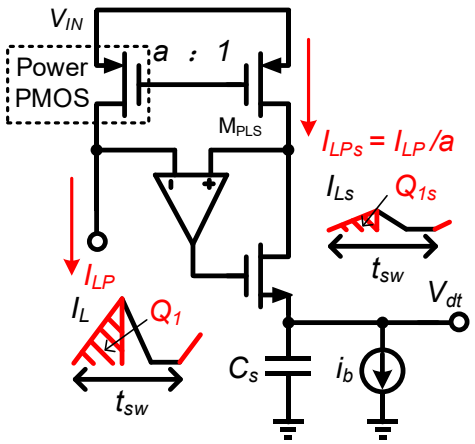


Fig. 11. Current sensing circuit with filtering capacitor in PWM control.

In PWM control, the relationship or transfer function between V_{dt} and I_{Load} is critical to design because it determines the load current level to switch the buck converter from PWM mode into DCT mode, which can be deduced with the help of Fig. 11. First, the sensed equivalent charge from the inductor L during magnetizing is described as:

$$Q_{1S} = \int_0^{t_{sw}} I_{LPS}(t)dt = \frac{\int_0^{t_{sw}} I_{Lp}(t)}{a} dt = \frac{Q_1}{a} \tag{12}$$

Where a is the current mirror ratio, t_{sw} is the PWM switching frequency. Then the sensed charge Q_{1S} can also be described as:

$$Q_{1s} = \frac{MQ_L}{a} = \frac{MI_{Load}t_{sw}}{a} \tag{13}$$

From Fig. 11 and (13), the voltage V_{dt} can be deduced by the total charge flows into the filtering capacitor C_s:

$$V_{dt} = \frac{Q_{1s} - i_b t_{sw}}{C_s} = \frac{Mt_{sw}\left(\frac{I_{Load}}{a} - i_b\right)}{C_s} \tag{14}$$

From (14), the relationship or transfer function between V_{dt} and I_{Load} can be obtained, which can help to design the criteria for PWM-to-DCT mode transition.

C. Mode Selection Stability Issue: Hysteresis Current Window

Under the mode selection scenario, if the hysteresis current window is not implemented, the buck converter may switch between the DCT and PWM modes rapidly when $I_{UBDCT} < I_{Load} < I_{LBPWM}$ as shown in Fig. 12(a), where I_{UBDCT} is the upper load current boundary of DCT control and I_{LBPWM} is the lower load current boundary of PWM control. When $I_{LBPWM} < I_{UBDCT}$ is designed, a hysteresis current window can be formed to ensure the stability during the mode transition.

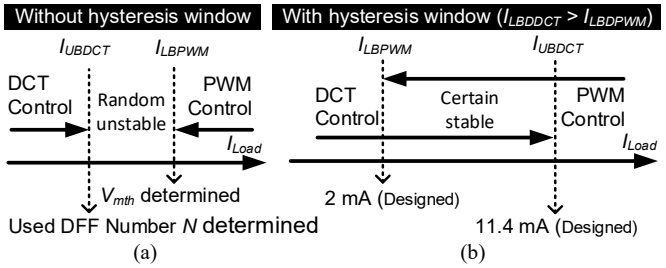


Fig. 12. Mode boundary current between DCT and PWM modes (a) without hysteresis window and (b) with hysteresis window.

Next, we would determine the I_{UBDCT} and I_{LBPWM} values. As mentioned before, the DCT-to-PWM and PWM-to-DCT mode selection criteria depends on the number of used DFF number N (we will analyze $N = 3$ case in the following) in the counter and the value of V_{mth} respectively.

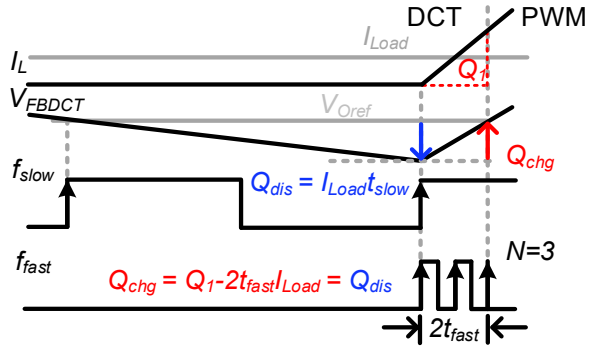


Fig. 13. Voltage drop study during DCT-to-PWM transition waveforms.

From Fig. 13, during DCT-to-PWM mode transition, the maximum voltage drop happens when 1) the output capacitor C_{OUT} discharges a complete t_{slow} period by I_{Load}, and 2) the DCT control operates and the output capacitor is charged by inductor Q_1 until $N = 3$ ($n = 2$) and then the converter changes into PWM mode. The boundary current I_{UBDCT} can be obtained by assuming $Q_{chg} = Q_{dis}$, yields,

$$Q_1 = I_{UBDCT}\left(\frac{1}{f_{slow}} + \frac{2}{f_{fast}}\right) \approx \frac{I_{UBDCT}}{f_{slow}} \quad (15)$$

Then I_{UBDCT} can be solved with the help of (2):

$$I_{UBDCT} = \frac{f_{slow}(V_{IN} - V_{OUT})(nt_{fast})^2}{2L} \quad (16)$$

In the case of $V_{IN} = 3.6$ V, $V_{OUT} = 1$ V and $n = 2$, the upper load current boundary of DCT control $I_{UBDCT} = 11.44$ mA.

During PWM-to-DCT transitions, the lower load current boundary of PWM control I_{LBPWM} can be solved by using (14) with setting $V_{dt} = V_{mth}$. Here we design $V_{mth} = V_{OUT}/10$ to against the variation caused by different output voltages, then we have:

$$I_{LBPWM} = a\left(\frac{V_{IN}C_s f_{sw}}{10} + i_b\right) \quad (17)$$

where $f_{sw} = 2.5$ MHz is the PWM switching frequency. Then these analog parameters a, C_s and i_b can be designed to satisfy the condition of the current hysteresis window. When $a = 2000$, $V_{IN} = 3.6$ V, $C_s = 1$ pF and $i_b = 100$ nA, $I_{LBPWM} = 2$ mA.

V. Low Power Bandgap Reference Design

The generated $V_{ref} = 1.2$ V is constant over different input/output range, PVT variations, load current conditions, etc. This is important to minimize the variations of the quiescent current of the controller originated from (1), especially for slow clock generator as described in Section III-C.

In order to achieve ultra-low quiescent current, the current consumption of the bandgap reference should be as low as possible. The works in [23], [24] present a sub-threshold, nano-ampere bandgap reference design without using a resistor. Fig. 14 shows the architecture of the nano-ampere bandgap reference circuit, which includes the start-up circuit, current reference circuit, bipolar junction transistor (BJT), proportional to absolute temperature (PTAT) voltage generators and voltage divider. V_{Oref} is the reference of buck converter's output voltage generated by a half-voltage divider.

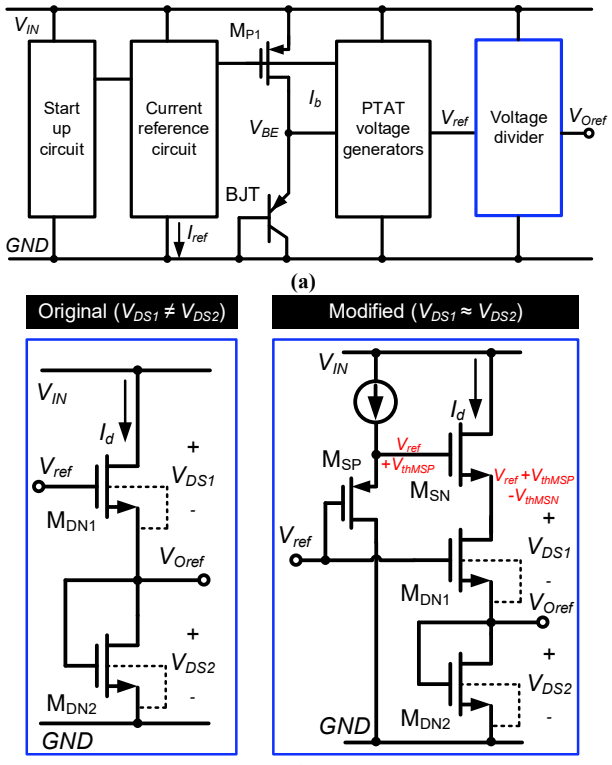


Fig. 14. (a) The Block diagram of the BGR and (b) the architecture of original [24] and modified half-voltage divider circuit in nano-ampere bandgap reference.

In the original half divider circuit [24], when both M_{DN1} and M_{DN2} are in saturation region as shown in Fig. 14(b), the current can be easily expressed as:

$$I_d = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS1} - V_{TH})^2(1 + \lambda V_{DS1}) \quad (18)$$

$$I_d = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS2} - V_{TH})^2(1 + \lambda V_{DS2}) \quad (19)$$

Where μ_n is the carrier mobility, $C_{OX}$is the gate-oxide unit-capacitance, $\frac{W}{L}$ is the aspect ratio, λ is the channel length modulation factor, $V_{DS1} = V_{IN} - V_{Oref}$, $V_{GS1} = V_{ref} - V_{Oref}$, $V_{DS2} = V_{GS2} = V_{Oref}$. Since the size of M_{DN1} and M_{DN2} are the same, their threshold voltage V_{TH} are the same as well. Then solving V_{ref} and V_{Oref} with (18) and (19) yields:

$$(V_{ref} - V_{Oref} - V_{TH})^2(1 + \lambda V_{DS1}) = (V_{Oref} - V_{TH})^2(1 + \lambda V_{DS2}) \quad (20)$$

From (20), $V_{ref} \approx 2V_{Oref}$ can be obtained when the difference between V_{DS1} and V_{DS2} is small. However, in this work, since V_{IN} varies from 2 V to 5 V, V_{DS1} (4.4 V when V_{IN} = 5 V) is far different from V_{DS2} (0.6 V), so that the channel length modulation effect cannot be neglected. Fig. 14(b) also shows the modified half-voltage divider proposed in this work. Compared with the original circuit, there are two source followers M_{SP} and M_{SN} trying to obtain the condition:

$$V_{DS1} \approx V_{DS2} = V_{Oref} \quad (21)$$

Finally, substitute (21) into (20), the channel length modulation effect can be neglected and the expected result is achieved:

$$V_{ref} \approx 2V_{Oref} \quad (22)$$

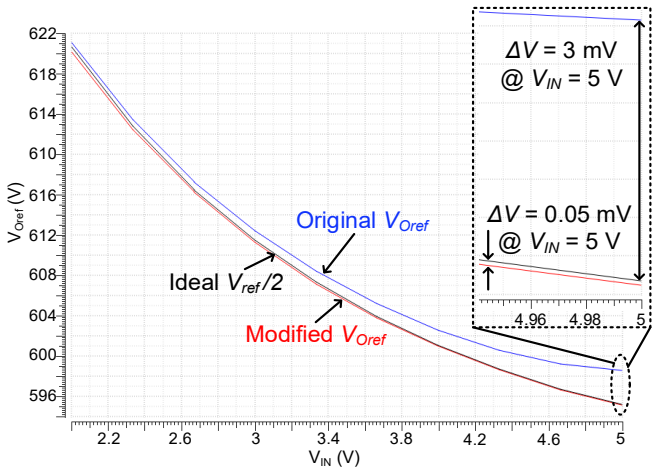


Fig. 15. Simulated ideal, original and modified V_{Oref} waveforms with respect to V_{IN} varies from 2 V to 5 V.

Fig. 15 exhibits the ideal (black), original (blue) and modified (red) output waveform of the half voltage divider with respect to different input voltage V_{IN}. From Fig. 15, the difference between the ideal case and original case is 3 mV, while the difference between the ideal case and modified case is 0.05 mV at the point V_{IN} = 5 V. It verifies that the modified voltage divider circuit is more consistent with the ideal case, which verifies the effectiveness of the modified circuit compared with the original design in [22].

VI. Experimental Results

The prototype is fabricated in a 0.18μm CMOS with 5 V thick oxide option, and the active area is 1×1.1 mm^2 with PAD-ring included, as shown in Fig. 16. Thanks to the proposed DCT control mode and low power DCT-to-PWM mode selection circuit, the converter achieves an I_q = 470 nA at V_{IN} = 2.0 V and V_{OUT} = 0.8 V, as shown in Fig. 17.

Fig. 18 shows the measured efficiency when V_{IN} = 3.6 V with V_{OUT} = 0.8V, 1.8V, 3.0V and I_{Load} from 10 μA to 50 mA. From Fig. 18, the peak efficiency is 92.7%/94.7% in DCT/PWM at I_{Load} = 100μA/5mA, respectively when V_{IN} = 3.6 V and V_{OUT} = 3.0 V. When V_{OUT} = 1.8 V and 3.0 V, the power efficiency is still >80% from 10 μA to 50 mA (5000x). When V_{OUT} = 0.8 V, the conversion ratio is low, thus efficiency will be lower than those with high conversion ratio, however, this design can still achieve the power efficiency >70% from 100 μA to 50 mA.

Fig. 19 presents when the I_{Load} changes between 1.4 mA and 14 mA gradually, the converter's output voltage can be regulated to its reference voltage (within ±2% accuracy), although the control mode has been switched automatically between DCT control and PWM control, which verifies the "seamless mode selection" in this design. It also shows the mode selection hysteresis window is located between 1.5 mA and 12.6 mA, which is consistent with the design.

Fig. 20 shows the measured waveforms with DCT and PWM modes in steady state under the same V_{IN} = 3.6 V, V_{OUT} = 1 V, and I_{Load} = 5 mA. From Fig. 20(a), the measured f_{slow} = 466 kHz and t_{fast} = 115 ns. From Fig. 20(b), the measured f_{sw} = 2.6 MHz.

Fig. 21 shows the load transient response between 6.67 μA and 50 mA with the mode selection design, the undershoot/overshoot voltage is 80/30mV at 11/60μs recovery time, which is comparable to the other works.

Fig. 22 shows the measured output ripple with respect to different load currents (from 10 μA to 2 mA) when V_{IN} = 3.6 V, V_{OUT} = 1 V and 1.8 V in DCT control.

From Table II, the undershoot voltage per load step of this work is 1.6 mV/mA, which is lower than that of [8], [11] and [14]. On the other hand, the load step per settling time (recovery speed) of this work is 4.54 mA/μs, which is much faster than that of [11]. In [8], it is fast (11.04 mA/μs) because the load transient response happens within one control mode only, thus it obtains a narrow output current range and lower light-load efficiency. Compared with [8] – [11] and [14], this work achieves better power efficiency with a wide V_{IN} and I_{Load} range as shown in Table II. This work also achieves a comparable I_q with bandgap reference circuit and internal oscillator included. From Table II, the proposed FOM of this work is competitive to the other works [8], [10]. From [9], it obtains the best FOM because the power consumption of the bandgap and oscillator are not included.

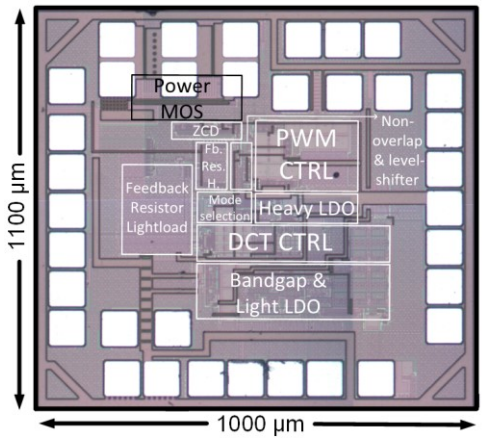


Fig. 16. Chip micrograph of the buck converter.

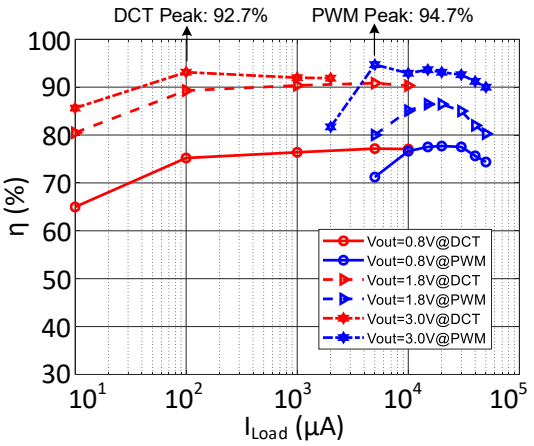


Fig. 18. Measured efficiency when V_{IN} = 3.6 V with respect to different V_{OUT}.

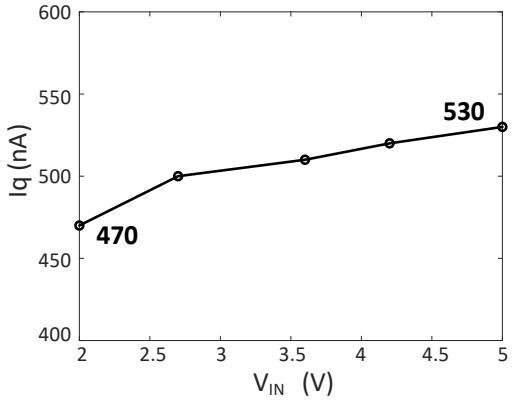


Fig. 17. Measured quiescent current I_q when V_{OUT} = 0.8V with respect to different V_{IN}.

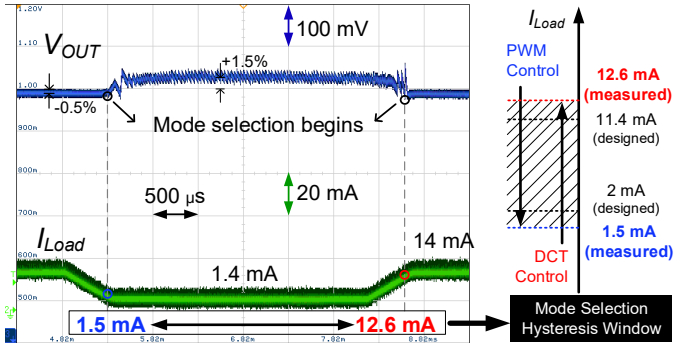
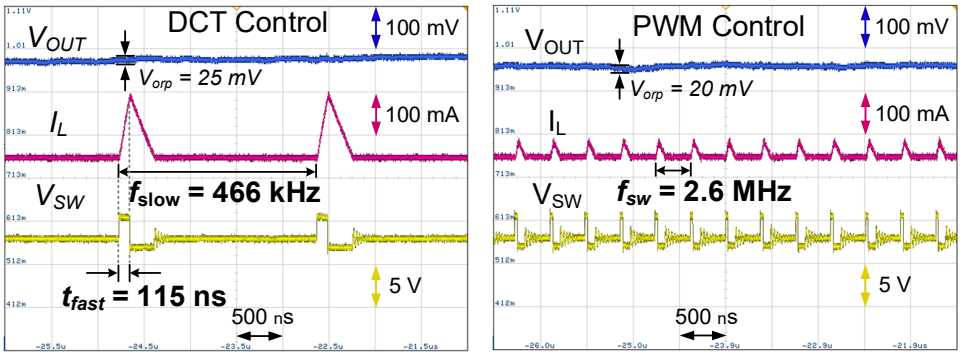


Fig. 19. Measured mode selection hysteresis window when V_{IN} = 3.6 V, V_{OUT} = 1 V and I_{Load} changes between 1.4 mA and 14 mA gradually.



(a) (b)

Fig. 20. Measured V_{OUT}, I_L and V_{sw} waveforms when V_{IN} = 3.6 V, I_{Load} = 5 mA, V_{OUT} = 1 V with (a) DCT and (b) PWM mode.

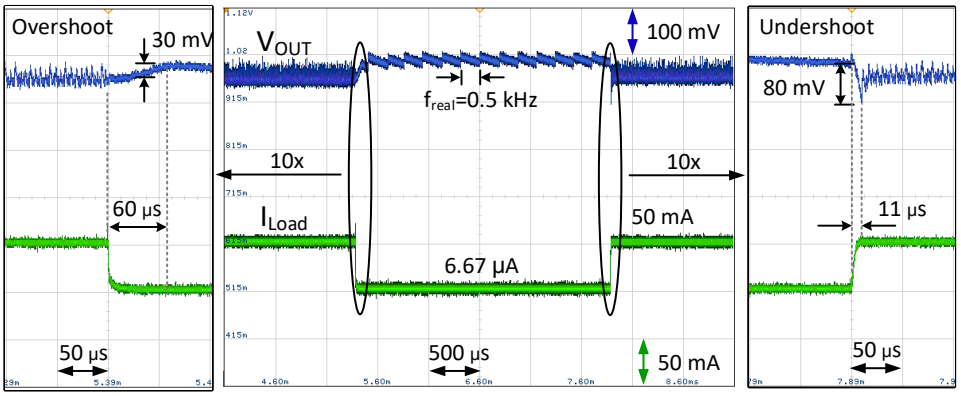


Fig. 21. Measured I_{Load} step change between 6.67µA and 50 mA when V_{IN} = 3.6 V and V_{OUT} = 1 V.

TABLE II. COMPARISON WITH STATE-OF-THE-ART LOW QUIESCENT CURRENT BUCK CONVERTERS

Parameter	**This work**	[11] S. Bandyopadhyay JSSC'2011	[14] S. Park TBCAS'2015	[9] P. Chen JSSC'2016	[10] Y. Park TPEL'2017	[8] F. Santoro JSSC'2018
Technology	**180nm**	45nm	180nm	180nm	130nm	130nm
V_{IN} (V)	**2-5**	2.8-4.2	2.5-3.3	0.55-1.0	2.2-3.3	1.8-3.3
V_{OUT} (V)	**0.8,1,1.2,1.8,3**	0.4-1.2	1	0.35-0.5	1.7	1.2
I_q (nA)	**470**	NA	NA	145 (w/o bandgap & oscillator)	500	440 (w/o bandgap)
Control Modes	**DCT+PWM**	PFM+PWM	PWM	AM+PFM+PWM	RM+PFM+PWM	SBHC
I_{Load} (mA)	**0.001-50**	0.02-100	0.045-4	0.0001-20	0.01-20	0.0001-2.65
L/C_{OUT} (µH/µF)	**2.2/4.7**	10/2	6.8/1.2	4.7/4.7	3/3	18/0.056
Efficiency (%)[a]	**85.6@10µA/ 92.7@100µA/ 93@10mA**	71@20µA/ 79@100µA/ 87@10mA	71@35µA / 82@100µA / 86.3@1.4mA	79@10µA/ 82@100µA/ 92@10mA	74.2@10µA/ 82.7@1mA/ 92.4@20mA	62@10µA/ 85@100µA/ 92.2@2.65mA
Area /mm^2	**1.1**	2.25 (w/o PAD-ring)	0.375 (w/o PAD-ring)	1.44	0.66	0.14 (w/o PAD-ring)
Undershoot/time (mV/µs)@load step	**80/11@ 6.67µA-50mA**	10/34@ 100µA-5mA	240/NA@ 50µA-4mA (w/o mode change)	NA	NA	30/0.24@ 100nA-2.65mA (w/o mode change)
Undershoot/Load step (mV/mA)[b]	1.6	2	60	NA	NA	11.3
Load step/Settling time (mA/µs)[c]	4.54	0.147	NA	NA	NA	11.04
FOM (pA/%)[b,d]	11	NA	NA	0.9	337	26.8

[a]: Estimate from figure, [b]: Smaller value is better, [c]: Larger value is better, [d]: FOM = $I_{Load\_min}\times I_q/(I_{Load\_max}\times Eff@10\mu A)$, where I_{Load_max}, I_{Load_min}, $Eff@10\mu A$ represents the maximum and minimum load current value and efficiency at 10µA.

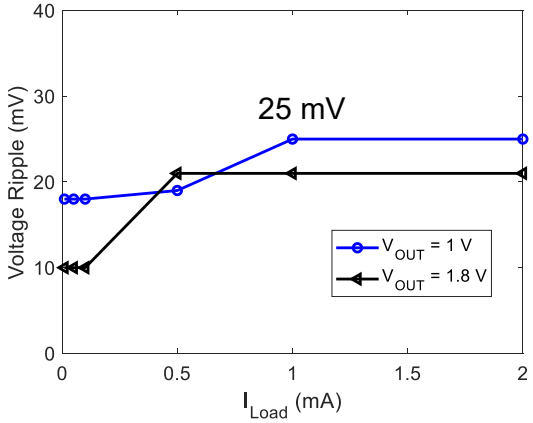


Fig. 22. Measured output voltage ripple with respect to different load current when V_{IN} = 3.6 V, V_{OUT} = 1 V and 1.8 V in DCT control.

VII. CONCLUSION

In this work, a DCT/PWM buck converter with low quiescent current, wide input/output voltages and load range, and seamless mode selection and transition consideration are implemented for IoT application. The theory and operation principle of the proposed low power DCT control is also analyzed and discussed. A simple counter-based digital current sensing circuit is designed for the DCT-to-PWM mode selection, without consuming any static current. The PWM-to-DCT mode selection circuit and a hysteresis window are also implemented to guarantee the smooth and stable mode transition between PWM and DCT modes. A current mode PWM control is applied to extend the load current range and to verify the proposed mode selection circuit design. The proposed buck converter achieves 470 nA quiescent current, including bandgap, internal LDO and oscillator. It also achieves a peak efficiency of 92.7% and 94.7% in DCT and PWM control, respectively, and >80% from 10 µA to 50 mA (5000x), with a wide input voltage from 2V to 5 V and load current range from 1 µA to 50 mA.

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