



A high PSR and high-precision current-mode bandgap reference with g_m boost self-regulated structure

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ABSTRACT

A high power supply rejection and high-precision current-mode bandgap reference system with a reliable start-up g_m boost self-regulated structure is presented in this paper. The g_m boost technology and high-precision compensation structure are adopted to improve the power supply rejection and precision of the output reference current, respectively. The proposed reference system has been designed in Semiconductor Manufacturing International Corporation (SMIC) 55 nm CMOS process. The simulation results show that with a supply voltage of 3.3 V, the power supply rejection is -101.3dB@DC , -60.23dB@1MHz and -55.6dB@10MHz , the temperature coefficient of the output reference current of proposed circuit is approximately $3.14 \text{ ppm}^{\circ}\text{C}$ in a temperature range from -40 to 125°C , the quiescent current consumption is $47.8 \mu\text{A}$ and the silicon area is 0.0992 mm^2 .

1. Introduction

The bandgap reference (BGR) circuit is an important module of systems-on-chip (SoCs) and used to provide stable and reliable temperature-independent reference voltage or current [1–8] for analog circuits and mixed-signal circuits, such as A/D converters, low dropout linear regulator and memory circuits. Almost all emerging memories require BGR modules, such as RRAM, MRAM, and PCRAM. Its performance largely determines the quality of the entire SoC. With the development of technology, some high-performance analog integrated circuits, such as high-precision analog-to-digital converters and low jitter phase-locked loops, etc., have put forward stricter requirements for the performance of BGR circuit with high power supply rejection (PSR) [9–14]. Moreover, in order to improve the integration of the circuit, more and more digital circuits, analog circuits, and even radio frequency circuits are integrated into complex SoCs, which

will lead to severe interference of the power supply by these circuit modules and often result in significant noise. The performance of the output reference voltage (V_{REF}) could be degraded by the noise, thereby deteriorating the overall system performance. In order to cope with noisy on-chip environments, the PSR performance and precision of BGR circuits are becoming increasingly important.

This paper proposes a high PSR and high-precision BGR system based

on a reliable start-up self-regulated (SR) circuit providing the reference operation voltage at a supply voltage of 3.3V to improve the above issues and meet the requirements of multi-level storage of PCRAM. The rest of this paper is organized as follows. Section II describes the operation principle of the conventional and proposed high PSR BGR technique. Section III describes the operation principle of the conventional current-mode BGR circuit with curvature-compensation and proposed high-precision BGR circuit with I_{NL} compensation. Section IV presents the simulation results that verify the accuracy and high PSR of the proposed BGR circuit. Finally, the conclusions are provided in Section V.

2. Principle of conventional and proposed high psr bgr technique

2.1. Conventional high PSR BGR technique

The popular technologies for improving PSR mainly include cascode current mirrors [9], MOSFET low-pass filters [10,11] and SR circuits [12–14] at the output terminal. As shown in Fig. 1, MP₁ is a cut-off PMOS transistor with an impedance over $1\text{G }\Omega$ and MN₁ acts as a capacitor, forming an RC low-pass filtering circuit based on MOSFETs.

Due to the extremely high impedance of MP₁, almost only DC signals can be transmitted to V_{out} , thus improving PSR. However, an extremely

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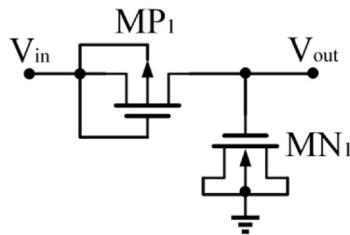


Fig. 1. MOSFET low-pass Filter in Ref. [11].

high resistance node is formed in V_{out} in this structure, which is prone to oscillation once disturbed in the circuit and starts very slowly without practical value.

The self-regulated technique is also a technique for improving the PSR of BGR circuits. As shown in Fig. 2, where PFL is positive feedback loop and NFL is negative feedback loop, the basic principle is to use the SR circuit to generate a stable, low ripple, self-regulated power supply to the BGR core circuit, thereby improving PSR performance of BGR circuit.

Due to the fact that the generation of V_{REG} requires the V_{REF} generated by the BGR core circuit, and the BGR core circuit also requires the V_{REG} to work properly, the start-up circuit of this structure needs to be carefully designed to ensure that the entire circuit can be started normally. In Fig. 2, during the power-on process, V_{REF1} outputs a signal in low level and M₃ is on, causing the upper electrode of C₃ to be at a high level while V_{REG} remains at a low level, thus preventing the BGR from starting. The start-up process in Ref. [9] also has the same problem, which poses some hidden trouble and could not be reliably started. On the other hand, the PSR of this SR structure is relatively low, which in turn affects the PSR of following BGR circuit.

2.2. Proposed high PSR BGR technique

A reliable start-up g_m boost self-regulated (GBSR) structure is proposed in this paper, as shown in Fig. 3.

consisted of R₁, R₂, EA and M₃ amplifies the g_{m3} by about $\beta \bullet A_{EA}$ times, where g_{m3} is the transconductance (g_m) of M₃, A_{EA} is the gain of the operational amplifier EA, and $\beta = \frac{R_1}{R_1+R_2}$ is a feedback coefficient, so that the equivalent g_m of GBSR circuit is

$$g_{GBSR} = \beta \bullet A_{EA} \bullet g_{m3} \quad (1)$$

The small-signal modeling of GBSR circuit is presented in Fig. 4. And the derived transfer function can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{1}{g_{GBSR} + \frac{1}{r_{o2}} + \frac{1}{r_{o3}} + \frac{1}{r_{o5}} + \left(g_{m5} - \frac{1}{r_{o3}} \right) \times \frac{g_{GBSR} r_{o3} r_{o4} + r_{o4}}{r_{o3} + r_{o4}}} \times \frac{1}{r_{o2}} \quad (2)$$

where r_{o2}, r_{o3}, r_{o5} are the small-signal output resistance of M₂, M₃, M₅

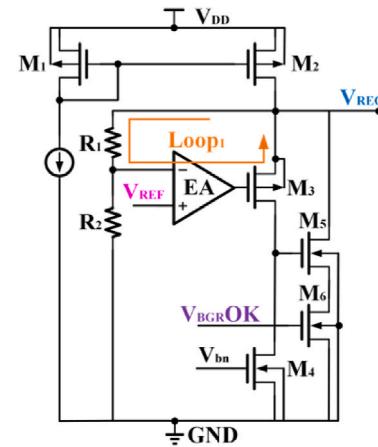


Fig. 3. Schematic of GBSR circuit proposed in this paper.

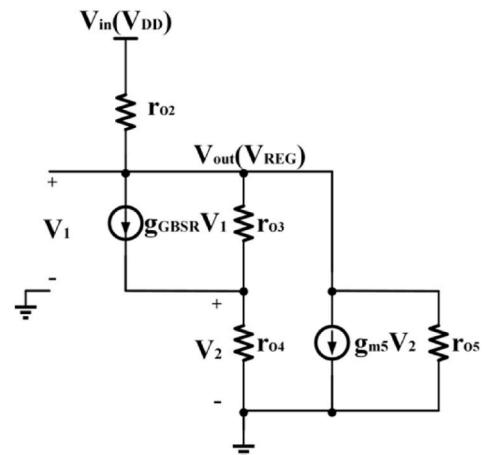


Fig. 4. Small-signal modeling of GBSR circuit.

respectively. Generally $g_m \approx 10g_{mb} \approx \frac{100}{r_o}$, where g_{mb} is equivalent g_m of body effect, g_{m5} is the g_m of M₅ and is much bigger than 1/r_{o2}, 1/r_{o3} and 1/r_{o5}, and g_{GBSR} is much greater than g_{m5}. So after simplifying complex equation (2), it can be concluded that

$$\frac{V_{out}}{V_{in}} \approx \frac{1}{g_{GBSR}(1 + g_{m5} \times r_{o3} \| r_{o4}) \times r_{o2}} \approx \frac{1}{g_{GBSR} \times g_{m5} \times r_{o3} \| r_{o4} \times r_{o2}} \quad (3)$$

And the small-signal resistance seen from V_{REG} to the ground can be expressed as

$$R_{REG} = \frac{1}{\beta \bullet A_{EA} g_{m3} (r_{o3} \| r_{o4}) g_{m5}} \quad (4)$$

Thus, the PSR_{GBSR} from V_{DD} to V_{REG} is divided by R_{REG} and r_{o2}, which can be expressed as

$$PSR_{GBSR} = \frac{1}{r_{o2} [\beta \bullet A_{EA} g_{m3} (r_{o3} \| r_{o4}) g_{m5}]} \quad (5)$$

The PSR of conventional SR circuits is only

$$PSR_{CONV_SR} = \frac{1}{r_{o2} g_{m3} (r_{o3} \| r_{o4}) g_{m5}} \quad (6)$$

Due to the increase in g_m of the SR circuit, the gain of Loop₁ increases, and the equivalent resistance from V_{REG} to ground is further reduced. Therefore, by comparing equations (5) and (6), it can be concluded that the PSR of GBSR structure proposed in this paper is $\beta \bullet A_{EA}$ times better than that of conventional SR structures.

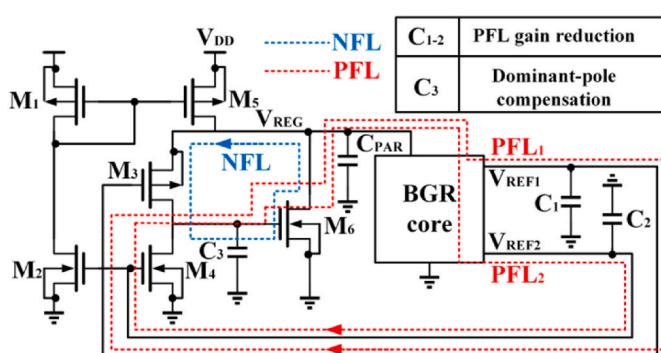


Fig. 2. Self-regulated technology in Ref. [14].

The GBSR structure is composed of R_1 , R_2 , error amplifier (EA) and M_2 - M_6 . The function of M_6 is to ensure the circuit normally start up when powered on. When M_6 turns on, it no longer affects the operation of the whole circuit. Loop₁

3. Principle of conventional and proposed BGR circuit

3.1. Conventional curvature-compensated BGR circuit

The structure of conventional curvature-compensated BGR circuit [5] is shown in Fig. 5.

According to the study of Tsividis et al. [15], the accurate analysis of temperature effects in V_{EB} -T characteristics can be expressed as

$$\begin{aligned} V_{EB}(T) &= V_{G0}(T_r) + \left(\frac{T}{T_r}\right)[V_{EB}(T_r) - V_{G0}(T_r)] - \\ &(n-\delta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \end{aligned} \quad (7)$$

where $V_{G0}(T_r)$ is the bandgap voltage of silicon at reference temperature T_r , n is a temperature-independent and process-dependent constant around 4, while δ is the factor of the temperature dependence of the collector current, which is equal to 1 if the current in the BJT is PTAT and goes to 0 when the current is temperature-independent, k is the Boltzmann's constant, and q is the charge of an electron.

The currents flowing into Q_1 and Q_2 are proportional to absolute temperature, so that the parameter δ in the expression of V_{EB} is equal to 1. While the currents flowing into Q_3 is temperature-independent, so that parameter δ is equal to 0 [8].

The V_{EB} of Q_1 and Q_2 can be expressed as

$$V_{EB,Q1,2} = V_{G0}\left(1 - \frac{T}{T_r}\right) + V_{EB0}\left(\frac{T}{T_r}\right) - (n-1)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \quad (8)$$

The current in M_1 is

$$I_{REF} = I_{PTAT} + I_{CTAT} - I_{NL} \quad (9)$$

which is a current with a low TC after high-order temperature nonlinear compensation.

V_{REF} can be expressed as

$$\begin{aligned} V_{REF} &= V_T \frac{R_6 \ln(N)}{R_2} + V_{EB,Q1,3} \frac{R_6}{R_{1,3}} - V_{NL} \frac{R_6}{R_{4,5}} \\ &= \frac{R_6}{R_{1,3}} \left(\frac{R_{1,3} \ln(N)}{R_2} + V_{EB,Q1,3} - \frac{R_{1,3}}{R_{4,5}} V_{NL} \right) \end{aligned} \quad (10)$$

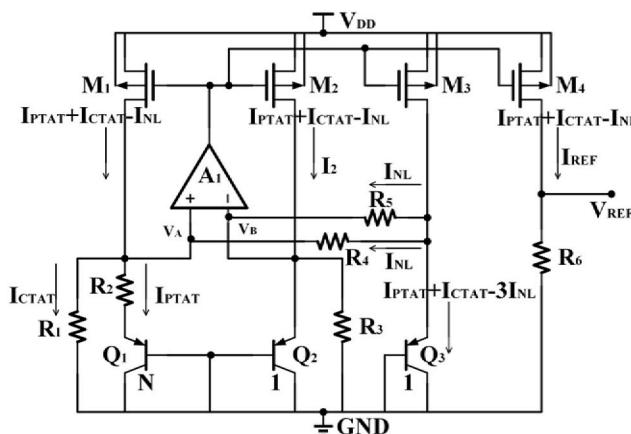


Fig. 5. Conventional curvature-compensated BGR circuit proposed by Malcovati [8].

However, according to Kirchhoff's law, the current flowing into Q_3 is

$$I_{REF} = I_{PTAT} + I_{CTAT} - 3I_{NL} \quad (11)$$

which is not totally temperature-independent and will affect the accuracy of V_{REF} . There are residual nonlinear terms and nonlinear currents (I_{NL}) should be compensated.

3.2. Proposed high-precision BGR circuit

On the basis of Malcovati [5], many methods to compensate the high-order terms have been presented [16–24]. This paper compensates for the excess nonlinear current flowing into Q_3 , as shown in Fig. 6.

Proposed high-precision nonlinear current compensation structure is composed of two operational amplifiers (op amps) A_2 and A_3 whose more details are presented in Section IV-A, two resistances $R_{4,5}$ which are equal to R_4 and R_5 , and M_5 - M_{10} .

According to the characteristic of op amps and Kirchhoff's law, a current equal to $2I_{NL}$ is generated, which can be expressed as

$$2I_{NL} = \frac{2V_B}{R_{4,5}} - \frac{2V_A}{R_{4,5}} \quad (12)$$

This current is then injected into the emitter of Q_3 , which will completely offset the excess high-order nonlinear temperature term of the current in Q_3 and reduce the temperature coefficient (TC) of V_{REF} . At this time, excess nonlinear currents in the third excess high-order term of equation (11) are eliminated and the current in equation (9) is achieved to flow into Q_3 , a novel high-precision current-mode BGR core structure is proposed in this paper. The difference of I_{REF} simulation results between two structure of Figs. 5 and 6 is shown in Section IV-B.

4. Simulation results

A high PSR and high-precision current-mode BGR circuit with a SR structure which is composed of a reliable GBSR circuit and a BGR core with high-precision nonlinear temperature current compensation circuit has been designed in SMIC 55 nm CMOS process and the 3.3V CMOS devices are adopted. The GBSR provides a self-regulated power supply V_{REG} isolated from the power supply V_{DD} for the BGR core circuit to improve the PSR of the output reference current (I_{REF}), as shown in Fig. 8, where Loop₁ is a voltage follower, Loop₂ is a negative feedback loop, and both of them are used to improve the stability of supply power in order to increase the PSR of the entire circuit. The design parameters of proposed high-precision current-mode BGR circuit are provided in Table 1.

4.1. Op amp

The circuit of the op amps EA, A_1 , A_2 and A_3 is provided in Fig. 7, where the input stage of this circuit mainly consists of a PMOS transistors differential pair M_{34} and M_{35} and a NMOS transistors differential pair M_{36} and M_{37} placed in parallel as a rail-to-rail differential input stage whose input common-mode voltage is from ground to power supply. The operating range of this structure is larger than that of single differential pairs input stage. The folded-cascode structure is used to increase the output impedance of the circuit, thereby increase the circuit gain and make the secondary pole far away from the main pole. The current source idc comes from internal bias circuit. The supply voltage of A_1 , A_2 and A_3 is supplied by V_{REG} , and the supply voltage of EA is supplied by V_{DD} .

The open-loop gain of the op amp in Fig. 7 is shown in Fig. 9. It can be seen that the DC open-loop gain is about 102.6 dB and the phase margin is 69.03° and gain margin is –20.31 dB, which means that the entire circuit operates well in a stable state.

The input offset mainly consists of two parts: the first part is the offset of differential pairs, and the second part is the offset of folded-cascode

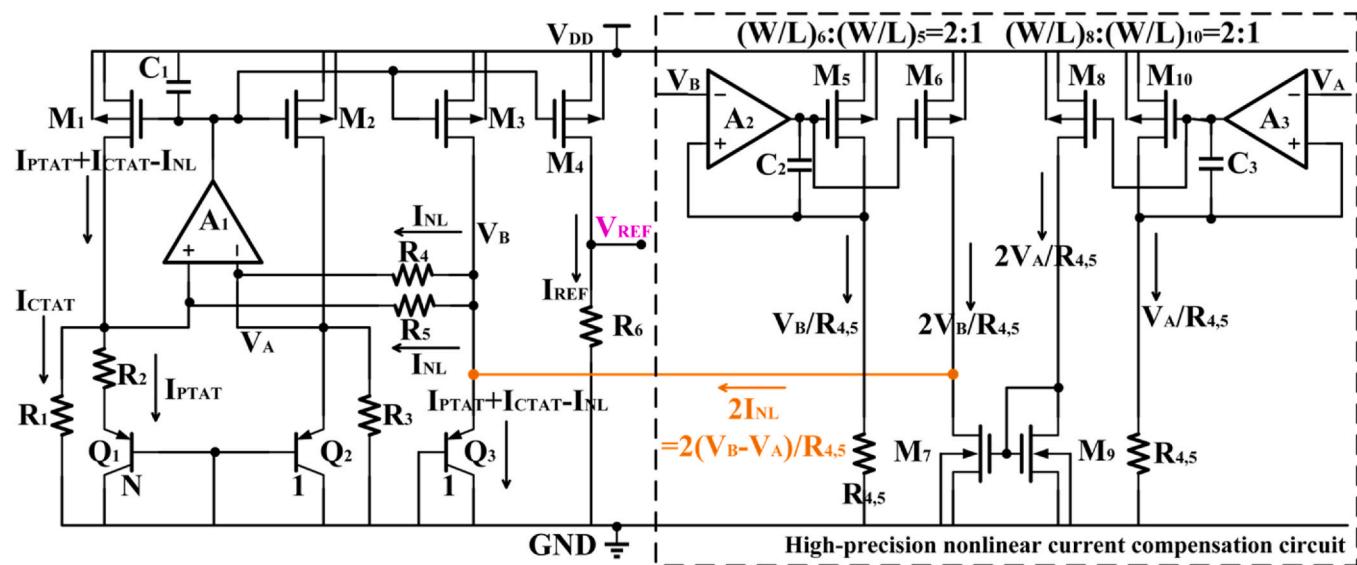


Fig. 6. Schematic of the BGR circuit proposed in this paper.

Table 1
Component sizes used in THE proposed BGR circuit.

Component	Parameter
M1 and M2	W = 3 μm , L = 8 μm , m = 1
M3 and M5	W = 8 μm , L = 0.6 μm , m = 8
M4	W = 1 μm , L = 2 μm , m = 2
M6	W = 3 μm , L = 0.8 μm , m = 1
M7, M9, M10, M11, M12, M13, M14, M17, M18, M20 and M22	W = 3 μm , L = 8 μm , m = 2
M8, M15, M16 and M23	W = 15 μm , L = 10 μm , m = 30
M19 and M21	W = 1.2 μm , L = 6 μm , m = 2
Q1	8 \times (5.6 μm \times 5.6 μm)
Q2 and Q3	1 \times (5.6 μm \times 5.6 μm)
R1 and R2	122.55 k Ω
R3 and R5	465.33 k Ω
R4	60.69 k Ω
R6 and R7	120.14 k Ω
R8	338 k Ω
R9	185.13 k Ω
R10	23.7 k Ω

load. Careful layout techniques, such as common centroid layout techniques, ensure appropriate matching between transistors, reduce random mismatch or ignore the mismatch caused by differential pairs in width errors. It is necessary to optimize the channel length of the differential pairs by reducing the overdrive voltage and appropriately increase the size of the differential pairs to reduce the mismatch caused by process errors.

The input offset voltage (V_{os}) with temperature sweep of the proposed op amp is shown in Fig. 10. It can be seen that V_{os} varies from 1.27 μV to 1.73 μV , and the curve almost linearly increases with temperature, within a reasonable range.

300 iterations Monte-Carlo simulation of the V_{os} are conducted and shown in Fig. 11. The simulation results show that V_{os} varies from 158.75 μA to 160.5 μA under the worst case scenario.

The noise of the op amp is mainly determined by the input stage. In this paper, the rail-to-rail input stage uses the PMOS differential pairs as the main input differential pairs to reduce flicker noise, due to its low noise. The NMOS differential pairs used as an auxiliary differential pairs can also operate normally when the input common-mode voltage is high and PMOS differential pairs enters the cut-off state. In addition, the noise component of the load device is scaled by the ratio of their $g_{m,\text{load}}$ to the $g_{m,\text{input}}$ of the input stage. Therefore, when designing an op amp, the g_m of input differential pairs needs to be greater than that of the load

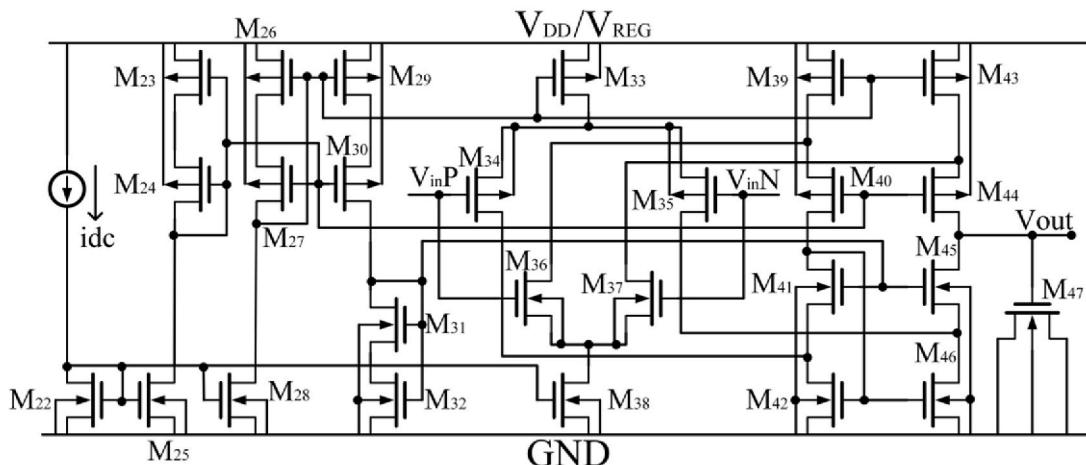


Fig. 7. The op amp EA, A1, A2 and A3 circuit in Fig. 6.

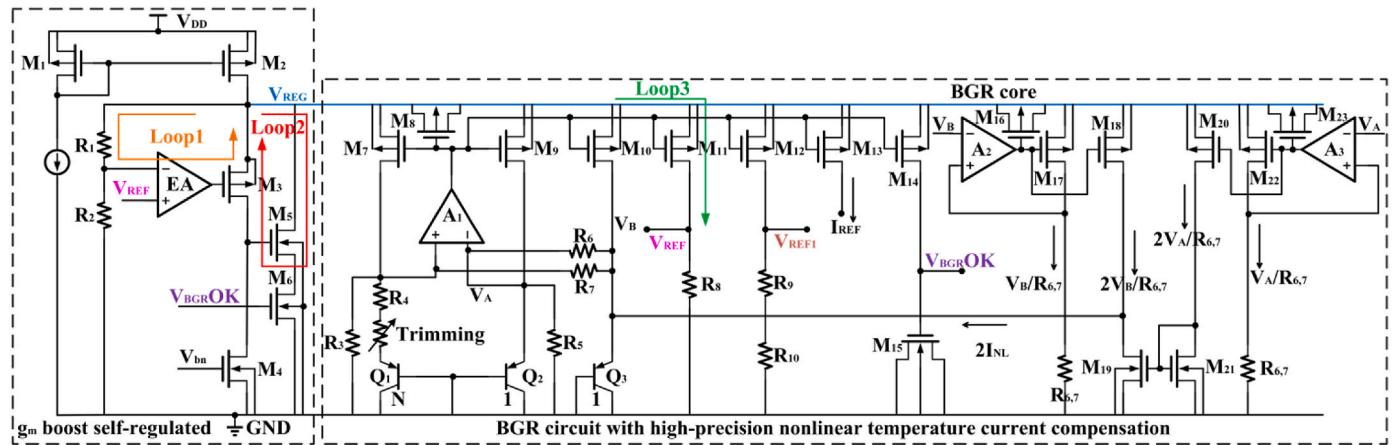


Fig. 8. Schematic of the GBSR and BGR circuit proposed in this paper.

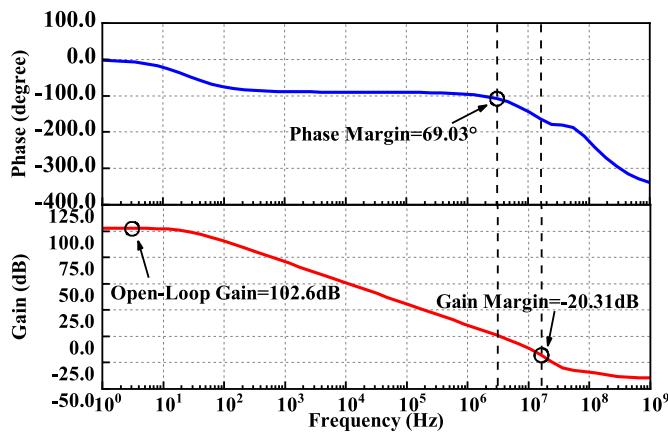
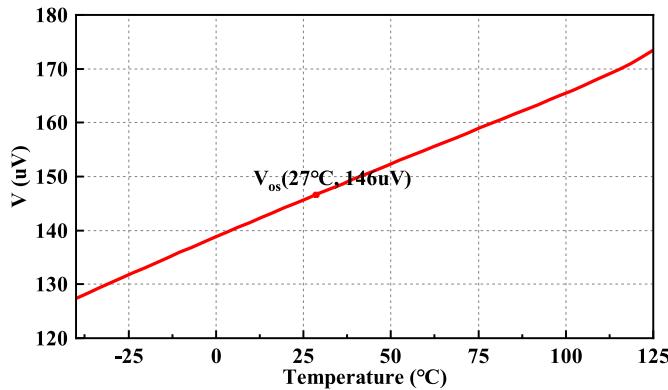


Fig. 9. Simulated open-loop gain and phase of circuit in Fig. 7.

Fig. 10. Simulated V_{os} with temperature sweep of circuit in Fig. 7.

to ensure low input referred noise.

The input noise of the proposed op amp is shown in Fig. 12. It can be seen that the input noise varies from $1.09\text{nV}/\sqrt{\text{Hz}}$ to $1.83\mu\text{V}/\sqrt{\text{Hz}}$ over the entire frequency range, within a reasonable range.

The dominant pole of the circuit is located at the output port. The product of equivalent impedance and capacitance is large, so the position of the pole is close to the DC point. And the non-dominant pole of the circuit is located at the node between the drain of M_{43} and the source of M_{44} , and the other pole is located between the source of M_{45} and the drain of M_{46} . The output impedance and parasitic capacitance of these two nodes are both small so that their poles are far from the dominant

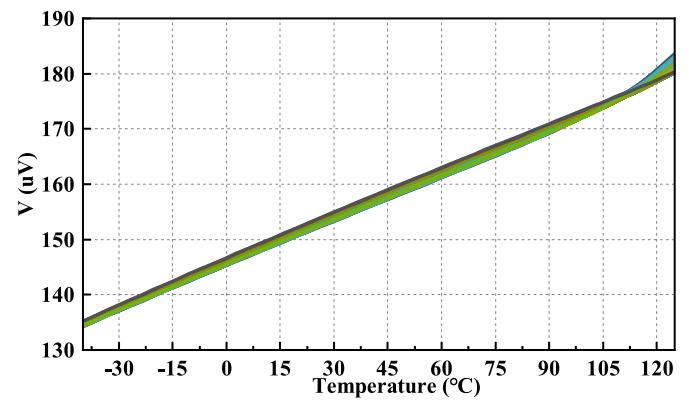
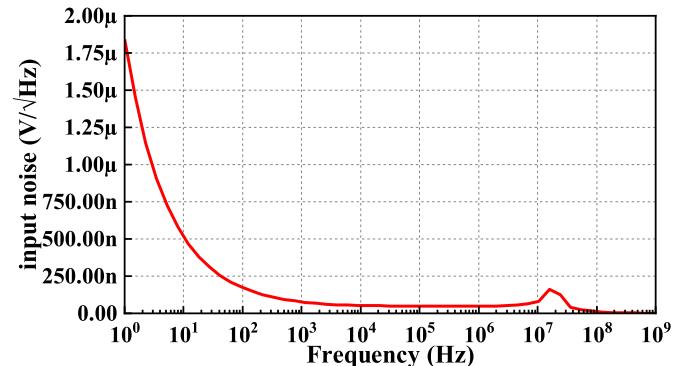
Fig. 11. Monte-Carlo simulation (300 iterations) of V_{os} with temperature sweep of circuit in Fig. 7.

Fig. 12. Simulated input noise of circuit in Fig. 7.

pole. So this circuit can be regarded as only one pole approximately and maintained stable through simple compensation.

4.2. Temperature characteristics

The temperature stability of the proposed BGR circuit is simulated over a temperature range from -40 to 125 °C. With a supply voltage of 3.3V, the output current reference I_{REF} is presented in Fig. 13. As the temperature increases, the curve of I_{REF} exhibits a peak and a trough, which is in agreement with the characteristic of high-order compensation and minimizes the variation in the output reference current.

The equation of TC can be expressed as

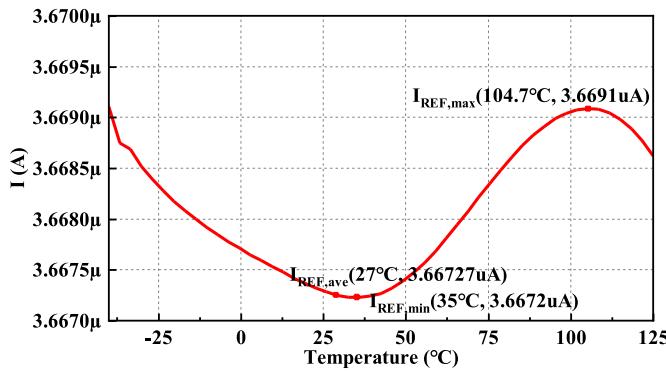


Fig. 13. Simulated I_{REF} with temperature sweep of circuit in Fig. 8.

$$TC = \frac{I_{\text{REF},\text{max}} - I_{\text{REF},\text{min}}}{I_{\text{REF},\text{ave}} \times (T_{\text{max}} - T_{\text{min}})} \times 10^6 \quad (13)$$

The fluctuation of I_{REF} over the whole temperature range is about 2 nA, varying from 3.6672 μA at 35 °C to 3.6691 μA at 104.7 °C exactly. So the TC can be calculated as 3.14 ppm/°C using (13).

A fixed high-precision $V_{\text{REF}1}$ can also be generated inside the BGR core circuit. The output I_{REF} can be converted into $V_{\text{REF}1}$ based on the demand for voltage of the subsequent circuit, which is more convenient for application. After obtaining I_{REF} , resistance with positive and negative TC can be combined in a certain proportion to counteract the temperature effect, resulting in resistance with a very low TC. As shown in Fig. 14, the output $V_{\text{REF}1}$ of approximately 833 mV is provided. Other precise reference voltages can also be generated by this way.

And when replacing the BGR core in Fig. 8 with the structure in Fig. 5, the I_{REF} simulation results are shown in Fig. 15.

According to equation (13), its TC is 4.96 ppm/°C, which can be seen that after the proposed high-order compensation, the stability of I_{REF} is better and the variation is smaller.

Monte-Carlo simulation is conducted to assess the circuit stability due to the influence of process and mismatch variations. 1000 iterations of the generated I_{REF} over a wide temperature range of 165 °C are shown in Fig. 16(a). The simulation results show that I_{REF} varies from 3.666 μA to 3.6753 μA under the worst case scenario. Fig. 16(b) presents the statistic distribution of TCs from 1000 iterations of Monte-Carlo simulations. By calculation, it can be concluded that the mean value μ of TC is 4.182 ppm/°C, and the standard deviation σ is 1.417 ppm/°C.

Fig. 17 shows the simulation results of I_{REF} versus temperature range of process corners including ff,fs,sf and ss. The maximum fluctuation between ff and ss is 9 nA. At the worst process corner ff, the TC is about 12.04 ppm/°C.

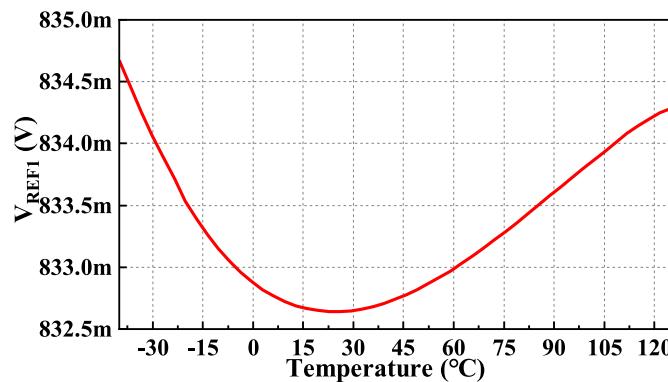


Fig. 14. Simulated $V_{\text{REF}1}$ with temperature sweep of circuit in Fig. 8.

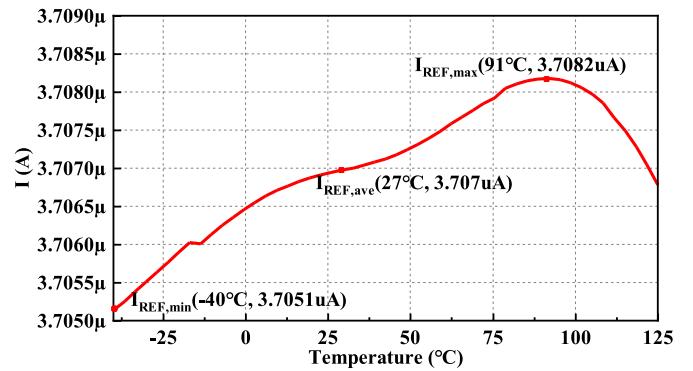


Fig. 15. Simulated I_{REF} with temperature sweep of the circuit that the BGR core in Fig. 8 is replaced with the structure in Fig. 5.

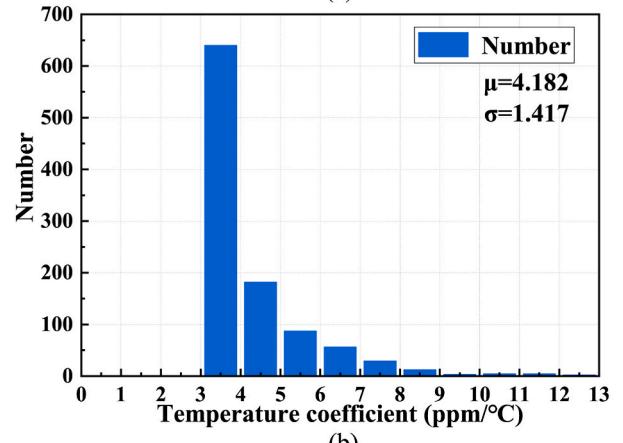
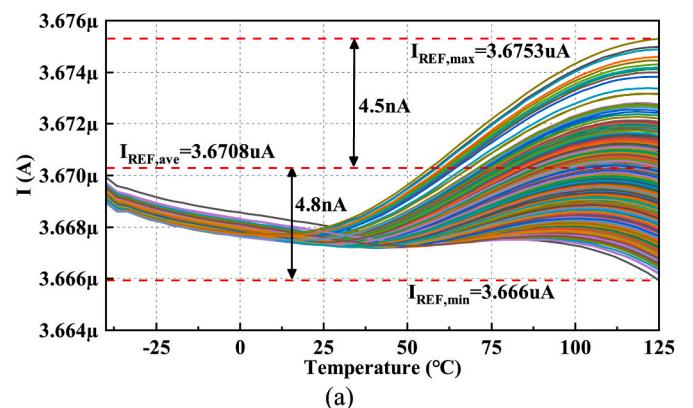


Fig. 16. Monte-Carlo simulation (1000 iterations) of I_{REF} across temperature.

4.3. Transient response

Fig. 18 illustrates the start-up process of proposed GBSR and BGR circuit with a supply voltage V_{DD} swept from 0V to 3.3V.

The power-on time of V_{DD} is equal to 1 ms. Firstly, make transistor M_2 conductive. The branch where M_5 is located is turned off due to the cutoff of M_6 . The current mirrored by M_4 is much smaller than the current flowing in M_2 , so V_{REG} is charged to a voltage slightly smaller than V_{DD} . When designing the GBSR circuit, the mirrored current obtained from M_2 is greater than the current required by BGR, with a certain margin left, so that BGR circuit can obtain a higher power supply voltage and start up safely.

When the BGR circuit successfully establishes a stable operation point, It takes around 1.3 ms for the BGR circuit to successfully reach a

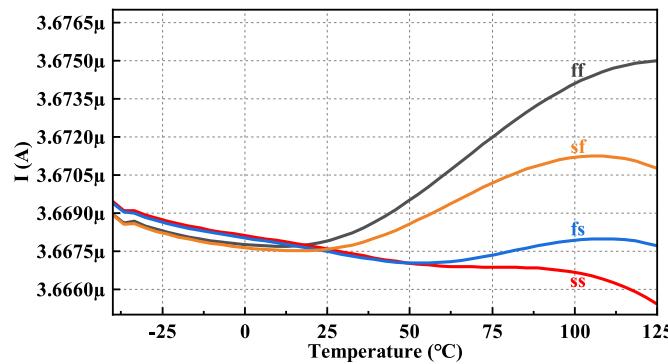


Fig. 17. The simulation results of I_{REF} versus temperature range of process corners including ff,fs,f_s and ss.

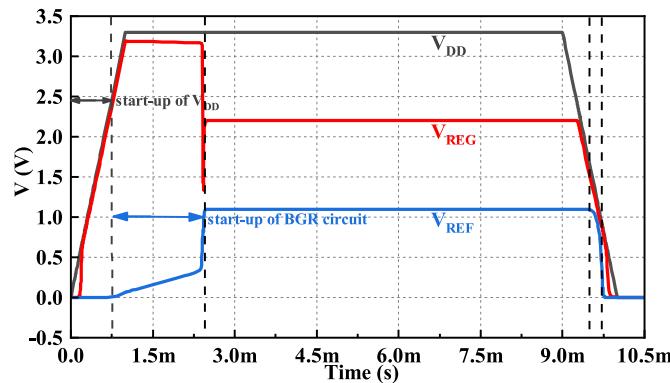


Fig. 18. The transient response of start-up and power-down process.

stable operation point, and then, the V_{BGROK} signal as presented in Fig. 8 is returned to the GBSR circuit, which makes M_6 turns on. Loop₂ where M_5 is located starts working, outputting the set V_{REG} which is twice the V_{REF} . The entire circuit reaches its normal operating state in approximately 2.3 ms.

Finally, V_{DD} decreases from 3.3 to 0 V within 1 ms during the power-down process at 9 ms. It can be seen that when the V_{DD} drops to 2.45V, V_{REG} begins to decrease slowly. At this time, the GBSR and BGR circuits can still operate normally. As V_{DD} continues to decrease, the circuit enters an abnormal state. V_{REF} can still maintain relatively stable performance till V_{DD} drops to 1.42V and V_{REG} is 1.31V. Until V_{DD} drops to 0.65 V, V_{REG} decreases vertically, the GBSR circuit is cutoff, and V_{REF} rapidly drops to 0V within 0.19 ms. The whole circuit turns off safely.

4.4. Stability

Due to the source follower structure of Loop₁, the main pole is at the drain output of M_2 , and compensation is only needed for EA and the BGR core circuit. There are many methods for frequency compensation. In this paper, M_8 used as capacity is adopted to connect the output terminal of the op amp A_1 to V_{REG} . Meanwhile, op amps A_2 and A_3 used to generate nonlinear currents rely on M_{14} and M_{21} used as Miller capacitors as compensation methods to ensure the stability of the two regulators, so that the entire system is stable too.

Fig. 19 shows AC analysis results of the proposed circuit in Fig. 8 for the gain and phase frequency response. It can be observed that the phase margin is better than 96.9° and the gain margin is about 18.5 dB. When the gain is 0 dB, the phase margin is much greater than 60° , which verifies the stability of the system.

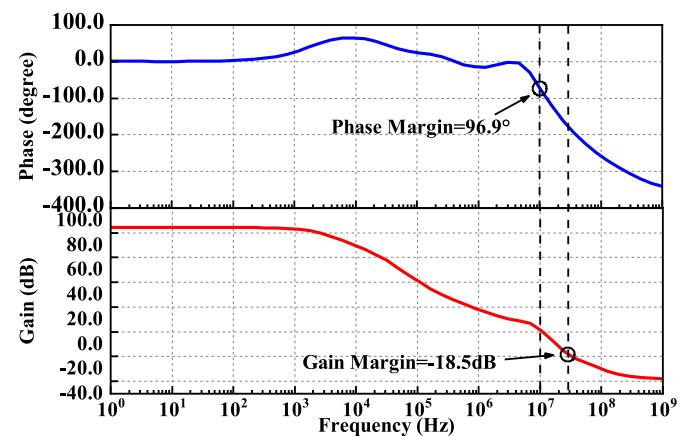


Fig. 19. The simulated results of gain and phase frequency response of the proposed circuit in Fig.8.

4.5. PSR

The proposed BGR circuit is powered by a bootstrap and self-regulated circuit. It is necessary to ensure that the self-regulated circuit has a high PSR in order to achieve a high PSR in the BGR circuit. Fig. 20 shows the PSR of the entire circuit, which is simulated from 1Hz to 1 GHz.

The PSR performance of GBSR circuit represented in red is about -99dB @DC, -49.55 dB @1 MHz and -25.3 dB @10 MHz. The PSR performance of BGR circuit represented in blue achieves -101.3 dB @DC, -60.23 dB @1 MHz and -55.6 dB @10 MHz. It can be seen that the PSR of the BGR circuit with V_{REG} as the power supply voltage has significantly improved.

The PSR simulated results of GBSR circuit and BGR circuit with temperature sweep are shown in Fig. 21. It can be seen that the variation of PSR at the same frequency over the whole temperature range is small.

The results of the 1000 iterations of Monte-Carlo analysis for mismatch and process variations are shown in Fig. 22, which ensures that the product yield of this parameter is more than 38 which means that the product yield can reach over 99 %.

The difference between the worst and best case scenario of the GBSR structure is 1.663 dB, and the difference between the worst and best case scenario of the BGR circuit is 1.474 dB, deviations are thus within a reasonable range.

4.6. Line regulation

Line regulation is also one of the key performances, which shows the robustness of the proposed PSR enhancement circuit under different supply voltage. Fig. 23 shows the simulated results of line regulation of

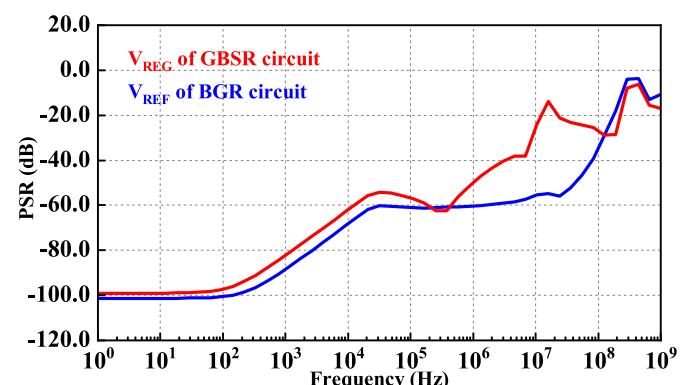


Fig. 20. PSR simulation results of GBSR and BGR circuit.

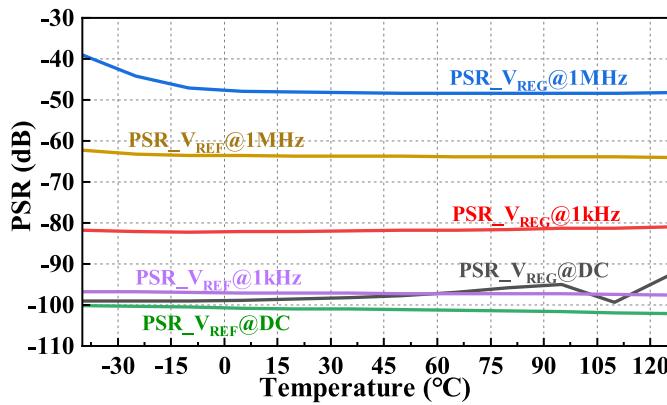


Fig. 21. PSR at different frequency over the whole temperature simulation results of GBSR and BGR circuit.

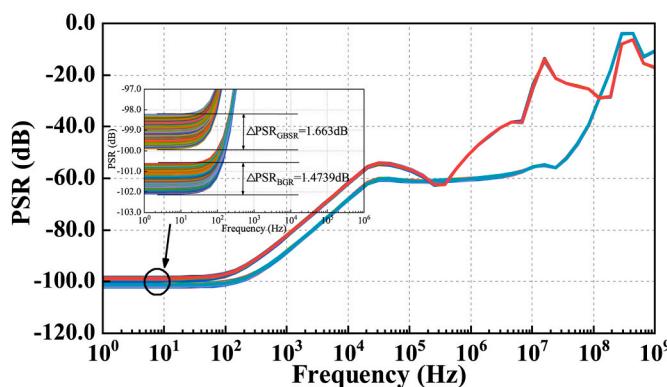


Fig. 22. Monte-Carlo simulation (1000 iterations) of PSR simulation results of GBSR and BGR circuit.

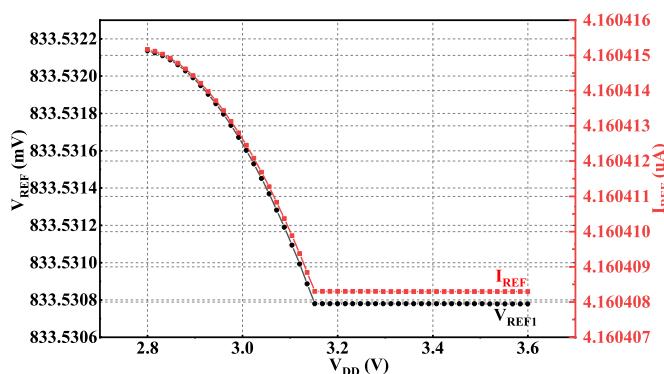


Fig. 23. The simulated results of line regulation of I_{REF} and V_{REF} .

I_{REF} and V_{REF} over a supply voltage from 2.8V to 3.6V.

It can be seen that I_{REF} varies from 4.160408 μ A to 4.160415 μ A and V_{REF} varies from 833.5308 mV to 833.5321 mV. By calculation, the line regulation can be obtained to be 0.000155 %/V.

Table 2 summarizes the circuit performance in comparison with other BGR circuits recently reported in the literature. It can be observed that among other structures, although this work has some concessions in terms of silicon area and quiescent current, it achieves a very good TC and a high PSR. It demonstrates an excellent insensitivity to the variations of temperature and supply voltage.

4.7. Post-layout simulations

Fig. 24 shows the layout of the proposed structure including the part of the BGR core with high-precision nonlinear current compensation circuit and the GBSR circuit in this paper which occupies 0.0992 mm² (including unmarked dummy devices) in SMIC 55 nm CMOS process. The results of the post-layout simulations are shown in Table 3.

5. Conclusion

In this paper, a high PSR and high-precision current-mode bandgap reference system has been designed and simulated in SMIC CMOS 55 nm process. In order to ensure successful fabricating, simulations of every process corner, Monte Carlo simulations and post-layout simulations have been conducted and the results are good. The simulation results verify that proposed SR structure can work reliably at power-on, the output I_{REF} with a good temperature-independence ($TC \approx 3.14$ ppm/°C) with a supply voltage of 3.3V and power supply rejection ability ($PSR \approx -101.3$ dB@DC, -60.23 dB@1MHz and -55.6 dB@10MHz). These results display an effective enhancement in the performance of the BGR circuit.

Data availability

Data will be made available on request.

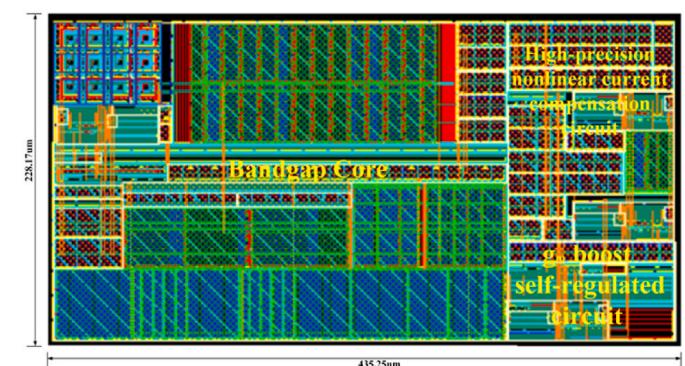


Fig. 24. Layout of the proposed GBSR and BGR circuits.

Table 2
Performance summary and comparisons with other previous works.

Specification	This work	[20]	[25]	[26]	[27]	[28]	[29]	[30]
Year	2023	2018	2020	2021	2021	2021	2021	2021
Process	CMOS 55 nm	CMOS 180 nm	CMOS 65 nm	CMOS 45 nm	CMOS 45 nm	CMOS 28 nm	CMOS 65 nm	CMOS 65 nm
Silicon area (mm ²)	0.0992	0.2225	0.0522	0.0779	0.09204	0.00369	N/A	0.033
Supply voltage (V)	3.3	3.5–5	0.5	1.05	1.05	1	0.95–1.2	1.0–1.4
Temp range (°C)	-40 to 125	-40 to 130	-40 to 120	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 100
TC (ppm/°C)	3.14	6.3	42	24.4	22.7	18.4	25	5
I_Q (μ A)	55.4	108	0.072	7.2	11.8	54.6	82	5.2
PSR (dB)	-101.3 dB@DC	-92dB@DC	-50dB@DC	-60dB@DC	-55dB@DC	-17dB	N/A	-91dB@DC

Table 3
Post-layout simulations of this work.

Specification	Parameter
Process	CMOS 55 nm
Supply voltage (V)	3.3
Temp range (°C)	-40 to 125
DC Gain (dB)	76.34
UGF (MHz)	10.5
Phase Margin (degree)	101.02
Module	BGR
TC (ppm/°C)	5.87
I_Q (μ A)	46.772
PSR (dB)	-108.3dB@DC -79.3dB@10kHz -70.4@10MHz
	GBSR 5.01 14.227 -107.3dB@DC -78.8dB@10kHz -28.1@10MHz

Declaration of competing interest

We declare that we have no financial and personal relationships with other people or organizations that can inappropriately influence our work, there is no professional or other personal interest of any nature or kind in any product, service and/or company that could be construed as influencing the position presented in, or the review of, the manuscript entitled.

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