DESIGN OF A BANDGAP VOLTAGE REFERENCE IN A 28 NM CMOS PROCESS

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Degree work presented as a requirement to qualify for the title of Electronic Engineer

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This work not only reflects the academic effort but also the unwavering love and support I have received from each of you. Each page is the result of your valuable contributions, and therefore, this achievement is as much yours as it is mine.

With love and deep gratitude,

- Jeison Herney Acevedo Velasquez

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Finally and most importantly, I would like to thank my family. Their unconditional support has been the engine that has driven me forward, and I am immensely grateful to have them by my side.

With appreciation,
- Eduardo Caballero Barajas

Dedicated to our families and friends.

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RESUMEN

TÍTULO: DISEÑO DE UNA REFERENCIA DE VOLTAJE BANDGAP EN UN PROCESO CMOS DE 28 NM [*]

AUTORES: EDUARDO CABALLERO BARAJAS
JEISON HERNEY ACEVEDO VELASQUEZ [**]

PALABRAS CLAVE: BANDGAP, CMOS, REFERENCIA DE VOLTAJE, PTAT, CTAT SoC.

DESCRIPCIÓN:
En el grupo de investigación Onchip se han fabricado en los últimos cinco años tres generaciones de SoC en un proceso CMOS de 180 nm. La nueva familia de microcontroladores que está desarrollando OnChip se implementará en un nodo de proceso CMOS más avanzado, concretamente en 28 nm. Esto implica nuevos desafíos en el diseño de bloques analógicos y digitales. La integración de bloques como LDO, ADC/DAC, comparadores, DC/DC y muchos más bloques requiere una referencia de voltaje estable y constante. Si la referencia de voltaje varía con el proceso, temperatura, carga, etc, el desempeño de todos los bloques dependientes, y consecuentemente el desempeño de todo el sistema, se verá comprometido. Por lo tanto, el diseño de una fuente de referencia de voltaje bandgap (BGR) es esencial para cualquier SoC, ya que el principio de funcionamiento detrás de este bloque le permite entregar un voltaje constante, cercano a la energía de banda prohibida del silicio, que es en gran medida independiente de las variaciones de PVT cuando adecuadamente diseñado. Esta es la razón por la que este bloque se diseñará en el microcontrolador, que será desarrollado por Onchip.

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[*] Trabajo de Grado

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ABSTRACT

TITLE: DESIGN OF A BANDGAP VOLTAGE REFERENCE IN A 28 NM CMOS PROCESS [*]

AUTHORS: EDUARDO CABALLERO BARAJAS
JEISON HERNEY ACEVEDO VELASQUEZ [**]

KEYWORDS: BANDGAP, CMOS, REFERENCE VOLTAGE, PTAT, CTAT, SOC.

DESCRIPTION:

In the Onchip research group, three generations of SoCs have been manufactured in a 180nm CMOS process over the last five years. The new family of microcontrollers that OnChip is developing will be implemented in a more advanced CMOS process node, concretely in 28 nm. This implies new challenges in the design of analog and digital blocks. The integration of blocks like LDOs, ADCs/DACs, comparators, DC/DCs, and many more blocks, requires a stable and constant voltage reference. If the voltage reference varies with the process, temperature, load, etc, the performance of all the dependent blocks, and conse- quently the performance of the entire system, will be compromised. Therefore, the design of a Bandgap voltage reference source (BGR) is essential to any SoC, since the working principle behind this block allows it to deliver a constant voltage, close to the bandgap energy of silicon, which is largely independent of PVT variations when properly designed. This is the reason why this block will be designed into the microcontroller, which will be developed by Onchip.

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[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor:SERGIO ANDRES RUEDA GOMEZ

INTRODUCTION

Integrated circuit technology is constantly evolving with the miniaturization of devices and the improvement in energy efficiency. In the era of high-speed, low-power electronics, the design of a stable and accurate voltage reference has become essential in the implementation of integrated circuits, especially in systems-on-chip (SoC).

Constant DC voltages that change minimally with the process, voltage, and temperature (PVT) are widely used in analog, digital, and mixed-signal circuits which require a fixed reference voltage to ensure reliability and accuracy. For instance, an ADC requires a stable voltage reference to achieve a high conversion accuracy, which is which is independent of the supply voltage. The fluctuations in the supply voltage, the processes, and the temperature variations are the main factors that affect the operation of the circuits, and especially in the integrated circuits it is a great challenge of design. Taking into account that the bias or reference voltage is a critical factor for a circuit, the design of a bandgap is essential for the operation of the other blocks in the system.

In this project, a bandgap voltage reference is designed in the 28 nm CMOS process, in order to achieve optimal stability and precision while meeting the design restrictions, for this, the design techniques and existing circuits in the literature will be investigated, and with a defined design strategy, the circuit and the layout are made, and later the results obtained will be compared. The project will also include a design methodology and analysis of critical performance factors in the 28 nm CMOS process and techniques to improve stability and precision.

This research work contributes to the development of future projects related to reference voltages or the design of integrated circuits through the methodology used, with

this it seeks to benefit designers of integrated circuits, students, and professors of the UIS. On the other hand, this project is expected to contribute to the development of the new family of microcontrollers in which the Onchip research group is working.

1. PROJECT OVERVIEW

1.1. MOTIVATION AND OBJECTIVES

The research project has dual objectives: research-driven objectives and personal aspirations. The research objective is to address a power management challenge by developing a high accuracy voltage reference circuit. In today's rapidly advancing technological landscape, the demand for reliable and accurate reference systems continues to grow, requiring innovative solutions.

This project offers a valuable chance to acquire hands-on experience in analog circuit design and establish the groundwork for enhancing technical skills. It serves as a vital accomplishment in personal and professional development in the integrated circuit field.

This project aims to design a bandgap voltage reference for a 28 nm CMOS process System-on-Chip (SoC). The project includes the selection of an architecture based on a state-of-the-art study, the design of the BGR block, its layout, and the verification of circuit performance.

1.2. BASIC OPERATING PRINCIPLE

A Bandgap Reference (BGR) is an integrated analog circuit designed to provide a constant output voltage reference that remains independent of various parameters such as temperature, supply voltage, and process variations (PVT), as shown in Fig 1. The voltage reference circuit is theoretically designed to produce an output voltage equivalent to the bandgap energy of the semiconductor material used. In this particular case, this is the energy differential between the conduction band and the valence band of

silicon, which is approximately 1.20 V[1].

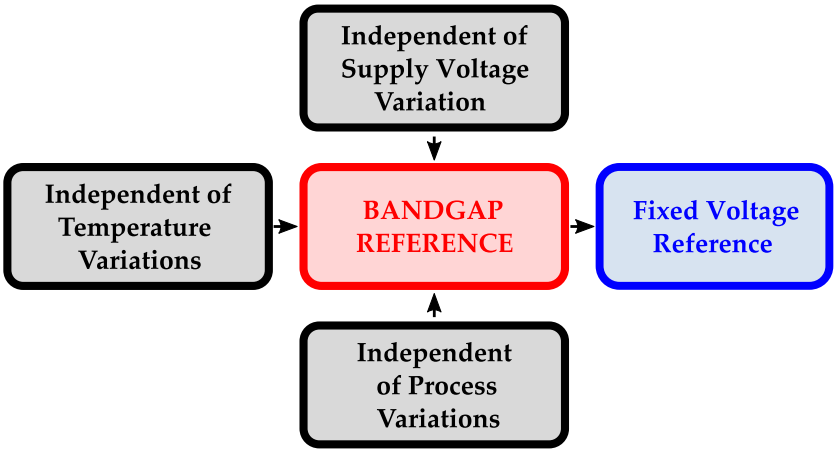

Figure 1. Block diagram of BGR.

A fundamental operational approach to generate a voltage value that remains constant with temperature is combining two electric signals: one that increases with temperature (TC $>$0) and another that exhibits the opposite behavior (TC $<$ 0). This combination is designed so that the resulting reference voltage is not affected by temperature variations, as illustrated in Fig 2. The signal with a negative Temperature Coefficient (TC) is called Complementary to Absolute Temperature (CTAT), while the signal with a positive TC is called Proportional to Absolute Temperature (PTAT).

The CTAT voltage could be generated by using the base-emitter junction of bipolar transistors, While the PTAT voltage could be derived from the difference between two CTAT voltages operating at different current densities. To compensate for the influence of the CTAT voltage, it is necessary to scale it by a constant factor *M*, as shown in Fig. 2.

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[1] Shivang PATEL and Amisha NAIK. "Design of Start-up Enabled Bandgap Voltage Reference". In: *2022 6th International Conference on Devices, Circuits and Systems (ICDCS)*. 2022, pp. 18–22. DOI: 10.1109/ICDCS54290.2022.9780858.

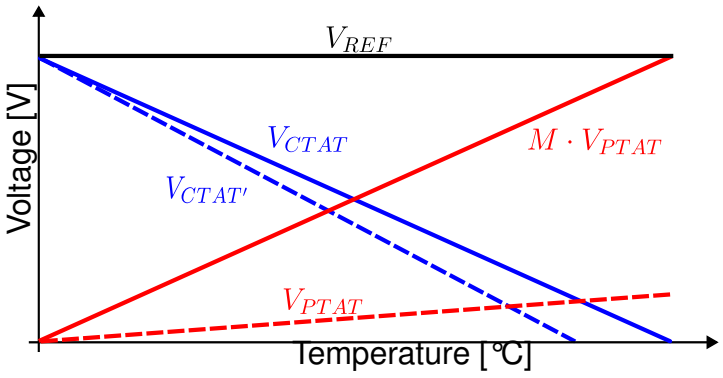

Figure 2. Principle of BGR.

Where:

$$V_{REF} = V_{CTAT} + M \cdot V_{PTAT} \tag{1}$$

Differentiating Eq. (1) with respect to the temperature yields

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{CTAT}}{\partial T} + M \cdot \frac{\partial V_{PTAT}}{\partial T} = 0 \tag{2}$$

And

$$M = -\frac{\partial V_{CTAT}}{\partial T} \Big/ \frac{\partial V_{PTAT}}{\partial T} \tag{3}$$

Nevertheless, it's important to note that the CTAT voltage generated by a bipolar transistor has a non-linear relationship with temperature. As a result, the described approach attempts to compensate for the linear terms, while the higher order terms represent some curvature of the resulting reference, resulting in a near-zero temperature coefficient (TC) over a wide range of temperatures, accompanied by an associated compensation error called the curvature error. This issue will be addressed and discussed in detail in later chapters.

1.3. PERFORMANCE MEASURES

A voltage reference should not only remain stable over temperature variations but also under transient conditions. This means that the output remains stable due to supply voltage variations and load noise. Consequently, a voltage reference circuit should have static and dynamic performance characteristics to meet the requirements.

1.3.1. Temperature Coefficient The temperature coefficient is the sensitivity of the circuit to temperature and specifies the drift of the reference voltage over a given operating range.

$$[h]TC = \frac{V_{refMAX} - V_{refMIN}}{V_{refAVG} \cdot (T_{MAX} - T_{MIN})} \cdot 10^6 \ \ [ppm/^\circ\mathrm{C}] \tag{4}$$

1.3.2. PSR The ability of the BGR to reject noise at a given frequency on the power rail is referred to as power supply rejection and is expressed by the following definition:

$$[h]PSR = 20 \cdot log\left(\frac{V_{REF}(f)}{V_{DD}(f)}\right) \ \ [dB] \tag{5}$$

1.3.3. Output Noise Low noise references are essential in high-resolution systems to maintain accuracy. In this context, the bandgap reference (BGR) has been specifically designed for a Successive Approximation Register Analog-to-Digital converter (SAR ADC).

White noise is fundamentally statistical, this means that it typically follows a probability distribution, which may include but is not limited to, the Gaussian distribution. It is therefore necessary to establish a relationship between a given noise spectral density and an equivalent peak-to-peak noise within the relevant bandwidth. To ensure the necessary precision, the peak-to-peak value must be lower than half of the Least Sig-

nificant Bit (LSB)[2]. The noise signal maintains a mean value of zero, and then the Root Mean Square (RMS) and standard deviation values are equivalent, as illustrated in Fig 3. In statistical terms, a 6.6RMS value corresponds to 99.9% of the total samples, while a 6RMS value represents 99.7% of the samples.

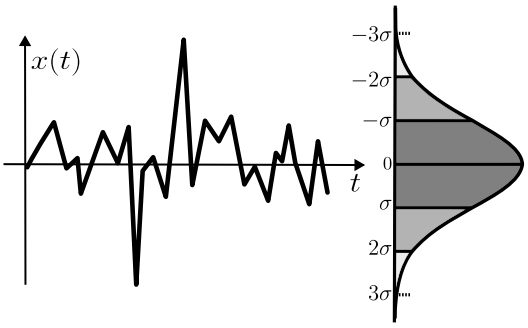

Figure 3. Normal noise distribution.

Assuming the peak-to-peak noise to 6(RMS), then, for an N-bit system with a full-scale reference voltage represented as V_{REF}, the required noise voltage can be expressed as follows:

$$[h]V_N \leq \frac{V_{REF}}{6 \cdot 2 \cdot 2^N} \ [V_{RMS}] \tag{6}$$

1.3.4. Stability To ensure stability in a BGR, it is necessary to establish a negative feedback loop with a phase margin typically set at 60°, a value generally considered optimal[3].

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[2] Walt JUNG, Walt KESTER, and James BRYANT. "SECTION 7-1 - Voltage References". In: *Data Conversion Handbook*. Ed. by Walt KESTER. Burlington: Newnes, 2005, pp. 443–464. DOI: https://doi.org/10.1016/B978-075067841-4/50028-2.

[3] B. RAZAVI. *Design of Analog CMOS Integrated Circuits*. 2nd. McGraw-Hill Education, 2017.

1.4. STATE OF THE ART

In the field of semiconductor technology, the search for an electric value that remains constant to temperature variations has driven researchers to explore the combination of two phenomena characterized by opposing Temperature Coefficients TCs. The pioneering work of Widlar in 1965[4] revealed the potential of base-emitter voltages from two transistors biased at different current densities, yielding a Proportional to Absolute Temperature (PTAT) difference. In 1971, he introduced the first bandgap circuit[5], marking a significant milestone.

In 1974, Brokaw presented an alternative topology,[6] using operational amplifiers (OPAMPs), which has since become a key component of many modern technologies. In 1978, a novel reference design emerged, notable for excluding bipolar devices[7]. This design employed NMOS transistors, which provided benefits such as reduced power consumption and layout area. However, it has been noted that the mismatch of MOS transistors can cause significant inaccuracies in these references.

Subsequent research has focused on the use of bipolar transistors within standard CMOS processes, with the aim of developing design techniques to reduce reference voltage variation. One study describes a curvature correction method that uses a sub-

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4 R. WIDLAR. "Some Circuit Design Techniques for Linear Integrated Circuits". In: *IEEE Transactions on Circuit Theory* 12.4 (1965), pp. 586–590. DOI: 10.1109/TCT.1965.1082512.

5 R.J. WIDLAR. "New developments in IC voltage regulators". In: *IEEE Journal of Solid-State Circuits* 6.1 (1971), pp. 2–7. DOI: 10.1109/JSSC.1971.1050151.

6 A.P. BROKAW. "A simple three-terminal IC bandgap reference". In: *IEEE Journal of Solid-State Circuits* 9.6 (1974), pp. 388–393. DOI: 10.1109/JSSC.1974.1050532.

7 R.A. BLAUSCHILD et al. "A new NMOS temperature-stable voltage reference". In: *IEEE Journal of Solid-State Circuits* 13.6 (1978), pp. 767–774. DOI: 10.1109/JSSC.1978.1052048.

threshold current generated by an NMOS transistor[8]. In addition, another work incorporates an optimized power supply rejection (PSR) stage that introduces supply-related noise into the bandgap loop to maintain a constant gate-source voltage in the upper current mirror[9].

Various architectural approaches have also been explored to achieve low noise performance, including the design of a switched capacitor amplifier with correlated double sampling techniques to reduce flicker noise[10], and the implementation of chopper stabilization techniques to mitigate offset and output noise[11] [12].
Simultaneously, a need has arisen for circuits capable of performing at low voltages, due to the decreasing supply voltages in new technologies. This has led to an increasing demand for generating reference voltages below the bandgap voltage[13].

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[8] Dalton COLOMBO et al. "Curvature correction method based on subthreshold currents for bandgap voltage references". In: *2012 IEEE 3rd Latin American Symposium on Circuits and Systems (LASCAS)*. 2012, pp. 1–4. DOI: 10.1109/LASCAS.2012.6180314.

[9] Wenguan LI, Ruohe YAO, and Lifang GUO. "A low power CMOS bandgap voltage reference with enhanced power supply rejection". In: *2009 IEEE 8th International Conference on ASIC*. 2009, pp. 300–304. DOI: 10.1109/ASICON.2009.5351450.

[10] A. N. LONGHITANO et al. "A compact low-noise fully differential bandgap voltage reference with intrinsic noise filtering". In: *2014 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*. 2014, pp. 1–4. DOI: 10.1109/PRIME.2014.6872687.

[11] Yuliang MA et al. "A Low Noise CMOS Bandgap Voltage Reference Using Chopper Stabilization Technique". In: *2020 IEEE 5th International Conference on Integrated Circuits and Microsystems (ICICM)*. 2020, pp. 184–187. DOI: 10.1109/ICICM50929.2020.9292198.

[12] Yueming JIANG and E.K.F. LEE. "A low voltage low 1/f noise CMOS bandgap reference". In: *2005 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2005, 3877–3880 Vol. 4. DOI: 10.1109/ISCAS.2005.1465477.

[13] H. BANBA et al. "A CMOS bandgap reference circuit with sub-1-V operation". In: *IEEE Journal of Solid-State Circuits* 34.5 (1999), pp. 670–674. DOI: 10.1109/4.760378.

1.5. DESIGN SPECIFICATIONS

The table below lists the key design specifications for the BGR. These specifications form the basis of the design process and guide the creation of a reference circuit that meets the identified performance criteria.

Table 1. Design specifications

Parameter	Min	Typ	Max
V_{REF} [V]		1.25	
TC [ppm/ $^{\circ}C$]			50
I_{VDD} [uA]			50
V_{NOISE} [uV_{RMS}]		125	
PSR @ DC [dB]		-60	
PSR_{MAX} [dB]			-30
V_{DD} [V]		1.8	
Area [mm^2]			0.026

2. BANDGAP CORE

2.1. BIPOLAR JUNCTION TRANSISTOR

Achieving a temperature-insensitive reference voltage starts by creating a controllable temperature-dependent one. The bipolar junction transistor (BJT) plays a crucial role in this task since it is often employed to generate temperature-dependent voltages. BJTs can be integrated into a typical CMOS process as parasitic elements and they are usually in a diode-connected setup. The BJT transistor's active region exhibits characteristics resembling the current-voltage relationship of a diode, particularly concerning the correlation between collector current and base-emitter voltage drop.[14]

$$I_C = I_S \left(\exp \left(\frac{V_{BE}}{V_T} \right) \right) \tag{7}$$

Here the saturation current is given by

$$I_S = \frac{q A_E n_i^2 \overline{D_p}}{W_B N_d} \tag{8}$$

Where A_E is the emitter area, and $\overline{D_p}$ is the average hole diffusivity constant in the base. The product of $W_B N_d$ is known as the Gummel number, which represents the number of impurities per unit area in the base [15].

Eq. (7) describes the voltage V_{BE} equation as follows.

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[14] Chi-Wah KOK and Wing-Shan TAM. *CMOS voltage references: an analytical and practical perspective*. John Wiley & Sons, 2012.

[15] Micheal AP PERTIJS and Johan HUIJSING. *Precision temperature sensors in CMOS technology*. Springer Science & Business Media, 2006.

$$V_{BE} = V_T \cdot \ln\left(\frac{I_C}{I_S}\right) \tag{9}$$

Where V_T represents the thermal voltage, it is equivalent to kT/q, where k is the Boltzmann constant, T is the absolute temperature in Kelvin, and q is the charge of an electron. Looking at Eq. (9), one might think that the base-emitter voltage of the transistor in a diode-connected configuration is proportional to absolute temperature. However, this is not the case because the term I_S exhibits a strong temperature dependence, resulting in a complementary characteristic, instead of a proportional one over a fixed range of temperatures.

In the work conducted in [16], an expression for V_{BE} is derived in Eq. (10), in which constant, linear, and higher-order terms are identified.

$$V_{BE} = \left\{V_{go} + (\eta - m)\frac{kT_r}{q}\right\} - \lambda T - \frac{1}{2}(\eta - m)\frac{kT_r}{q}\left(\frac{T - T_r}{T_r}\right)^2 \tag{10}$$

Where

$$\lambda = \frac{\left\{V_{go} + (\eta - m)\frac{kT_r}{q}\right\} - V_{BE}(T_r)}{T_r} \tag{11}$$

Writing V_{BE} in this form makes it easier to understand what goes into it. Here V_{go} is the extrapolated bandgap voltage at 0 Kelvin; $\eta = 4 - n$, where n is a constant depending on the concentration and profile of the transistor base, and thus n is a variable depending on the fabrication process. The value of m is obtained by assuming that the collector current is proportional to a power of the temperature, $I_C \propto T^m$.[16]

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[16] Guijie WANG. "CMOS bandgap references and temperature sensors and their applications". In: (2005).

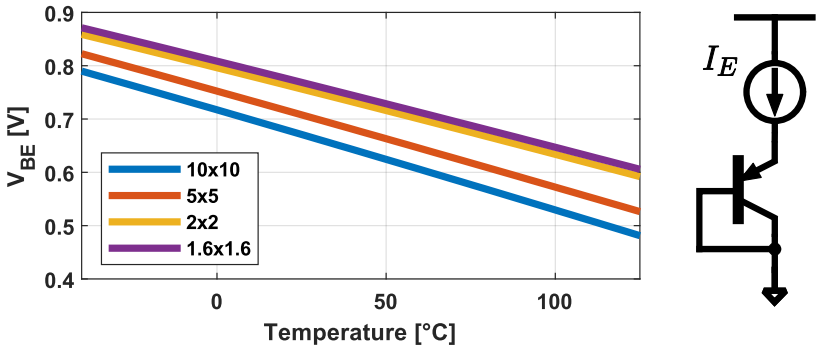

Figure 4. CTAT curves, voltage dependence V_{BE} for each of the transistors of the technology at a fixed current of $3[\mu A]$, the dimensions are given in $\mu m x \mu m$

As shown in Fig.4, in the temperature range of $[-45, 120]$ Celsius degrees, a compensation of the linear terms of V_{BE} in Eq.(10) will be performed in this work, specifically the linear dependence of a $2\mu m x 2\mu m$ PNP transistor at a reference temperature of 27 Celsius degrees, and the base-emitter voltage variation given by

$$\frac{\partial V_{BE}(T)}{\partial T} = -1.606[mV/K] \tag{12}$$

To compensate for higher-order terms, it is necessary to generate controllable electrical variables that are proportional to the type of compensation desired. However, this type of compensation is beyond the scope of this work.

2.1.1. PTAT generation Now, a reference voltage is desired, in this case, V_{go}, which corresponds to the bandgap voltage in silicon and is essentially a variable that does not depend on temperature or the manufacturing process. Therefore, in order to isolate this term from Eq.(9), it is necessary to generate a curve that compensates for the other linear terms in the expression.

Let's first look at the behavior of linear functions. If you have two negatively sloped

lines, one steeper than the other, and they share the same y-intercept point b, then taking the difference between them would result in a function that depends purely on the slopes of the lines, m_1 and m_2.

$$y_1 = -m_1 x + b; \quad y_2 = -m_2 x + b$$

$$y_3 = y_1 - y_2 = (m_2 - m_1)x \quad m_2 > m_1 \tag{13}$$

The resulting function, y_3, will be a function that increases with the variable x; where x is the temperature in this case. Note that this curve now starts from the origin, so that $y_3(0) = 0$.

Thus, to generate a function that increases with temperature, it is necessary to take the difference between two functions with different negative slopes. Bringing this analysis to circuits, given a current $N \cdot I_C$ passing through a BJT in diode-connected mode, it will result in a less steep slope compared to the same BJT with a current of I_C. This can be observed in Fig.5

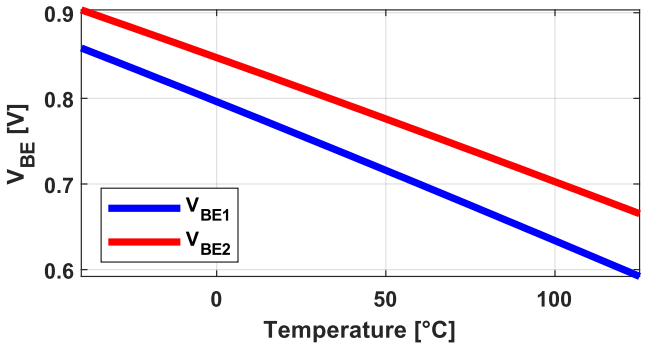

Figure 5. CTAT curves of a $2\mu m x 2\mu m$ BJT for different current densities

$$\frac{\partial V_{BE_1}}{\partial T_r} = -1.606[mV/K] \qquad \frac{\partial V_{BE_2}}{\partial T_r} = -1.432[mV/K] \tag{14}$$

Using the expression for V_{BE} from Eq. (9), we have

$$\Delta V_{BE_{1,2}} = V_{BE_2} - V_{BE_1} \tag{15}$$

$$\Delta V_{BE_{1,2}} = V_T \ln\left(\frac{NI_C}{I_S}\right) - V_T \ln\left(\frac{I_C}{I_S}\right) \tag{16}$$

$$\Delta V_{BE_{1,2}} = V_T \ln(N) \tag{17}$$

From the Eq.(17) results in a function ΔV_{BE}, in which the higher order terms have been canceled out, and it varies proportionally to the absolute temperature (PTAT), as can be seen in the Fig.6.

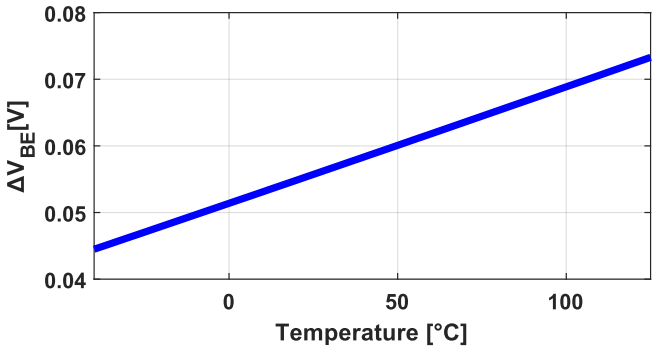

Figure 6. PTAT curve of ΔV_{BE} with respect to temperature

To generate the bandgap reference voltage, this PTAT curve obtained needs to be scaled by a factor M to compensate for the CTAT characteristic of the voltage V_{BE}.

2.1.2. BJT en el proceso CMOS The BJTs available in a CMOS manufacturing process are typically parasitic elements. In the TSMC 28nm technology node, only vertical bipolar transistors can be found, as shown in Fig. 7, where the collector is

formed by the substrate and is connected to the ground. This configuration limits the interconnections to only common-collector configurations [16]. Since these are parasitic elements, they often exhibit a significantly degraded current gain (β_F). This is primarily due to the depth of the base and the high doping levels used to create the n-well. [15]

$$\beta = \frac{I_C}{I_B} \tag{18}$$

Even though the manufacturing process is not optimized for BJT operation, these vertical transistors still exhibit good performance with respect to the current-voltage characteristic ($I_C - V_{BE}$)[16].

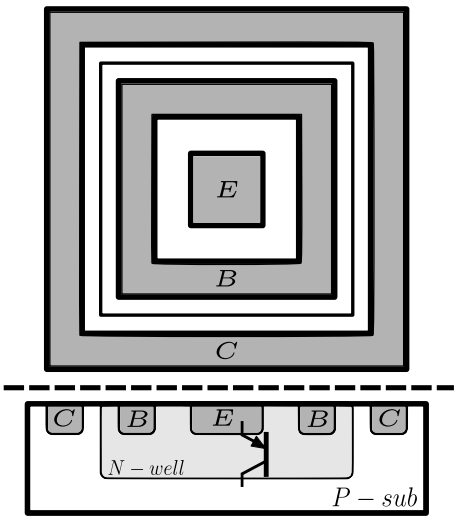

Figure 7. Top and cross-sectional view of a vertical BTJ in 28nm

2.1.3. IE - VBE Characteristics In the configuration in which the BJT transistor is connected as shown in Fig. 4, it can be observed that the collector current is not equal to the current entering through the emitter. This is because the common-base current-gain α_F is less than 1, which is a consequence of having a very small β_F. In the 28nm technology, the β_F of transistors can vary depending on the emitter size and typically falls within the range of $0.643 < \beta_F < 1.447$, see Fig. 8

As mentioned in [15], to have a well-defined collector current-emitter voltage characteristic, the parameter α_F should not vary within the range of bias currents being used, in other words, β_F should remain constant within this operating range.

$$I_C = \alpha_F I_E = \frac{\beta_F}{1+\beta_F} \cdot I_E \tag{19}$$

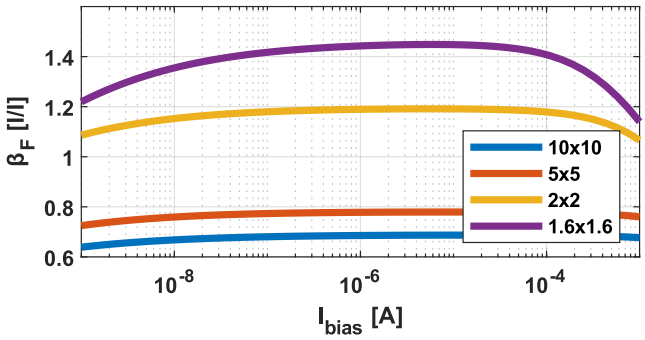

Figure 8. β_F of each transistor in the technology with respect to a bias current

2.2. MOSFET

Signal generators with CTAT characteristics can be obtained from a MOSFET transistor. Therefore, based on what was discussed in the previous section, it is possible to generate a PTAT signal using these devices.

For this type of operation, MOS devices should operate in subthreshold (weak inversion) mode. This condition is necessary because it is in this region that the drain current exhibits an exponential relationship with the gate-source voltage (V_{gs}). This behavior is similar to what was observed with BJTs, and it is required to derive the PTAT component [17].

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[17] A Rincon-Mora GABRIEL et al. “Voltage References, From Diodes to Precision High-Order Bandgap

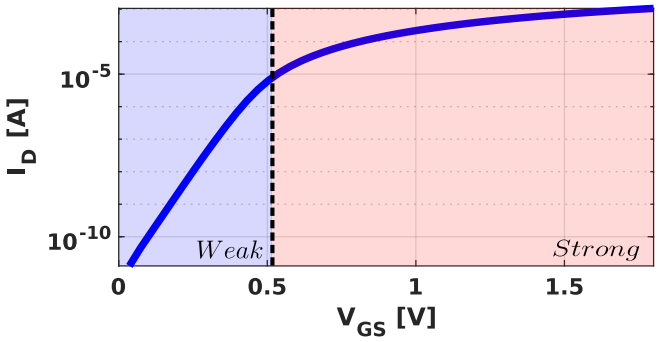


Figure 9. Semilog plot of I_D versus V_{GS} for a $1\mu m/1\mu m$ NMOS transistor

The equation describing the behavior of the MOSFET transistor in a diode configuration in subtreshold is given by:

$$I_D = \hat{I_{D,leak}} S \exp\left(\frac{V_{GS}}{\zeta_n V_T}\right) \tag{20}$$

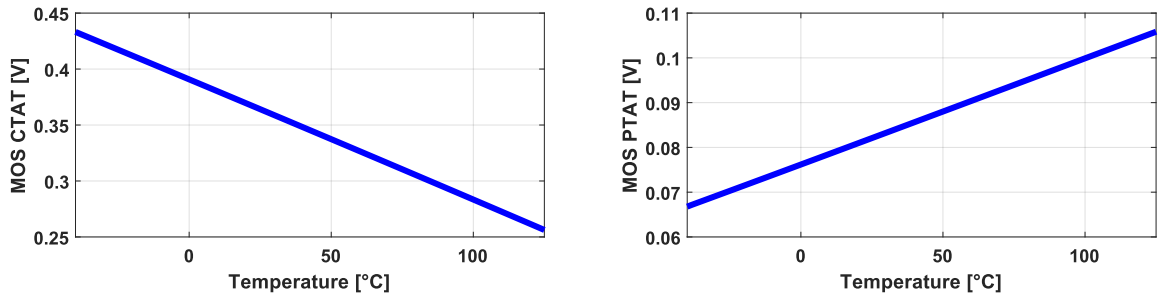
Where $I_{D,leak}$ is the drain-to-substrate leakage current. These leakage currents can be quite significant compared to the weak-inversion transistor current as the temperature increases[17]. This could pose a problem. S is the channel aspect ratio, defined as the ratio of channel width to channel length, W/L, and

$$\zeta = 1 + \frac{C_D}{C_{ox}} \tag{21}$$

is a non-ideality factor that depends on the depletion capacitance C_D and gate oxide capacitance C_{ox} in such a way that $1 < \zeta < 2$

Fig 10. presents the CTAT and PTAT curves of an NMOS transistor, as was done in section 2.1.1. The PTAT curve results from the difference between two CTAT components with different slopes. The bias current, in this case, is $50[nA]$, therefore the transistor is operating in the sub-threshold region.

Circuits". In: *Georgia Institute of Technology* (2002).



(a) (b)

Figure 10. CTAT and PTAT curves for a diode-connected NMOS transistor with $W/L = 1\mu m/1\mu m$

2.3. BJT VS MOSFET

In the selection of the devices that will be integrated into the bandgap core, BJT transistors were preferred over MOS devices. This is due to the fact that BJTs exhibit fewer variations in the manufacturing process and, importantly, do not exhibit significant voltage variations as MOSFET transistors do. This is due to MOSFETs having intrinsic matching issues.[14]

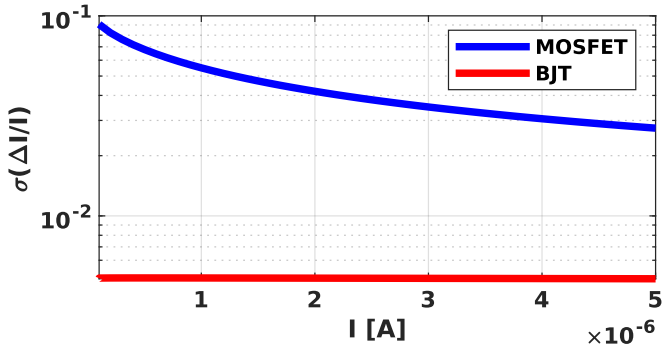


Figure 11. Matching versus I_{bias} for a $2\mu m/2\mu m$ BJT and a $8.2\mu m/2\mu m$ NMOS

MOS transistors that are designed exactly the same on a chip frequently exhibit discrepancies in device characteristics, such as threshold voltage and drain current, because of inconsistencies and random factors in the manufacturing process. These

disparities are typically classified as MOS transistor mismatch[18].

2.4. Bandgap Core

In section 2.1.1, we discussed how to generate a PTAT component. Now, let's explore how this translates to an electronic circuit. In Fig. 12, a typical topology for the core of the bandgap can be observed.

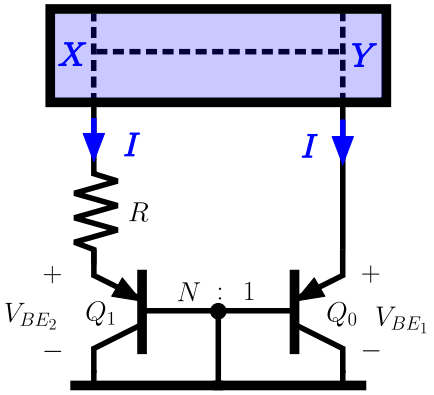


Figure 12. Bandgap core, with a black box

With Q_0 and Q_1, we obtain the CTAT components. Now, it is necessary for one slope to be steeper than the other. This is achieved by scaling Q_1 by a factor of N; this means that Q_1 is N times Q_0 transistor in parallel, such that the current passing through each of the transistors is I/N.

$$V_{BE_1} = V_T \ln\left(\frac{I}{I_S}\right) \qquad V_{BE_2} = V_T \ln\left(\frac{I}{NI_S}\right) \tag{22}$$

Once these slopes are obtained, the subtraction between them is achieved by taking the voltage difference across the resistor R. This implies that node X is equal to Y

[18] Qiang ZHANG et al. "SPICE modeling and quick estimation of MOSFET mismatch based on BSIM3 model and parametric tests". In: *IEEE Journal of Solid-State Circuits* 36.10 (2001), pp. 1592–1595.

resulting in a PTAT current.

$$\Delta V_{BE} = V_T \ln(N) \tag{23}$$

$$I = \frac{\Delta V_{BE}}{R} = \frac{V_T \ln(N)}{R} \tag{24}$$

For the bandgap core to perform correctly, two important aspects must be taken into account: Nodes X and Y must tend to the same value, and the currents I flowing through each branch must be equal.

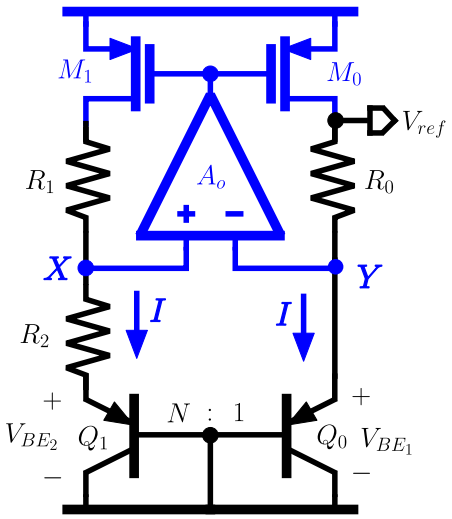


Figure 13. Bandgap core with the OPAMP and current mirrors

Given the conditions described above, the amplifier A_o will keep the voltages at nodes X and Y equal when operating in a negative feedback setup. This phenomenon is described in chapter 3.2. To generate the same current through each branch, PMOS transistors M_0 and M_1 are used, note that they have the same voltage drop V_{SG} and therefore generate the same current. A more detailed analysis of the use of these transistors as current mirrors can be found in the chapter 3.1.

Here the current I is given by

$$I = \frac{V_T \ln(N)}{R_2} \tag{25}$$

And V_{ref} will be

$$V_{ref} = IR_0 + V_{BE_1} \qquad V_{ref} = V_{BE_1} + \frac{R_0}{R_2} V_T \ln(N) \tag{26}$$

As was mentioned in Eq.(1), V_{ref} is composed by $V_{CTAT} = V_{BE_1}$, $V_{PTAT} = V_T \ln(N)$ and a factor $M = R_0/R_2$. Note that if resistors R_0 and R_1 are fabricated from the same material, the relationship between them will always remain constant as the temperature varies. This should be taken into account when selecting the resistors to be used.

3. CIRCUIT IMPLEMENTATION

This chapter covers everything related to the design process and the considerations made to meet each of the specifications given in section 1.5.

3.1. MIRRORS AND MATCHING

As discussed in the previous chapter, the currents that flow through each of the branches have to be equal, as presented in Fig 13, when this is not the case there will be a compensation error. Thus, it is important to understand the possible factors that would cause the currents to differ from each other.

3.1.1. Error due to finite output resistance One of the main error sources that can be identified is the mirroring error due to channel modulation, meaning that different values of V_{SD} will result in a greater or lesser current variation depending on the channel length of the transistor. The channel-length modulation coefficient λ is inversely proportional to L, therefore to lower the value of λ, L must be increased.

As observed in Fig.14(a). a transistor with a larger L will represent a smaller variation in current due to the variation in V_{SD}.

$$I_{SD} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG} - |V_{TH}|\right)^2\left(1 + \lambda V_{SD}\right) \tag{27}$$

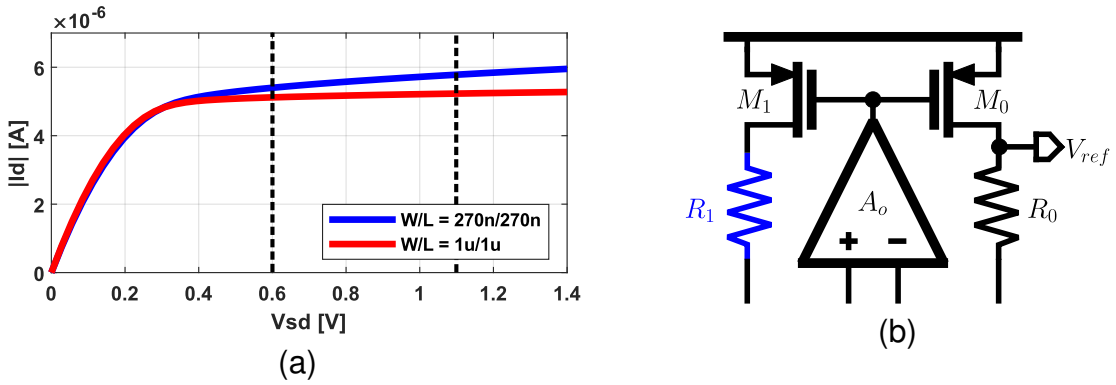


Figure 14. (a)$|I_d|$ against V_{sd}; (b) Upper section of the bandgap topology

In addition to a large L, R_1 was introduced to make the voltage drop V_{SD} seen by transistors M_0 and M_1 very similar, improving the mirroring.

3.1.2. Matching between devices The mismatch characteristics of closely spaced devices result from systematic and random variations in geometric and process parameters. The conventional strategy for mitigating the effects of random variation is to increase the area of the critical matching devices until the random mismatch effects are minimized to an acceptable level, in this case, the matching due to the BJTs presented in Fig. 11.

The experimental results shown in the state of the art indicate that variations in threshold voltage and current factor are the major causes of discrepancies in drain-source current or gate-source voltage for a matched pair of MOS transistors. These random variations follow a normal distribution with a mean of zero and a variance that depends on the device area[19]. The difference ΔV_T between the threshold voltages of a pair of

[19] Peter R KINGET. "Device mismatch and tradeoffs in the design of analog circuits". In: *IEEE Journal of Solid-State Circuits* 40.6 (2005), pp. 1212–1224.

MOS transistors is usually described as [20]:

$$\sigma_{\Delta V_T} = \frac{A_{V_T}}{\sqrt{WL}} \tag{28}$$

Where W is the gate width and L the gate length, and the proportional constant A_{V_T} is technology-dependent[19]. In Fig. 15 there is a common setup for the simulation of mismatch, here transistors M_0, M_1 and M_2 have a relation ratio $W/L = 1/1[\mu m/\mu m]$, where M_0 is fixed, this means that it does not present variation.

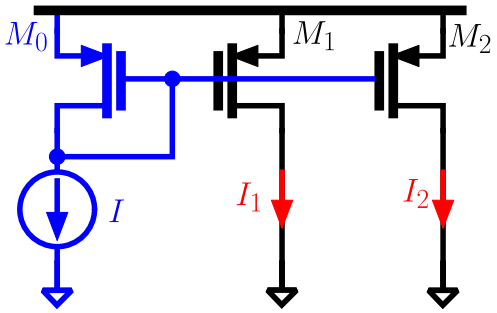


Figure 15. Setup for matching measurement

For a fixed current $I = 3[\mu A]$, thus $V_{ov} = 240[mV]$ the matching is plotted in Fig. 16 varying the dimensions W and L proportionally with a constant k such as:

$$\frac{W}{L} = \left(\frac{k \cdot W}{k \cdot L}\right) \tag{29}$$

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[20] Marcel JM PELGROM, Hans P TUINHOUT, and Maarten VERTREGT. "Transistor matching in analog CMOS applications". In: *International electron devices meeting 1998. technical digest (Cat. No. 98CH36217)*. IEEE. 1998, pp. 915–918.

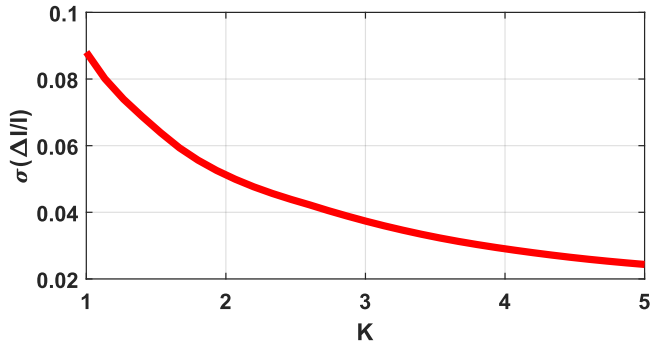

Figure 16. Matching plot against k

As can be seen, increasing the dimensions of the transistors improves the matching between them. This is also due to the larger L, resulting in a higher r_o, which reduces the error caused by finite impedance.

Furthermore, as mentioned at the beginning of the section, variations in threshold voltage are one of the main causes of errors in drain currents. When performing simulations in process corners and Monte Carlo analyses, the threshold voltage is one of the parameters that exhibit the most variation. Therefore, to have a lower variation in currents I_1 and I_2, the voltage V_{SG} should be much greater than the threshold voltage V_{th}. This can be easily observed in the quadratic equation for current.

$$I_{SD} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{SG} - |V_{th_p}|\right)^2 \tag{30}$$

Fig. 17 shows the improvement of the matching between the devices by increasing the overdrive voltage $V_{ov} = V_{SG} - |V_{th_p}|$ which is the same as making V_{SG} higher, this curve is made by sweeping the reference current I thus fixing the V_{SG} of the reference transistor M_0.

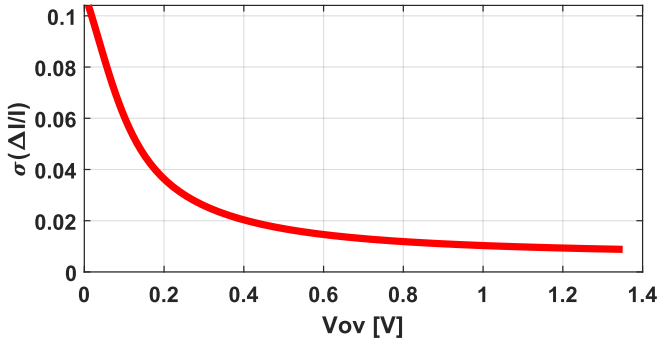

Figure 17. Mismatch against overdrive voltage

Thus, to improve the matching between the transistors in the current mirror, there are two ways to do it: by increasing the dimensions W and L, and ensuring that they have a higher overdrive voltage.

3.2. FEEDBACK

For the OPAMP-based BGR, two feedback loops, one negative and one positive, are presented as shown in Fig. 18(a), this could be simplified as shown in Fig. 18(b), where Ao is the gain of the OPAMP and $-\beta^-$ and $-\beta^+$ are the gains from the output of the OPAMP to its input terminals.
The negative feedback factor is given by:

$$\beta^- = g_m \left(\left[\frac{1}{g_{m_Q}} \parallel r_\pi \right] + R_2 \right) \tag{31}$$

Where g_m is the transconductance of $M_{0,1}$, g_{mQ} and r_π is the transconductance and input impedance respectively of $Q_{0,1}$. The positive feedback factor is given by:

$$\beta^+ = g_m \left[\frac{1}{g_{mQ}} \parallel r_\pi \right] \tag{32}$$

For stability analysis, $\beta^- > \beta^+$ is required, and this criterion is satisfied by the above

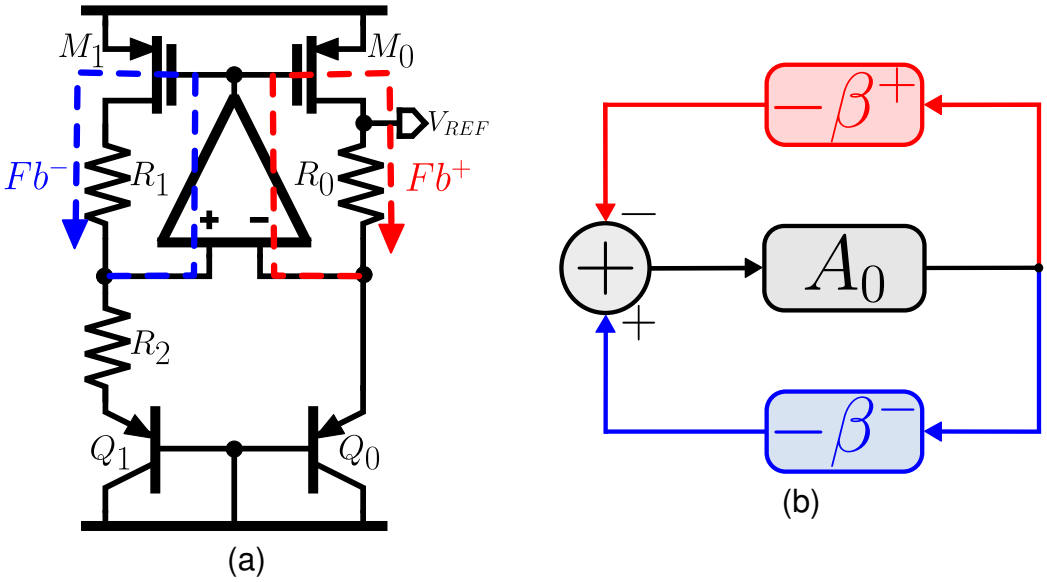

Figure 18. (a) Feedback loops; (b) Block diagram

two relations.

As mentioned, the drain of M_0 and M_1 are at the same voltage, however, the voltage reference should be taken in the positive feedback loop, because with a capacitor in the output, the positive feedback loop then has an even lower gain at high frequencies, satisfying $\beta^- > \beta^+$.

To see this phenomenon a capacitor is added in the positive and negative loop, and the loop gain is measured as shown in Fig 19.
Where the magnitude of the total loop gain at low frequencies is given by:

$$\mid LG \mid = A_0(\beta^- - \beta^+) \tag{33}$$

$$\mid LG \mid = A_0 \cdot g_m \cdot R_2 \tag{34}$$

Stability can be evaluated by varying VDD over time and analyzing the output response

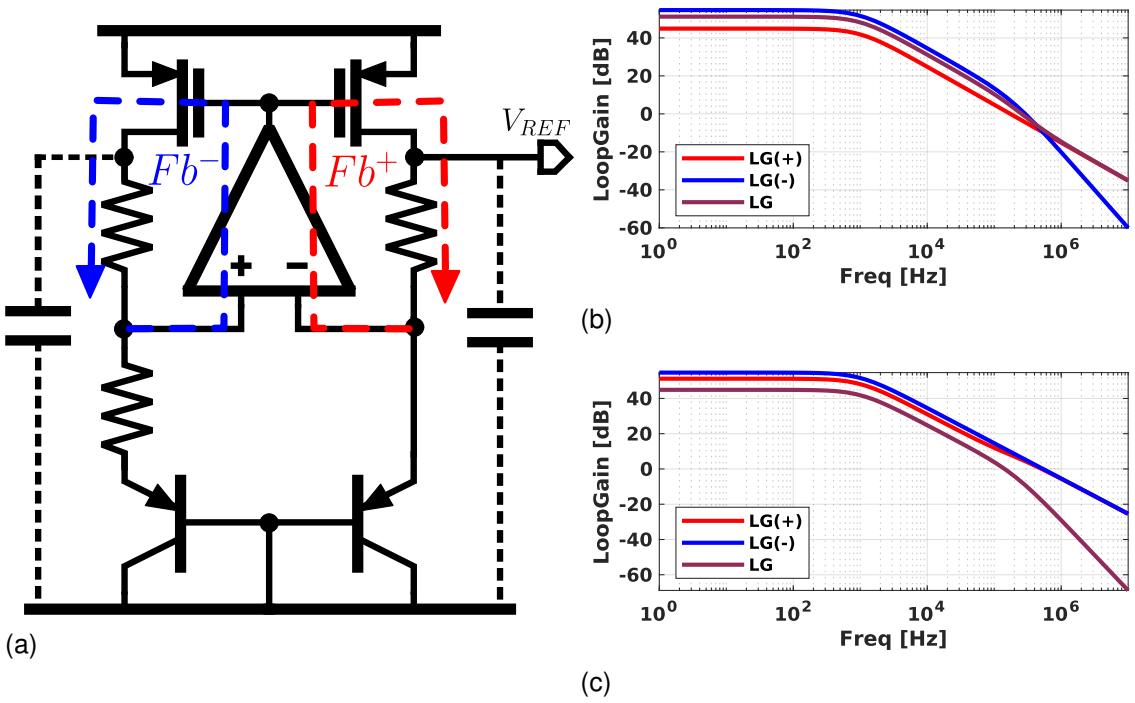

Figure 19. (a) schematic with caps; (b) Loop gain with a cap in Fb^-; (c) Loop gain with a cap in Fb^+

in the cases shown in Fig. 19(b) and Fig. 19(c). The results are shown below:

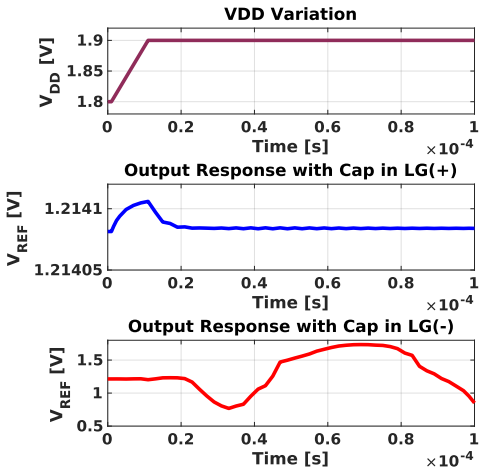

Figure 20. Output response with C_{OUT}.

3.3. PSR

Power supply rejection (PSR) measures the ability of the BGR to suppress power supply noise from its output. The small signal analysis is shown in Fig. 21.

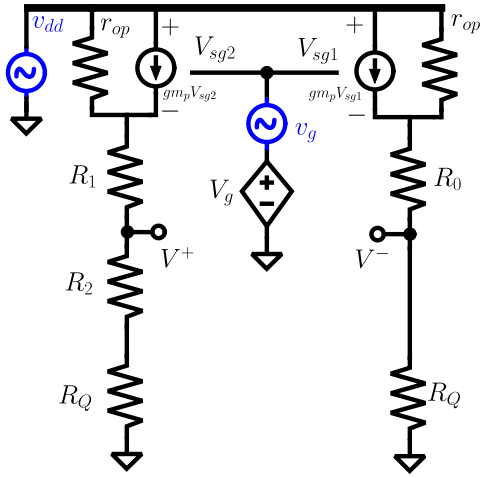

Figure 21. Small signal analysis for PSR

Where, $V_g = A_0(V^+ - V^-)$, $R_Q = [1/gm_Q||r_\pi]$ and $v_g = A_\pi v_{dd}$ where A_π is the relation of how much signal from the source is seen in the output of the amplifier (v_g/v_{dd}), this term can vary according to the error amplifier (EA) topology being used. The PSR of this topology of BGR at DC is given by:

$$PSR = 20\log\left[\left(\frac{R_Q + R_2}{R_0}\right)\left(\frac{1 - A_\pi}{A_o}\right)\right] \tag{35}$$

At Eq. (35) if $A_\pi = 0$, the only way to make the PSR lower is to increase the gain of the EA, but if somehow $A_\pi = 1$, the PSR will go to minus infinity.

Numerous publications have been made to achieve that at the output of the EA $A_\pi = 1$, this is done by the inclusion of an additional stage at the output of the EA in which there is a p-type diode connection that is coupling the signal from the power supply to the

output[21] [22] [23].

Adding another stage to the circuit would mean adding another branch that would draw current. In the development of the BGR design, we did not find it convenient to do this, as we were constrained by the total current consumption specification in the circuit. Therefore, an alternative method was explored to ensure that the signal at the output of the EA would appear similar to the v_{dd} signal thus $A_\pi = 1$.

The work done in [24] uses this method to improve the PSR in a linear dropout regulator (LDO). An intuitive analysis is performed to determine which topologies would be able to achieve this. In Fig. 22(a), there is an NMOS differential pair, and in Fig. 22(b), its small-signal model for calculating the PSR, where

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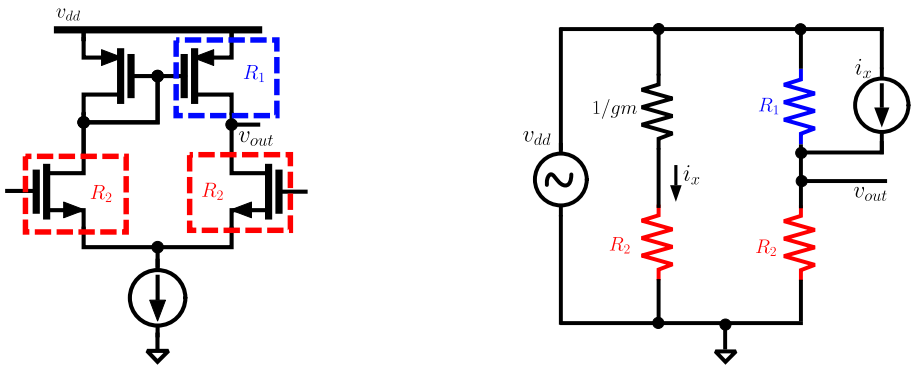
[21] Wenguan LI, Ruohe YAO, and Lifang GUO. "A low power CMOS bandgap voltage reference with enhanced power supply rejection". In: *2009 IEEE 8th International Conference on ASIC*. IEEE. 2009, pp. 300–304.

[22] Jiapeng SHEN and Shengxi DIAO. "A Sub-1 ppm/° C TC Bandgap Voltage Reference with High Power Supply Rejection". In: *2022 15th International Congress on Image and Signal Processing, BioMedical Engineering and Informatics (CISP-BMEI)*. IEEE. 2022, pp. 1–4.

[23] Siew Kuok HOON, Jun CHEN, and Franco MALOBERTI. "An improved bandgap reference with high power supply rejection". In: *2002 IEEE International Symposium on Circuits and Systems (ISCAS)*. vol. 5. IEEE. 2002, pp. V–V.

[24] Vishal GUPTA, Gabriel A RINCÓN-MORA, and Prasun RAHA. "Analysis and design of monolithic, high PSR, linear regulators for SoC applications". In: *IEEE International SOC Conference, 2004. Proceedings.* IEEE. 2004, pp. 311–315.



(a) (b)

Figure 22. (a) NMOS differential pair; (b) PSR small-signal analysis

$$v_{out} = v_{dd}\left(\frac{R_2}{R_1+R_2}\right) + i_x(R_1||R_2) \tag{36}$$

Assuming that $R_2 \gg 1/gm$

$$v_{out} = v_{dd}\left(\frac{R_2}{R_1+R_2}\right) + \frac{v_{dd}}{R_2}\left(\frac{R_1R_2}{R_1+R_2}\right) = v_{dd} \tag{37}$$

$$A_\pi = \frac{v_{out}}{v_{dd}} = 1 \tag{38}$$

Following this analysis, the PSR of a folded cascode amplifier can be derived too as is shown in Fig. 23

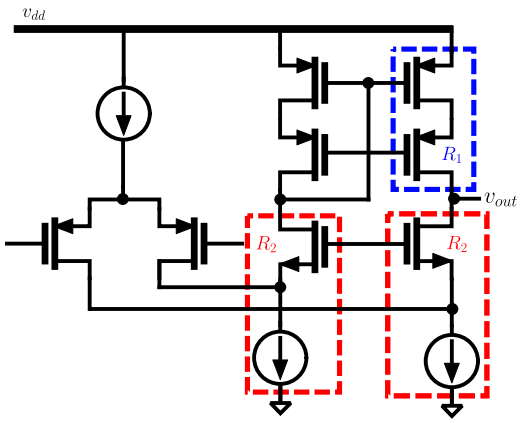


Figure 23. Folded cascode schematic

Where the elements in the boxes are equivalents to the ones present in Fig. 22(b). With this insight, if any amplifier topology can be represented in the form shown in Fig. 22(b), it can be established that the supply ripple appears at the output[24].

In Fig. 24, a comparison of the PSR is presented for two amplifiers with the same gain of $70[dB]$ but with different A_π gain.

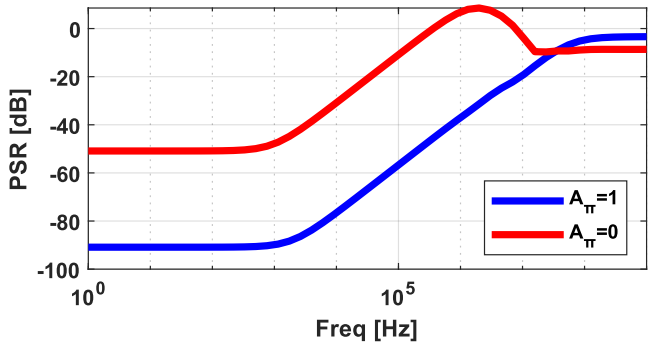


Figure 24. PSR comparison

As expected, when $A_\pi = 1$, there is an improvement in PSR up to $-40[dB]$ compared to an amplifier that does not see the power supply ripple at its output.

3.4. Error Amplifier

When selecting an EA architecture, it is essential to prioritize a high differential gain and a $A_\pi = 1^{24}$. Additionally, it is important to consider the input common mode range, as V_{BE} typically ranges from about 500 mV to 850 mV.

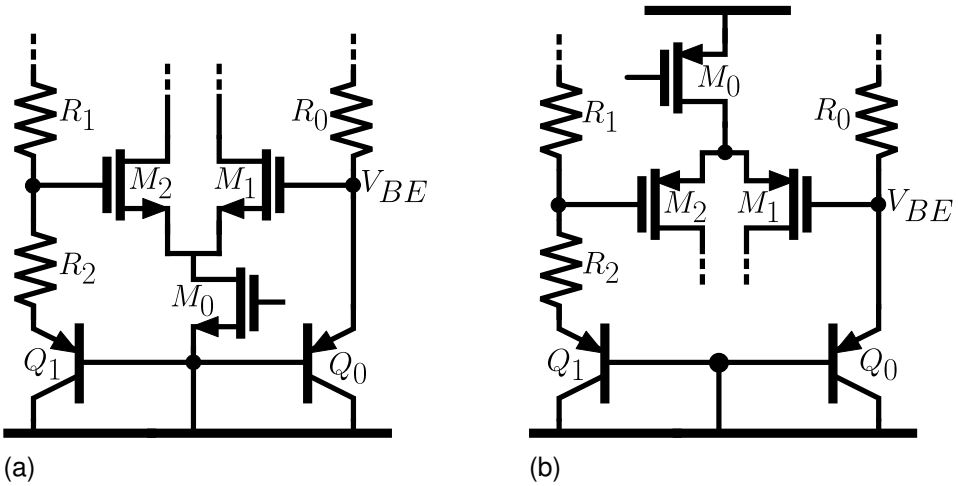


Figure 25. Input stage:(a) N-type; (b) P-type

For an EA with an NMOS input as shown in Fig. 25(a), V_{BE} must meet the following condition:

$$V_{BE} > V_{GS_1} + V_{OV_0} \tag{39}$$

The V_{OV_0} must satisfy the following criterion with the assumption that $V_{GS_1} \approx V_{TH_1}$:

$$V_{OV_0} < V_{BE} - V_{TH_1} \tag{40}$$

For an EA with PMOS input as shown in Fig. 25(b), the V_{BE} must meet:

$$V_{BE} > V_{DD} - V_{OV_0} - V_{SG_1} \tag{41}$$

Therefore

$$V_{OV_0} < V_{DD} - V_{BE} - V_{TH_1} \tag{42}$$

According to Eq. (40) and Eq. (42), it is better to use a PMOS input because M_0 has more voltage headroom and therefore making it a more ideal current source.
Fig. 26 shows the schematic of the used amplifier, where M_{0-10} represents a folded cascode configuration and M_{11-15} conforms the bias circuit.

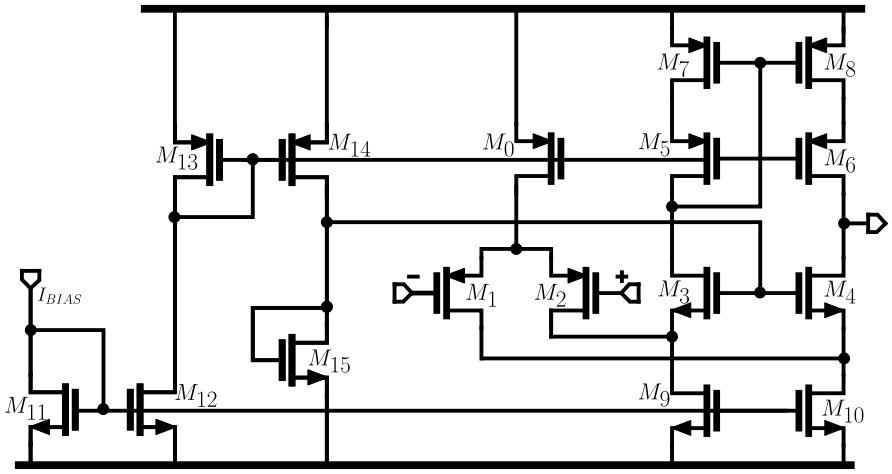


Figure 26. Folded cascode schematic

A copy of the current mirror in the bandgap circuit provides the bias current through M_2, as shown in Fig. 27.

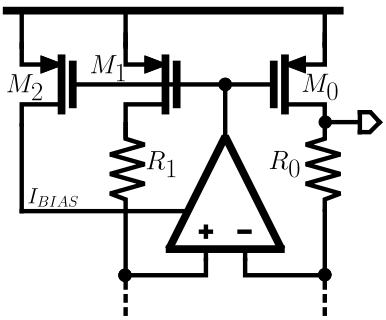
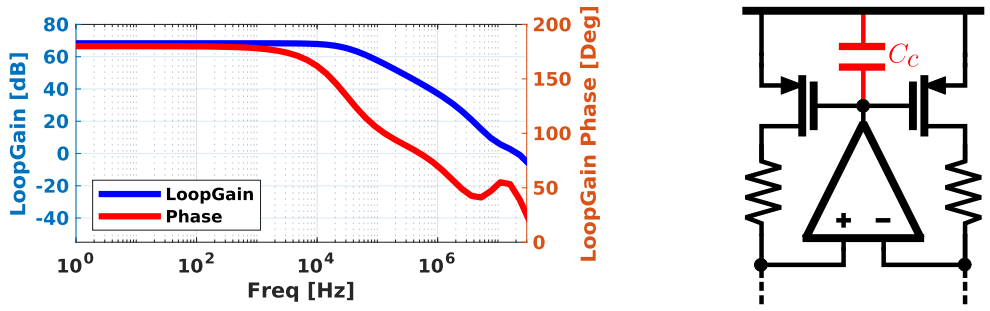


Figure 27. Opamp biasing

3.5. STABILITY

As shown in Fig. 28(a), uncompensated amplification results in a low phase margin. When a step response is imposed, oscillations occur, which is undesirable in this circuit.



(a) (b)

Figure 28. (a)Loop gain without compensation; (b) Schematic with C_c

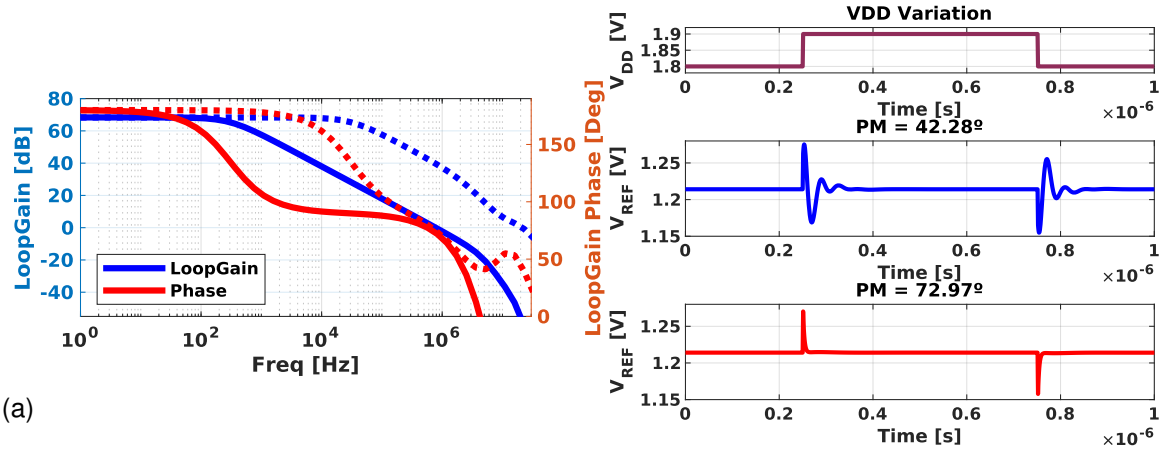
The dominant pole is associated with the output node of the EA and the load capacitor provides the compensation [25]. There are two ways of performing this compensation. One is to connect a capacitor C_c from the amplifier output to the ground, while the other method uses a capacitor C_c placed between the amplifier output and the power supply, as shown in Fig. 28(b). Taking into account the work discussed in section 3.3, if a capacitor is placed between the EA output and the power supply node, variations in V_{DD} will be reflected directly at the amplifier output at high frequencies. This will improve the PSR at high frequencies.

This compensation can be achieved by directly connecting a capacitor between these nodes. Alternatively, It can also be obtained by using the parasitic capacitance imposed by the transistors that make up the current mirror. The only way to increase the

[25] Paul R GRAY et al. *Analysis and design of analog integrated circuits*. John Wiley & Sons, 2009.

capacitance seen at the input of these transistors is by making the mirrors larger. As discussed in Section 3.1, this is beneficial as it improves matching between them.

With a compensation capacitor of $5.5[pF]$, a PM of 67.72 degrees is achieved, as shown in Fig. 29(a). The step response is then evaluated before and after compensation, as shown in Fig. 29.



(a)

(b)

Figure 29. (a) Compensation C_C; (b) Step response

3.6. NOISE

Analyzing different components such as the amplifier and resistors is critical to identify their respective noise contributions. In order to do this for the amplifier shown in Fig. 26, it's necessary to determine both the flicker and thermal noise contributions, to achieve this, the noise spectral density is calculated.

The input-related flicker noise is expressed as follows:

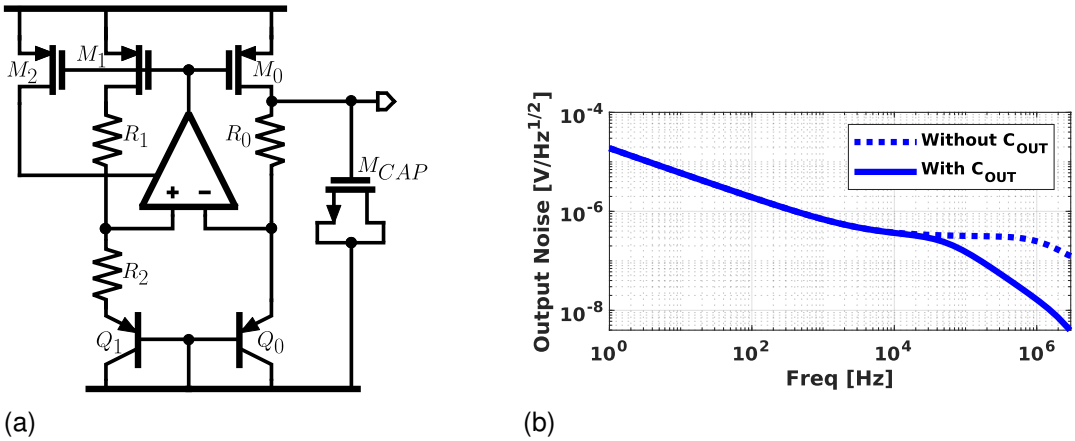
$$V_{N_{IN}}^2(f) = \frac{2\kappa}{g_{m1}^2 f}\left(\frac{g_{m1}^2}{(C_{ox}WL)_1} + \frac{g_{m8}^2}{(C_{ox}WL)_8} + \frac{g_{m10}^2}{(C_{ox}WL)_{10}}\right) \tag{43}$$

where κ is a process-dependent constant. The input-referred thermal noise is given by:

$$V_{N_{IN}}^2(f) = \frac{8kT\gamma}{g_{m1}^2}(g_{m1} + g_{m8} + g_{m10}) \tag{44}$$

k is the Boltzmann constant and γ is a process-dependent constant. Eq. (43) and (44) show that the noise contribution from the amplifier can be reduced by increasing the transistor size and decreasing the transconductance (g_m) of M_{7-10}. Additionally, when the compensation capacitor is introduced as discussed in section 3.5, reducing the amplifier's bandwidth can reduce thermal noise.

After that, the thermal noise from the resistors remained quite high, and given the current limitations, it was necessary to add a capacitor at the output of the circuit., as shown in Fig. 30(a). An NMOS transistor was selected for its higher capacitance per unit area compared to other technology capacitors such as Metal-Isulator-Metal (MIM) or Metal-Oxide-Metal (MOM) capacitors. The effect of the M_{CAP} can be seen in the noise spectral density of Fig. 30(b).



(a) (b)

Figure 30. (a) Schematic with M_{CAP}; (b) Noise spectral density

3.7. START-UP

This BGR topology, as shown in Fig. 13, exhibits two conditions in which the system is stable. The first condition is when the currents passing through each of the branches are equal to zero ($I = 0$), so the voltage V_{BE} will also be zero, resulting in

$$V_{ref} = V_{BE} + IR_0 = 0 \tag{45}$$

The negative feedback loop will maintain this state by ensuring that the gate voltage of the mirrors, V_g, equals $V_s = V_{DD}$. This condition is evident in Fig.31, where it is marked as **undesired**.

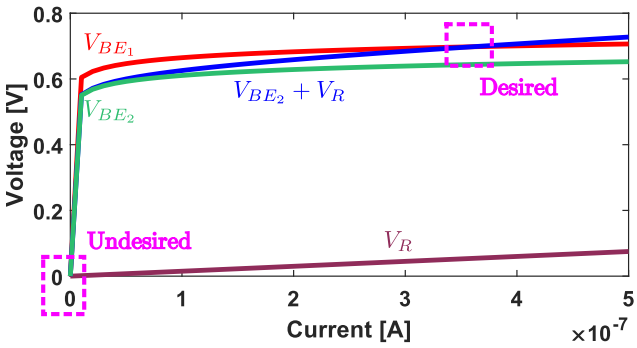


Figure 31. Start-up stable operations points

Now, to avoid the **undesired** condition a start-up circuit is used involving node charge/discharge as shown in Fig. 32. to force the reference towards the desired bias condition. Once this point is reached, the negative feedback loop will maintain this state.

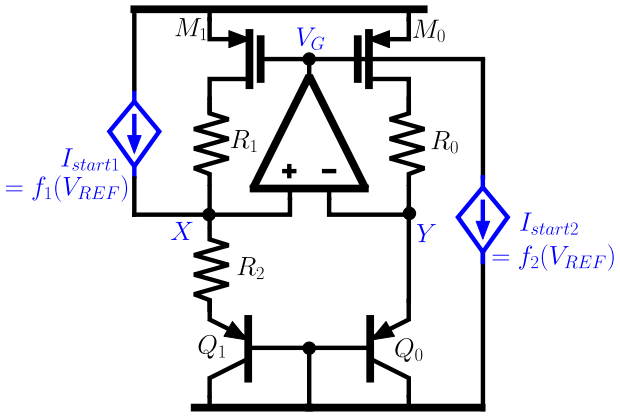


Figure 32. Start-up topologies [26]

The start-up circuit consists of a function that senses V_{ref}, when it is at the undesired bias point, the start-up block is triggered to bring the BGR block to the desired state. Once it reaches this state, the start-up block should turn off to avoid consuming current and affecting the dynamics of the bandgap reference.

In the case where I_{start1} is active, current is injected into node X generating a voltage drop across resistor R_2, thereby forcing a voltage at node Y because of the negative feedback loop and thus a current through this branch. On the other hand, if I_{start2} is implemented it will discharge the node V_G, thus increasing the voltage drop V_{SG} in such a way that the current will begin to flow through each of the branches of the BGR circuit.

For the implementation of the start-up circuit, the configuration shown in Fig. 33 was used.

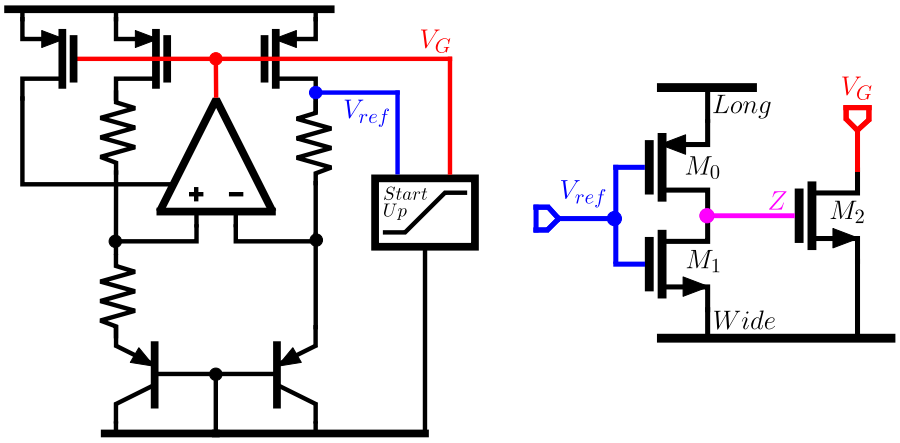


Figure 33. Inverter Start-up

It consists of an inverter that senses the reference voltage V_{ref}. If $V_{ref} = 0$, node Z will be high, allowing current flow through transistor M_2, bringing node V_G close to the ground. And when the voltage V_{ref} starts to increase until it exceeds a certain threshold, which is controlled by the dimensions of the transistors M_0 and M_1 that make up the inverter, node Z will be low so that no current is flowing through M_2 anymore. This behavior can be observed in Fig. 34.

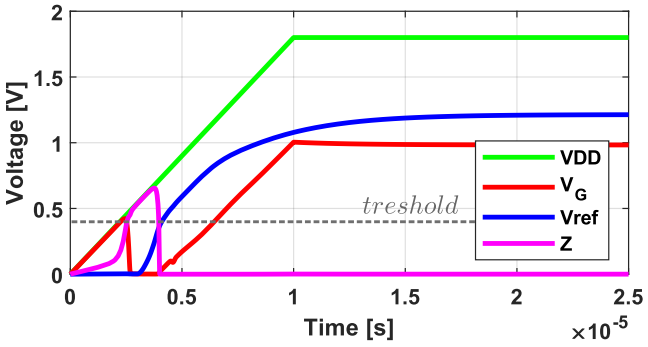


Figure 34. System response to a 10 μs rise time in the supply voltage.

Now, let's see how the BGR block would respond to an atypical condition. In Figure 35, a setup is performed in which, once V_{ref} stabilizes at the desired value, it is forced

to be zero to observe how the system would respond in this scenario, checking if the Start-up block comes into action.

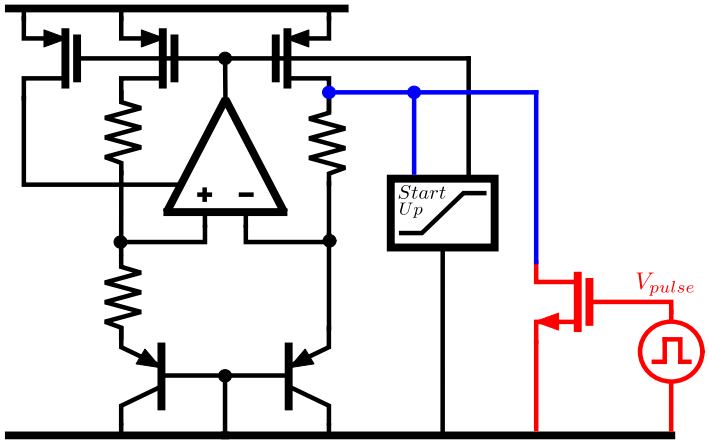


Figure 35. Set-up for perturbance at V_{ref}

As can be seen in Fig. 36, in response to this disturbance, the Start-up block will act in such a way that V_{ref} returns to the desired condition.

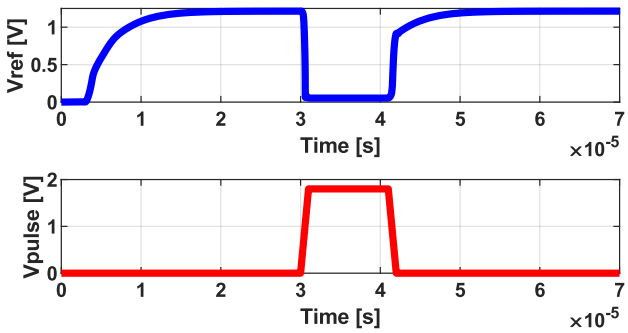


Figure 36. Response of the BGR block to a disturbance at V_{ref}

4. RESULTS

4.1. FINAL DIMENSIONS

This section shows the final dimensions of each element in the bandgap voltage reference circuit.

4.1.1. Circuit top The dimensions of the BGR circuit shown in Fig. 30(a) are detailed in Table 2. The letter **S** represents the number of transistors in series and **P** represents the number of transistors in parallel for each transistor in parallel.

Table 2. Final dimensions for the top circuit

Name	W/L [um/um]	P	S
$\mathbf{M_0}$	0.7/2	24	14
$\mathbf{M_1}$	0.7/2	24	14
$\mathbf{M_2}$	0.7/2	6	14
$\mathbf{Q_0}$	2/2	1	1
$\mathbf{Q_1}$	2/2	8	1
$\mathbf{M_{CAP}}$	1/2	732	1

Poly-silicon resistors were used in the resistor design because this material has a higher resistance per unit area. The results are presented in Table 3.

Table 3. Final resistor dimensions

Name	Type	R [Ω]	P	S
$\mathbf{R_0}$	Rpoly	4.694 k	1	32
$\mathbf{R_1}$	Rpoly	4.694 k	1	32
$\mathbf{R_2}$	Rpoly	4.4164 k	1	4

4.1.2. OPAMP The dimensions of the OPAMP circuit shown in Fig. 26 are detailed in Table 4

Table 4. Final dimensions for the Op-Amp

Name	W/L [um/um]	P	S
$\mathbf{M_0}$	1/2	3	1
$\mathbf{M_1}$	1/2	80	1
$\mathbf{M_2}$	1/2	80	1
$\mathbf{M_3}$	1/2	18	1
$\mathbf{M_4}$	1/2	18	1
$\mathbf{M_5}$	1.2/1	28	1
$\mathbf{M_6}$	1.2/1	28	1
$\mathbf{M_7}$	1.1/2	8	4
$\mathbf{M_8}$	1.1/2	8	4
$\mathbf{M_9}$	1/2	6	6
$\mathbf{M_{10}}$	1/2	6	6
$\mathbf{M_{11}}$	0.275/2	1	4
$\mathbf{M_{12}}$	0.365/2	1	8
$\mathbf{M_{13}}$	0.350/2	1	2
$\mathbf{M_{14}}$	0.350/2	2	2
$\mathbf{M_{15}}$	0.290/2	1	5

4.1.3. Start-Up The dimensions of the Start-up circuit shown in Fig. 33 are detailed in Table 5

Table 5. Final dimensions for the start-up circuit

Name	W/L [um/um]	P	S
$\mathbf{M_0}$	0.3/2	1	1
$\mathbf{M_1}$	0.270/0.5	4	1
$\mathbf{M_2}$	1/0.5	10	1

4.2. CORNERS

The results shown represent typical and worst-case simulations, considering variations in power supply, temperature, and process conditions.

4.2.1. PSR The worst cases of PSR occur when the circuit is at 125ºC since this is where the startup is consuming a maximum current of $213[nA]$, which generates an additional path between V_{DD} and V_{REF}.

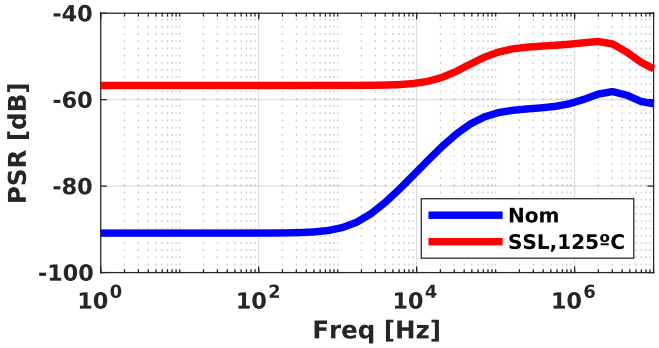


Figure 37. Nominal and Worst corner.

4.2.2. TC The worst cases occur when the power supply is decreased and the transistors have high V_{TH}, showing a variation of $4[mV]$ at the reference temperature.

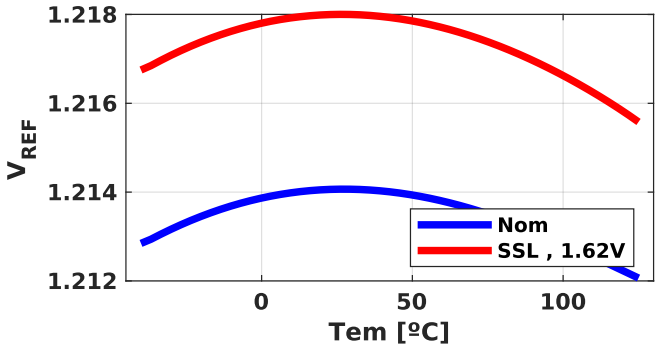
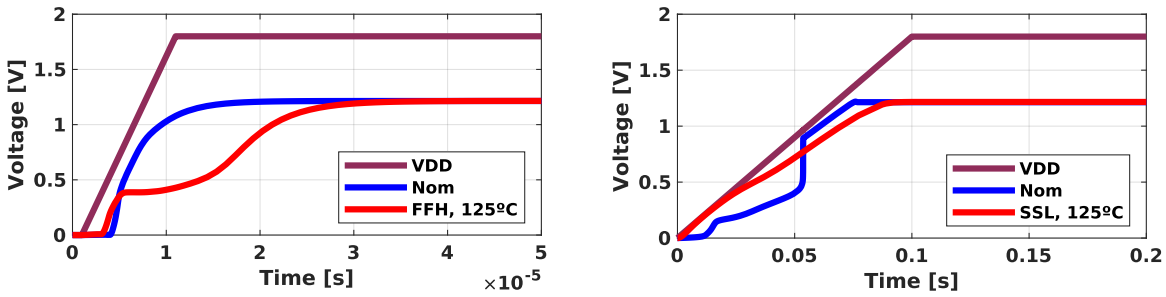


Figure 38. Nominal and Worst corner.

4.2.3. Start-up Various supply rise times were considered for the startup simulations. Fig. 39(a) shows the reference voltage response with a $10[\mu s]$ rise time, where the worst case in the setting time of V_{REF} is $30\mu s$. Fig. 39(b) shows a setting time of $90[ms]$ for a $100[ms]$ rise time.



(a) (b)

Figure 39. Start-up response for: (a) Tr=10us; (b) Tr=0.1s

4.2.4. Noise The worse cases occur at high temperatures, increasing the integrated noise from $114[\mu V_{RMS}]$ to $129.8[\mu V_{RMS}]$.

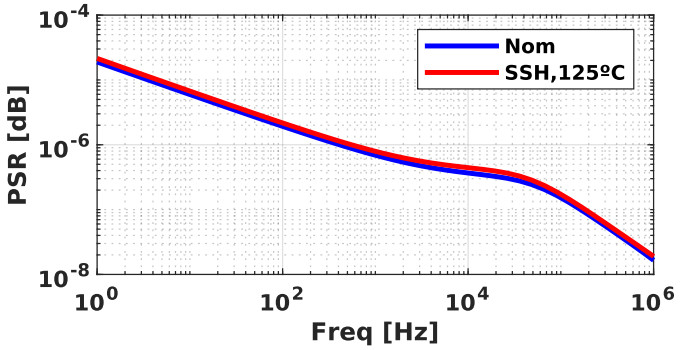


Figure 40. Nominal and Worst corner for Noise.

4.3. MONTECARLO

A Montecarlo analysis is performed with 1000 simulations per parameter, the results are shown below:

Table 6. Montecarlo results

Parameter	Min	Max	Typ	Std
V_{REF} [V]	1.194	1.233	1.213	6.327m
TC [ppm/ $^{\circ}C$]	4.723	39.87	13.4	4.7
I_{VDD} [uA]	17.22	46.49	28.9	2.728
V_{NOISE} [uV_{RMS}]	99.7	132.2	114.1	2.71
PSR @ DC [dB]	-133.4	–56.32	-76.1	8.47
PSR_{MAX} [dB]	-60	-48	-57	1.24
PM [deg]	-61	-72.87	-67.72	669m

Table. 6 shows that all the values obtained are within the given specifications, particularly the low temperature coefficient and the high power supply rejection.

4.4. LAYOUT

The BGR layout is shown in Fig. 41 and consists of six blocks. Each block is designed to achieve a square and compact shape.

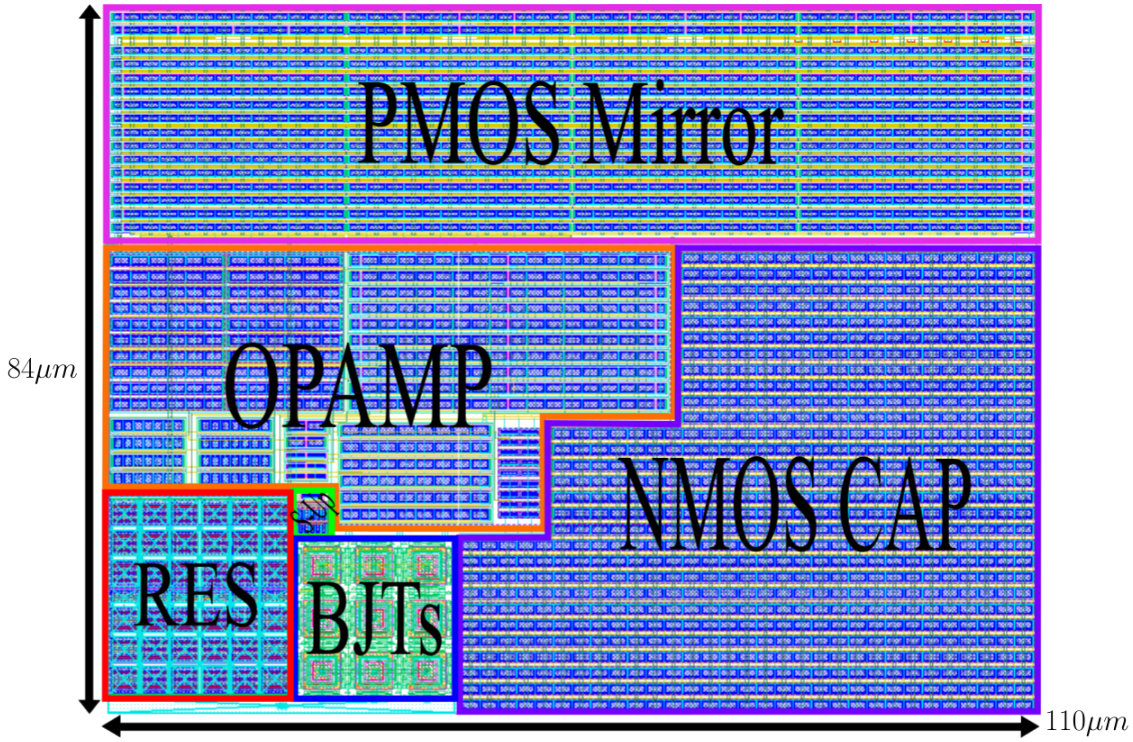


Figure 41. Layout.

Key considerations include:

- Use of interdigitated and common centroid techniques: These have been used to improve matching characteristics, with the inclusion of dummy devices and guard rings for the most critical transistors. Similarly, dummy structures were used for the resistors.
- Metal Layer Choices: The design employs even-numbered metal layers for horizontal connections and odd-numbered layers for vertical connections to simplify routing. In addition, two or more vias were used to reduce the resistance between the metal layers.
- Capacitor placement: The capacitor was divided into three parts, strategically placed as the final element of the layout. This method had two benefits: it filled

empty spaces and made the design more compact.

4.5. RESULTS COMPARISON

Table. 7 provides a comparison of our design with similar works. It includes Guerinii, a microcontroller developed by the Onchip Research Group in 2018, as well as a master's thesis and three research papers, where a good performance is observed compared to the other ones.

Table 7. Results comparison

	This work	**Guerinii**	**MSc Thesis**[27]	**Research Paper** [28]	**Research Paper**[29]	**Research Paper**[30]
Process	28 nm CMOS	180 nm CMOS	180 nm CMOS	16 nm FINFET	65 nm CMOS	55 nm CMOS
V_{REF} [V]	1.213	1.259	1.225	1.225	1.2	1.2
TC [ppm/$^{\circ}$C]	13.4 [-40,125]	8.833 [-40,125]	1.6 [-20,140]	24.68 [-40,125]	9.8 [-20,150]	7.7 [-40,85]
I_{VDD} [uA]	28.9	29.45	28.9	188	N/A	36
V_{NOISE} [uV_{RMS}]	114.1	352.4	N/A	N/A	N/A	N/A
PSR @ DC [dB]	-76.1	-45.92	-60	N/A	-70	-78
PM [deg]	67.72	83.66	60	97	N/A	N/A
Area [mm^2]	0.00924	0.026	0.0308	0.011	N/A	N/A

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

A bandgap voltage reference has been designed to be employed in a System-on-Chip (SoC) in a 28 nm TSMC CMOS process node. For the design process, each of the elements that are part of the bandgap voltage reference block was studied, and based on this, decisions were made to improve the circuit's performance. A novel technique has been employed to enhance Power Supply Rejection (PSR), where an improvement of -40 dB at low frequencies was achieved and various methods to reduce noise have been introduced, achieving an integrated noise in the 1 Hz to 5 MHz band of 114 μV_{rms}.

Layout design has been optimized to improve device matching and achieve a compact layout through techniques such as common centroid, interdigitation, and the use of dummy devices. Simulation results, including corner cases and Monte Carlo analyses, meet the specified requirements, highlighting excellent PSR performance and area efficiency compared to alternative designs.

5.2. Future Work

- Perform post-layout simulations to observe the effects of parasitic capacitances and resistances. Due to problems with the simulation tool, it was not possible to extract parasitic, and therefore post-layout simulations could not be executed.
- Implementation of trimming techniques to fine-tune circuit parameters post-fabrication. Beyond the constraints imposed by fabrication conditions, it is common practice to use ”trimming” techniques to calibrate the fabricated circuit, allowing adjustments to be made to improve the accuracy of the circuit. This post-fabrication calibration

is used to achieve the accuracy levels required by the voltage reference design specification.

- The enhancement of the temperature coefficient of the bandgap reference by implementing higher-order compensation techniques. While this study focused primarily on linear compensation to achieve a nearly proportional-to-absolute-temperature characteristic, exploring more advanced compensation schemes could lead to even better TC performance.

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