Universidad Industrial de Santander

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School of Electrical, Electronic and Telecommunications Engineering

MICROELECTRONICS REPORT#1

Fabián Camilo Chacón Vargas, fabian2214192@correo.uis.edu.co

***Abstract*—An approach to short-channel transistor technology, comparing its advantages with technologies in other lengths and introducing some of the phenomenons it can produce on a small scale.**

I. Short-Channel Effects in Semiconductor Devices

A. Saturation Velocity

This is the maximum speed charge carriers can reach in a semiconductor under a strong electric field. At low fields, velocity increases with the field, but at high fields, frequent scattering with the lattice limits further acceleration. Affect in high-speed, as it impacts current flow and switching speed

$$v_{\text{sat}} = \frac{\mu E}{1 + \left(\frac{\mu E}{v_{\text{sat, max}}}\right)^{\beta}}, \tag{1}$$

where:

- μ: Carrier mobility ($\text{cm}^2/\text{V}\cdot\text{s}$),
- E: Electric field (V/cm),
- $v_{\text{sat, max}}$: Maximum saturation velocity ($\sim 10^7$ cm/s for electrons),
- β: Empirical fitting parameter

B. Substrate Current-Induced Body Effect (SCBE)

This is a phenomenon in MOSFETs where the gate's control over the barrier potential is weakened when the channel length is reduced. This happens because the channel is influenced by the source and drain electric fields, which lowers the threshold voltage and increases leakage currents. [1]

$$I_{\text{sub}} = \frac{A_i}{B_i} I_{ds} \left(V_{ds} - V_{\text{dsat}}\right) \exp\left(-\frac{B_i}{V_{ds} - V_{\text{dsat}}}\right) \tag{2}$$

C. Drain-Induced Barrier Lowering (DIBL)

A high drain voltage lowers the potential barrier at the source of the DIBL, a short-channel phenomenon in MOSFETs that facilitates easy charge carrier flow. Device performance is impacted as a result of increased leakage current and decreased threshold voltage.

$$V_{\text{th}} = V_{\text{th0}} - \eta \cdot V_{\text{ds}}, \tag{3}$$

$$\eta = \frac{3t_{\text{ox}}}{L_{\text{eff}} \cdot \sqrt{\frac{\epsilon_{\text{si}}}{\epsilon_{\text{ox}}}}} \tag{4}$$

where:

- V_{th0}: Long-channel threshold voltage,
- t_{ox}: Oxide thickness (nm),
- L_{eff}: Effective channel length (nm),
- $\epsilon_{\text{si}}/\epsilon_{\text{ox}}$: Si/$SiO_2$ permittivity ratio ($\sim 3.9/11.7$).

D. Halo Implantations

This is a process that introduces highly doped areas close to the source and drain to lessen short-channel effects. These halo implants work to resist the effects of drain-induced barrier lowering (DIBL) and other short-channel events, which helps regulate the threshold voltage and inhibit undesired leakage currents.

E. Gate Leakage Current

When the oxide layer is very thin, quantum tuning causes this undesired current to flow through the gate oxide of a MOSFET. The performance of contemporary transistors is impacted by this leakage, which raises power consumption and heat generation.

F. Diffusion Leakage Current

When the oxide layer is very thin, quantum tuning causes this undesired current to flow through the gate oxide of a MOSFET. The performance of contemporary transistors is impacted by this leakage, which raises power consumption and heat generation.

G. Gain Transit Frequency Product, short-channel technology

For long channel lengths, the above equation can be written:

$$GFT = g_m r_o \cdot f_T = \frac{g_m^2}{2\pi C_{gs}} \cdot \frac{1}{\lambda I_D} = \frac{3\mu_n}{2\pi L^2 \lambda} \propto \frac{\mu_n}{L} \tag{5}$$

Short-channel effects are made worse by downscaling channel lengths ($L_{\text{eff}} \downarrow$). Halo implants, which raise the nominal threshold voltage (V_{th0}) while suppressing DIBL, lessen electrostatic control, which intensifies DIBL ($\eta \uparrow$) and SCBE ($\lambda \uparrow$). These effects are amplified by increasing the drain voltage ($V_{\text{ds}} \uparrow$), which lowers V_{th} by impact lateral field . Although they increase tunneling leakage, thinner gate oxides ($t_{\text{ox}} \downarrow$) improve gate capacitance ($C_{\text{ox}} \uparrow$). At high fields, saturation velocity restricts carrier mobility, while substrate currents and diffusion jeopardize thermal stability.

Parameter	NMOS			PMOS		
	W/L=5 (L=0.18um)	W/L=5 (L=0.4um)	W/L=5 (L=1um)	W/L=5 (L=0.18um)	W/L=5 (L=0.4um)	PMOS W/L=5 (L=1um)
Id	26.45u	35.44u	56.3u	19.1	17.22u	17.4u
Vgs	681m	733m	771m	788m	781m	789m
Vds	700m	700m	700m	700m	700m	700m
Vsb	0	0	0	0	0	0
Vth	555.9m	543.9m	495.5m	569.9m	519.3m	497.7m
Vov	125.1m	189.1m	275.5m	218.1m	261.7m	291.3m
Vdsat	119.7m	181.8m	243.6m	191.5m	232.8m	266.6m
Vds-Vdsat	580.3m	518.2m	456.4m	508.5m	467.2m	433.4m
gm	232.6u	272.3u	353.2 u	121.9u	103u	97.55u
gmb	68.32u	80.47u	96.69 u	44.81u	36.25u	34.22u
ro	119.8k	247.2k	305.3 k	190.1k	521.6k	1.109 M
gmro	27.85	67.33	107.8	23.17	53.72	108.2
gm/Id	8.792	7.683	6.273	6.382	5.981	5.607
Cgs	1.369 f	5.956 f	35.32 f	1.415 f	6.132 f	34.81 f
Cgd	340.7 a	770.5 a	1.987 f	393.1 a	874.8 a	2.23 f
ft	27.04 G	7.277 G	1.591 G	36.87 G	8.359 G	1.707 G
FTGMID	237.73G	55.90 G	9.98 G	235.30 G	49.995 G	9.57 G
GFT	753.064G	489.96 G	171.509 G	854.277 G	449.045 G	184.69

Figure 1. Simulation data for NMOS and PMOS transistors maximized.

II. CONSOLIDATION OF CHARACTERIZATION DEVELOPED

To ensure a strong inversion during the characterization process, these dependencies will be maintained as shown in the figure [2]:

	Weak inversion		Strong inversion	
Criteria	Δov = Vgs - Vth	Vds	Δov = Vgs - Vth	Δvd = Vds - Vdsat
Triode	< 80mV	n.a	> 100mV	< 0V
Saturation		> 130mV		> 50mV
when 80mV<Δov<100mV we assume same as in strong inv.				

Figure 2. Biasing conditions check

In each of the reference transistors analyzed, it was found that the curves exhibited identical behavior in their shape, differing only in the magnitude of their values in the figure[3].

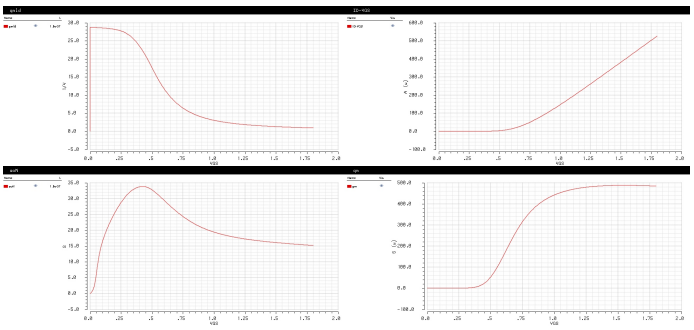

Figure 3. Curve behavior

Maximizing $f_T * (g_m/I_D)$ implies achieving the **highest effective relationship between frequency capability** (f_T) **and gain efficiency** (g_m/I_D), making it a key parameter for designing energy-efficient high-frequency amplifiers and analog systems.Using the console code xmax(FTGMID 1), max was extracted as an additional design parameter; this relationship is also visible here in the figure [4].

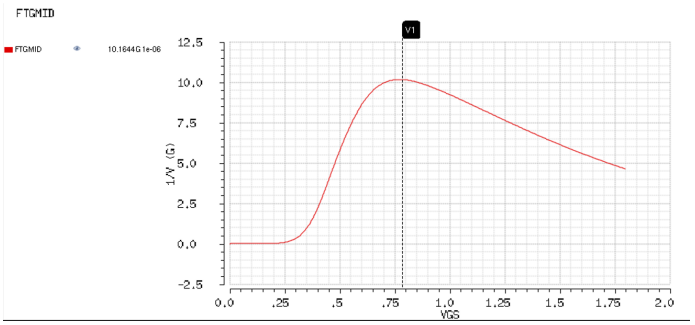

Figure 4. FTGMID

The maximum for each length of transistor can be seen in the figure [1] where all the parameters for each reference transistor can be observed.

III. DEVICE DESIGN

A. First design

This design required the creation of an NMOS transistor with $f_T \geq 10$ GHz and I_D = 100uA. The design methodology employed in this work was based on using the f_T vs V_{GS} curve to determine the bias voltage at which the transition

frequency exceeds 10 GHz. Subsequently, the **design by scaling** methodology was applied to find the design current by increasing the channel length.

To determine the design current, the following equations were used :

$$\frac{I_{D,\text{design}}}{I_{D,\text{ref}}} = \frac{W_{\text{design}}}{W_{\text{ref}}} \tag{6}$$

$$W_{\text{design}} = W_{\text{ref}} \cdot \frac{I_{D,\text{design}}}{I_{D,\text{ref}}} \tag{7}$$

These equations were used to find the required W_{design} needed to achieve the desired current. In the figure [5] Each of the parameters extracted from the design can be seen, where for L=1um the specifications of the transistor could not be met due to its dimensions due to technological limitations.

Parameter	NMOS		
	(W=22.5 um) (L=0.18um)	(W=2.753um) (L=0.4um)	(W=5.8327 um) (L=1um)
Id	100.3 u	100u	100u
Vgs	530m	845.4 m	845.4 m
Vds	700m	700m	700m
Vsb	0	0	0
Vth	559.1m	544.2m	494,8m
Vov	29.1 m	301.2m	350.6m
Vdsat	61.88m	247.4m	494,8m
Vds-Vdsat	638.12m	452.6m	205.2
gm	1.811m	529u	507.6u
gmb	518.9u	155.9u	136.8u
ro	19.8k	85.54k	165.8k
gmro	35.85	45.25	84.16
gm/Id	18.05	5.29	5.076
Cgs	28.67 f	8.419f	41.74f
Cgd	8.109 f	1.086f	2.378f
ft	10.05 G	10G	1.936G
FTGMID	181.402 G	52.9 G	9.82 G
GFT	360.292 G	452.2 G	162.933 G
AREA	4.05p	1.1012p	5.8327p

Figure 5. parameters of the first design

To meet the specifications of the problem, the most optimal design is L=0.4um, since the dimensions allow us to reach the transition frequency without difficulties an good gain and it could be observed that it was the one that obtained the lowest parasitic capacitances in the design, it is a stable design that does not sacrifice gain and maximizes the area being the smallest area obtained in this design.

B. Second design

This design required the creation of an NMOS transistor with $gmro \geq 100$ and I_D = 10uA. The strategy methodology used in this design was based on the curves of r_o vs VDS, in order to obtain the highest possible VDS to obtain the greatest gain in r_0 each of the lengths, after this the by scaling methodology used in the previous design was followed.

It is observed that L=0.18um did not meet the specifications necessary for the design, due to current limitations it could not be scaled to gm and ro could not grow further since it was at its maximum value, once again technological limitations can be identified.

Parameter	NMOS		
	(W=394n um) (L=0.18um)	(W=526.1nm) (L=0.4um)	(W=978.8n um) (L=1um)
Id	11.51u	10.5u	9.995
Vgs	653m	743m	771m
Vds	1.03	1.6	771m
Vsb	0	0	0
Vth	541.2m	543.3m	511.4m
Vdsat	116.2m	187m	243.5
gm	104.6u	77.2u	64.04u
gmb	30.03u	22.92u	18.78u
ro	375.8k	1.558M	1.895M
gmro	39.31	120.2	121.4
gm/Id	9.091	7.352	6.412
Cgs	582.1a	1.552f	6.803f
Cgd	134.3a	167.6a	379.3a
ft	28.61G	8.049G	1.499G
AREA	70.91f	210.44f	978.8f

Figure 6. parameters of the second design

Under the limitations of this design, the best option was L=1um since it did not present problems in its gain and also for the given application it is the one that best meets the specifications, needing a lower VDS than the other lengths,where its only disadvantage is the area.

C. Third design

This design required the creation of an NMOS transistor with $gm = 0.3mS$ and $VDsat$ = 0.3V.

The methodology used for this design consisted of using the Vdsat vs. VGS curve to find the VDsat that met the design conditions. The following relationship was then used:

$$\frac{g_{m,\text{design}}}{g_{m,\text{ref}}} = \frac{I_{D,\text{design}}}{I_{D,\text{ref}}} \tag{8}$$

$$I_{D,\text{design}} = \frac{g_{m,\text{design}}}{\left(\frac{g_{m,\text{ref}}}{I_{D,\text{ref}}}\right)} \tag{9}$$

Using the gmid op curve and equation 9, the design current that provides the design gm is determined.

In this case all the transistors met the design conditions, the one that obtained the best performance in proportion to the conditions is the one with L=0.1um since it can be seen that it obtained a smaller area compared to the other cases, in addition to obtaining a better frequency response where its only disadvantage is the gain.

Parameter	PMOS		
	(W=1.42 um) (L=0.18um)	(W=4.64um) (L=0.4um)	(W=13.71 um) (L=1um)
Id	83.88u	66.52u	59.57u
Vgs	1.014	879m	832.257m
Vds	771m	771m	771m
Vth	573.6m	525.1m	500.2m
Vdsat	299.7m	293.6m	300m
gm	296.3u	309.u	299.8u
gm/Id	3.532	4.659	5.033
gmb	113.7u	111.2u	106.1u
ro	48.95k	155.5k	348.7k
Cgs	2.295f	14.45f	95.66f
Cgd	638.9a	2.048f	6.047f
ft	46.5G	10.69G	1.948G
AREA	255.6f	1.856p	13.71p

Figure 7. parameters of the third design

IV. Conclusions

- A proportional relationship was observed between the device gain and its parasitic capacitances in each of the designs, and an inversely proportional relationship between the speed of the devices and their lengths.
- Technological limitations were observed in some designs that did not allow compliance with the specifications given by SiNiCo, evidencing strong dependencies between the transistor length and other parameters, making some designs unfeasible.
- The scaling methodology proved to be very useful, as it allows the designer to first search for appropriate design conditions and then, through a relationship between their lengths, modify the current, affecting only a few design parameters.

The reader is invited to view the development of each of the captures and samplings performed during the design, along with bibliographic material to better understand the phenomena of short-channel technology, by visiting the GitHub repository. [2]

References

[1] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 4th ed. Hoboken, NJ, USA: Wiley-IEEE Press, 2019.

[2] F. C. Vargas, "Microelectronics repository," https://github.com/FabianChacon3/Microelectronics-repository, 2025, accessed: 2025-03-14.