Universidad de Costa Rica
Facultad de Ingeniería
Escuela de Ingeniería Eléctrica
IE-0624 Laboratorio de Microcontroladores
I ciclo 2025

Laboratorio 1
Introducción a microcontroladores y manejo de GPIOS

Fabian Sander Hangen C07336
Grupo 01

Profesor: MSc. Marco Villalta Fallas

25 de Marzo de 2025

Índice

1. Introducción

En este laboratorio se desarrolló un simulador de dado utilizando el microcontrolador `PIC12F683`, acompañado de LEDs, resistencias y un botón de entrada. El propósito principal fue introducir el manejo de los pines de entrada y salida (*GPIOs*), así como la generación de números aleatorios dentro del microcontrolador. Para ello, se diseñó un circuito que, al presionar el botón, enciende una cantidad de LEDs correspondiente a la cara del dado obtenida, con valores comprendidos entre 1 y 6.

El diseño del circuito consideró medidas de protección mediante el uso de resistencias en serie con los LEDs y el botón de entrada. Asimismo, se incluyó un capacitor en la alimentación para mitigar fluctuaciones en la tensión de suministro. La implementación del software se realizó en lenguaje C, asegurando una programación eficiente y optimizada para las limitaciones del microcontrolador, evitando operaciones costosas en términos de procesamiento.

Para verificar la correcta operación del sistema, se utilizó la herramienta de simulación SimulIDE que permitió analizar el comportamiento de las señales eléctricas en diferentes puntos del circuito. Se realizaron mediciones de voltajes y corrientes, garantizando que los valores obtenidos coincidieran con los esperados teóricamente. Además, se comprobó que el software generara de manera aleatoria los valores de salida, asegurando un comportamiento impredecible y uniforme del dado electrónico.

Se verificó que el algoritmo desarrollado cumple con los requerimientos de funcionalidad y eficiencia, logrando representar de manera confiable las diferentes caras del dado mediante el encendido de los LEDs.

En conclusión, este laboratorio permitió reforzar conceptos fundamentales de electrónica digital-analógica y programación, además de introducir una metodología de desarrollo estructurada para el curso. Se pudo constatar la importancia del diseño eficiente en sistemas con restricciones de hardware, así como la relevancia del análisis de señales para validar su correcto funcionamiento.

El repositorio del proyecto se encuentra disponible en el siguiente enlace:
https://github.com/FabianSander1/microcontroladoresFabianS.git

2. Nota Teórica

2.1. Información General del Microcontrolador

Para el desarrollo de este laboratorio se utilizó el microcontrolador PIC12F683, un dispositivo de 8 bits con arquitectura RISC, perteneciente a la familia de microcontroladores CMOS de Microchip. Este modelo es ideal para aplicaciones de baja complejidad, por lo que resulta adecuado para la implementación del dado electrónico propuesto en el experimento. El PIC12F683 cuenta con un conjunto reducido de 35 instrucciones, lo que facilita su programación y optimización [1].

Este microcontrolador dispone de 6 pines de entrada/salida (*GPIOs*) que pueden operar tanto como entradas digitales como salidas, y tienen una capacidad de corriente máxima de 25 mA por pin. Adicionalmente, incorpora un convertidor analógico-digital (ADC) de 10 bits con cuatro canales de entrada, una memoria EEPROM de 128 bytes para almacenamiento de datos y un comparador analógico. También incluye un oscilador interno de 8 MHz, permitiendo configuraciones sin necesidad de un oscilador externo[1].

Se muestra una imagen del diagrama de bloques de este microcontrolador y en la siguiente un diagrama de su apariencia física.

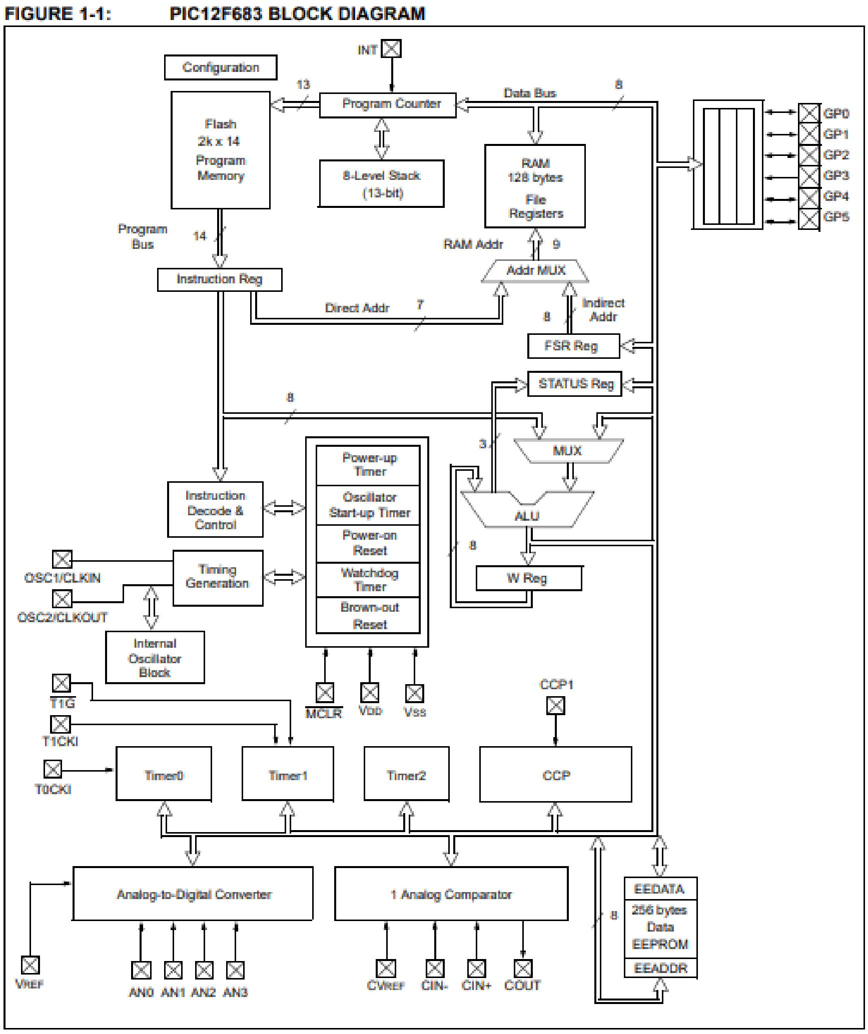


Figura 1: Diagrama de bloques del PIC12F683 [1].

Se muestra una imagen física del microcontrolador.

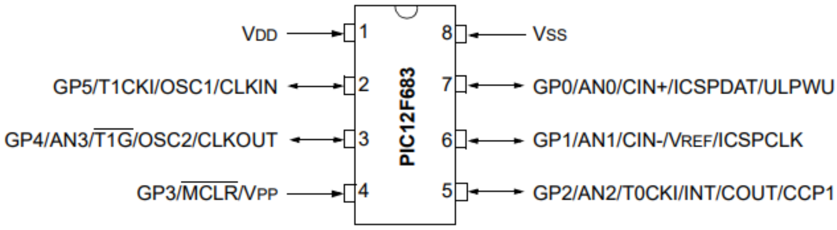


Figura 2: Imagen física del PIC12F683 [1].

2.2. Periféricos

El `PIC12F683` cuenta con diversos periféricos que permiten ampliar su funcionalidad en aplicaciones. Algunos de los más relevantes incluyen:

- **GPIOs:** Seis pines configurables como entradas o salidas digitales, utilizados en este experimento para controlar los LEDs y recibir la señal del botón de entrada [1].
- **Conversor ADC:** Dispone de un módulo de conversión analógica a digital de 10 bits, aunque no fue necesario en esta práctica [1].
- **Temporizadores:** Cuenta con un temporizador de 8 bits (`TMR0`) que permite la implementación de retardos precisos sin necesidad de consumir ciclos de CPU en bucles de espera [1].
- **Memoria EEPROM:** Proporciona almacenamiento no volátil para guardar configuraciones o valores aleatorios generados [1].
- **Oscilador interno:** Permite operar sin necesidad de un cristal externo, simplificando el diseño del circuito [1].

Pin	Nombre	Función	Características
1	GP5	I/O digital	Entrada/Salida, PWM, CCP
2	GP4	I/O digital	Entrada/Salida, PWM, CCP
3	GP3	I/O digital	Entrada/Salida
4	GP2	I/O digital	Entrada/Salida, Interrupción
5	GP1	I/O digital	Entrada/Salida
6	GP0	I/O digital	Entrada/Salida, Interrupción
7	VDD	Alimentación	+5V
8	VSS	Tierra	0V

Tabla 1: Resumen de Pines del PIC12F683 [1]

2.3. Registros

Para la correcta configuración y operación del `PIC12F683`, es fundamental el uso de registros internos que controlan las funcionalidades del microcontrolador. Los registros más importantes utilizados en este laboratorio incluyen:

- **CONFIG:** Define configuraciones esenciales del microcontrolador, como la desactivación del *Watchdog Timer* para evitar reinicios no deseados [1].

- **TRISIO:** Permite establecer la dirección de los pines *GPIO* como entradas (1) o salidas (0). En este laboratorio, todos los pines fueron configurados como salidas, excepto el GP5, que se utilizó como entrada para el botón [1].
- **GPIO:** Controla el estado lógico de los pines, permitiendo encender o apagar los LEDs en función del número aleatorio generado [1].

El uso eficiente de estos registros permitió implementar un sistema funcional y optimizado, asegurando un correcto manejo de los LEDs y la detección del botón sin generar conflictos en la configuración de los pines.

2.4. Características Eléctricas

En la hoja de datos se pueden encontrar las características eléctricas de este microcontrolador.

15.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias	-40° to +125°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss	-0.3V to +13.5V
Voltage on all other pins with respect to V_{SS}	-0.3V to (V_{DD} + 0.3V)
Total power dissipation(1)	800 mW
Maximum current out of V_{SS} pin	95 mA
Maximum current into V_{DD} pin	95 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	± 20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD})	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by GPIO	90 mA
Maximum current sourced GPIO	90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OI} \times I_{OL})$.

Figura 3: Características Eléctricas del PIC12F683 [1].

2.5. Lista de Componentes y precios

En este apartado se presenta la lista de componentes utilizados junto con sus respectivos precios. La justificación de la selección de cada componente se abordará en la sección de desarrollo. Cabe destacar que en esta lista no se incluyen instrumentos de medición como voltímetros, amperímetros u osciloscopios.

Componente	Especificación	Cantidad	Precio unitario	Precio total
LED Rojo	2,1Vth	6	75 colones	450 colones
Resistencia	35 Ohms	3	40 colones	120 colones
Resistencia	140 Ohms	1	69 colones	69 colones
Resistencia	1k Ohms	1	40 colones	40 colones
Capacitor	5uF	1	2506 colones	2506 colones
Botón	-	1	89 colones	89 colones
Microcontrolador	PIC12F683	1	1114 colones	1114 colones

Tabla 2: Lista de componentes utilizados en el circuito [2] [3] [4] [5].

3. Desarrollo

3.1. Diseño del Código

El diseño del código se realizó en lenguaje `C`, haciendo uso de las librerías específicas para el microcontrolador `PIC12F683`.

A continuación, se describen las funciones implementadas y su propósito dentro del programa.

Se define el registro de configuración para desactivar el *Watchdog Timer*, evitando así reinicios inesperados del sistema. Además, se configura el registro `OPTION_REG` para habilitar el temporizador interno `TMR0` con un preescalador de 1:256, lo cual permite tener un valor cambiante constantemente como base para generar aleatoriedad.

```
typedef unsigned int word;
word __at 0x2007 __CONFIG = (_WDTE_OFF);

...

OPTION_REG = 0b00000111; // Configura TMR0 con preescalador 1:256
```

Se declara una variable global llamada `numeroActual`, que puede utilizarse para mantener el estado del último valor del dado, aunque en este caso se genera un número nuevo cada vez que se presiona el botón.

```
volatile uint8_t numeroActual = 1;
```

La función `rand_con_timer()` se encarga de generar un número doaleatorio entre 1 y 6. Para ello, utiliza una semilla estática y la combina con el valor actual del temporizador `TMR0` mediante una operación XOR. Posteriormente, realiza una rotación de bits y limita el resultado al rango deseado mediante una operación módulo.

```
uint8_t rand_con_timer(void) {
    static uint8_t semilla = 0x5A; // Semilla inicial arbitraria
    semilla ^= TMR0;               // Mezcla con el valor del temporizador
    semilla = (semilla << 1) | (semilla >> 7); // Rotaci n de bits
    uint8_t r = (semilla % 6) + 1; // Rango de 1 a 6
    return r;
}
```

Se implementa un retardo utilizando bucles anidados. Esta función es utilizada para mantener encendidos los LEDs por un corto periodo de tiempo antes de apagarlos, simulando el efecto de mostrar una cara del dado.

```
void delay(unsigned int intervaloTiempo) {
    unsigned int contadorExterno, contadorInterno;
    for (contadorExterno = 0; contadorExterno < intervaloTiempo; contadorExterno++)
        for (contadorInterno = 0; contadorInterno < 1275; contadorInterno++);
}
```

En la función principal se configuran los pines del microcontrolador: el pin `GP5` se utiliza como entrada para el botón, mientras que el resto se configura como salidas para controlar los LEDs. Cuando el usuario presiona el botón, se genera un número aleatorio con la función **`rand_con_timer()`** y se activa el conjunto de LEDs correspondiente a la cara del dado obtenida. Si el botón no está presionado, se apagan todos los LEDs.

```
void main(void) {
    TRISIO = 0b00100000; // GP5 como entrada, el resto como salida
    GPIO = 0x00;         // Inicializa los pines en bajo
    OPTION_REG = 0b00000111; // Activa TMR0 con preescalador 1:256

    unsigned int tiempoEspera = 200;
    unsigned int numeroAleatorio = 0;

    while (1) {
        if (GP5) {
            numeroAleatorio = rand_con_timer();
            switch (numeroAleatorio) {
                case 1:
                    GP1 = 1;
                    delay(tiempoEspera);
                    GP1 = 0;
                    break;
                case 2:
                    GP0 = 1;
                    delay(tiempoEspera);
                    GP0 = 0;
                    break;
                case 3:
                    GPIO = 0b00000011;
                    delay(tiempoEspera);
                    GPIO = 0;
                    break;
                case 4:
                    GPIO = 0b00000101;
                    delay(tiempoEspera);
                    GPIO = 0;
                    break;
                case 5:
                    GPIO = 0b00000111;
                    delay(tiempoEspera);
                    GPIO = 0;
                    break;
                case 6:
                    GPIO = 0b00010101;
                    delay(tiempoEspera);
                    GPIO = 0;
                    break;
            }
```

```
        } else {
            GPIO = 0x00;
        }
    }
}
```

Este diseño cumple con los objetivos del laboratorio, permitiendo simular el lanzamiento de un dado mediante la activación de un botón. La incorporación del temporizador interno como fuente de entropía mejora la aleatoriedad del número generado. Además, el uso de estructuras simples y control directo del hardware asegura compatibilidad con los recursos limitados del `PIC12F683`.

3.1.1. Diagrama de Flujo

A continuación se puede observar el diagrama de flujo del programa explicado en la sección anterior.

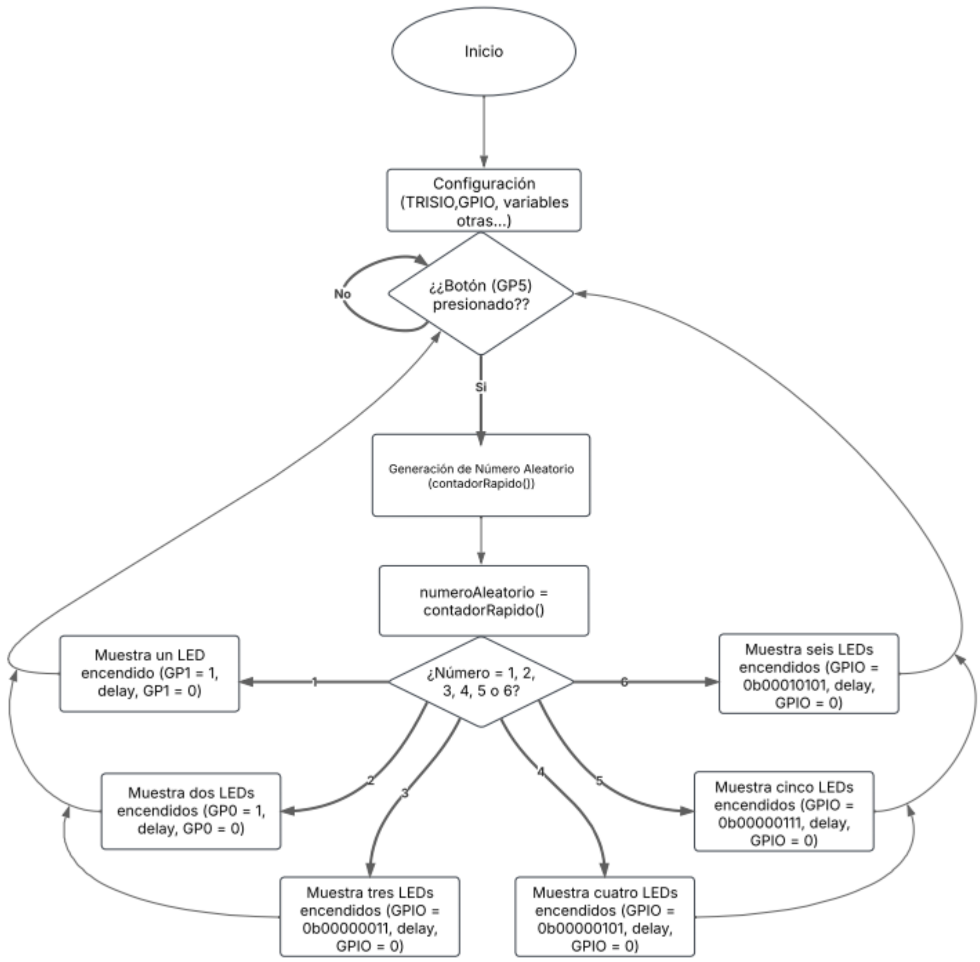


Figura 4: Diagrama de flujo del programa.

3.2. Diseño del Circuito

En este apartado se describen los fundamentos del diseño eléctrico del sistema, incluyendo la selección de valores para las resistencias, el esquema de conexión de los LEDs y la estrategia utilizada para mitigar los efectos del rebote en la lectura del botón.

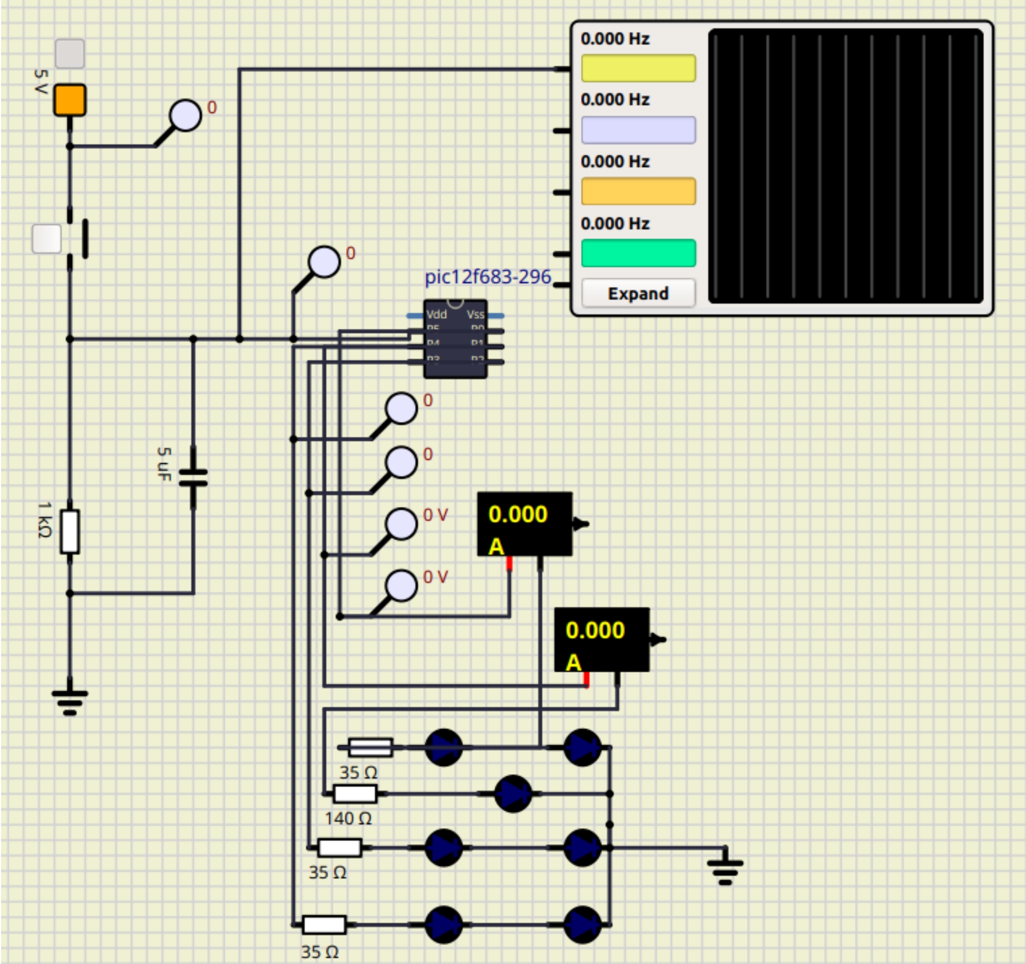


Figura 5: Circuito completo.

3.2.1. Diseño General

Los componentes y las conexiones se han diseñado para asegurar una correcta operación del sistema, garantizando tanto la funcionalidad esperada como la protección de los elementos electrónicos.

El circuito es alimentado por una fuente de 5V, ya que es el voltaje de operación recomendado para el PIC12F683 y los demás componentes. Se pueden observar dos conexiones a tierra en el circuito: una utilizada para la referencia del microcontrolador y otra asociada al circuito de LEDs, lo que permite un retorno de corriente adecuado y minimiza problemas de ruido eléctrico.

3.2.2. Diseño de los LEDs y resistencias limitadoras

Los LEDs están dispuestos en un patrón que representa las caras de un dado convencional de seis caras. Esto permite que, dependiendo del número generado por el microcontrolador, se encienda un conjunto específico de LEDs para mostrar visualmente el resultado.

Cada LED tiene en serie una resistencia limitadora para controlar la corriente que circula a través de él. Esto es necesario para evitar daños en los LEDs y asegurar su correcto funcionamiento. En este caso, se han utilizado resistencias de 35Ω y 140Ω, seleccionadas para mantener una corriente adecuada y prolongar la vida útil de los LEDs. Las resistencias de protección se calcularon de la siguiente manera:

Para LEDs en serie [6]:

$$R = \frac{V_{DD} - 2 \cdot V_{LED}}{I_{Max}} = \frac{4{,}89 - 2 \cdot 2{,}1}{20mA} = 34{,}5\Omega$$

Para LED solo [6]:

$$R = \frac{V_{DD} - 2 \cdot V_{LED}}{I_{Max}} = \frac{4{,}89 - 2{,}1}{20mA} = 139{,}5\Omega$$

3.2.3. Entradas y salidas del microcontrolador

El microcontrolador `PIC12F683` tiene asignadas las siguientes funciones:

- **Entrada**: Un botón conectado a `GP5`, el cual permite que el usuario "lance" el dado. Se ha implementado un circuito de *debounce* con un filtro RC ($1k\Omega$ **y 5µF**) para evitar lecturas erróneas debido a rebotes mecánicos.
- **Salidas**: Se utilizan pines `GP0, GP1, GP2, GP3, GP4` para controlar los LEDs y representar las diferentes caras del dado.

3.2.4. Diseño de lectura contra rebote

Para evitar lecturas erróneas causadas por los rebotes mecánicos del botón en `GP5`, se implementó un filtro RC con una resistencia de $1k\Omega$ y un capacitor de $5\mu F$. Este filtro suaviza la señal y garantiza una transición estable al detectar una pulsación. La constante de tiempo del circuito se calcula como:

$$\tau = R \cdot C = (1k\Omega) \cdot (5\mu F) = 5ms$$

Dado que los rebotes típicos duran entre 5 y 20 ms, el tiempo de estabilización aproximado es:

$$t_{\text{estable}} \approx 5 \cdot \tau = 25ms$$

Este valor permite filtrar correctamente los rebotes sin introducir retardos significativos en la detección del botón.

3.2.5. Mediciones y verificación del circuito

Para verificar el correcto funcionamiento del circuito, se han incluido instrumentos de medición:

- **Medidores de corriente**: Se han colocado amperímetros en los puntos de salida del microcontrolador para medir la corriente suministrada a los LEDs. Esto permite verificar que las resistencias limitadoras están cumpliendo su función y que la corriente no excede los límites del microcontrolador.
- **Medidor de voltaje**: Se ha incorporado un osciloscopio digital para monitorear el comportamiento de la señal de entrada al microcontrolador, lo que permite analizar si el efecto rebote ha sido eliminado. Además de los voltímetros de salida en cada pin para saber el voltaje con el que se alimenta cada LED.

Este diseño asegura un funcionamiento confiable y eficiente del dado electrónico, optimizando el uso de los recursos del `PIC12F683` y garantizando una correcta representación visual del número generado.

4. Análisis de Resultados

En este apartado se presentan los resultados obtenidos en la simulación del dado electrónico, verificando el correcto funcionamiento del sistema en los seis posibles resultados y la efectividad del filtro *debounce* en la entrada del botón.

4.1. Verificación de las seis caras del dado

Para validar el correcto funcionamiento del dado electrónico, se realizaron pruebas activando el botón de entrada y observando la salida de los LEDs en cada uno de los seis casos posibles. Se verificó que, para cada número generado por el microcontrolador, se enciende la configuración correcta de LEDs que representa la cara del dado correspondiente.

A continuación, se describen las configuraciones obtenidas:

- **Caso 1**: Se enciende un solo LED central.

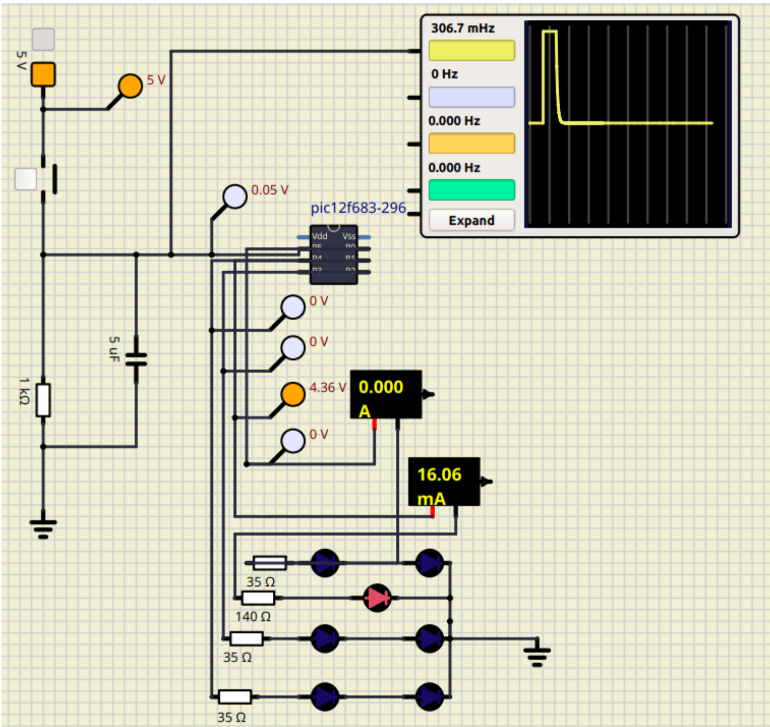


Figura 6: Circuito caso 1.

- **Caso 2**: Se encienden dos LEDs en esquinas opuestas.

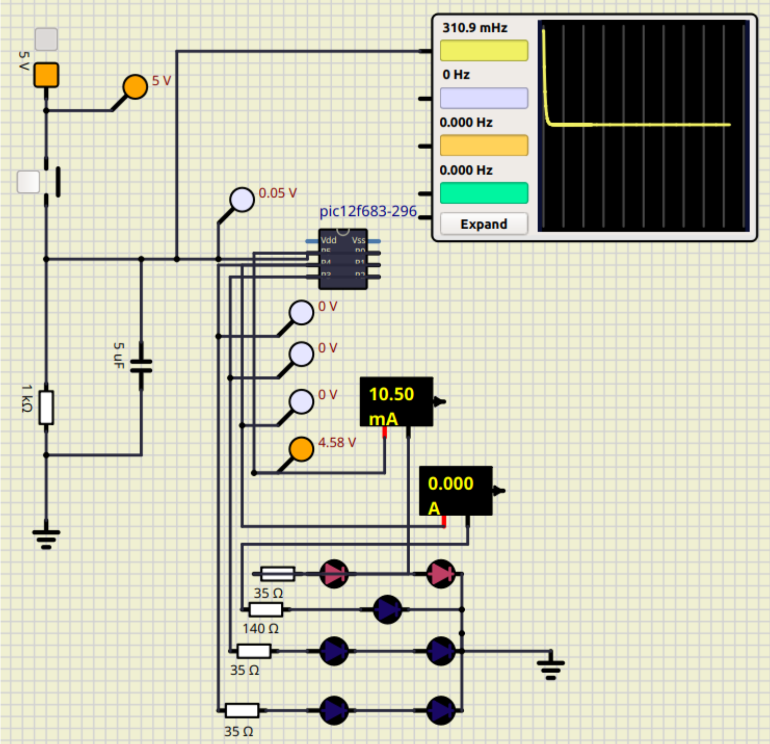


Figura 7: Circuito caso 2.

- **Caso 3**: Se encienden tres LEDs en disposición diagonal.

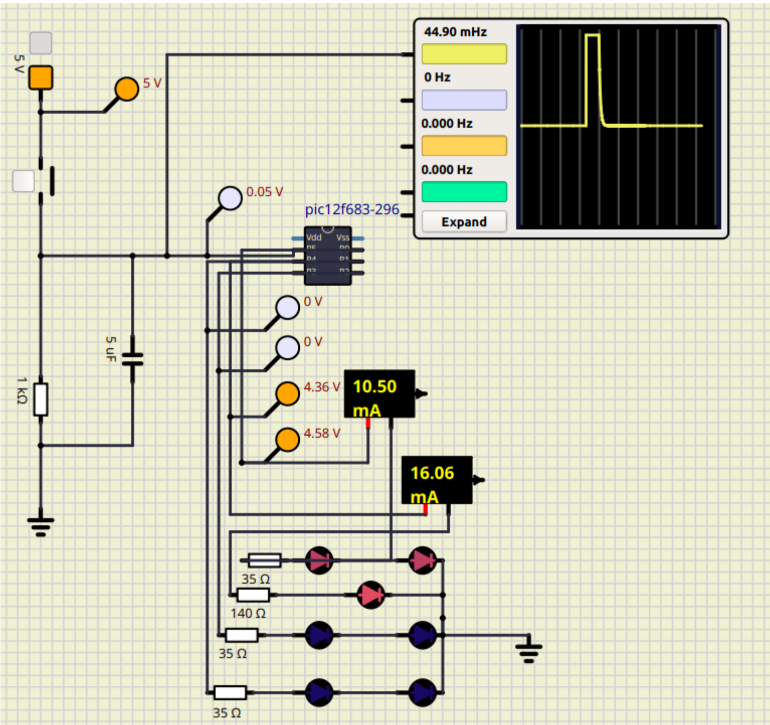


Figura 8: Circuito caso 3.

- **Caso 4**: Se encienden cuatro LEDs en las esquinas.

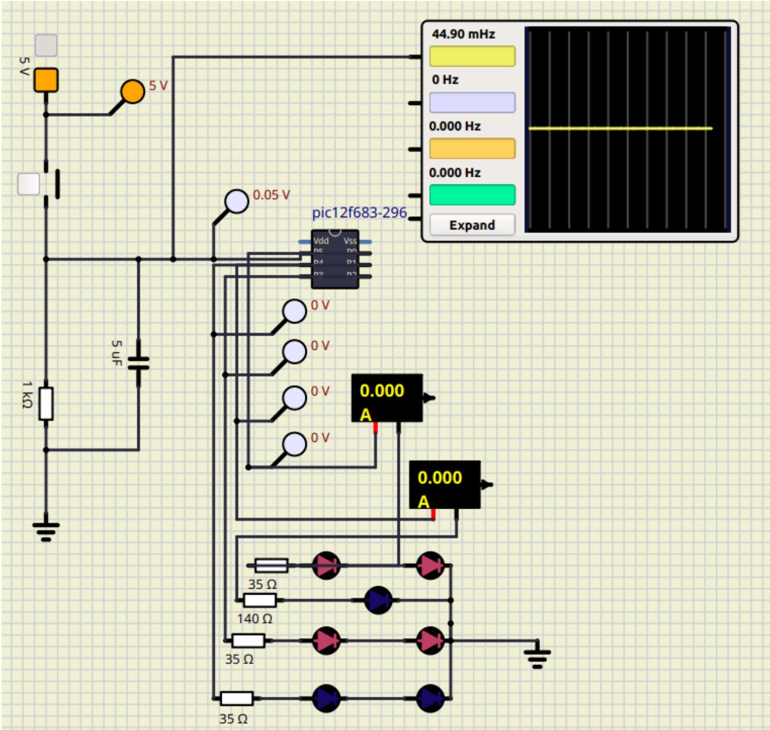


Figura 9: Circuito caso 4.

- **Caso 5**: Se encienden cinco LEDs, formando un patrón con el LED central encendido.

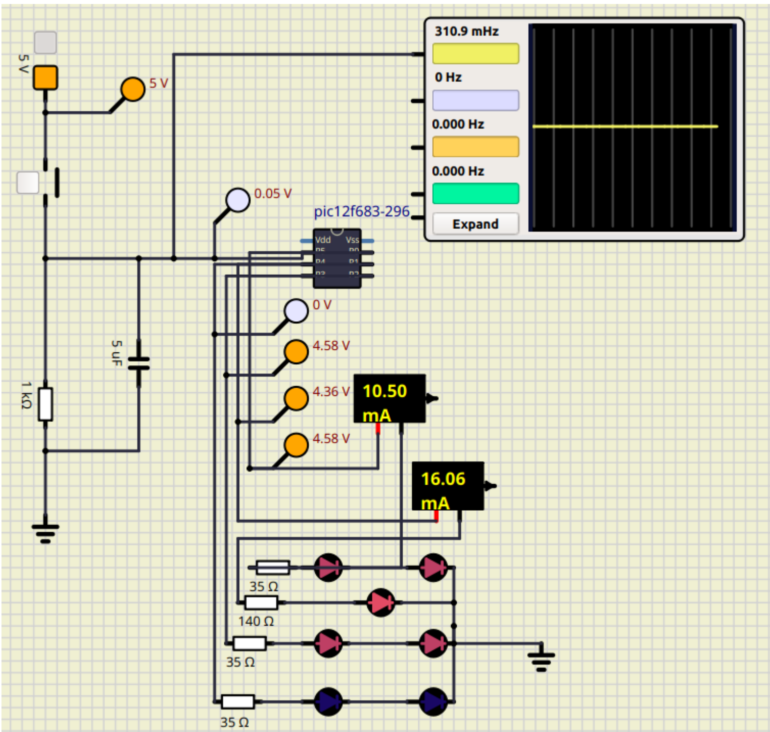


Figura 10: Circuito caso 5.

- **Caso 6**: Se encienden los seis LEDs del arreglo.

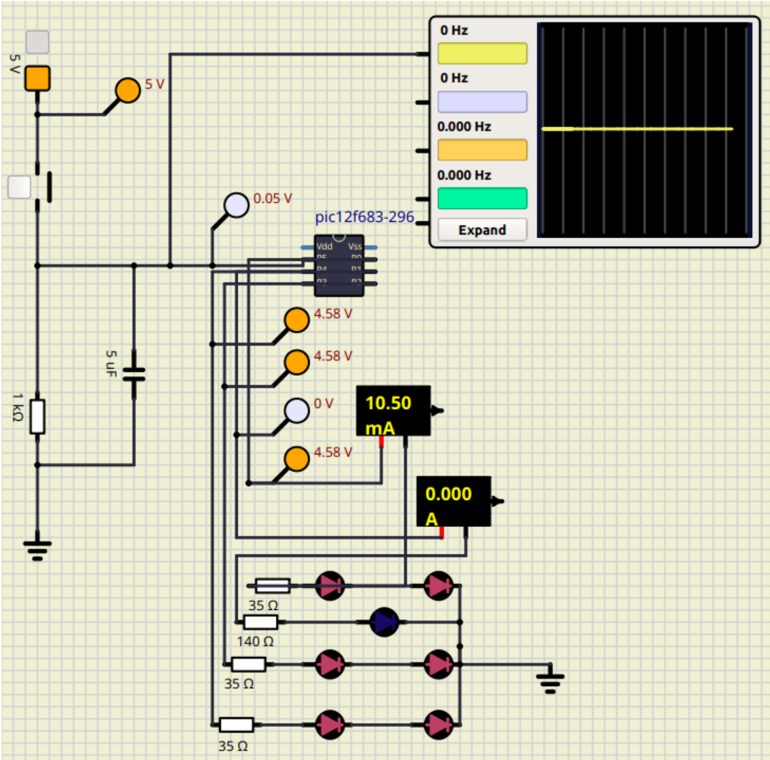


Figura 11: Circuito caso 6.

Los resultados obtenidos muestran que el sistema responde correctamente a la generación de números aleatorios, encendiendo los LEDs de acuerdo con la cara del dado generada.

4.2. Verificación del efecto rebote

Para comprobar la efectividad del sistema de prevención de rebotes mecánicos, se utilizó un osciloscopio digital para visualizar la señal del botón de entrada antes y después del filtro RC implementado.

En contraste, después de aplicar el filtro RC ($1k\Omega$ y 5µF), la señal procesada se muestra estable y libre de fluctuaciones, confirmando la efectividad del sistema.

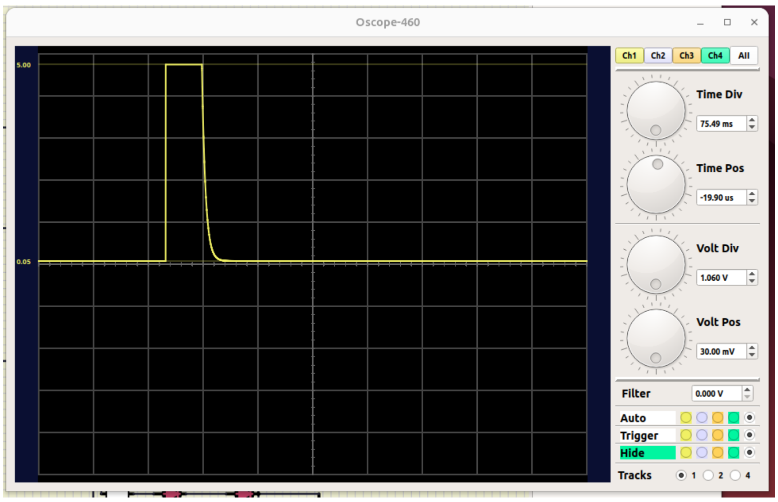


Figura 12: Señal sin efecto rebote.

Los resultados muestran que la implementación del filtro RC ha logrado estabilizar la señal de entrada, permitiendo una detección confiable del botón sin la necesidad de un procesamiento adicional en software.

4.3. Conclusión de los resultados

Los experimentos realizados confirman que el sistema funciona según lo esperado:

- Las seis configuraciones de LEDs se activan correctamente según el número generado.
- La señal del botón es estabilizada de manera efectiva mediante el filtro RC, eliminando los efectos de rebote.

Por lo tanto, el diseño del circuito cumple con los objetivos del laboratorio, logrando una simulación funcional y precisa de un dado electrónico con el microcontrolador `PIC12F683`.

5. Conclusiones y Recomendaciones

5.1. Conclusiones

El desarrollo de este laboratorio permitió la implementación de un dado electrónico utilizando el microcontrolador `PIC12F683`, demostrando que es posible generar números aleatorios y controlar la activación de LEDs con recursos limitados. A pesar de la baja capacidad de memoria y procesamiento de este microcontrolador, se logró un diseño eficiente y funcional, cumpliendo con los requerimientos del experimento.

El uso del temporizador interno `TMR0` como fuente de entropía permitió mejorar la aleatoriedad en la generación de números, evitando secuencias predecibles en el encendido de los LEDs. Además, se verificó que las seis configuraciones posibles del dado se activan correctamente según el número generado, asegurando la correspondencia entre la salida visual y la lógica implementada en el código.

Desde el punto de vista del hardware, el uso de resistencias limitadoras en los LEDs permitió evitar sobrecorrientes que pudieran dañar tanto los LEDs como el microcontrolador. Asimismo, la implementación de un filtro RC ($1k\Omega$ y 5µF) en la entrada del botón demostró ser efectiva para la eliminación de rebotes mecánicos, logrando una señal de entrada estable y confiable.

El análisis mediante herramientas de simulación permitió validar el correcto funcionamiento del sistema antes de una implementación física, verificando la correspondencia entre las señales esperadas y los resultados obtenidos en la simulación. Esto permitió optimizar el diseño y asegurar su funcionamiento sin necesidad de realizar múltiples pruebas en hardware real.

5.2. Recomendaciones

Para futuros proyectos similares, se recomienda considerar los siguientes aspectos:

- Consulta de la hoja de datos del microcontrolador: Es fundamental revisar la documentación técnica del PIC12F683 para comprender su configuración, capacidades eléctricas y restricciones, evitando posibles errores en la programación o daños en el circuito.

- Uso de filtros adecuados para entrada de botones: Si bien el filtro RC utilizado resolvió el problema del rebote, es importante considerar que puede introducir retardos en la detección del botón. En aplicaciones más exigentes, se podría evaluar una combinación de filtrado por hardware y software.

- Protección del circuito: La inclusión de resistencias en serie con los LEDs y el uso de configuraciones pull-down en los pines de entrada son estrategias esenciales para garantizar la estabilidad y protección del sistema, evitando sobrecargas o estados indeterminados en la entrada del microcontrolador.

- Validación en simulación antes de la implementación física: La herramienta SimulIDE permitió verificar el comportamiento del circuito antes de una hipotética implementación en hardware real. Se recomienda siempre realizar pruebas en simulación para detectar posibles errores y optimizar el diseño sin riesgo de dañar componentes físicos.

Referencias

[1] M. T. Inc., *PIC12F683 Data Sheet*, 2007, Último acceso: 20 de marzo de 2025. [Online]. Available: https://ww1.microchip.com/downloads/en/devicedoc/41211d_.pdf

[2] C. Cibernética, "Cr cibernética - tienda de componentes electrónicos," 2025, Último acceso: 20 de marzo de 2025. [Online]. Available: https://www.crcibernetica.com/

[3] S. C. Rica, "Steren costa rica - electrónica y tecnología," 2025, Último acceso: 20 de marzo de 2025. [Online]. Available: https://www.steren.cr/

[4] M. Electronics, "Microchip pic12f683 - microcontrolador de 8 bits," 2025, Último acceso: 20 de marzo de 2025. [Online]. Available: https://www.mouser.co.cr/ProductDetail/Microchip-Technology/PIC12F683-I-P?qs=hklUZQQMghM0LQewpz5IdQ%3D%3D&srsltid=AfmBOoq0c9vVQwwyIGFXtRMn-VHmrOs4A1lIIidz6a-MI2kqA_IYqf6o

[5] Mouser Electronics, "Capacitors - 5 µF Selection," 2025, Último acceso: 21 de marzo de 2025. [Online]. Available: https://www.mouser.co.cr/c/?capacitance=5%20uF&srsltid=AfmBOook3eiVmcSMtzlavynUT34fYEzO_t81PGDidhI4EHsAjETaoFk8

[6] AG Electrónica, "LEDY5DYT - Datasheet," 2025, Último acceso: 21 de marzo de 2025. [Online]. Available: https://agelectronica.lat/pdfs/textos/L/LEDY5DYT.PDF

6. Apéndices

En esta sección se presentan documentos de referencia utilizados en el desarrollo del laboratorio, incluyendo hojas de datos de los componentes electrónicos empleados, como el microcontrolador PIC12F683, resistencias y LEDs. Estos documentos contienen información técnica relevante sobre las características eléctricas, diagramas de conexión y parámetros de funcionamiento de cada componente, lo que permite una mejor comprensión del diseño del circuito y su implementación.

PIC12F683
Data Sheet

8-Pin Flash-Based, 8-Bit
CMOS Microcontrollers with
nanoWatt Technology

PIC12F683

8-Pin Flash-Based, 8-Bit CMOS Microcontrollers with nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM Retention: > 40 years

Low-Power Features:

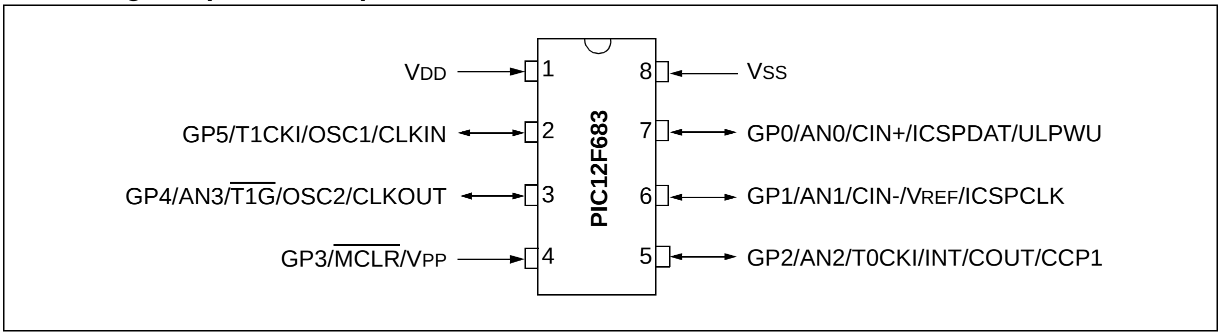
- Standby Current:
  - 50 nA @ 2.0V, typical
- Operating Current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 220 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Peripheral Features:

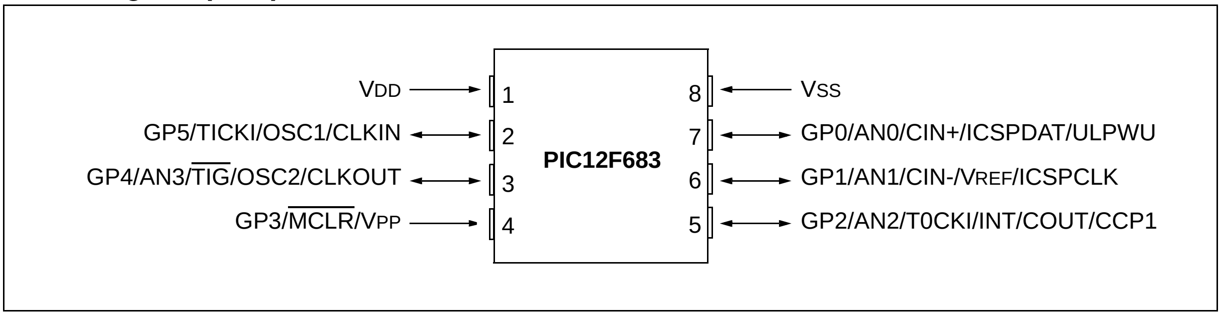
- 6 I/O pins with individual direction control:
  - High current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
  - Ultra Low-Power Wake-up on GP0
- Analog Comparator module with:
  - One analog comparator
  - Programmable on-chip voltage reference (CVREF) module (% of VDD)
  - Comparator inputs and output externally accessible
- A/D Converter:
  - 10-bit resolution and 4 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module:
  - 16-bit Capture, max resolution 12.5 ns
  - Compare, max resolution 200 ns
  - 10-bit PWM, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit
	Flash (words)	SRAM (bytes)	EEPROM (bytes)				
PIC12F683	2048	128	256	6	4	1	2/1

8-Pin Diagram (PDIP, SOIC)



8-Pin Diagram (DFN)



8-Pin Diagram (DFN-S)

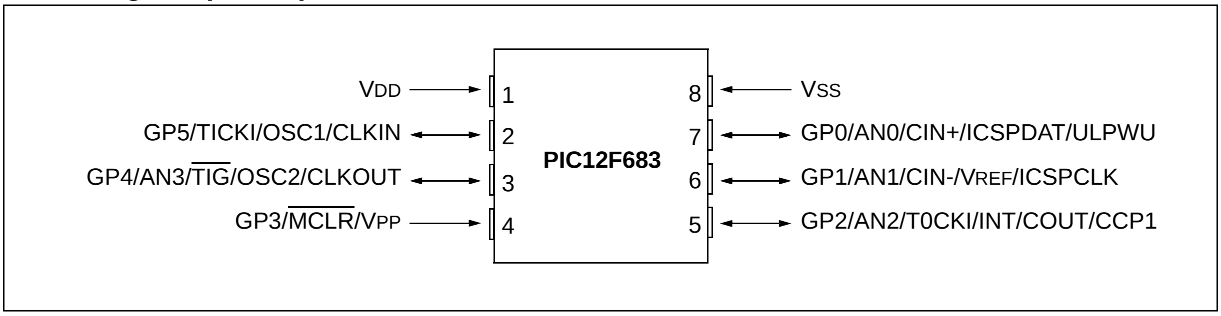


TABLE 1: 8-PIN SUMMARY

I/O	Pin	Analog	Comparators	Timer	CCP	Interrupts	Pull-ups	Basic
GP0	7	AN0	CIN+	—	—	IOC	Y	ICSPDAT/ULPWU
GP1	6	AN1/VREF	CIN-	—	—	IOC	Y	ICSPCLK
GP2	5	AN2	COUT	T0CKI	CCP1	INT/IOC	Y	—
GP3(1)	4	—	—	—	—	IOC	Y(2)	$\overline{\text{MCLR}}$/VPP
GP4	3	AN3	—	$\overline{\text{T1G}}$	—	IOC	Y	OSC2/CLKOUT
GP5	2	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
—	1	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external $\overline{\text{MCLR}}$.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com** or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

NOTES:

1.0 DEVICE OVERVIEW

The PIC12F683 is covered by this data sheet. It is available in 8-pin PDIP, SOIC and DFN-S packages. Figure 1-1 shows a block diagram of the PIC12F683 device. Table 1-1 shows the pinout description.

FIGURE 1-1: PIC12F683 BLOCK DIAGRAM

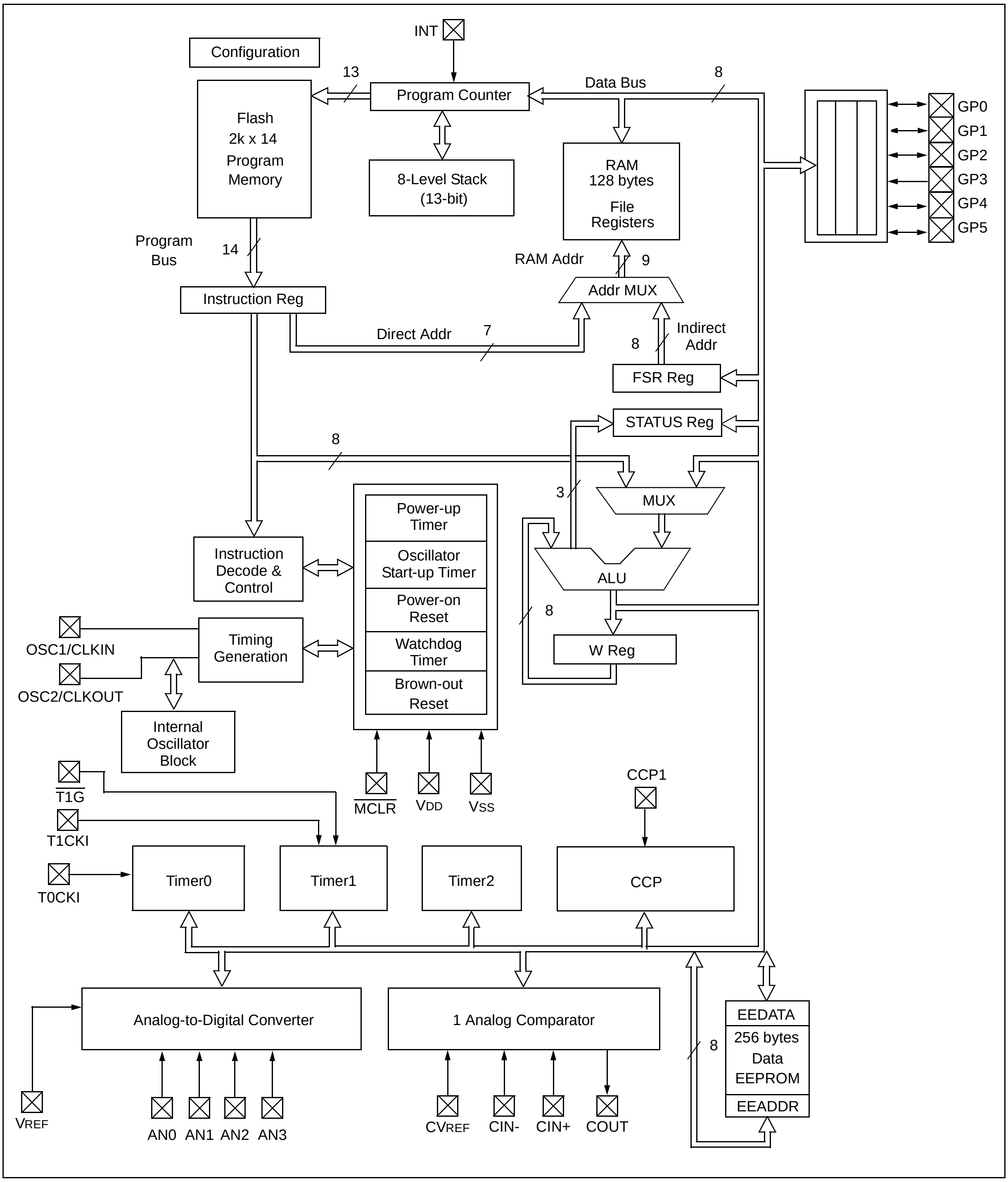


TABLE 1-1: PIC12F683 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
VDD	VDD	Power	—	Positive supply
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
GP4/AN3/$\overline{\text{T1G}}$/OSC2/CLKOUT	GP4	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	$\overline{\text{T1G}}$	ST	—	Timer1 gate
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
GP3/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	GPIO input with interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
	VPP	HV	—	Programming voltage
GP2/AN2/T0CKI/INT/COUT/CCP1	GP2	ST	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	COUT	—	CMOS	Comparator 1 output
	CCP1	ST	CMOS	Capture input/Compare output/PWM output
GP1/AN1/CIN-/VREF/ICSPCLK	GP1	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	CIN-	AN	—	Comparator 1 input
	VREF	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
GP0/AN0/CIN+/ICSPDAT/ULPWU	GP0	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	CIN+	AN	—	Comparator 1 input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
	ULPWU	AN	—	Ultra Low-Power Wake-up input
VSS	VSS	Power	—	Ground reference

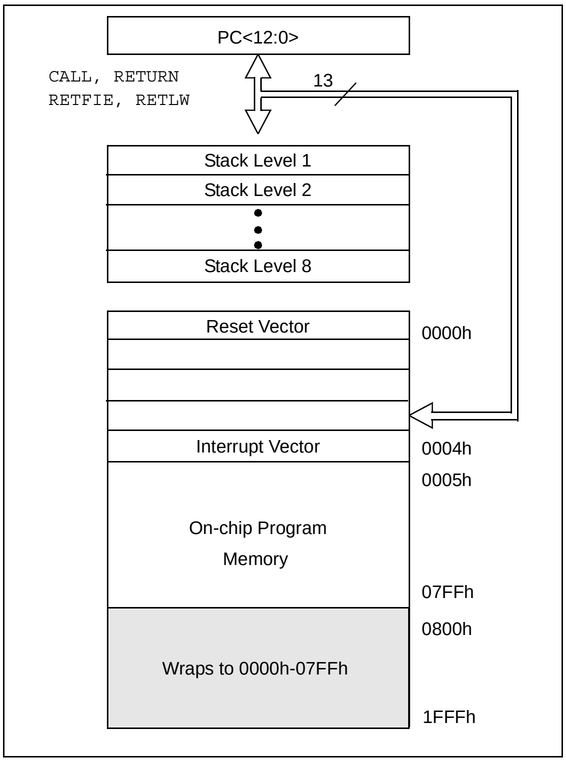
Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; HV = High Voltage; XTAL = Crystal

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F683 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC12F683 is physically implemented. Accessing a location above these boundaries will cause a wraparound within the first 2K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F683



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. RP0 of the STATUS register is the bank select bit.

<u>RP0</u>

0 → Bank 0 is selected

1 → Bank 1 is selected

Note:	The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 in the PIC12F683. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE PIC12F683

BANK 0	File Address	BANK 1	File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h
TMR0	01h	OPTION_REG	81h
PCL	02h	PCL	82h
STATUS	03h	STATUS	83h
FSR	04h	FSR	84h
GPIO	05h	TRISIO	85h
	06h		86h
	07h		87h
	08h		88h
	09h		89h
PCLATH	0Ah	PCLATH	8Ah
INTCON	0Bh	INTCON	8Bh
PIR1	0Ch	PIE1	8Ch
	0Dh		8Dh
TMR1L	0Eh	PCON	8Eh
TMR1H	0Fh	OSCCON	8Fh
T1CON	10h	OSCTUNE	90h
TMR2	11h		91h
T2CON	12h	PR2	92h
CCPR1L	13h		93h
CCPR1H	14h		94h
CCP1CON	15h	WPU	95h
	16h	IOC	96h
	17h		97h
WDTCON	18h		98h
CMCON0	19h	VRCON	99h
CMCON1	1Ah	EEDAT	9Ah
	1Bh	EEADR	9Bh
	1Ch	EECON1	9Ch
	1Dh	EECON2(1)	9Dh
ADRESH	1Eh	ADRESL	9Eh
ADCON0	1Fh	ANSEL	9Fh
General Purpose Registers 96 Bytes	20h–7Fh	General Purpose Registers 32 Bytes	A0h–BFh
			C0h–EFh
		Accesses 70h-7Fh	F0h–FFh

Shaded: Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

TABLE 2-1: PIC12F683 SPECIAL REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	17, 90
01h	TMR0	Timer0 Module Register								xxxx xxxx	41, 90
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17, 90
03h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	11, 90
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	17, 90
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	31, 90
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	17, 90
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	13, 90
0Ch	PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	15, 90
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	44, 90
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	44, 90
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	47, 90
11h	TMR2	Timer2 Module Register								0000 0000	49, 90
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	50, 90
13h	CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	76, 90
14h	CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	76, 90
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	75, 90
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	97, 90
19h	CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	56, 90
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	57, 90
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	61,90
1Fh	ADCON0	ADFM	VCFG	—	—	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	00-- 0000	65,90

Legend: – = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

TABLE 2-2: PIC12F683 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								`xxxx xxxx`	17, 90
81h	OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	`1111 1111`	12, 90
82h	PCL	Program Counter's (PC) Least Significant Byte								`0000 0000`	17, 90
83h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	`0001 1xxx`	11, 90
84h	FSR	Indirect Data Memory Address Pointer								`xxxx xxxx`	17, 90
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	`--11 1111`	32, 90
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					`---0 0000`	17, 90
8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	`0000 0000`	13, 90
8Ch	PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	`000- 0000`	14, 90
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	`--01 --qq`	16, 90
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS(2)	HTS	LTS	SCS	`-110 x000`	20, 90
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	`---0 0000`	24, 90
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Module Period Register								`1111 1111`	49, 90
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	WPU(3)	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	`--11 -111`	34, 90
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	`--00 0000`	34, 90
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	`0-0- 0000`	58, 90
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	`0000 0000`	71, 90
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	`0000 0000`	71, 90
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	`---- x000`	72, 91
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								`---- ----`	72, 91
9Eh	ADRESL	Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result								`xxxx xxxx`	66, 91
9Fh	ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	`-000 1111`	33, 91

Legend: – = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: OSTS bit of the OSCCON register reset to '`0`' with Dual Speed Start-up and LP, HS or XT selected as the oscillator.

3: GP3 pull-up is enabled when MCLRE is '`1`' in the Configuration Word register.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- Arithmetic status of the ALU
- Reset status
- Bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the “Instruction Set Summary”.

> **Note 1:** Bits IRP and RP1 of the STATUS register are not used by the PIC12F683 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
>
> **2:** The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** This bit is reserved and should be maintained as ‘`0`’

bit 6 **RP1:** This bit is reserved and should be maintained as ‘`0`’

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
`1` = Bank 1 (80h – FFh)
`0` = Bank 0 (00h – 7Fh)

bit 4 **$\overline{\text{TO}}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions), For $\overline{\text{Borrow}}$, the polarity is reversed.
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit(1) (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- TMR0/WDT prescaler
- External GP2/INT interrupt
- TMR0
- Weak pull-ups on GPIO

Note:	To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit of the OPTION register to '1' See **Section 5.1.3 "Software Programmable Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	**$\overline{\text{GPPU}}$:** GPIO Pull-up Enable bit 1 = GPIO pull-ups are disabled 0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register
bit 6	**INTEDG:** Interrupt Edge Select bit 1 = Interrupt on rising edge of INT pin 0 = Interrupt on falling edge of INT pin
bit 5	**T0CS:** Timer0 Clock Source Select bit 1 = Transition on T0CKI pin 0 = Internal instruction cycle clock (FOSC/4)
bit 4	**T0SE:** Timer0 Source Edge Select bit 1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-high transition on T0CKI pin
bit 3	**PSA:** Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module
bit 2-0	**PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available. See **Section 12.6 "Watchdog Timer (WDT)"** for more information.

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** GP2/INT External Interrupt Enable bit
1 = Enables the GP2/INT external interrupt
0 = Disables the GP2/INT external interrupt

bit 3 **GPIE:** GPIO Change Interrupt Enable bit[(1)]
1 = Enables the GPIO change interrupt
0 = Disables the GPIO change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit[(2)]
1 = Timer0 register has overflowed (must be cleared in software)
0 = Timer0 register did not overflow

bit 1 **INTF:** GP2/INT External Interrupt Flag bit
1 = The GP2/INT external interrupt occurred (must be cleared in software)
0 = The GP2/INT external interrupt did not occur

bit 0 **GPIF:** GPIO Change Interrupt Flag bit
1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software)
0 = None of the GPIO <5:0> pins have changed state

Note 1: IOC register must also be enabled.
2: T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.

2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

Note:	Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **CMIE:** Comparator Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the oscillator fail interrupt
0 = Disables the oscillator fail interrupt

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started

bit 6 **ADIF:** A/D Interrupt Flag bit
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **CMIF:** Comparator Interrupt Flag bit
1 = Comparator 1 output has changed (must be cleared in software)
0 = Comparator 1 output has not changed

bit 2 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = System oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = System clock operating

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

2.2.2.6 PCON Register

The Power Control (PCON) register contains flag bits (see Table 12-2) to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Brown-out Reset ($\overline{\text{BOR}}$)
- Watchdog Timer Reset (WDT)
- External $\overline{\text{MCLR}}$ Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the $\overline{\text{BOR}}$.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	R/W-0	R/W-1	U-0	U-0	R/W-0	R/W-x
—	—	ULPWUE	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **ULPWUE:** Ultra Low-Power Wake-Up Enable bit
1 = Ultra Low-Power Wake-up enabled
0 = Ultra Low-Power Wake-up disabled

bit 4 **SBOREN:** Software BOR Enable bit(1)
1 = BOR enabled
0 = BOR disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

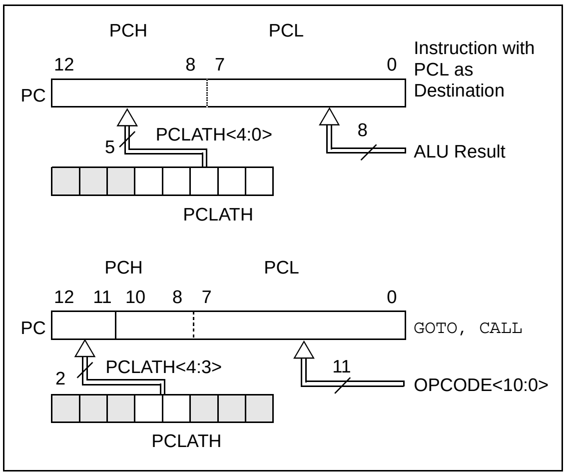
bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the $\overline{\text{BOR}}$.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a `CALL` or `GOTO` instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed `GOTO` is accomplished by adding an offset to the program counter (`ADDWF PCL`). When performing a table read using a computed `GOTO` method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note *AN556, "Implementing a Table Read"* (DS00556).

2.3.2 STACK

The PIC12F683 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a `CALL` instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or a `RETFIE` instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1:	There are no Status bits to indicate stack overflow or stack underflow conditions.
2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL`, `RETURN`, `RETLW` and `RETFIE` instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

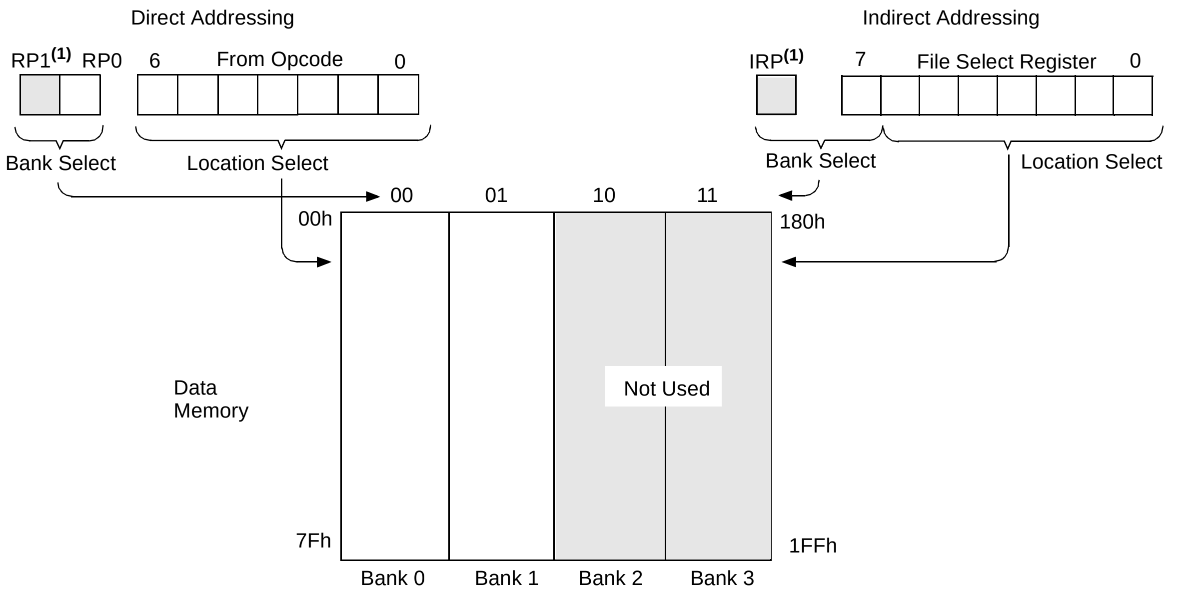
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit of the STATUS register, as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
        MOVLW   0x20     ;initialize pointer
        MOVWF   FSR      ;to RAM
NEXT    CLRF    INDF     ;clear INDF register
        INCF    FSR      ;inc pointer
        BTFSS   FSR,4    ;all done?
        GOTO    NEXT     ;no clear next
CONTINUE                 ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC12F683



For memory map detail, see Figure 2-2.

Note 1: The RP1 and IRP bits are reserved; always maintain these bits clear.

3.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

3.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the Oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

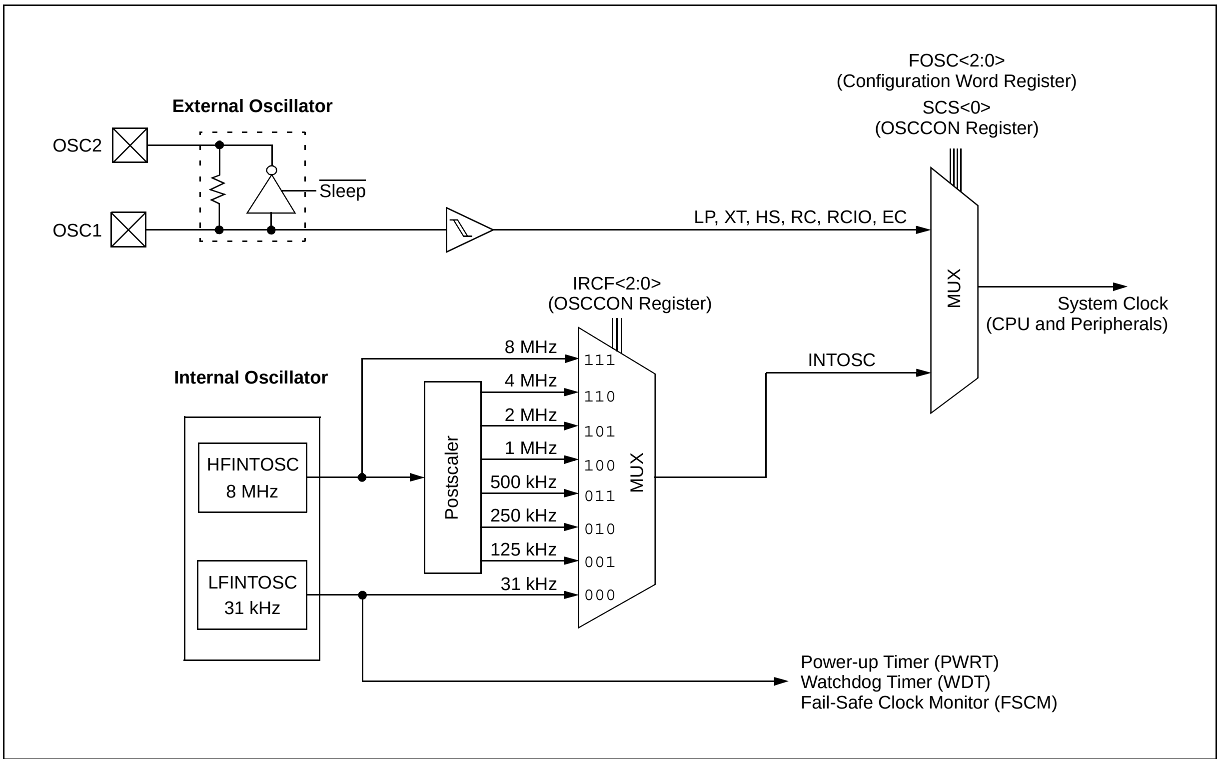
- Selectable system clock source between external or internal via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.

The Oscillator module can be configured in one of eight clock modes.

1. EC – External clock with I/O on OSC2/CLKOUT.
2. LP – 32 kHz Low-Power Crystal mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with FOSC/4 output on OSC2/CLKOUT.
6. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
7. INTOSC – Internal oscillator with FOSC/4 output on OSC2 and I/O on OSC1/CLKIN.
8. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The internal clock can be generated from two internal oscillators. The HFINTOSC is a calibrated high-frequency oscillator. The LFINTOSC is an uncalibrated low-frequency oscillator.

FIGURE 3-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



3.2 Oscillator Control

The Oscillator Control (OSCCON) register (Figure 3-1) controls the system clock and frequency selection options. The OSCCON register contains the following bits:

- Frequency selection bits (IRCF)
- Frequency Status bits (HTS, LTS)
- System clock control bits (OSTS, SCS)

REGISTER 3-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R/W-1	R/W-1	R/W-0	R-1	R-0	R-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS(1)	HTS	LTS	SCS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits
111 = 8 MHz
110 = 4 MHz (default)
101 = 2 MHz
100 = 1 MHz
011 = 500 kHz
010 = 250 kHz
001 = 125 kHz
000 = 31 kHz (LFINTOSC)

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit(1)
1 = Device is running from the external clock defined by FOSC<2:0> of the Configuration Word register
0 = Device is running from the internal oscillator (HFINTOSC or LFINTOSC)

bit 2 **HTS:** HFINTOSC Status bit (High Frequency – 8 MHz to 125 kHz)
1 = HFINTOSC is stable
0 = HFINTOSC is not stable

bit 1 **LTS:** LFINTOSC Stable bit (Low Frequency – 31 kHz)
1 = LFINTOSC is stable
0 = LFINTOSC is not stable

bit 0 **SCS:** System Clock Select bit
1 = Internal oscillator is used for system clock
0 = Clock source defined by FOSC<2:0> of the Configuration Word register

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.

3.3 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bit of the OSCCON register. See **Section 3.6 "Clock Switching"** for additional information.

3.4 External Clock Modes

3.4.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 3.7 "Two-Speed Clock Start-up Mode"**).

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

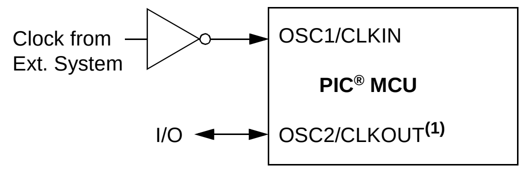
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	31 kHz 125 kHz to 8 MHz	Oscillator Warm-Up Delay (T_{WARM})
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz	1 cycle of each
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)
LFINTOSC (31 kHz)	HFINTOSC	125 kHz to 8 MHz	1 μs (approx.)

3.4.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Alternate pin functions are listed in the ***Device Overview***.

3.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 3-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

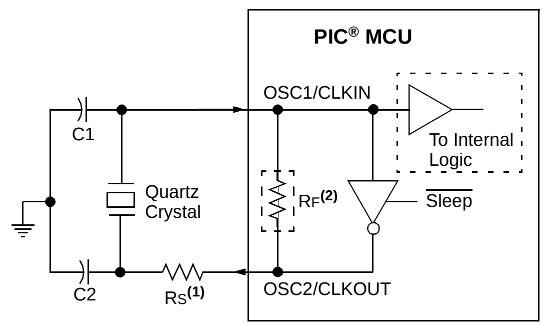
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

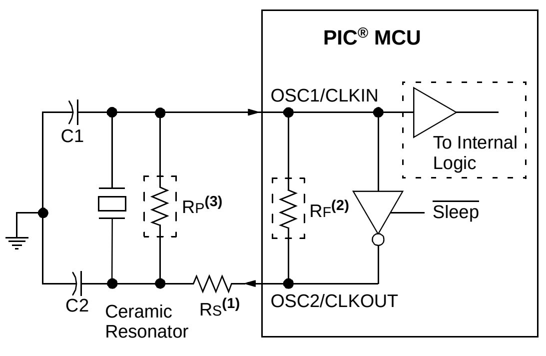
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

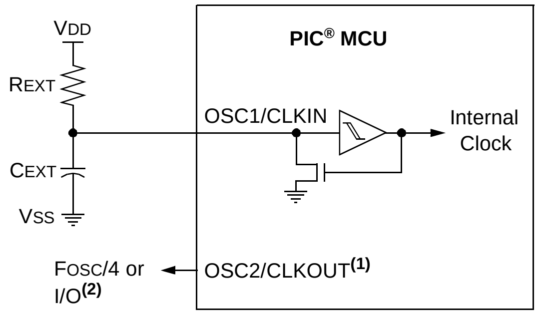
3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

3.4.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.

FIGURE 3-5: EXTERNAL RC MODES



Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ, <3V
3 kΩ ≤ REXT ≤ 100 kΩ, 3-5V
CEXT > 20 pF, 2-5V

Note 1: Alternate pin functions are listed in the ***Device Overview***.
2: Output depends upon RC or RCIO clock mode.

In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.5 Internal Clock Modes

The Oscillator module has two independent, internal oscillators that can be configured or selected as the system clock source.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 3-2).
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit of the OSCCON register. See **Section 3.6 "Clock Switching"** for more information.

3.5.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 12.0 "Special Features of the CPU"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

3.5.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 3-2).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the IRCF<2:0> bits of the OSCCON register. See **Section 3.5.4 "Frequency Select Bits (IRCF)"** for more information.

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz by setting the IRCF<2:0> bits of the OSCCON register ≠ `000`. Then, set the System Clock Source (SCS) bit of the OSCCON register to '`1`' or enable Two-Speed Start-up by setting the IESO bit in the Configuration Word register (CONFIG) to '`1`'.

The HF Internal Oscillator (HTS) bit of the OSCCON register indicates whether the HFINTOSC is stable or not.

3.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-2).

The default value of the OSCTUNE register is ‘0’. The value is a 5-bit two’s complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

3.5.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). Select 31 kHz, via software, using the IRCF<2:0> bits of the OSCCON register. See **Section 3.5.4 “Frequency Select Bits (IRCF)”** for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<2:0> bits of the OSCCON register = `000`) as the system clock source (SCS bit of the OSCCON register = `1`), or when any of the following are enabled:

- Two-Speed Start-up IESO bit of the Configuration Word register = `1` and IRCF<2:0> bits of the OSCCON register = `000`
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit of the OSCCON register indicates whether the LFINTOSC is stable or not.

3.5.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz (LFINTOSC)

Note:	Following any Reset, the IRCF<2:0> bits of the OSCCON register are set to ‘`110`’ and the frequency selection is set to 4 MHz. The user can modify the IRCF bits to select a different frequency.

3.5.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power (see Figure 3-6). If this is the case, there is a delay after the IRCF<2:0> bits of the OSCCON register are modified before the frequency selection takes place. The LTS and HTS bits of the OSCCON register will reflect the current active status of the LFINTOSC and HFINTOSC oscillators. The timing of a frequency selection is as follows:

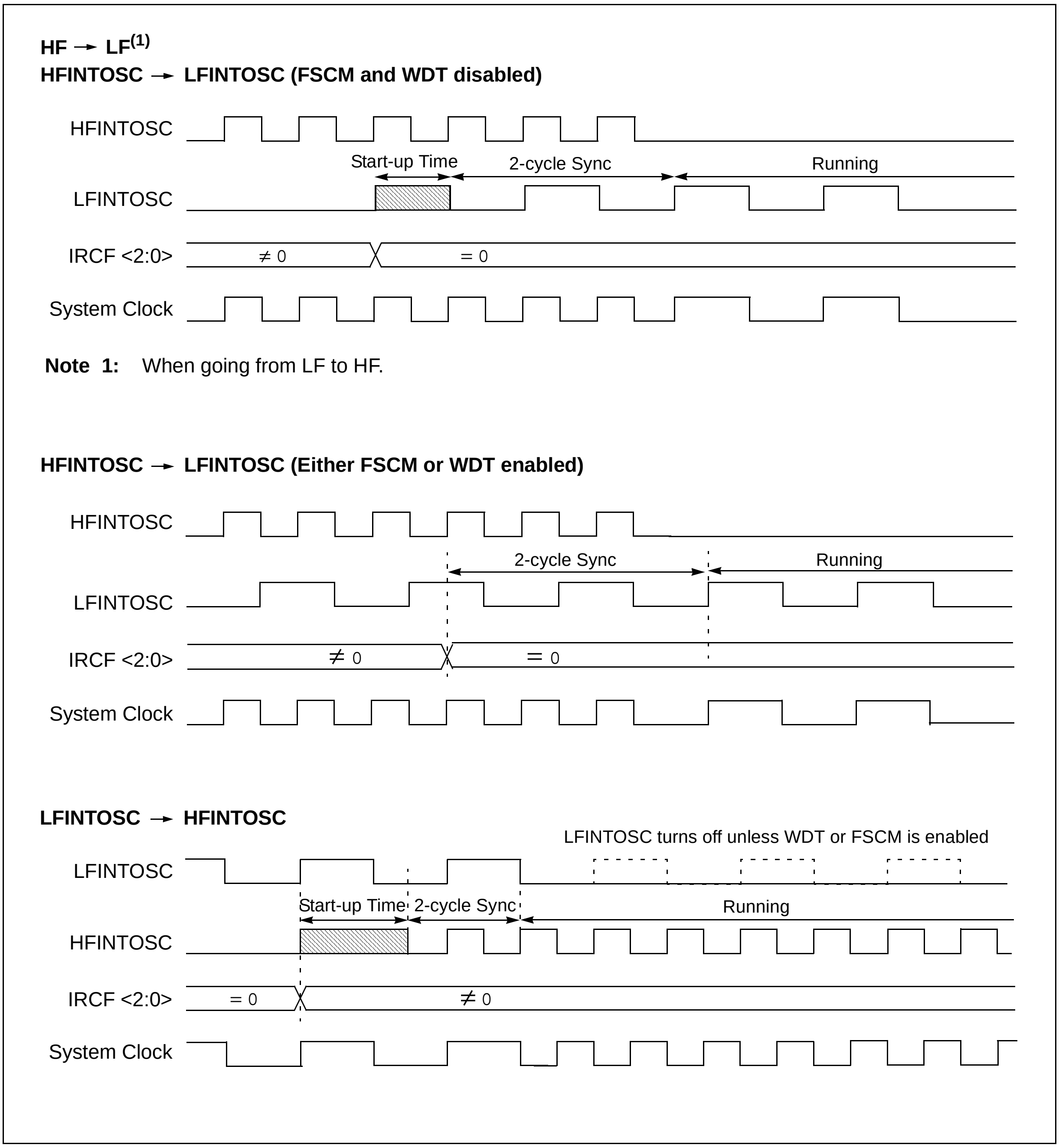
1. IRCF<2:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKOUT is now connected with the new clock. LTS and HTS bits of the OSCCON register are updated as required.
6. Clock switch is complete.

See Figure 3-1 for more details.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

Start-up delay specifications are located in the ***Electrical Specifications Chapter of this data sheet, under AC Specifications (Oscillator Module)***.

FIGURE 3-6: INTERNAL OSCILLATOR SWITCH TIMING



3.6 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit of the OSCCON register.

3.6.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bit of the OSCCON register = `0`, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When the SCS bit of the OSCCON register = `1`, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<2:0> bits of the OSCCON register. After a Reset, the SCS bit of the OSCCON register is always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit of the OSCCON register. The user can monitor the OSTS bit of the OSCCON register to determine the current system clock source.

3.6.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCCON register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.7 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note:	Executing a `SLEEP` instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear.

When the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.4.1 “Oscillator Start-up Timer (OST)”**). The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

3.7.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word register) = `1`; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = `0`.
- FOSC<2:0> bits in the Configuration Word register (CONFIG) configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

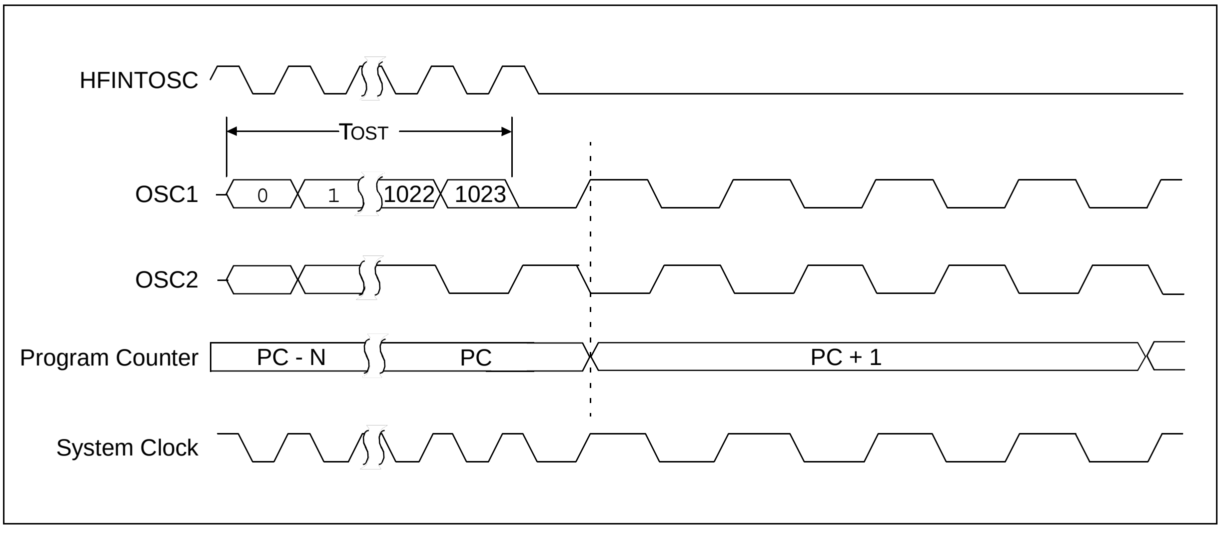
3.7.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bits of the OSCCON register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

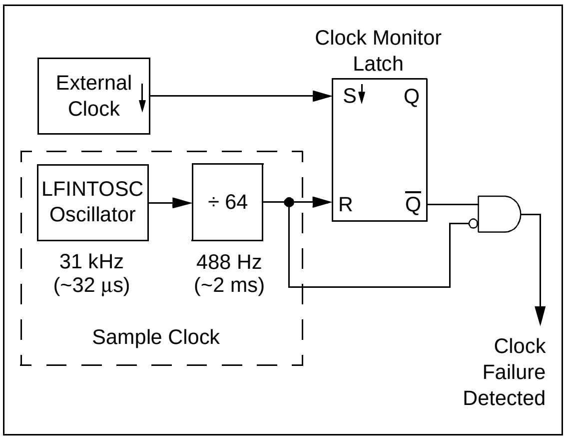
FIGURE 3-7: TWO-SPEED START-UP



3.8 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Word register (CONFIG). The FSCM is applicable to all external oscillator modes (LP, XT, HS, EC, RC and RCIO).

FIGURE 3-8: FSCM BLOCK DIAGRAM



3.8.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 3-8. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the primary clock goes low.

3.8.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR1 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

3.8.3 FAIL-SAFE CONDITION CLEARING

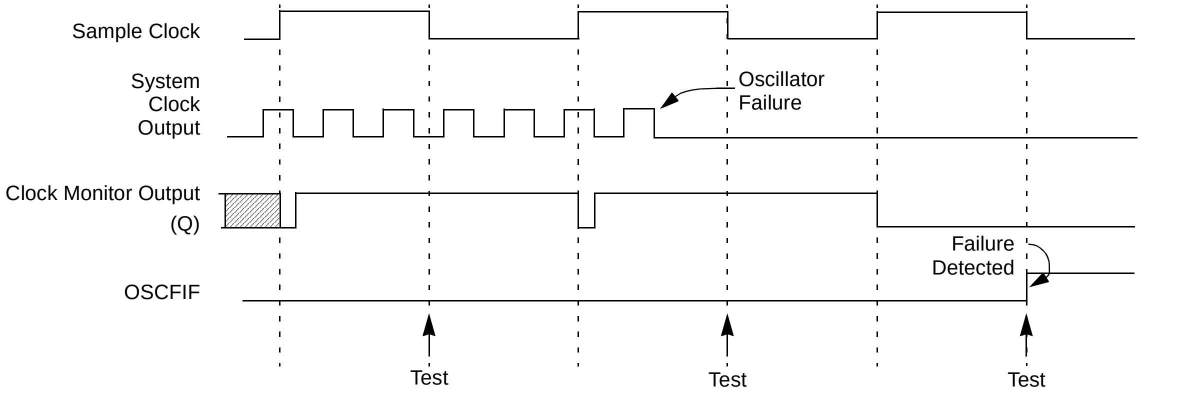
The Fail-Safe condition is cleared after a Reset, executing a `SLEEP` instruction or toggling the SCS bit of the OSCCON register. When the SCS bit is toggled, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

3.8.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note:	Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify the oscillator start-up and that the system clock switchover has successfully completed.

FIGURE 3-9: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets[(1)]
CONFIG[(2)]	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 x000	-110 x000
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.

4.0 GPIO PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 GPIO and the TRISIO Registers

GPIO is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISIO. Setting a TRISIO bit (= `1`) will make the corresponding GPIO pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISIO bit (= `0`) will make the corresponding GPIO pin an output (i.e., put the contents of the output latch on the selected pin). An exception is GP3, which is input only and its TRISIO bit will always read as '`1`'. Example 4-1 shows how to initialize GPIO.

Reading the GPIO register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. GP3 reads '`0`' when MCLRE = `1`.

The TRISIO register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '`0`'.

Note:	The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '`0`'.

EXAMPLE 4-1: INITIALIZING GPIO

```
BANKSEL  GPIO      ;
CLRF     GPIO      ;Init GPIO
MOVLW    07h       ;Set GP<2:0> to
MOVWF    CMCON0    ;digital I/O
BANKSEL  ANSEL     ;
CLRF     ANSEL     ;digital I/O
MOVLW    0Ch       ;Set GP<3:2> as inputs
MOVWF    TRISIO    ;and set GP<5:4,1:0>
                   ;as outputs
```

REGISTER 4-1: GPIO: GENERAL PURPOSE I/O REGISTER

U-0	U-0	R/W-x	R/W-0	R-x	R/W-0	R/W-0	R/W-0
—	—	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6	**Unimplemented**: Read as '`0`'
bit 5-0	**GP<5:0>**: GPIO I/O Pin bit `1` = Port pin is > V_{IH} `0` = Port pin is < V_{IL}

REGISTER 4-2: TRISIO GPIO TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISIO5[(2,3)]	TRISIO4[(2)]	TRISIO3[(1)]	TRISIO2	TRISIO1	TRISIO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6	**Unimplemented**: Read as ‘0’
bit 5:4	**TRISIO<5:4>:** GPIO Tri-State Control bit 1 = GPIO pin configured as an input (tri-stated) 0 = GPIO pin configured as an output
bit 3	**TRISIO<3>:** GPIO Tri-State Control bit Input only
bit 2:0	**TRISIO<2:0>:** GPIO Tri-State Control bit 1 = GPIO pin configured as an input (tri-stated) 0 = GPIO pin configured as an output

Note 1: TRISIO<3> always reads ‘1’.
2: TRISIO<5:4> always reads ‘1’ in XT, HS and LP OSC modes.
3: TRISIO<5> always reads ‘1’ in RC and RCIO and EC modes.

4.2 Additional Pin Functions

Every GPIO pin on the PIC12F683 has an interrupt-on-change option and a weak pull-up option. GP0 has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 ANSEL REGISTER

The ANSEL register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

4.2.2 WEAK PULL-UPS

Each of the GPIO pins, except GP3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 4-4. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{GPPU}}$ bit of the OPTION register). A weak pull-up is automatically enabled for GP3 when configured as $\overline{\text{MCLR}}$ and disabled when GP3 is an I/O. There is no software control of the $\overline{\text{MCLR}}$ pull-up.

4.2.3 INTERRUPT-ON-CHANGE

Each of the GPIO pins is individually configurable as an interrupt-on-change pin. Control bits IOCx enable or disable the interrupt function for each pin. Refer to Register 4-5. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The ‘mismatch’ outputs of the last read are OR’d together to set the GPIO Change Interrupt Flag bit (GPIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of GPIO. This will end the mismatch condition, then,
b) Clear the flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor Brown-out Reset. After these resets, the GPIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.

REGISTER 4-3: ANSEL: ANALOG SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**: Read as ‘0’

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits
000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64

bit 3-0 **ANS<3:0>**: Analog Select bits
Analog select between analog or digital function on pins AN<3:0>, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 4-4: WPU: WEAK PULL-UP REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-4 **WPU<5:4>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

bit 3 **Unimplemented**: Read as ‘0’

bit 2-0 **WPU<2:0>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{GPPU}}$ must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).
3: The GP3 pull-up is enabled when configured as $\overline{\text{MCLR}}$ and disabled as an I/O in the Configuration Word.
4: WPU<5:4> always reads ‘1’ in XT, HS and LP OSC modes.

REGISTER 4-5: IOC: INTERRUPT-ON-CHANGE GPIO REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOC<5:0>:** Interrupt-on-change GPIO Control bits
1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.
2: IOC<5:4> always reads ‘0’ in XT, HS and LP OSC modes.

4.2.4 ULTRA LOW-POWER WAKE-UP

The Ultra Low-Power Wake-up (ULPWU) on GP0 allows a slow falling voltage to generate an interrupt-on-change on GP0 without excess current consumption. The mode is selected by setting the ULPWUE bit of the PCON register. This enables a small current sink which can be used to discharge a capacitor on GP0.

To use this feature, the GP0 pin is configured to output '1' to charge the capacitor, interrupt-on-change for GP0 is enabled and GP0 is configured as an input. The ULPWUE bit is set to begin the discharge and a SLEEP instruction is performed. When the voltage on GP0 drops below V_{IL}, an interrupt will be generated which will cause the device to wake-up. Depending on the state of the GIE bit of the INTCON register, the device will either jump to the interrupt vector (0004h) or execute the next instruction when the interrupt event occurs. See **Section 4.2.3 "Interrupt-on-Change"** and **Section 12.4.3 "GPIO Interrupt"** for more information.

This feature provides a low-power technique for periodically waking up the device from Sleep. The time-out is dependent on the discharge time of the RC circuit on GP0. See Example 4-2 for initializing the Ultra Low-Power Wake-up module.

The series resistor provides overcurrent protection for the GP0 pin and can allow for software calibration of the time-out (see Figure 4-1). A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The Ultra Low-Power Wake-up peripheral can also be configured as a simple Programmable Low-Voltage Detect or temperature sensor.

Note:	For more information, refer to the Application Note *AN879, "Using the Microchip Ultra Low-Power Wake-up Module"* (DS00879).

EXAMPLE 4-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

```
BANKSEL  CMCON0       ;
MOVLW    H'7'         ;Turn off
MOVWF    CMCON0       ;comparators
BANKSEL  ANSEL        ;
BCF      ANSEL,0      ;RA0 to digital I/O
BCF      TRISA,0      ;Output high to
BANKSEL  PORTA        ;
BSF      PORTA,0      ;charge capacitor
CALL     CapDelay     ;
BANKSEL  PCON         ;
BSF      PCON,ULPWUE  ;Enable ULP Wake-up
BSF      IOCA,0       ;Select RA0 IOC
BSF      TRISA,0      ;RA0 to input
MOVLW    B'10001000'  ;Enable interrupt
MOVWF    INTCON       ; and clear flag
SLEEP                 ;Wait for IOC
NOP                   ;
```

4.2.5 PIN DESCRIPTIONS AND DIAGRAMS

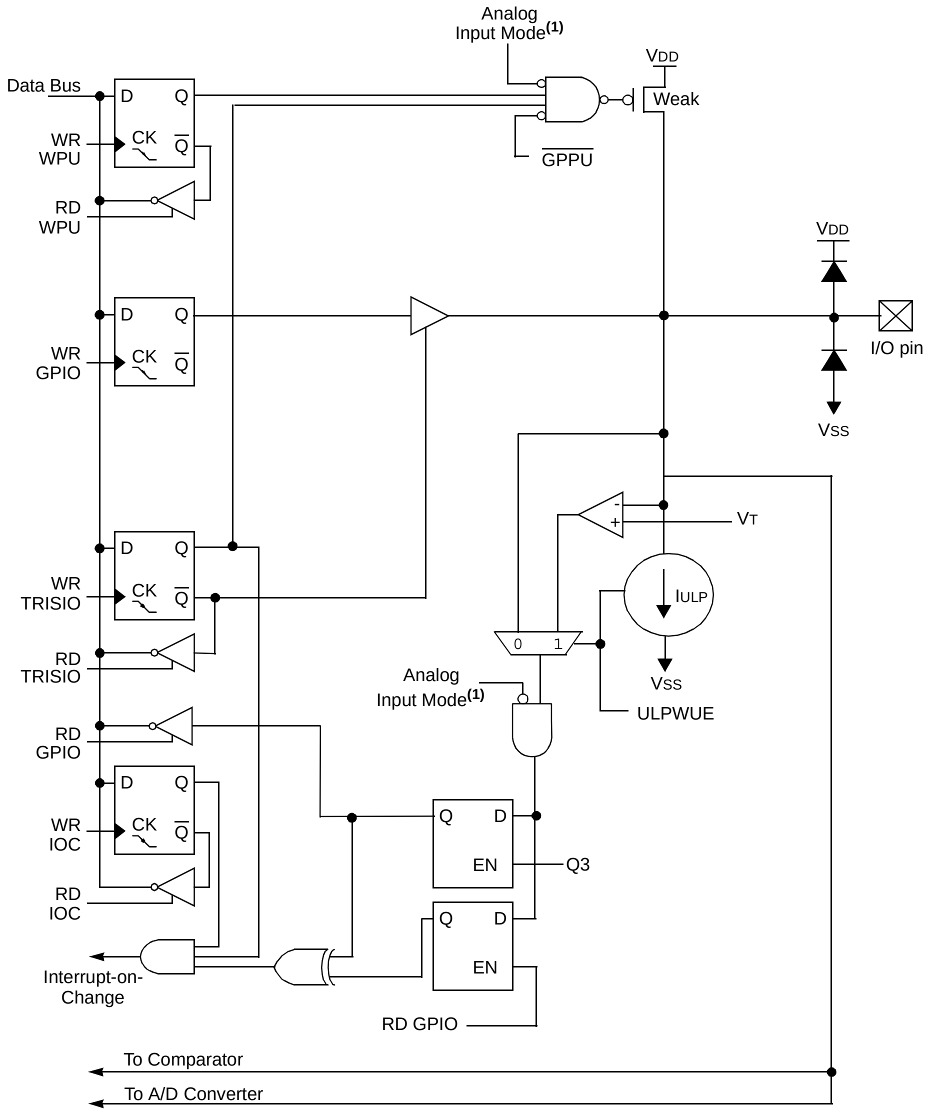
Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the ADC, refer to the appropriate section in this data sheet.

4.2.5.1 GP0/AN0/CIN+/ICSPDAT/ULPWU

Figure 4-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog input to the comparator
- In-Circuit Serial Programming™ data
- an analog input to the Ultra Low-Power Wake-up

FIGURE 4-1: BLOCK DIAGRAM OF GP0



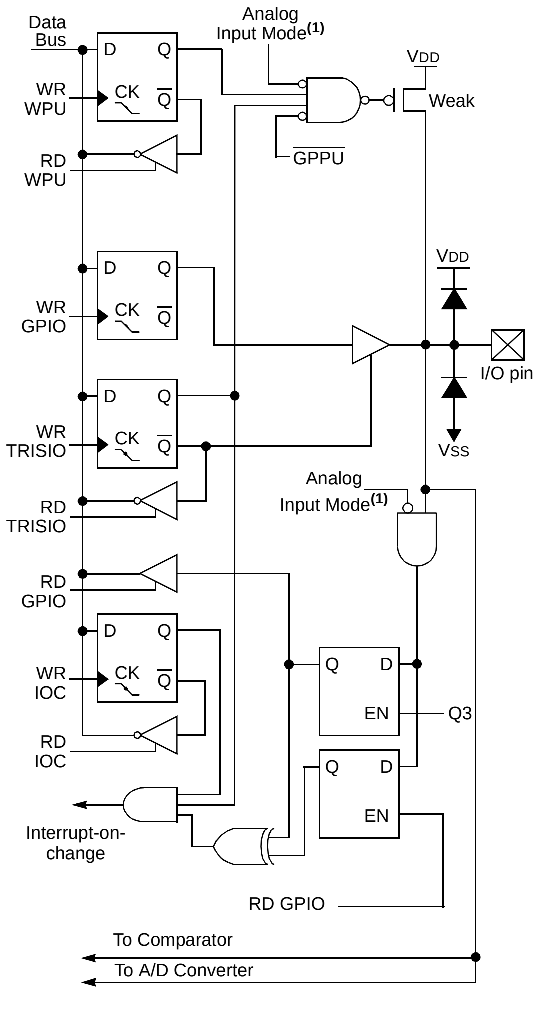
Note 1: Comparator mode and ANSEL determines Analog Input mode.

4.2.5.2 GP1/AN1/CIN-/VREF/ICSPCLK

Figure 4-2 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a analog input to the comparator
- a voltage reference input for the ADC
- In-Circuit Serial Programming clock

FIGURE 4-2: BLOCK DIAGRAM OF GP1



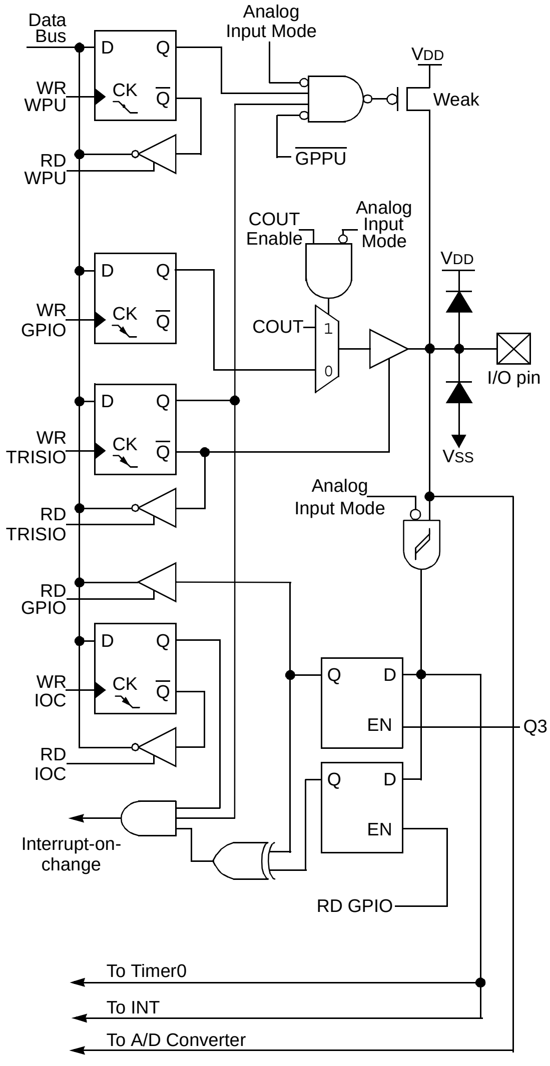
Note 1: Comparator mode and ANSEL determines Analog Input mode.

4.2.5.3 GP2/AN2/T0CKI/INT/COUT/CCP1

Figure 4-3 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- the clock input for Timer0
- an external edge triggered interrupt
- a digital output from the Comparator
- a digital input/output for the CCP (refer to **Section 11.0 "Capture/Compare/PWM (CCP) Module"**).

FIGURE 4-3: BLOCK DIAGRAM OF GP2



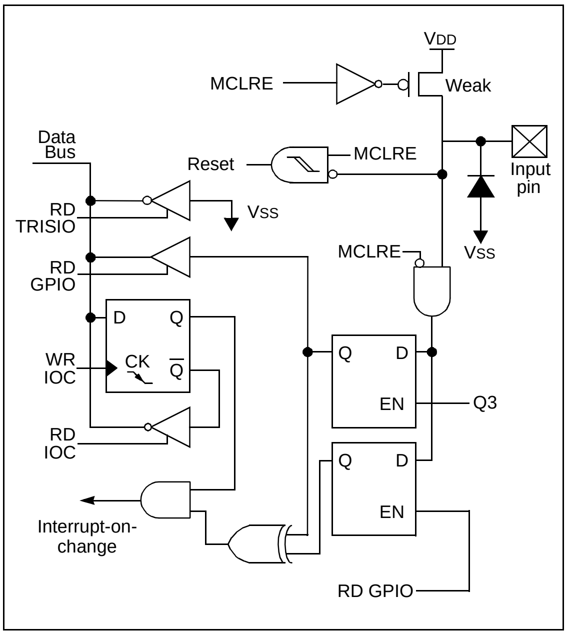
Note 1: Comparator mode and ANSEL determines Analog Input mode.

4.2.5.4 GP3/$\overline{MCLR}$/VPP

Figure 4-4 shows the diagram for this pin. The GP3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up

FIGURE 4-4: BLOCK DIAGRAM OF GP3

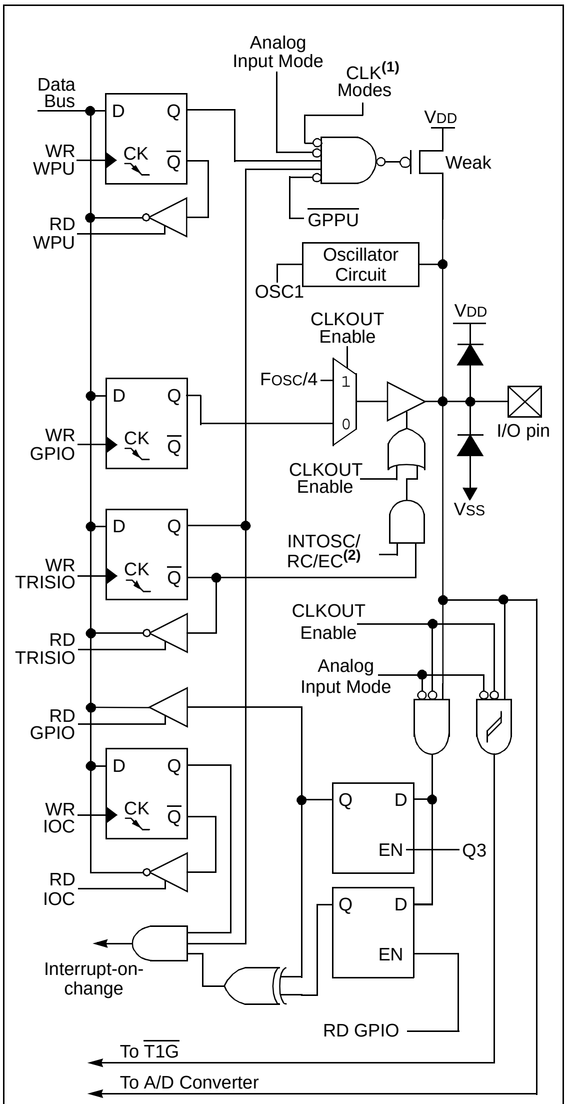


4.2.5.5 GP4/AN3/$\overline{T1G}$/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a Timer1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF GP4



Note 1: CLK modes are XT, HS, LP, optional LP oscillator and CLKOUT Enable.

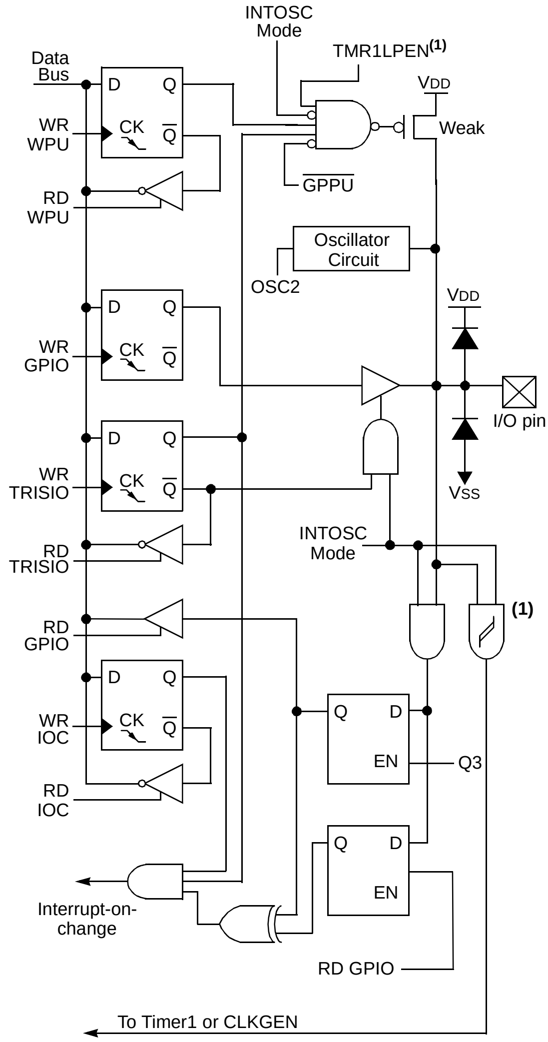
2: With CLKOUT option.

4.2.5.6 GP5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF GP5



Note 1: Timer1 LP oscillator enabled.

2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
PCON	—	—	ULPWUE	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	--01 --qq	--0u --uu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--x0 x000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	0000 0000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
WPU	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	--11 -111

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by GPIO.

NOTES:

5.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 5-1 is a block diagram of the Timer0 module.

5.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

5.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to ‘0’.

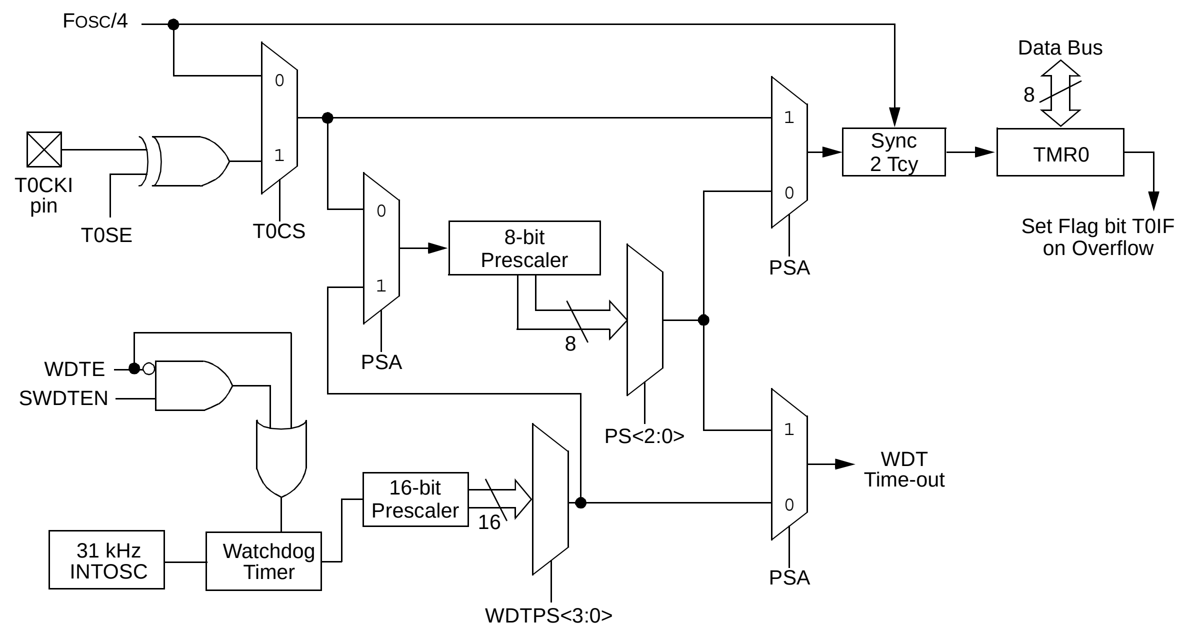
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

5.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to ‘1’.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.
2: SWDTEN and WDTPS<3:0> are bits in the WDTCON register.
3: WDTE bit is in the Configuration Word register.

5.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

When the prescaler is assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT.

5.1.3.1 Switching Prescaler Between Timer0 and WDT Modules

As a result of having the prescaler assigned to either Timer0 or the WDT, it is possible to generate an unintended device Reset when switching prescaler values. When changing the prescaler assignment from Timer0 to the WDT module, the instruction sequence shown in Example 5-1, must be executed.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0 → WDT)

```
BANKSEL  TMR0             ;
CLRWDT                    ;Clear WDT
CLRF     TMR0             ;Clear TMR0 and
                          ;prescaler
BANKSEL  OPTION_REG       ;
BSF      OPTION_REG,PSA   ;Select WDT
CLRWDT                    ;
                          ;
MOVLW    b'11111000'      ;Mask prescaler
ANDWF    OPTION_REG,W     ;bits
IORLW    b'00000101'      ;Set WDT prescaler
MOVWF    OPTION_REG       ;to 1:32
```

When changing the prescaler assignment from the WDT to the Timer0 module, the following instruction sequence must be executed (see Example 5-2).

EXAMPLE 5-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDT                 ;Clear WDT and
                       ;prescaler
BANKSEL OPTION_REG     ;
MOVLW   b'11110000'    ;Mask TMR0 select and
ANDWF   OPTION_REG,W   ;prescaler bits
IORLW   b'00000011'    ;Set prescale to 1:16
MOVWF   OPTION_REG     ;
```

5.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit must be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

5.1.5 USING TIMER0 WITH AN EXTERNAL CLOCK

When Timer0 is in Counter mode, the synchronization of the T0CKI input and the Timer0 register is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, the high and low periods of the external clock source must meet the timing requirements as shown in the **Section 15.0 "Electrical Specifications"**.

REGISTER 5-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{GPPU}}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available. See **Section 12.6 "Watchdog Timer (WDT)"** for more information.

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or $\overline{\text{T1G}}$ pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Special Event Trigger (with CCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

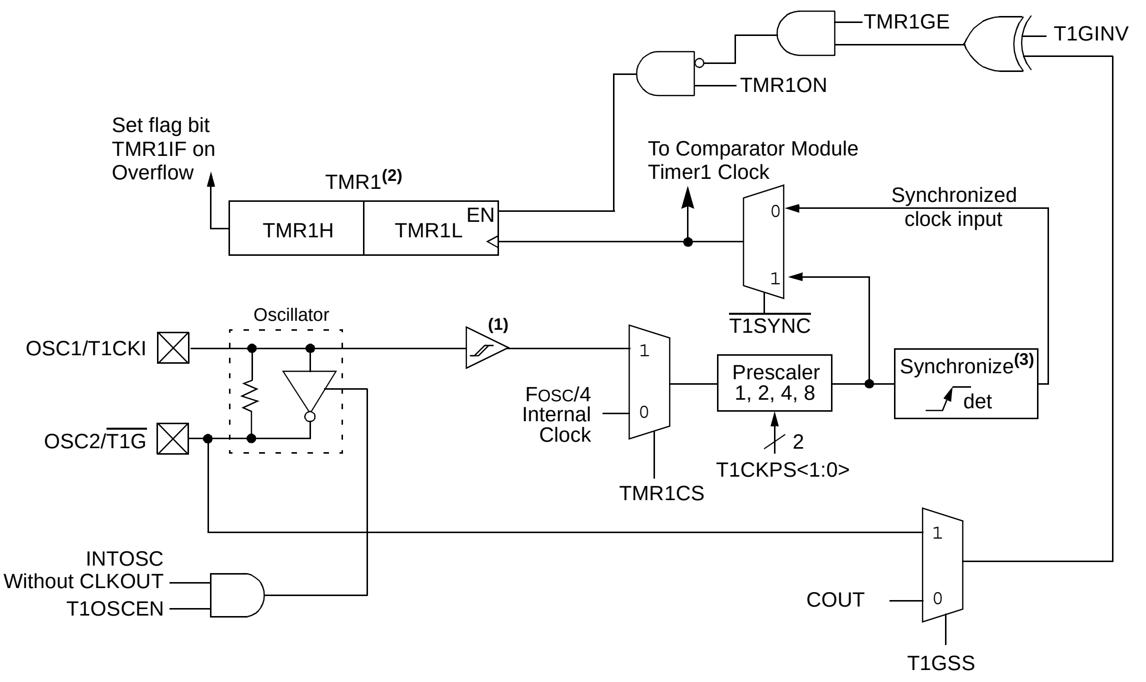
When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = `0`, the clock source is FOSC/4. When TMR1CS = `1`, the clock source is supplied externally.

Clock Source	TMR1CS
FOSC/4	0
T1CKI pin	1

FIGURE 6-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is low power type when using LP oscillator, or high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

6.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

6.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

> **Note:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

6.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

6.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (amplifier output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO<5:4> bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as '`0`' and TRISIO5 and TRISIO4 bits read as '`1`'.

> **Note:** The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

> **Note:** When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TTMR1L register pair.

6.6 Timer1 Gate

Timer1 gate source is software configurable to be the $\overline{\text{T1G}}$ pin or the output of the Comparator. This allows the device to directly time external events using $\overline{\text{T1G}}$ or analog events using Comparator 2. See the CMCON1 register (**Register 8-2**) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

> **Note:** TMR1GE bit of the T1CON register must be set to use either $\overline{\text{T1G}}$ or COUT as the Timer1 gate source. See **Register 8-2** for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the $\overline{\text{T1G}}$ pin or Comparator 2 output. This configures Timer1 to measure either the active-high or active-low time between events.

6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

6.9 CCP Special Event Trigger

If a CCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see ***Section on CCP***.

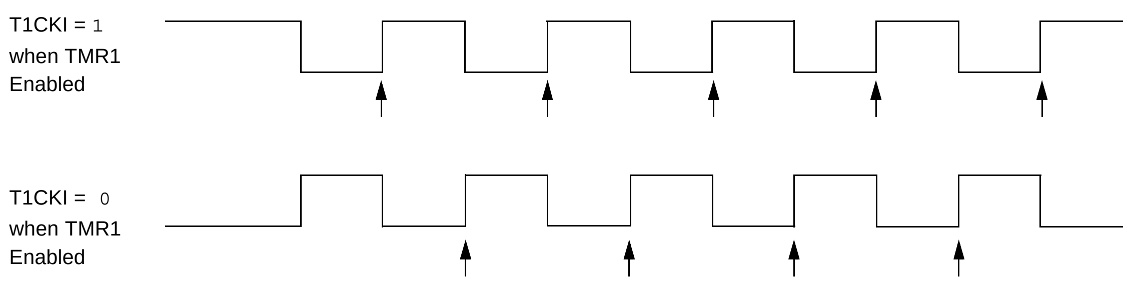
6.10 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 8.0 “Comparator Module”**.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

6.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit(1)
- `1` = Timer1 gate is active-high (Timer1 counts when gate is high)
- `0` = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit(2)
- If TMR1ON = `0`:
- This bit is ignored
- If TMR1ON = `1`:
- `1` = Timer1 is on if Timer1 gate is not active
- `0` = Timer1 is on

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
- `11` = 1:8 Prescale Value
- `10` = 1:4 Prescale Value
- `01` = 1:2 Prescale Value
- `00` = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
- If INTOSC without CLKOUT oscillator is active:
- `1` = LP oscillator is enabled for Timer1 clock
- `0` = LP oscillator is off
- Else:
- This bit is ignored. LP oscillator is disabled.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
- TMR1CS = `1`:
- `1` = Do not synchronize external clock input
- `0` = Synchronize external clock input
- TMR1CS = `0`:
- This bit is ignored. Timer1 uses the internal clock

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
- `1` = External clock from T1CKI pin (on the rising edge)
- `0` = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
- `1` = Enables Timer1
- `0` = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or COUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CONFIG[(1)]	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.
Note 1: See Configuration Word register (Register 12-1) for operation of all register bits.

7.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 7-1 for a block diagram of Timer2.

7.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (FOSC/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

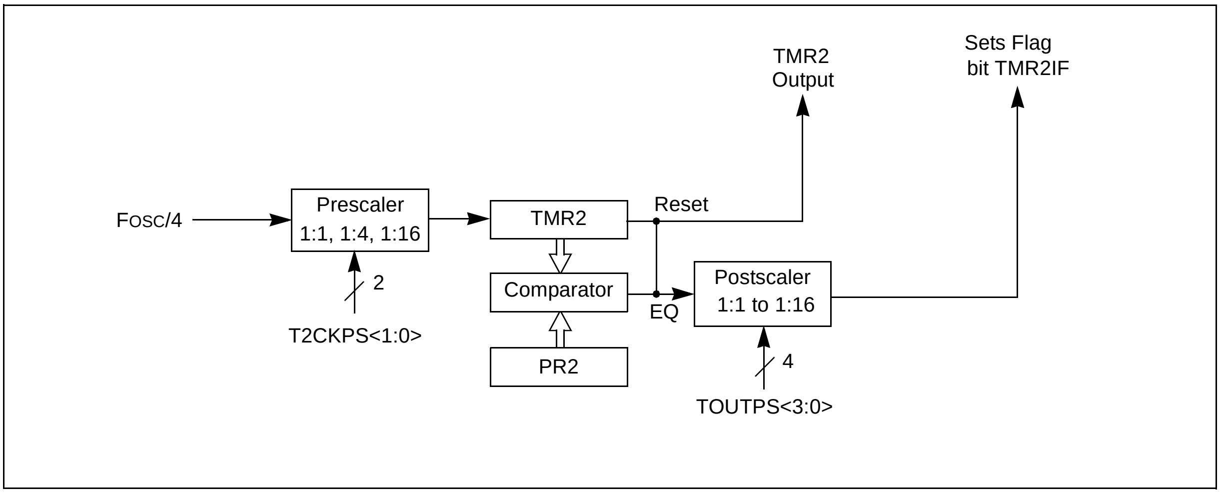
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset, or Brown-out Reset).

Note:	TMR2 is not cleared when T2CON is written.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



REGISTER 7-1: T2CON: TIMER 2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits
- 0000 = 1:1 Postscaler
- 0001 = 1:2 Postscaler
- 0010 = 1:3 Postscaler
- 0011 = 1:4 Postscaler
- 0100 = 1:5 Postscaler
- 0101 = 1:6 Postscaler
- 0110 = 1:7 Postscaler
- 0111 = 1:8 Postscaler
- 1000 = 1:9 Postscaler
- 1001 = 1:10 Postscaler
- 1010 = 1:11 Postscaler
- 1011 = 1:12 Postscaler
- 1100 = 1:13 Postscaler
- 1101 = 1:14 Postscaler
- 1110 = 1:15 Postscaler
- 1111 = 1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit
- 1 = Timer2 is on
- 0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits
- 00 = Prescaler is 1
- 01 = Prescaler is 4
- 1x = Prescaler is 16

TABLE 7-1: SUMMARY OF ASSOCIATED TIMER2 REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
PR2	Timer2 Module Period Register								1111 1111	1111 1111
TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as ‘0’. Shaded cells are not used for Timer2 module.

8.0 COMPARATOR MODULE

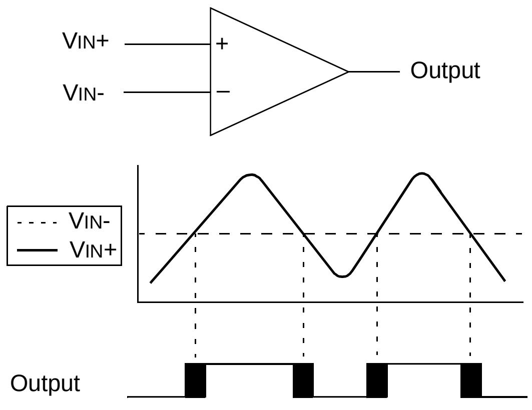
Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The analog comparator module includes the following features:

- Multiple comparator configurations
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference

8.1 Comparator Overview

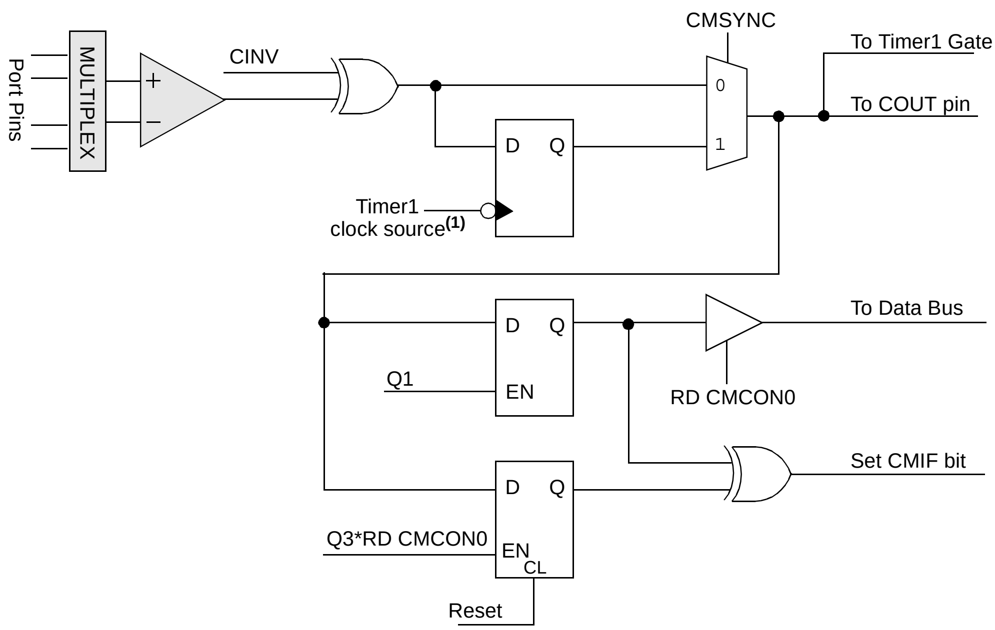
The comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 8-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

FIGURE 8-2: COMPARATOR OUTPUT BLOCK DIAGRAM



Note 1: Comparator output is latched on falling edge of Timer1 clock source.

2: Q1 and Q3 are phases of the four-phase system clock (FOSC).

3: Q1 is held high during Sleep mode.

8.2 Analog Input Connection Considerations

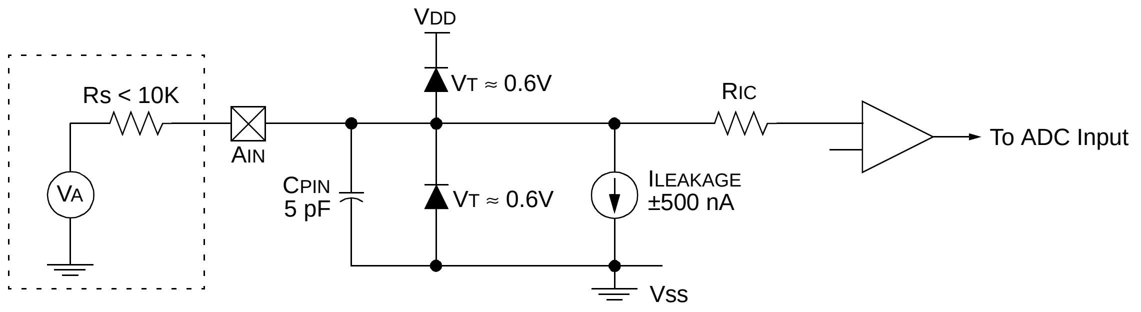
A simplified circuit for an analog input is shown in Figure 8-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to V_{DD} and V_{SS}. The analog input, therefore, must be between V_{SS} and V_{DD}. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 8-3: ANALOG INPUT MODEL



Legend:
- C_{PIN} = Input Capacitance
- $I_{LEAKAGE}$ = Leakage Current at the pin due to various junctions
- R_{IC} = Interconnect Resistance
- R_S = Source Impedance
- V_A = Analog Voltage
- V_T = Threshold Voltage

8.3 Comparator Configuration

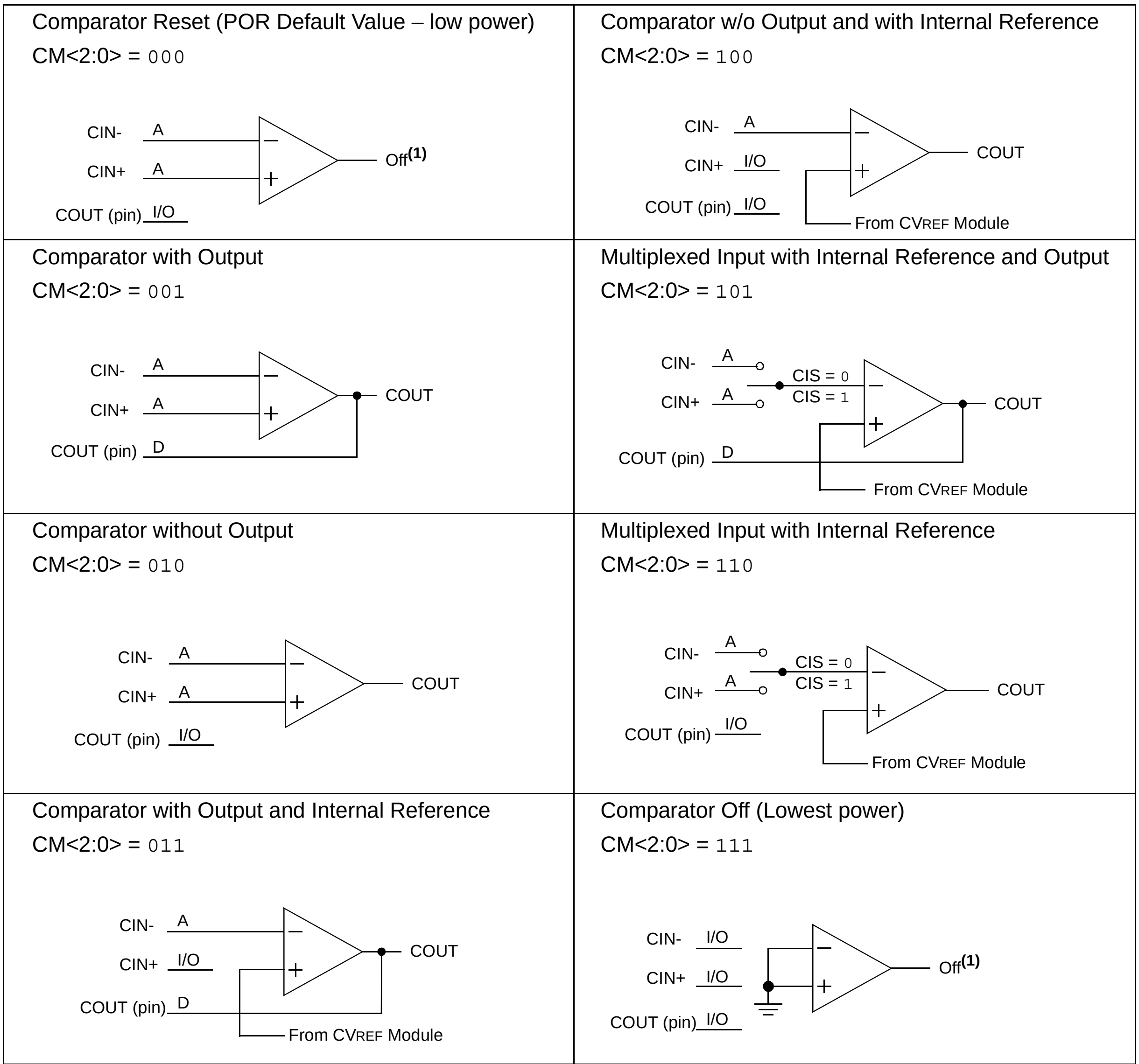
There are eight modes of operation for the comparator. The CM<2:0> bits of the CMCON0 register are used to select these modes as shown in Figure 8-4.

- Analog function (A): digital input buffer is disabled
- Digital function (D): comparator digital output, overrides port function
- Normal port function (I/O): independent of comparator

The port pins denoted as “A” will read as a ‘0’ regardless of the state of the I/O pin or the I/O control TRIS bit. Pins used as analog inputs should also have the corresponding TRIS bit set to ‘1’ to disable the digital output driver. Pins denoted as “D” should have the corresponding TRIS bit set to ‘0’ to enable the digital output driver.

Note:	Comparator interrupts should be disabled during a Comparator mode change to prevent unintended interrupts.

FIGURE 8-4: COMPARATOR I/O OPERATING MODES



Legend:	A = Analog Input, ports always reads ‘0’	CIS = Comparator Input Switch (CMCON0<3>)
	I/O = Normal port I/O	D = Comparator Digital Output
Note 1:	Reads as ‘0’, unless CINV = 1.	

8.4 Comparator Control

The CMCON0 register (Register 8-1) provides access to the following comparator features:

- Mode selection
- Output state
- Output polarity
- Input switch

8.4.1 COMPARATOR OUTPUT STATE

The Comparator state can always be read internally via the COUT bit of the CMCON0 register. The comparator state may also be directed to the COUT pin in the following modes:

- CM<2:0> = `001`
- CM<2:0> = `011`
- CM<2:0> = `101`

When one of the above modes is selected, the associated TRIS bit of the COUT pin must be cleared.

8.4.2 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CINV bit of the CMCON0 register. Clearing CINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 8-1.

TABLE 8-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CINV	COUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

Note: COUT refers to both the register bit and output pin.

8.4.3 COMPARATOR INPUT SWITCH

The inverting input of the comparator may be switched between two analog pins in the following modes:

- CM<2:0> = `101`
- CM<2:0> = `110`

In the above modes, both pins remain in analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

8.5 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 15.0 "Electrical Specifications"** for more details.

8.6 Comparator Interrupt Operation

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8.2). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. The mismatch condition will persist, holding the CMIF bit of the PIR1 register true, until either the CMCON0 register is read or the comparator output returns to the previous state.

Note:	A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred.

The CMIF bit of the PIR1 register, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CMIF bit of the PIR1 register will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON0. This will end the mismatch condition.

b) Clear the CMIF interrupt flag.

A persistent mismatch condition will preclude clearing the CMIF interrupt flag. Reading CMCON0 will end the mismatch condition and allow the CMIF bit to be cleared.

Note:	If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF interrupt flag may not get set.

FIGURE 8-5: COMPARATOR INTERRUPT TIMING W/O CMCON0 READ

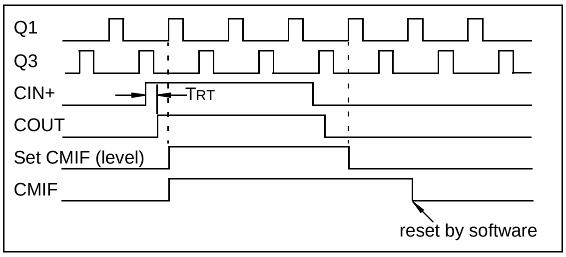
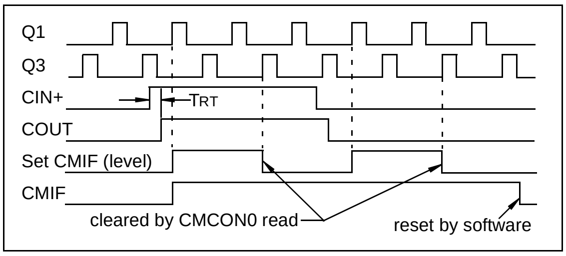


FIGURE 8-6: COMPARATOR INTERRUPT TIMING WITH CMCON0 READ



Note 1:	If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF of the PIR1 register interrupt flag may not get set.
2:	When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 µs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

8.7 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in **Section 15.0 "Electrical Specifications"**. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. The comparator is turned off by selecting mode CM<2:0> = `000` or CM<2:0> = `111` of the CMCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CMIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the Sleep instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the Interrupt Service Routine.

8.8 Effects of a Reset

A device Reset forces the CMCON0 and CMCON1 registers to their Reset states. This forces the Comparator module to be in the Comparator Reset mode (CM<2:0> = `000`). Thus, all comparator inputs are analog inputs with the comparator disabled to consume the smallest current possible.

REGISTER 8-1: CMCON0: COMPARATOR CONFIGURATION REGISTER

U-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COUT	—	CINV	CIS	CM2	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '`0`'

bit 6 **COUT:** Comparator Output bit
<u>When CINV = `0`:</u>
`1` = $V_{IN+} > V_{IN-}$
`0` = $V_{IN+} < V_{IN-}$
<u>When CINV = `1`:</u>
`1` = $V_{IN+} < V_{IN-}$
`0` = $V_{IN+} > V_{IN-}$

bit 5 **Unimplemented:** Read as '`0`'

bit 4 **CINV:** Comparator Output Inversion bit
`1` = Output inverted
`0` = Output not inverted

bit 3 **CIS:** Comparator Input Switch bit
<u>When CM<2:0> = `110` or `101`:</u>
`1` = CIN+ connects to V_{IN-}
`0` = CIN- connects to V_{IN-}
<u>When CM<2:0> = `0xx` or `100` or `111`:</u>
CIS has no effect.

bit 2-0 **CM<2:0>:** Comparator Mode bits (See Figure 8-5)
`000` = CIN pins are configured as analog, COUT pin configured as I/O, Comparator output turned off
`001` = CIN pins are configured as analog, COUT pin configured as Comparator output
`010` = CIN pins are configured as analog, COUT pin configured as I/O, Comparator output available internally
`011` = CIN- pin is configured as analog, CIN+ pin is configured as I/O, COUT pin configured as Comparator output, CV_{REF} is non-inverting input
`100` = CIN- pin is configured as analog, CIN+ pin is configured as I/O, COUT pin is configured as I/O, Comparator output available internally, CV_{REF} is non-inverting input
`101` = CIN pins are configured as analog and multiplexed, COUT pin is configured as Comparator output, CV_{REF} is non-inverting input
`110` = CIN pins are configured as analog and multiplexed, COUT pin is configured as I/O, Comparator output available internally, CV_{REF} is non-inverting input
`111` = CIN pins are configured as I/O, COUT pin is configured as I/O, Comparator output disabled, Comparator off.

8.9 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See **Section 6.0 “Timer1 Module with Gate Control”** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

8.10 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 8-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

REGISTER 8-2: CMCON1: COMPARATOR CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	CMSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **T1GSS:** Timer1 Gate Source Select bit(1)
- 1 = Timer 1 Gate Source is $\overline{\text{T1G}}$ pin (pin should be configured as digital input)
- 0 = Timer 1 Gate Source is comparator output

bit 0 **CMSYNC:** Comparator Output Synchronization bit(2)
- 1 = Output is synchronized with falling edge of Timer1 clock
- 0 = Output is asynchronous

Note 1: Refer to **Section 6.6 “Timer1 Gate”**.

2: Refer to Figure 8-2.

8.11 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to VSS
- Ratiometric with VDD

The VRCON register (Register 8-3) controls the Voltage Reference module shown in Figure 8-7.

8.11.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

8.11.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 8-1: CVREF OUTPUT VOLTAGE

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR\langle 3:0\rangle/24) \times VDD$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VDD/4) + (VR\langle 3:0\rangle \times VDD/32)$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 8-1.

8.11.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

8.11.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 15.0 "Electrical Specifications"**.

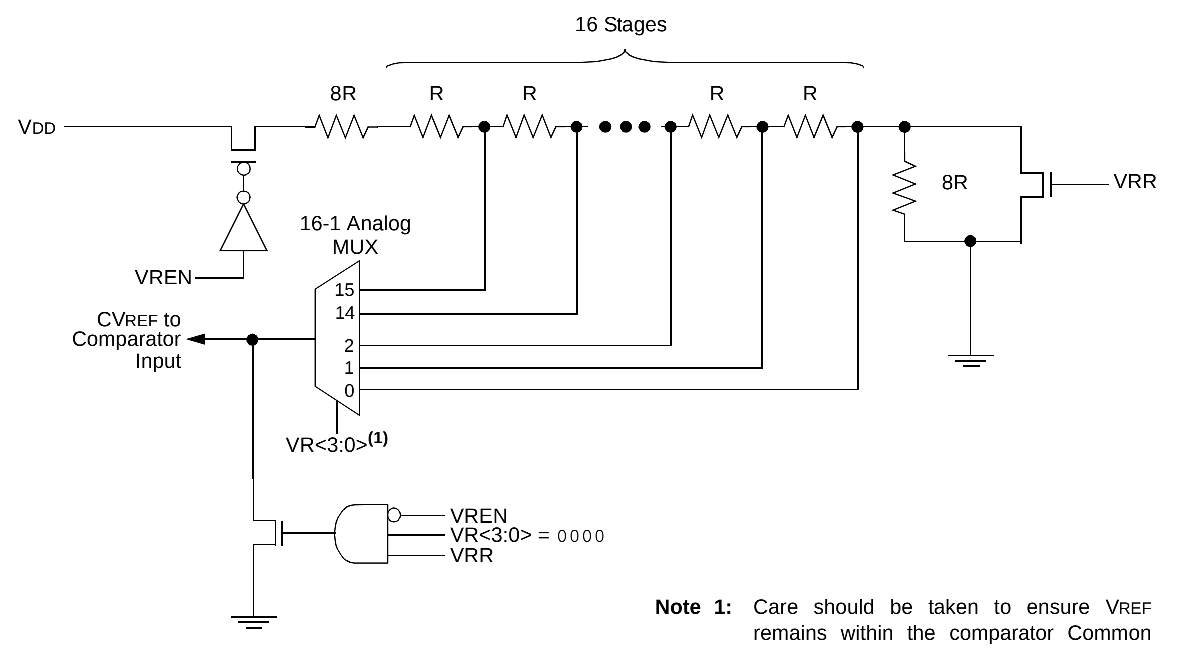
REGISTER 8-3: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	—	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	**VREN:** CVREF Enable bit 1 = CVREF circuit powered on 0 = CVREF circuit powered down, no IDD drain and CVREF = VSS.
bit 6	**Unimplemented:** Read as '0'
bit 5	**VRR:** CVREF Range Selection bit 1 = Low range 0 = High range
bit 4	**Unimplemented:** Read as '0'
bit 3-0	**VR<3:0>:** CVREF Value Selection $0 \leq$ VR<3:0> ≤ 15 When VRR = 1: CVREF = (VR<3:0>/24) * VDD When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32) * VDD

FIGURE 8-7: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



Note 1: Care should be taken to ensure VREF remains within the comparator Common mode input range. See **Section 15.0 “Electrical Specifications”** for more detail.

TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	-0-0 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as ‘0’. Shaded cells are not used for comparator.

NOTES:

9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

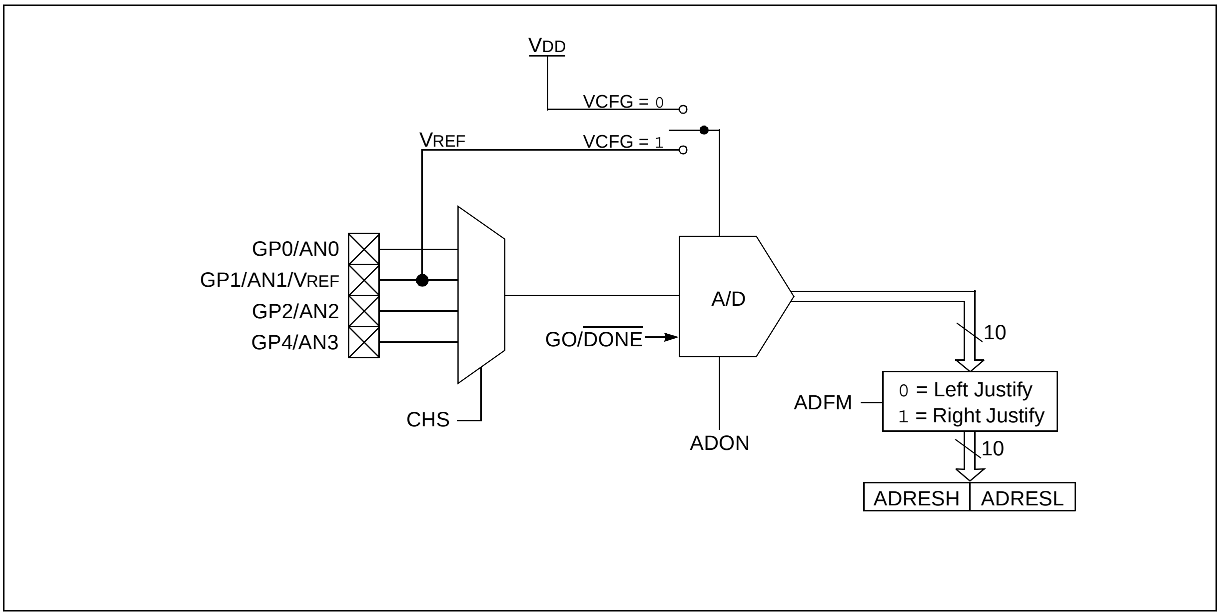
The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 9-1 shows the block diagram of the ADC.

FIGURE 9-1: ADC BLOCK DIAGRAM



9.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- GPIO configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 GPIO CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding GPIO section for more information.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 "ADC Operation"** for more information.

9.1.3 ADC VOLTAGE REFERENCE

The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either VDD or an external voltage source. The negative voltage reference is always connected to the ground reference.

9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ANSEL register. There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 9-2.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 15.0 "Electrical Specifications"** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note:	Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

TABLE 9-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES (VDD ≥ 3.0V)

ADC Clock Period (TAD)		Device Frequency (FOSC)			
ADC Clock Source	**ADCS<2:0>**	**20 MHz**	**8 MHz**	**4 MHz**	**1 MHz**
FOSC/2	000	100 ns(2)	250 ns(2)	500 ns(2)	2.0 μs
FOSC/4	100	200 ns(2)	500 ns(2)	1.0 μs(2)	4.0 μs
FOSC/8	001	400 ns(2)	1.0 μs(2)	2.0 μs	8.0 μs(3)
FOSC/16	101	800 ns(2)	2.0 μs	4.0 μs	16.0 μs(3)
FOSC/32	010	1.6 μs	4.0 μs	8.0 μs(3)	32.0 μs(3)
FOSC/64	110	3.2 μs	8.0 μs(3)	16.0 μs(3)	64.0 μs(3)
FRC	x11	2-6 μs(1,4)	2-6 μs(1,4)	2-6 μs(1,4)	2-6 μs(1,4)

Legend: Shaded cells are outside of recommended range.

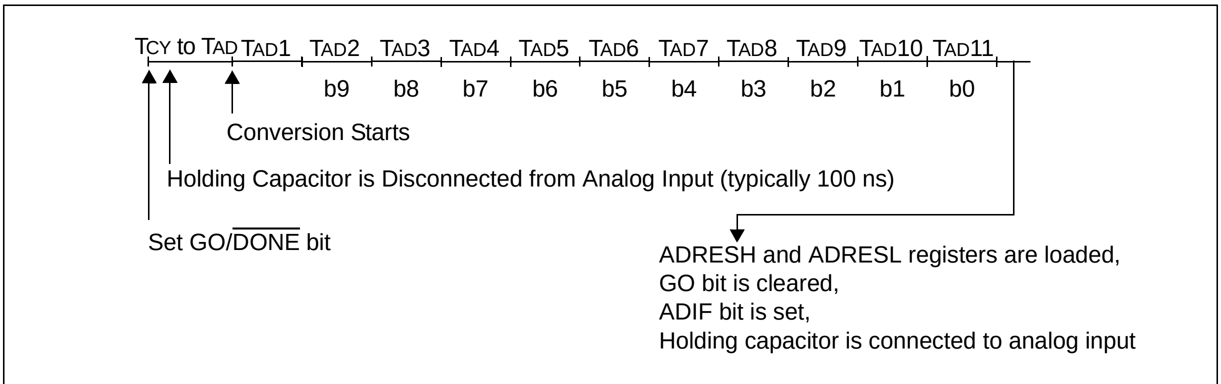
Note 1: The FRC source has a typical TAD time of 4 μs for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



9.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

> **Note:** The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the `SLEEP` instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the interrupt service routine.

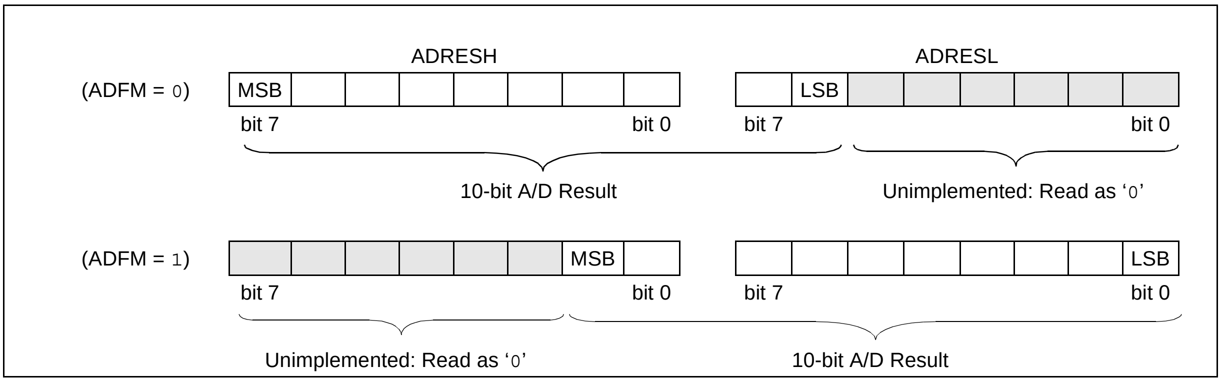
Please see **Section 12.4 “Interrupts”** for more information.

9.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 9-3 shows the two output formats.

FIGURE 9-3: 10-BIT A/D CONVERSION RESULT FORMAT



9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a ‘1’. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a ‘1’ will start the Analog-to-Digital conversion.

> **Note:** The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the ADC. Refer to **Section 9.2.6 “A/D Conversion Procedure”**.

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

> **Note:** A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The CCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 11.0 "Capture/Compare/PWM (CCP) Module"** for more information.

9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure GPIO Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt**(1)**
4. Wait the required acquisition time**(2)**.
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1:	The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.
2:	See **Section 9.3 "A/D Acquisition Requirements"**.

EXAMPLE 9-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and GP0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL  TRISIO        ;
BSF      TRISIO,0      ;Set GP0 to input
BANKSEL  ANSEL         ;
MOVLW    B'01110001'   ;ADC Frc clock,
IORWF    ANSEL         ; and GP0 as analog
BANKSEL  ADCON0        ;
MOVLW    B'10000001'   ;Right justify,
MOVWF    ADCON0        ;Vdd Vref, AN0, On
CALL     SampleTime    ;Acquisiton delay
BSF      ADCON0,GO     ;Start conversion
BTFSC    ADCON0,GO     ;Is conversion done?
GOTO     $-1           ;No, test again
BANKSEL  ADRESH        ;
MOVF     ADRESH,W      ;Read upper 2 bits
MOVWF    RESULTHI      ;Store in GPR space
BANKSEL  ADRESL        ;
MOVF     ADRESL,W      ;Read lower 8 bits
MOVWF    RESULTLO      ;Store in GPR space
```

9.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	—	—	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG:** Voltage Reference bit
1 = V_{REF} pin
0 = V_{DD}

bit 5-4 **Unimplemented:** Read as '0'

bit 3-2 **CHS<1:0>: Analog Channel Select bits**
00 = AN0
01 = AN1
10 = AN2
11 = AN3

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

REGISTER 9-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 9-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Reserved**: Do not use.

REGISTER 9-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Reserved**: Do not use.

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

REGISTER 9-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 9-4. **The maximum recommended impedance for analog sources is 10 kΩ**. As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$
\begin{aligned}
T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
&= T_{AMP} + T_C + T_{COFF} \\
&= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]
\end{aligned}
$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \qquad ;[1]\ V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \qquad ;[2]\ V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_c}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \qquad ;\text{combining [1] and [2]}$$

Solving for T_C:

$$
\begin{aligned}
T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047) \\
&= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885) \\
&= 1.37\mu s
\end{aligned}
$$

Therefore:

$$
\begin{aligned}
T_{ACQ} &= 2\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\
&= 4.67\mu s
\end{aligned}
$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 9-4: ANALOG INPUT MODEL

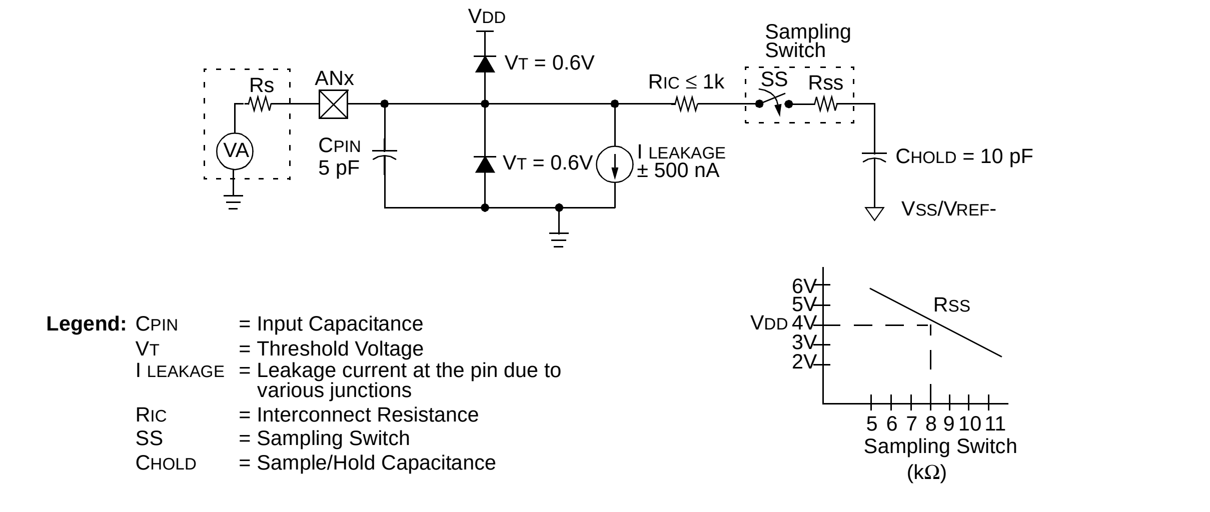


FIGURE 9-5: ADC TRANSFER FUNCTION

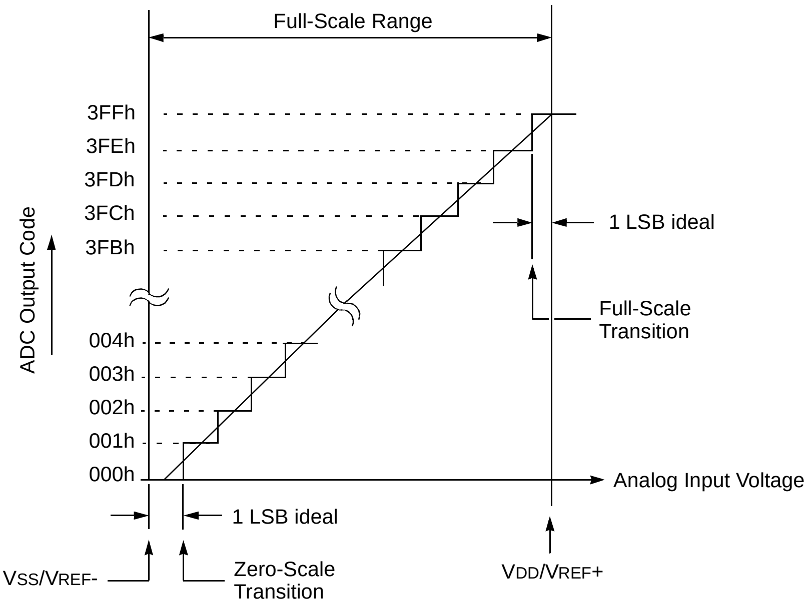


TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG	—	—	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	00-- 0000	0000 0000
ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as ‘0’. Shaded cells are not used for ADC module.

NOTES:

10.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDAT
- EEADR

EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F683 has 256 bytes of data EEPROM with an address range from 0h to FFh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip-to-chip. Please refer to AC Specifications in **Section 15.0 "Electrical Specifications"** for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access the data EEPROM data and will read zeroes.

REGISTER 10-1: EEDAT: EEPROM DATA REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EEDATn**: Byte Value to Write To or Read From Data EEPROM bits

REGISTER 10-2: EEADR: EEPROM ADDRESS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EEADR**: Specifies One of 256 Locations for EEPROM Read/Write Operation bits

10.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit of the PIR1 register, is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note:	The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 10-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:			
S = Bit can only be set			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOR Reset)
0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
0 = Does not initiate an EEPROM read

10.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD of the EECON1 register, as shown in Example 10-1. The data is available, at the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 10-1: DATA EEPROM READ

```
BANKSEL   EEADR        ;
MOVLW     CONFIG_ADDR ;
MOVWF     EEADR        ;Address to read
BSF       EECON1,RD    ;EE Read
MOVF      EEDAT,W      ;Move data to W
```

10.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 10-2.

EXAMPLE 10-2: DATA EEPROM WRITE

```
          BANKSEL  EECON1       ;
          BSF      EECON1,WREN  ;Enable write
          BCF      INTCON,GIE   ;Disable INTs
          BTFSC    INTCON,GIE   ;See AN576
          GOTO     $-2          ;
Required  MOVLW    55h          ;Unlock write
Sequence  MOVWF    EECON2       ;
          MOVLW    AAh          ;
          MOVWF    EECON2       ;
          BSF      EECON1,WR    ;Start the write
          BSF      INTCON,GIE   ;Enable INTS
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit of the PIR1 register must be cleared by software.

10.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 10-3) to the desired value to be written.

EXAMPLE 10-3: WRITE VERIFY

```
BANKSEL EEDAT       ;
MOVF    EEDAT,W     ;EEDAT not changed
                    ;from previous write
BSF     EECON1,RD   ;YES, Read the
                    ;value written
XORWF   EEDAT,W
BTFSS   STATUS,Z    ;Is data the same
GOTO    WRITE_ERR   ;No, handle error
:                   ;Yes, continue
```

10.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

10.5 Protection Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- Brown-out
- Power Glitch
- Software Malfunction

10.6 Data EEPROM Operation During Code-Protect

Data memory can be code-protected by programming the $\overline{\text{CPD}}$ bit in the Configuration Word register (Register 12-1) to '0'.

When the data memory is code-protected, the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations in program memory to '0' will also help prevent data memory code protection from becoming breached.

TABLE 10-1: SUMMARY OF ASSOCIATED DATA EEPROM REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
EECON2(1)	EEPROM Control Register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the Data EEPROM module.

Note 1: EECON2 is not a physical register.

11.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event.The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

The timer resources used by the module are shown in Table 11-1

Additional information on CCP modules is available in the Application Note AN594, *"Using the CCP Modules"* (DS00594).

TABLE 11-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 11-1: CCP1CON: CCP1 CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** CCP Mode Select bits

`0000` = Capture/Compare/PWM off (resets CCP module)
`0001` = Unused (reserved)
`0010` = Unused (reserved)
`0011` = Unused (reserved)
`0100` = Capture mode, every falling edge
`0101` = Capture mode, every rising edge
`0110` = Capture mode, every 4th rising edge
`0111` = Capture mode, every 16th rising edge
`1000` = Compare mode, set output on match (CCP1IF bit is set)
`1001` = Compare mode, clear output on match (CCP1IF bit is set)
`1010` = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
`1011` = Compare mode, trigger special event (CCP1IF bit is set, TMR1 is reset and A/D conversion is started if the ADC module is enabled. CCP1 pin is unaffected.)
`110x` = PWM mode active-high
`111x` = PWM mode active-low

11.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

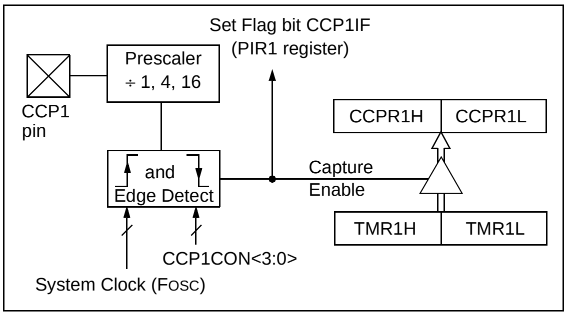
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 11-1).

11.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCP1 pin is configured as an output, a write to the GPIO port can cause a capture condition.

FIGURE 11-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



11.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

11.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

11.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 11-1).

EXAMPLE 11-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                    ; the new prescaler
                    ; move value and CCP ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ; value
```

11.2 Compare Mode

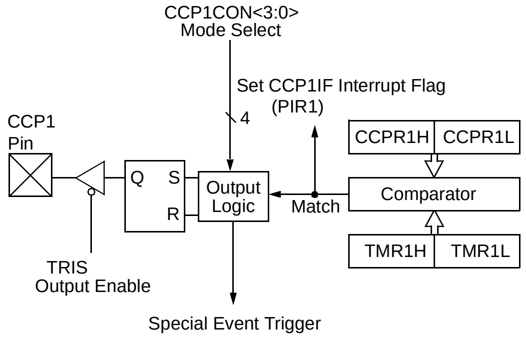
In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

- Toggle the CCP1 output.
- Set the CCP1 output.
- Clear the CCP1 output.
- Generate a Special Event Trigger.
- Generate a Software Interrupt.

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register.

All Compare modes can generate an interrupt.

FIGURE 11-2: COMPARE MODE OPERATION BLOCK DIAGRAM



Special Event Trigger will:

- Clear TMR1H and TMR1L registers.
- NOT set interrupt flag bit TMR1IF of the PIR1 register.
- Set the GO/$\overline{\text{DONE}}$ bit to start the ADC conversion.

11.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note:	Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the GPIO I/O data latch.

11.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

11.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = `1010`), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

11.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = `1011`), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (see the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

Note 1:	The Special Event Trigger from the CCP module does not set interrupt flag bit TMRxIF of the PIR1 register.
2:	Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

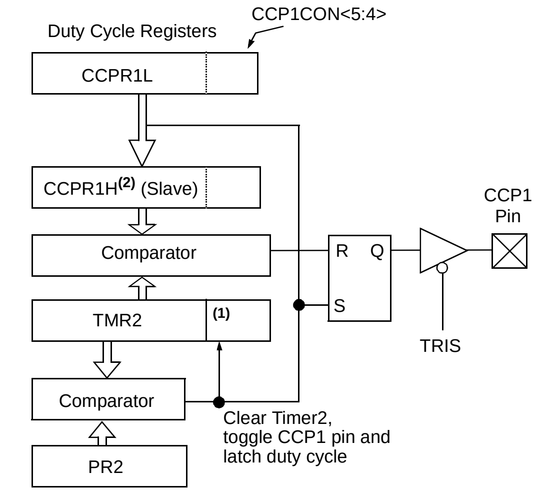
Note:	Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

Figure 11-1 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 11.3.7 "Setup for PWM Operation"**.

FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM

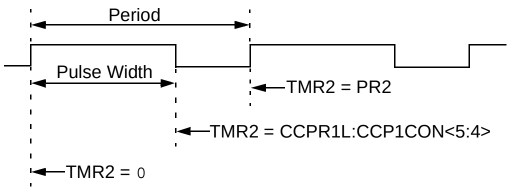


Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPR1H is a read-only register.

The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 11-4: CCP PWM OUTPUT



11.3.1 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 11-1.

EQUATION 11-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

Note:	The Timer2 postscaler (see **Section 7.0 "Timer2 Module"**) is not used in the determination of the PWM frequency.

11.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the CCP1<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 11-2 is used to calculate the PWM pulse width.

Equation 11-3 is used to calculate the PWM duty cycle ratio.

EQUATION 11-2: PULSE WIDTH

$$Pulse\ Width = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

EQUATION 11-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPR1L{:}CCP1CON\langle 5{:}4\rangle)}{4(PR2+1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 11-1).

11.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 11-4.

EQUATION 11-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2+1)]}{\log(2)}\ bits$$

Note:	If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 11-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 11-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

11.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 3.0 "Oscillator Module (With Fail-Safe Clock Monitor)"** for additional details.

11.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

11.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and DC1B bits of the CCP1CON register.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register.
   - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
   - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
   - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
   - Enable the CCP1 pin output driver by clearing the associated TRIS bit.

TABLE 11-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte (LSB)								xxxx xxxx	xxxx xxxx
CCPR1H	Capture/Compare/PWM Register 1 High Byte (MSB)								xxxx xxxx	xxxx xxxx
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	0000 0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	xxxx xxxx
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	xxxx xxxx
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture and Compare.

TABLE 11-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte (LSB)								xxxx xxxx	xxxx xxxx
CCPR1H	Capture/Compare/PWM Register 1 High Byte (MSB)								xxxx xxxx	xxxx xxxx
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	-000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	-000 0000
PR2	Timer2 Period Register								1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2	Timer2 Module Register								0000 0000	0000 0000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the PWM.

NOTES:

12.0 SPECIAL FEATURES OF THE CPU

The PIC12F683 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator Selection
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™

The PIC12F683 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

> **Note:** Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information.

12.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

REGISTER 12-1: CONFIG: CONFIGURATION WORD REGISTER

—	—	—	—	FCMEN	IESO	BOREN1	BOREN0
bit 15							bit 8

$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable'	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented**: Read as '1'

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enabled bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 10 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled
0 = Internal External Switchover mode is disabled

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 7 **$\overline{\text{CPD}}$:** Data Code Protection bit(2)
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 6 **$\overline{\text{CP}}$:** Code Protection bit(3)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** GP3/$\overline{\text{MCLR}}$ pin function select bit(4)
1 = GP3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = GP3/$\overline{\text{MCLR}}$ pin function is digital input, $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
110 = RCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire data EEPROM will be erased when the code protection is turned off.
3: The entire program memory will be erased when the code protection is turned off.
4: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

12.2 Calibration Bits

Brown-out Reset (BOR), Power-on Reset (POR) and 8 MHz internal oscillator (HFINTOSC) are factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2009h). The Calibration Word is not erased when using the specified bulk erase sequence in the "*PIC12F6XX/16F6XX Memory Programming Specification"* (DS41244) and thus, does not require reprogramming.

12.3 Reset

The PIC12F683 differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) WDT Reset during normal operation
c) WDT Reset during Sleep
d) $\overline{\text{MCLR}}$ Reset during normal operation
e) $\overline{\text{MCLR}}$ Reset during Sleep
f) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

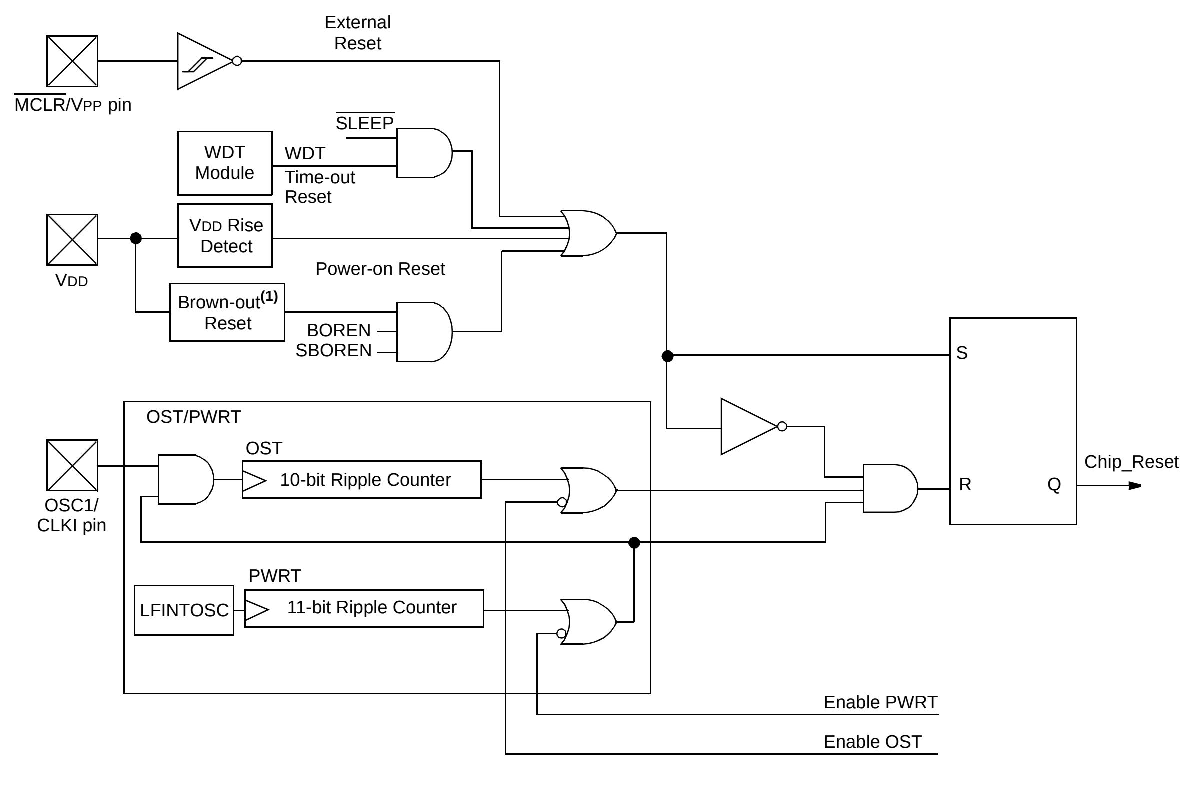
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 12-1).

12.3.1 POWER-ON RESET

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See **Section 15.0 "Electrical Specifications"** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until V_{DD} reaches V_{BOD} (see **Section 12.3.4 "Brown-Out Reset (BOR)"**).

Note:	The POR circuit does not produce an internal Reset when V_{DD} declines. To re-enable the POR, V_{DD} must reach Vss for a minimum of 100 µs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note *AN607, "Power-up Trouble Shooting"* (DS00607).

12.3.2 MCLR

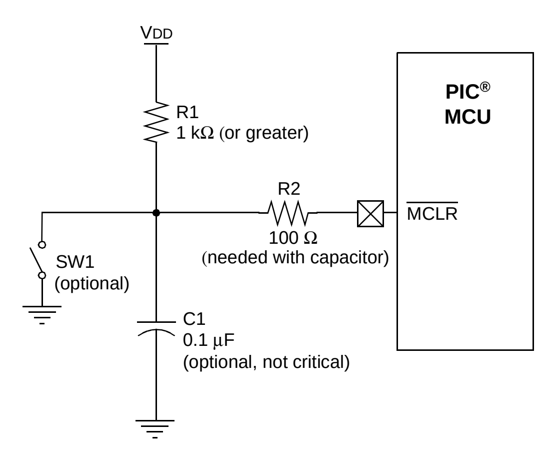
PIC12F683 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to V_{DD}. The use of an RC network, as shown in Figure 12-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = `0`, the Reset signal to the chip is generated internally. When the MCLRE = `1`, the GP3/MCLR pin becomes an external Reset input. In this mode, the GP3/MCLR pin has a weak pull-up to V_{DD}.

FIGURE 12-2: RECOMMENDED MCLR CIRCUIT



12.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.5 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A Configuration bit, PWRTE, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 15.0 "Electrical Specifications"**).

Note:	Voltage spikes below V_{SS} at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to V_{SS}.

12.3.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = `01`, the SBOREN bit of the PCON register enables/disables the BOR, allowing it to be controlled in software. By selecting BOREN<1:0> = `10`, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 12-1 for the Configuration Word definition.

A brown-out occurs when VDD falls below VBOR for greater than parameter TBOR (see **Section 15.0 "Electrical Specifications"**). The brown-out condition will reset the device. This will occur regardless of VDD slew rate. A Brown-out Reset may not occur if VDD falls below VBOR for less than parameter TBOR.

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 12-3). If enabled, the Power-up Timer will be invoked by the Reset and keep the chip in Reset an additional 64 ms.

Note:	The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word register.

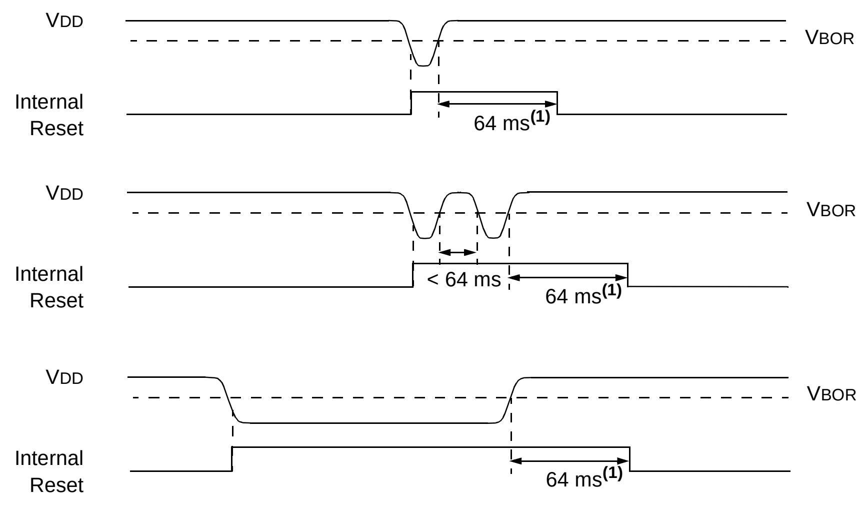
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

12.3.5 BOR CALIBRATION

The PIC12F683 stores the BOR calibration values in fuses located in the Calibration Word register (2008h). The Calibration Word register is not erased when using the specified bulk erase sequence in the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) and thus, does not require reprogramming.

Note:	Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for more information.

FIGURE 12-3: BROWN-OUT SITUATIONS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '`0`'.

12.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 3.7.2 "Two-Speed Start-up Sequence"** and **Section 3.8 "Fail-Safe Clock Monitor"**).

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC12F683 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

12.3.7 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 4.2.4 "Ultra Low-Power Wake-up"** and **Section 12.3.4 "Brown-Out Reset (BOR)"**.

TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	
XT, HS, LP	TPWRT + 1024 • TOSC	1024 • TOSC	TPWRT + 1024 • TOSC	1024 • TOSC	1024 • TOSC
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 12-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets(1)
CONFIG(2)	BOREN1	BOREN0	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
PCON			—	—	ULPWUE	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	--01 --qq	--0u --uu
STATUS			IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.
Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.
2: See Configuration Word register (Register 12-1) for operation of all register bits.

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$)

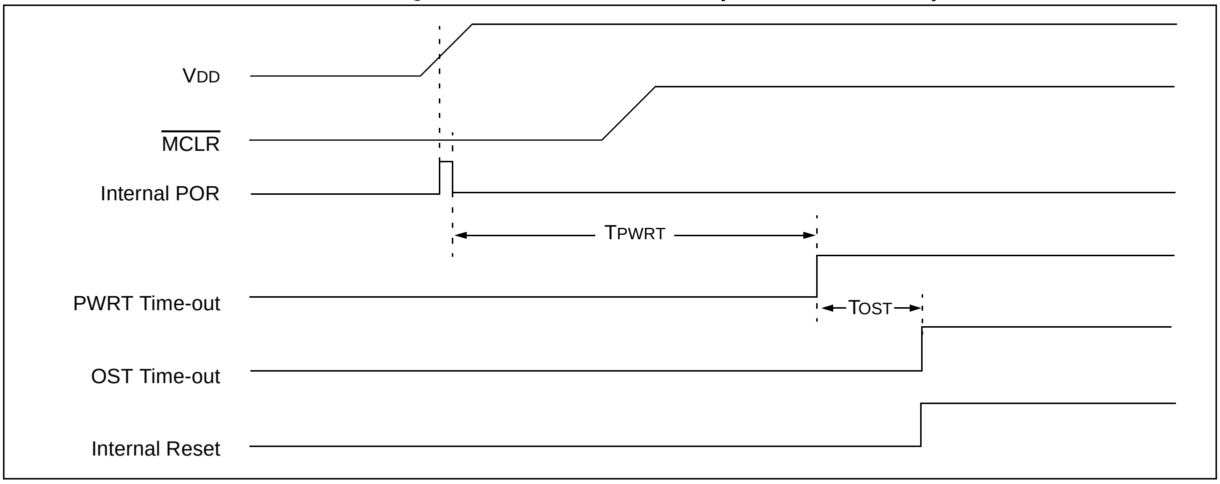


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$)

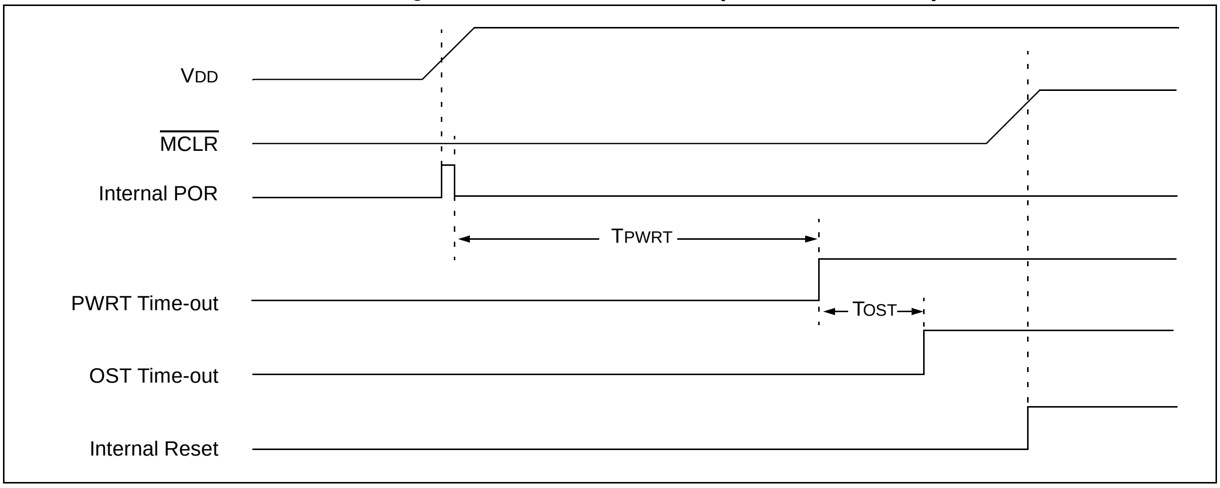


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ WITH V_{DD})

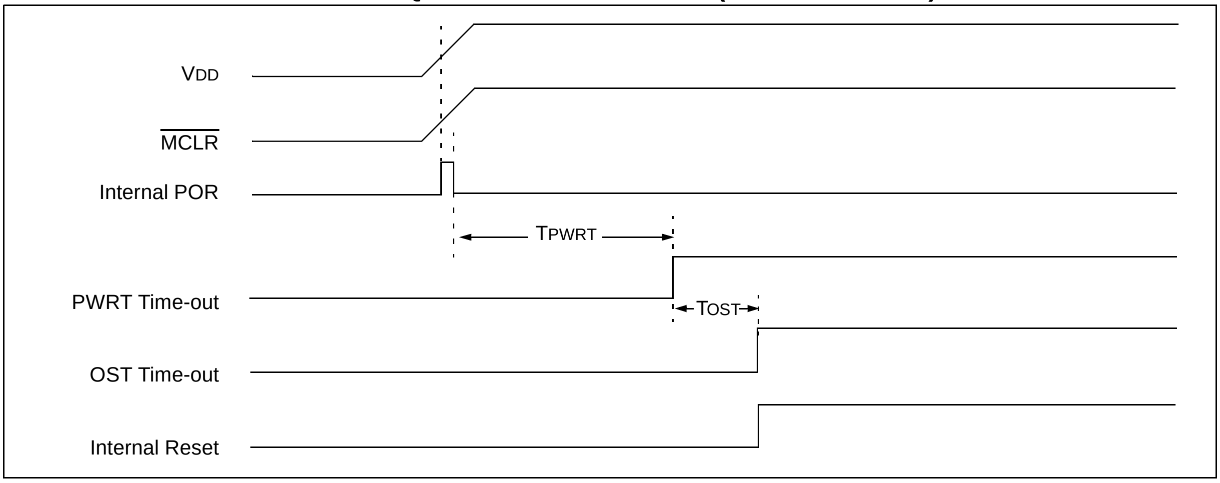


TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1)	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	05h	--x0 x000	--x0 x000	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	15h	--00 0000	--00 0000	--uu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
CMCON0	19h	0000 0000	0000 0000	uuuu uuuu
CMCON1	20h	---- --10	---- --10	---- --uu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	00-- 0000	00-- 0000	uu-- uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISIO	85h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	--01 --0x	--0u --uu(1,5)	--uu --uu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
WPU	95h	--11 -111	--11 -111	uuuu uuuu
IOC	96h	--00 0000	--00 0000	--uu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDAT	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If V_{DD} goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	$\overline{MCLR}$ Reset WDT Reset Brown-out Reset[(1)]	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
EECON1	9Ch	`---- x000`	`---- q000`	`---- uuuu`
EECON2	9Dh	`---- ----`	`---- ----`	`---- ----`
ADRESL	9Eh	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
ANSEL	9Fh	`-000 1111`	`-000 1111`	`-uuu uuuu`

Legend: `u` = unchanged, `x` = unknown, – = unimplemented bit, reads as ‘`0`’, `q` = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = `0`. All other Resets will cause bit 0 = `u`.

TABLE 12-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	`0001 1xxx`	`--01 --0x`
$\overline{MCLR}$ Reset during Normal Operation	000h	`000u uuuu`	`--0u --uu`
$\overline{MCLR}$ Reset during Sleep	000h	`0001 0uuu`	`--0u --uu`
WDT Reset	000h	`0000 uuuu`	`--0u --uu`
WDT Wake-up	PC + 1	`uuu0 0uuu`	`--uu --uu`
Brown-out Reset	000h	`0001 1uuu`	`--01 --10`
Interrupt Wake-up from Sleep	PC + 1[(1)]	`uuu1 0uuu`	`--uu --uu`

Legend: `u` = unchanged, `x` = unknown, – = unimplemented bit, reads as ‘`0`’.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

12.4 Interrupts

The PIC12F683 has multiple interrupt sources:

- External Interrupt GP2/INT
- Timer0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- GPIO Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 register. The corresponding interrupt enable bit is contained in the PIE1 register.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

For external interrupt events, such as the INT pin or GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

> **Note 1:** Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
>
> **2:** When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, data EEPROM or Enhanced CCP modules, refer to the respective peripheral section.

12.4.1 GP2/INT INTERRUPT

The external interrupt on the GP2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 12.7 "Power-Down Mode (Sleep)"** for details on Sleep and Figure 12-10 for timing of wake-up from Sleep through GP2/INT interrupt.

> **Note:** The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

12.4.2 TIMER0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing the T0IE bit of the INTCON register. See **Section 5.0 "Timer0 Module"** for operation of the Timer0 module.

12.4.3 GPIO INTERRUPT

An input change on GPIO change sets the GPIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the GPIE bit of the INTCON register. Plus, individual pins can be configured through the IOC register.

Note:	If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.

FIGURE 12-7: INTERRUPT LOGIC

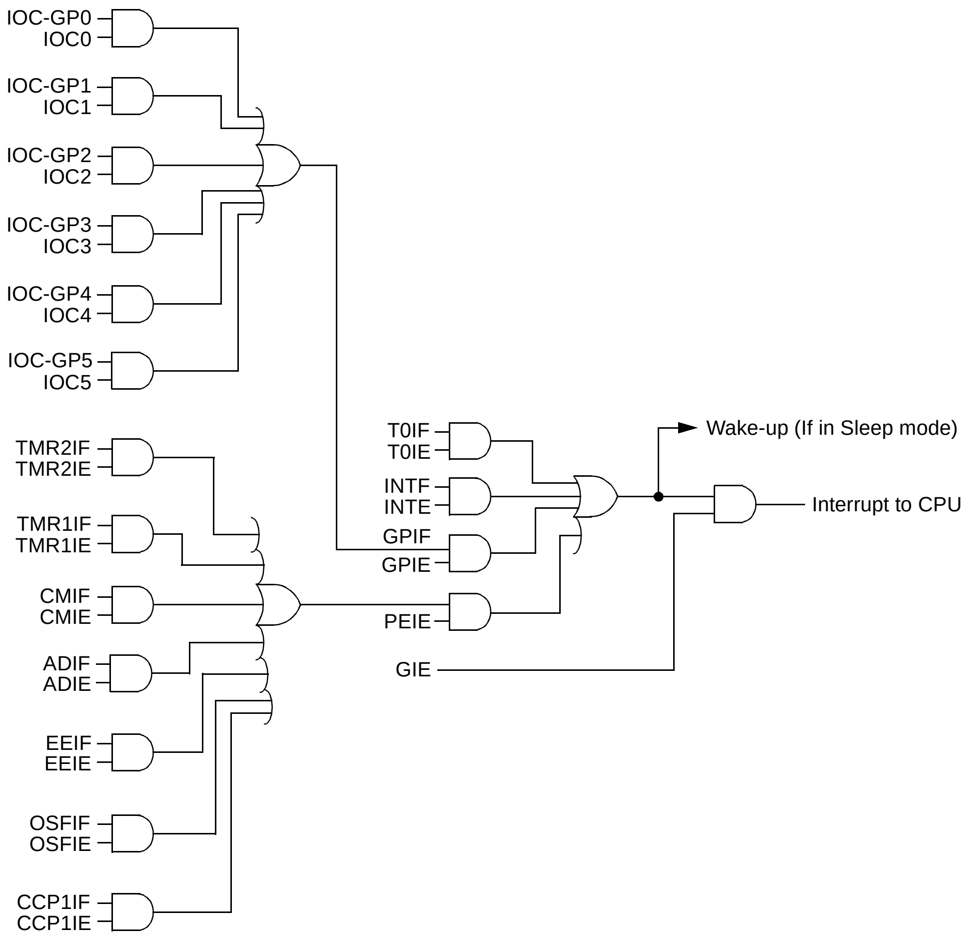
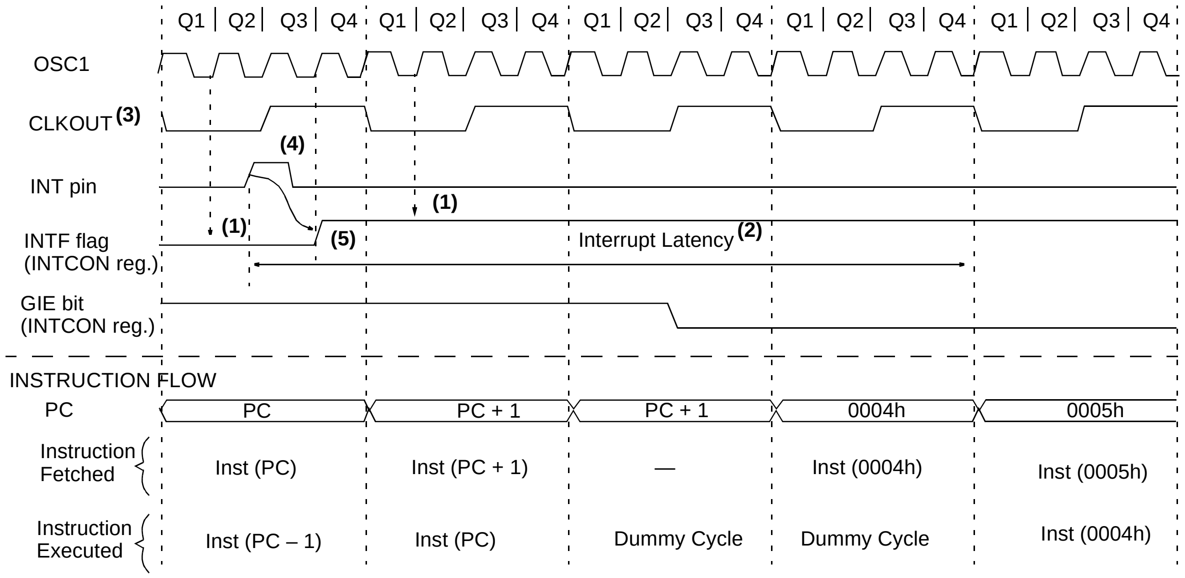


FIGURE 12-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 15.0 “Electrical Specifications”**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, – = unimplemented read as ‘0’, q = value depends upon condition. Shaded cells are not used by the interrupt module.

12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the lower 16 bytes of all banks are common in the PIC12F683 (see Figure 2-2), temporary holding registers, W_TEMP and STATUS_TEMP, should be placed in here. These 16 locations do not require banking and therefore, makes it easier to context save and restore. The same code shown in Example 12-1 can be used to:

- Store the W register.
- Store the STATUS register.
- Execute the ISR code.
- Restore the Status (and Bank Select Bit register).
- Restore the W register.

Note:	The PIC12F683 normally does not require saving the PCLATH. However, if computed `GOTO`'s are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

12.6 Watchdog Timer (WDT)

The WDT has the following features:

- Operates from the LFINTOSC (31 kHz)
- Contains a 16-bit prescaler
- Shares an 8-bit prescaler with Timer0
- Time-out period is from 1 ms to 268 seconds
- Configuration bit and software controlled

WDT is cleared under certain conditions described in Table 12-7.

12.6.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit of the OSCCON register does not reflect that the LFINTOSC is enabled.

The value of WDTCON is '`---0 1000`' on all Resets. This gives a nominal time base of 17 ms.

Note:	When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

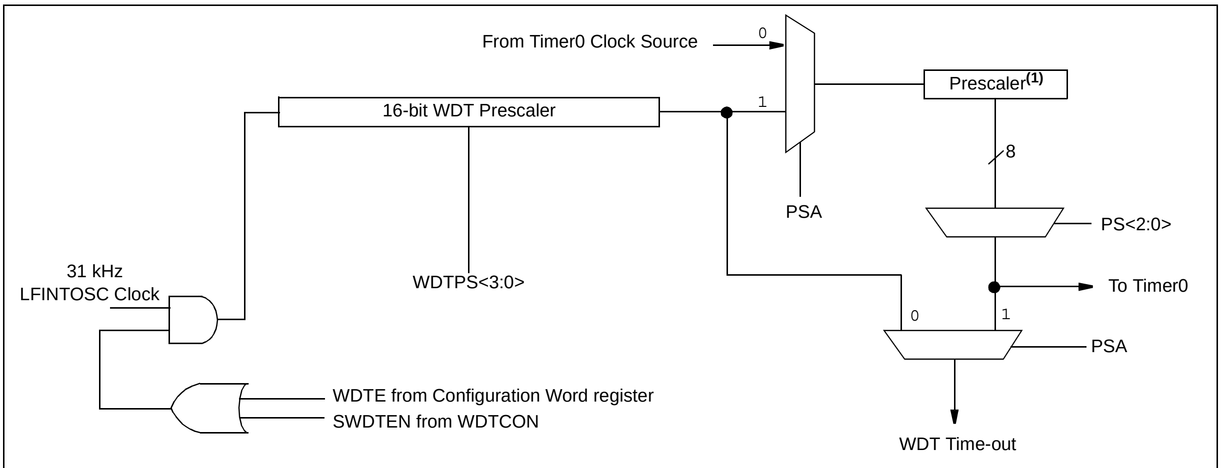
12.6.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit of the WDTCON register has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits of the OPTION register have the same function as in previous versions of the PIC12F683 Family of microcontrollers. See **Section 5.0 "Timer0 Module"** for more information.

FIGURE 12-9: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This is the shared Timer0/WDT prescaler. See **Section 5.0 "Timer0 Module"** for more information.

TABLE 12-7: WDT STATUS

Conditions	WDT
WDTE = `0`	Cleared
`CLRWDT` Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

REGISTER 12-2: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

`0000` = 1:32
`0001` = 1:64
`0010` = 1:128
`0011` = 1:256
`0100` = 1:512 (Reset value)
`0101` = 1:1024
`0110` = 1:2048
`0111` = 1:4096
`1000` = 1:8192
`1001` = 1:16384
`1010` = 1:32768
`1011` = 1:65536
`1100` = Reserved
`1101` = Reserved
`1110` = Reserved
`1111` = Reserved

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer[(1)]

`1` = WDT is turned on
`0` = WDT is turned off (Reset value)

Note 1: If WDTE Configuration bit = `1`, then WDT is always enabled, irrespective of this control bit. If WDTE Configuration bit = `0`, then it is possible to turn WDT on/off with this control bit.

TABLE 12-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN	`---0 1000`	`---0 1000`
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	`1111 1111`	`1111 1111`
CONFIG	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 12-1 for operation of all Configuration Word register bits.

12.7 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- $\overline{PD}$ bit in the STATUS register is cleared.
- $\overline{TO}$ bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at V_{DD} or V_{SS}, with no external circuitry drawing current from the I/O pin and the comparators and CV_{REF} should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The $\overline{MCLR}$ pin must be at a logic high level.

Note:	It should be noted that a Reset generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

12.7.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on $\overline{MCLR}$ pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from GP2/INT pin, GPIO change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of a device Reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when Sleep is invoked. $\overline{TO}$ bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. Timer1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ECCP Capture mode interrupt.
3. A/D conversion (when A/D clock source is FRC).
4. EEPROM write operation completion.
5. Comparator output changes state.
6. Interrupt-on-change.
7. External Interrupt from INT pin.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note:	If the global interrupts are disabled (GIE is cleared) and any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

12.7.2 WAKE-UP USING INTERRUPTS

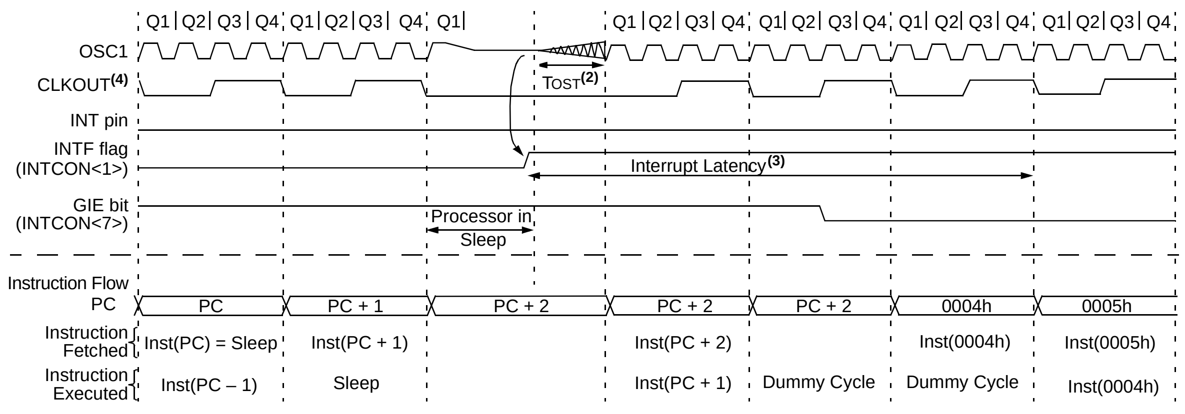
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the $\overline{TO}$ bit will not be set and the $\overline{PD}$ bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will Immediately wake-up from Sleep. The SLEEP instruction is executed. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction. See Figure 12-10 for more details.

FIGURE 12-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.
2: T_{OST} = 1024 T_{OSC} (drawing not to scale). This delay does not apply to EC and RCIO Oscillator modes.
3: GIE = `1` assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = `0`, execution will continue in-line.
4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

12.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information.

12.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

12.10 In-Circuit Serial Programming™

The PIC12F683 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

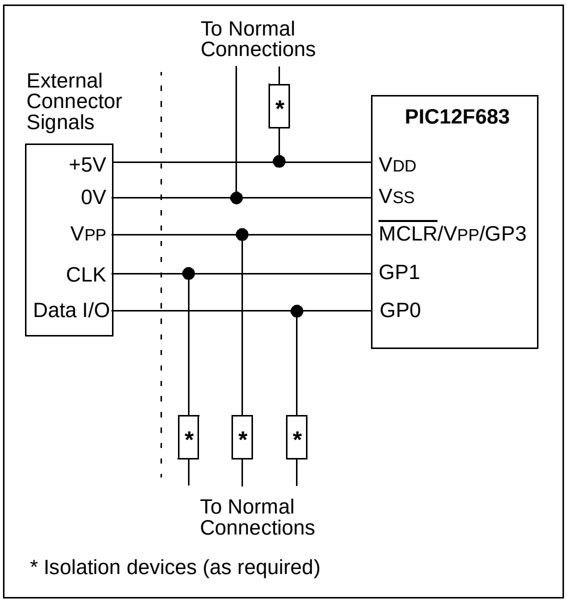
- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH}. See the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information. GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 12-11.

FIGURE 12-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



12.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with a 14-pin device is not practical. A special 14-pin PIC12F683 ICD device is used with MPLAB ICD 2 to provide separate clock, data and $\overline{MCLR}$ pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC12F683 device. The debugging adapter is the only source of the ICD device.

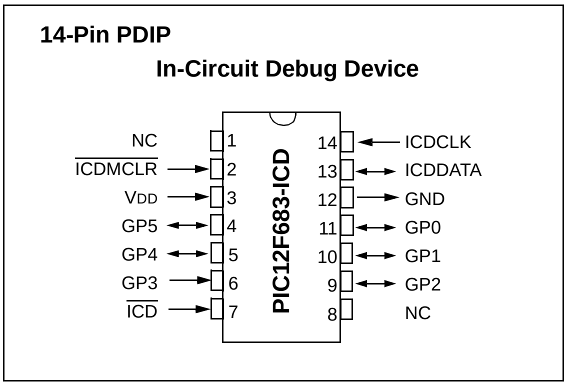
When the $\overline{ICD}$ pin on the PIC12F683 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-9 shows which features are consumed by the background debugger.

TABLE 12-9: DEBUGGER RESOURCES

Resource	Description
Stack	1 level
Program Memory	Address 0h must be `NOP` 700h-7FFh

For more information, see "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 12-12: 14-PIN ICD PINOUT



13.0 INSTRUCTION SET SUMMARY

The PIC12F683 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

Table 13-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a `NOP`.

All instruction examples use the format '`0xhh`' to represent a hexadecimal number, where '`h`' signifies a hexadecimal digit.

13.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a `CLRF PORTA` instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RAIF flag.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= `0` or `1`). The assembler will generate code with x = `0`. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = `0`: store result in W, d = `1`: store result in file register f. Default is d = `1`.
PC	Program Counter
$\overline{TO}$	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
$\overline{PD}$	Power-down bit

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

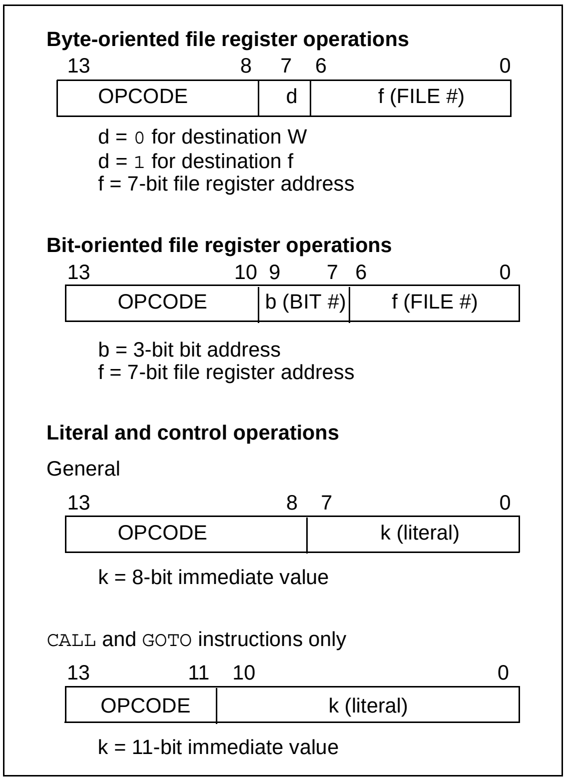


TABLE 13-2: PIC12F683 INSTRUCTION SET

Mnemonic,	Operands	Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	**1, 2**
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	**1, 2**
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	**2**
CLRW	–	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	**1, 2**
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	**1, 2**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	00	1011	dfff	ffff		**1, 2, 3**
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	**1, 2**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	00	1111	dfff	ffff		**1, 2, 3**
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	**1, 2**
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	**1, 2**
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	–	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	**1, 2**
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	**1, 2**
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	**1, 2**
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		**1, 2**
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	**1, 2**
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		**1, 2**
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		**1, 2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 **(2)**	01	10bb	bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 **(2)**	01	11bb	bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	–	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF GPIO, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

13.2 Instruction Descriptions

ADDLW	**Add literal and W**
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	**Add W and f**
Syntax:	[*label*] ADDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	**AND literal with W**
Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	**AND W with f**
Syntax:	[*label*] ANDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	**Bit Clear f**
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	**Bit Set f**
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	**Bit Test f, Skip if Clear**
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BTFSS	**Bit Test f, Skip if Set**
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = `1`
Status Affected:	None
Description:	If bit ‘b’ in register ‘f’ is ‘`0`’, the next instruction is executed. If bit ‘b’ is ‘`1`’, then the next instruction is discarded and a `NOP` is executed instead, making this a 2-cycle instruction.

CLRWDT	**Clear Watchdog Timer**
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT `0` → WDT prescaler, `1` → $\overline{TO}$ `1` → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	`CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

CALL	**Call Subroutine**
Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. `CALL` is a two-cycle instruction.

COMF	**Complement f**
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ d ∈ [`0`,`1`]
Operation:	$(\overline{f})$ → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are complemented. If ‘d’ is ‘`0`’, the result is stored in W. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

CLRF	**Clear f**
Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	00h → (f) `1` → Z
Status Affected:	Z
Description:	The contents of register ‘f’ are cleared and the Z bit is set.

DECF	**Decrement f**
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ d ∈ [`0`,`1`]
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is ‘`0`’, the result is stored in the W register. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

CLRW	**Clear W**
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) `1` → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘1’, the next instruction is executed. If the result is ‘0’, then a NOP is executed instead, making it a 2-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	0 ≤ k ≤ 2047
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘1’, the next instruction is executed. If the result is ‘0’, a NOP is executed instead, making it a 2-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[*label*] IORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR’ed with the eight-bit literal ‘k’. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register ‘f’. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

MOVF — **Move f**

Syntax:	[*label*] MOVF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	`MOVF FSR, 0` After Instruction W = value in FSR register Z = 1

MOVWF — **Move W to f**

Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 127
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register ‘f’.
Words:	1
Cycles:	1
Example:	`MOVW OPTION F` Before Instruction OPTION = 0xFF W = 0x4F After Instruction OPTION = 0x4F W = 0x4F

MOVLW — **Move literal to W**

Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal ‘k’ is loaded into W register. The “don’t cares” will assemble as ‘0’s.
Words:	1
Cycles:	1
Example:	`MOVLW 0x5A` After Instruction W = 0x5A

NOP — **No Operation**

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	`RETFIE` After Interrupt PC = TOS GIE = 1

RETLW	Return with literal in W
Syntax:	[*label*] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2

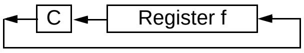
<u>Example:</u>

```
        CALL TABLE;W contains table
            ;offset value
        •   ;W now has table value
TABLE   •
        •
        ADDWF PC  ;W = offset
        RETLW k1  ;Begin table
        RETLW k2  ;
        •
        •
        •
        RETLW kn  ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLF	**Rotate Left f through Carry**
Syntax:	[*label*] RLF f,d
Operands:	$0 \le f \le 127$ $d \in$ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words:	1
Cycles:	1
Example:	`RLF REG1,0`

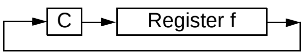
Before Instruction

```
REG1   =   1110 0110
C      =   0
```

After Instruction

```
REG1   =   1110 0110
W      =   1100 1100
C      =   1
```

RRF	**Rotate Right f through Carry**
Syntax:	[*label*] RRF f,d
Operands:	$0 \le f \le 127$ $d \in$ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP	**Enter Sleep mode**
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h $\rightarrow$ WDT, 0 $\rightarrow$ WDT prescaler, 1 $\rightarrow$ $\overline{TO}$, 0 $\rightarrow$ $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBLW	**Subtract W from literal**
Syntax:	[*label*] SUBLW k
Operands:	$0 \le k \le 255$
Operation:	k - (W) $\rightarrow$ (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W $\le$ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> $\le$ k<3:0>

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

NOTES:

14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit micro-controller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

14.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

14.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

14.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

14.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

14.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

14.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

14.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

14.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *"Product Selector Guide"* (DS00148) for the complete list of demonstration, development and evaluation kits.

15.0 ELECTRICAL SPECIFICATIONS

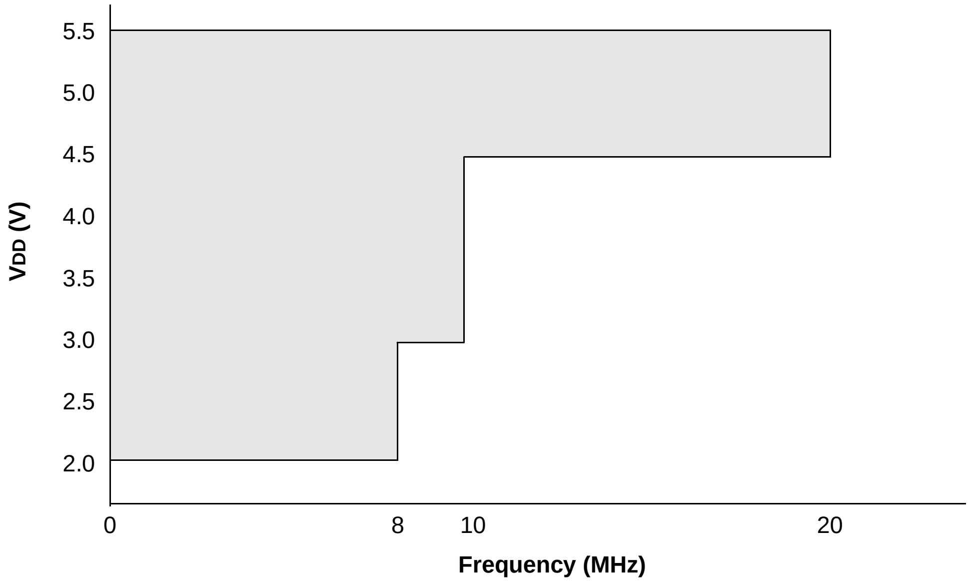
Absolute Maximum Ratings(†)

Ambient temperature under bias .... -40° to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss .... -0.3V to +13.5V
Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) .... 800 mW
Maximum current out of V_{SS} pin .... 95 mA
Maximum current into V_{DD} pin .... 95 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) .... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) .... ± 20 mA
Maximum output current sunk by any I/O pin .... 25 mA
Maximum output current sourced by any I/O pin .... 25 mA
Maximum current sunk by GPIO .... 90 mA
Maximum current sourced GPIO .... 90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$.

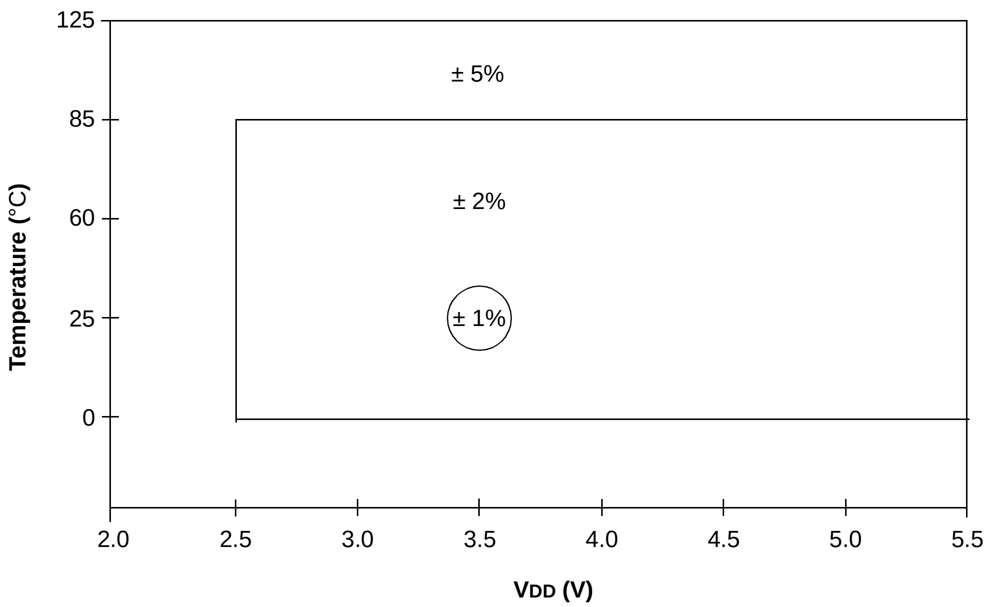
† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

FIGURE 15-1: PIC12F683 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



15.1 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**	2.0	—	5.5	V	FOSC < = 8 MHz: HFINTOSC, EC
D001			2.0	—	5.5	V	FOSC < = 4 MHz
D001C			3.0	—	5.5	V	FOSC < = 10 MHz
D001D			4.5	—	5.5	V	FOSC < = 20 MHz
D002*	VDR	**RAM Data Retention Voltage**(1)	1.5	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3.1 "Power-on Reset"** for details.
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 12.3.1 "Power-on Reset"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

15.2 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for industrial -40°C ≤ T_A ≤ +125°C for extended					
Param No.	**Device Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
						V_{DD}	**Note**
D010	**Supply Current (I_{DD})(1, 2)**	—	11	16	μA	2.0	F_{OSC} = 32 kHz LP Oscillator mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011*		—	140	240	μA	2.0	F_{OSC} = 1 MHz XT Oscillator mode
		—	220	380	μA	3.0	
		—	380	550	μA	5.0	
D012		—	260	360	μA	2.0	F_{OSC} = 4 MHz XT Oscillator mode
		—	420	650	μA	3.0	
		—	0.8	1.1	mA	5.0	
D013*		—	130	220	μA	2.0	F_{OSC} = 1 MHz EC Oscillator mode
		—	215	360	μA	3.0	
		—	360	520	μA	5.0	
D014		—	220	340	μA	2.0	F_{OSC} = 4 MHz EC Oscillator mode
		—	375	550	μA	3.0	
		—	0.65	1.0	mA	5.0	
D015		—	8	20	μA	2.0	F_{OSC} = 31 kHz LFINTOSC mode
		—	16	40	μA	3.0	
		—	31	65	μA	5.0	
D016*		—	340	450	μA	2.0	F_{OSC} = 4 MHz HFINTOSC mode
		—	500	700	μA	3.0	
		—	0.8	1.2	mA	5.0	
D017		—	410	650	μA	2.0	F_{OSC} = 8 MHz HFINTOSC mode
		—	700	950	μA	3.0	
		—	1.30	1.65	mA	5.0	
D018		—	230	400	μA	2.0	F_{OSC} = 4 MHz EXTRC mode(3)
		—	400	680	μA	3.0	
		—	0.63	1.1	mA	5.0	
D019		—	2.6	3.25	mA	4.5	F_{OSC} = 20 MHz HS Oscillator mode
		—	2.8	3.35	mA	5.0	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

15.3 DC Characteristics: PIC12F683-I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions: VDD	Conditions: Note
D020	**Power-down Base Current(IPD)(2)**	—	0.05	1.2	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	1.5	μA	3.0	
		—	0.35	1.8	μA	5.0	
		—	150	500	nA	3.0	-40°C ≤ TA ≤ +25°C
D021		—	1.0	2.2	μA	2.0	WDT Current(1)
		—	2.0	4.0	μA	3.0	
		—	3.0	7.0	μA	5.0	
D022		—	42	60	μA	3.0	BOR Current(1)
		—	85	122	μA	5.0	
D023		—	32	45	μA	2.0	Comparator Current(1), both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024		—	30	36	μA	2.0	CVREF Current(1) (high range)
		—	45	55	μA	3.0	
		—	75	95	μA	5.0	
D025*		—	39	47	μA	2.0	CVREF Current(1) (low range)
		—	59	72	μA	3.0	
		—	98	124	μA	5.0	
D026		—	4.5	7.0	μA	2.0	T1OSC Current(1), 32.768 kHz
		—	5.0	8.0	μA	3.0	
		—	6.0	12	μA	5.0	
D027		—	0.30	1.6	μA	3.0	A/D Current(1), no conversion in progress
		—	0.36	1.9	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.4 DC Characteristics: PIC12F683-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions: VDD	Conditions: Note
D020E	**Power-down Base Current (IPD)(2)**	—	0.05	9	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	11	μA	3.0	
		—	0.35	15	μA	5.0	
D021E		—	1	17.5	μA	2.0	WDT Current(1)
		—	2	19	μA	3.0	
		—	3	22	μA	5.0	
D022E		—	42	65	μA	3.0	BOR Current(1)
		—	85	127	μA	5.0	
D023E		—	32	45	μA	2.0	Comparator Current(1), both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024E		—	30	70	μA	2.0	CVREF Current(1) (high range)
		—	45	90	μA	3.0	
		—	75	120	μA	5.0	
D025E*		—	39	91	μA	2.0	CVREF Current(1) (low range)
		—	59	117	μA	3.0	
		—	98	156	μA	5.0	
D026E		—	4.5	25	μA	2.0	T1OSC Current(1), 32.768 kHz
		—	5	30	μA	3.0	
		—	6	40	μA	5.0	
D027E		—	0.30	12	μA	3.0	A/D Current(1), no conversion in progress
		—	0.36	16	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

15.5 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O Port:					
D030		with TTL buffer	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			Vss	—	0.15 VDD	V	2.0V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer	Vss	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
D032		$\overline{MCLR}$, OSC1 (RC mode)(1)	VSS	—	0.2 VDD	V	
D033		OSC1 (XT and LP modes)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)	VSS	—	0.3 VDD	V	
	VIH	Input High Voltage					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	VDD	V	2.0V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	2.0V ≤ VDD ≤ 5.5V
D042		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	**(Note 1)**
	IIL	Input Leakage Current(2)					
D060		I/O ports	—	± 0.1	± 1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D061		$\overline{MCLR}$(3)	—	± 0.1	± 5	μA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070*	IPUR	GPIO Weak Pull-up Current	50	250	400	μA	VDD = 5.0V, VPIN = VSS
	VOL	Output Low Voltage(5)					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
	VOH	Output High Voltage(5)					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 10.4.1 “Using the Data EEPROM”** for additional information.

5: Including OSC2 in CLKOUT mode.

15.5 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D100	IULP	Ultra Low-Power Wake-Up Current	—	200	—	nA	See Application Note AN879, "*Using the Microchip Ultra Low-Power Wake-up Module*" (DS00879)
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write Cycle Time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(4)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 10.4.1 "Using the Data EEPROM"** for additional information.

5: Including OSC2 in CLKOUT mode.

15.6 Thermal Considerations

Param No.	Sym	Characteristic	Typ	Units	Conditions
Standard Operating Conditions (unless otherwise stated) Operating temperature $-40°C \le T_A \le +125°C$					
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	84.6	°C/W	8-pin PDIP package
			163.0	°C/W	8-pin SOIC package
			52.4	°C/W	8-pin DFN-S 4x4x0.9 mm package
			46.3	°C/W	8-pin DFN-S 6x5 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	41.2	°C/W	8-pin PDIP package
			38.8	°C/W	8-pin SOIC package
			3.0	°C/W	8-pin DFN-S 4x4x0.9 mm package
			2.6	°C/W	8-pin DFN-S 6x5 mm package
TH03	T_J	Junction Temperature	150	°C	For derated power calculations
TH04	PD	Power Dissipation	—	W	PD = $P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ **(NOTE 1)**
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = (T_J - T_A)/\theta_{JA}$ **(NOTE 2, 3)**

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (P_{DER}).

15.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

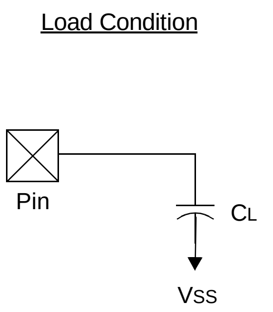
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{\text{RD}}$
cs	$\overline{\text{CS}}$	rw	$\overline{\text{RD}}$ or $\overline{\text{WR}}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{\text{SS}}$
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	$\overline{\text{MCLR}}$	wr	$\overline{\text{WR}}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 15-3: LOAD CONDITIONS



Legend: C_L = 50 pF for all pins
15 pF for OSC2 output

15.8 AC Characteristics: PIC12F683 (Industrial, Extended)

FIGURE 15-4: CLOCK TIMING

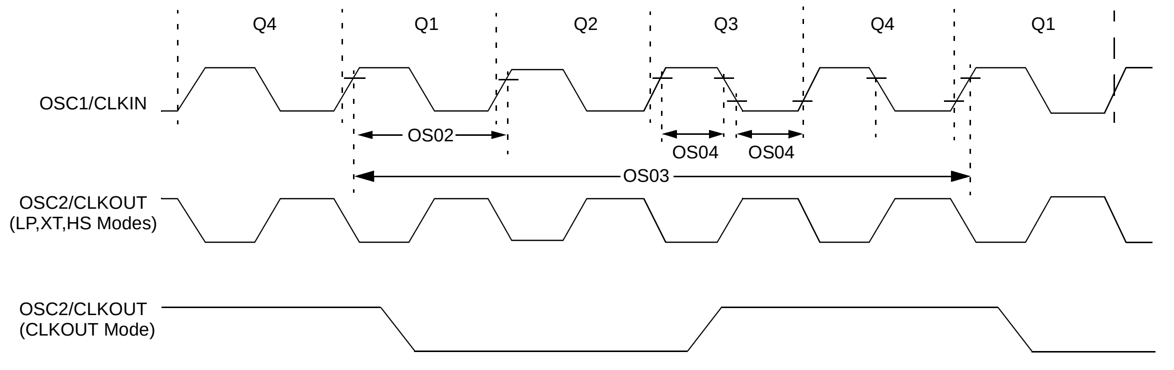


TABLE 15-1: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS01	FOSC	External CLKIN Frequency(1)	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency(1)	—	32.768	—	kHz	LP Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
OS02	TOSC	External CLKIN Period(1)	27	—	•	μs	LP Oscillator mode
			250	—	•	ns	XT Oscillator mode
			50	—	•	ns	HS Oscillator mode
			50	—	•	ns	EC Oscillator mode
		Oscillator Period(1)	—	30.5	—	μs	LP Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
OS03	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	2	—	—	μs	LP oscillator
			100	—	—	ns	XT oscillator
			20	—	—	ns	HS oscillator
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	0	—	•	ns	LP oscillator
			0	—	•	ns	XT oscillator
			0	—	•	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

TABLE 15-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristic**	**Freq. Tolerance**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
OS06	TWARM	Internal Oscillator Switch when running(3)	—	—	—	2	TOSC	Slowest clock
OS07	TSC	Fail-Safe Sample Clock Period(1)	—	—	21	—	ms	LFINTOSC/64
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(2)	±1%	7.92	8.0	8.08	MHz	VDD = 3.5V, 25°C
			±2%	7.84	8.0	8.16	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	7.60	8.0	8.40	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS09*	LFOSC	Internal Uncalibrated LFINTOSC Frequency	—	15	31	45	kHz	
OS10*	TIOSC ST	HFINTOSC Oscillator Wake-up from Sleep Start-up Time	—	5.5	12	24	µs	VDD = 2.0V, -40°C to +85°C
			—	3.5	7	14	µs	VDD = 3.0V, -40°C to +85°C
			—	3	6	11	µs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

FIGURE 15-5: CLKOUT AND I/O TIMING

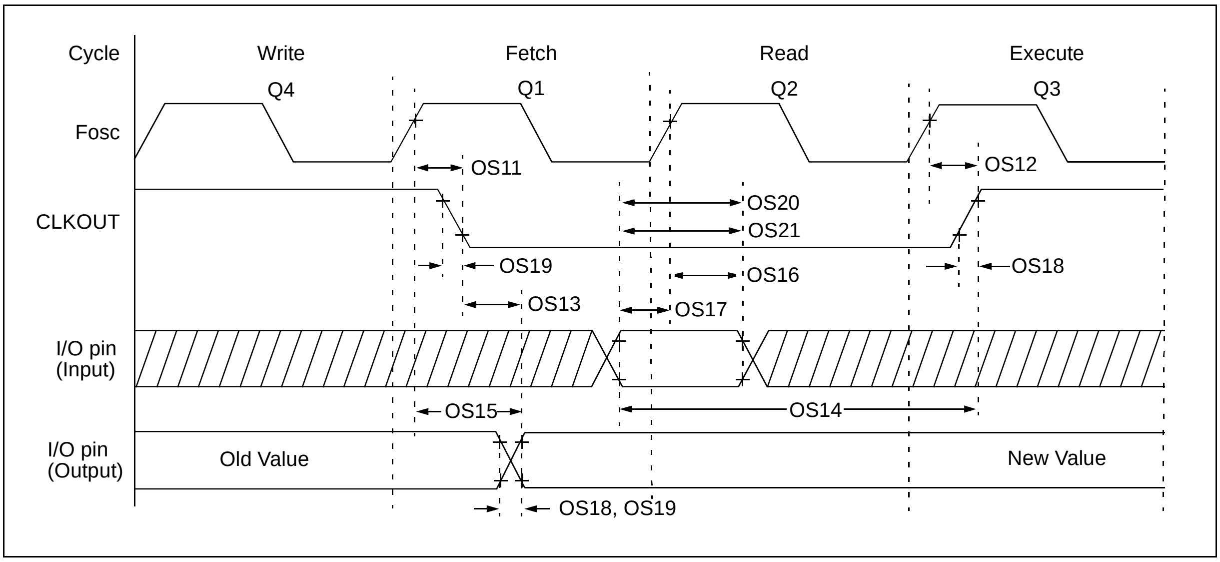


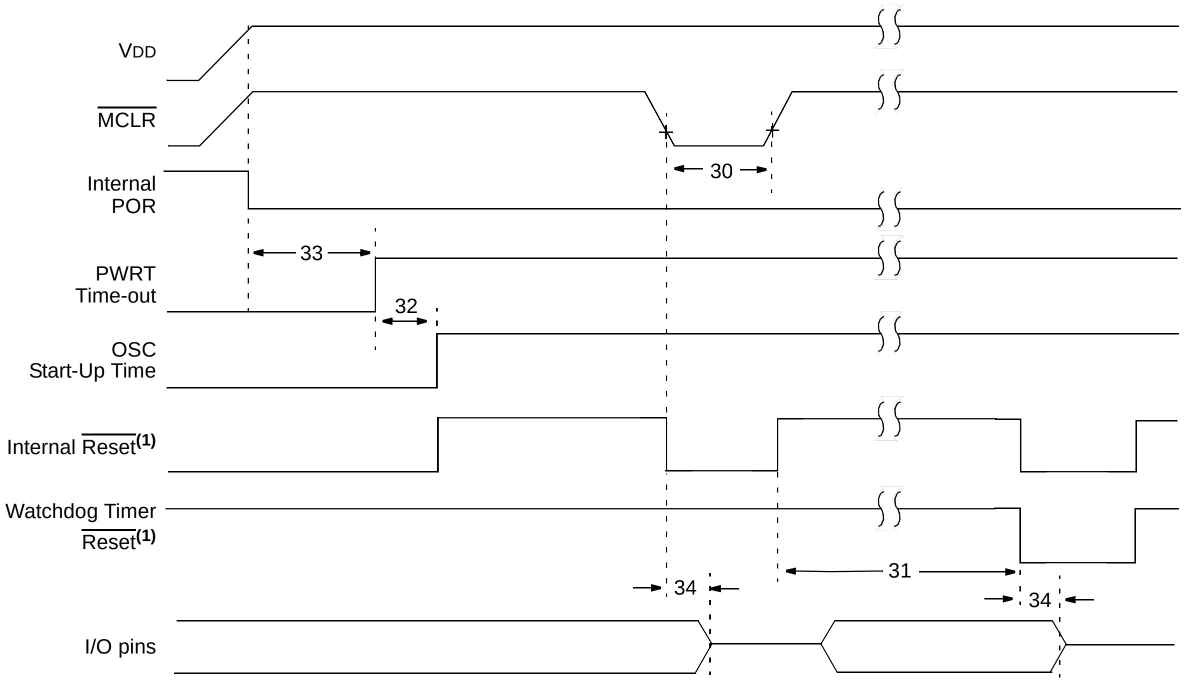
TABLE 15-3: CLKOUT AND I/O TIMING PARAMETERS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS11	TOSH2CKL	FOSC↑ to CLKOUT↓ (1)	—	—	70	ns	VDD = 5.0V
OS12	TOSH2CKH	FOSC↑ to CLKOUT↑ (1)	—	—	72	ns	VDD = 5.0V
OS13	TCKL2IOV	CLKOUT↓ to Port out valid(1)	—	—	20	ns	
OS14	TIOV2CKH	Port input valid before CLKOUT↑(1)	TOSC + 200 ns	—	—	ns	
OS15*	TOSH2IOV	FOSC↑ (Q1 cycle) to Port out valid	—	50	70	ns	VDD = 5.0V
OS16	TOSH2IOI	FOSC↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 5.0V
OS17	TIOV2OSH	Port input valid to FOSC↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TIOR	Port output rise time(2)	— —	15 40	72 32	ns	VDD = 2.0V VDD = 5.0V
OS19	TIOF	Port output fall time(2)	— —	28 15	55 30	ns	VDD = 2.0V VDD = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TGPP	GPIO interrupt-on-change new input level time	TCY	—	—	ns	

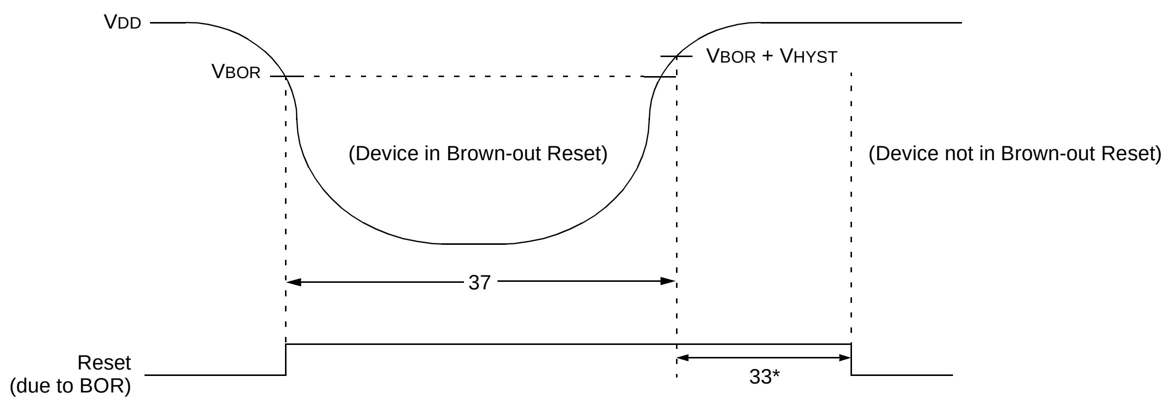
* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated.
Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.
2: Includes OSC2 in CLKOUT mode.

FIGURE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

FIGURE 15-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS



* 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '0'.

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2 5	— —	— —	µs µs	VDD = 5V, -40°C to +85°C VDD = 5V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	16 16	29 31	ms ms	VDD = 5V, -40°C to +85°C VDD = 5V
32	TOST	Oscillation Start-up Timer Period(1, 2)	—	1024	—	TOSC	**(NOTE 3)**
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	VBOR	Brown-out Reset Voltage	2.0	—	2.2	V	**(NOTE 4)**
36*	VHYST	Brown-out Reset Hysteresis	—	50	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	µs	VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 15-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

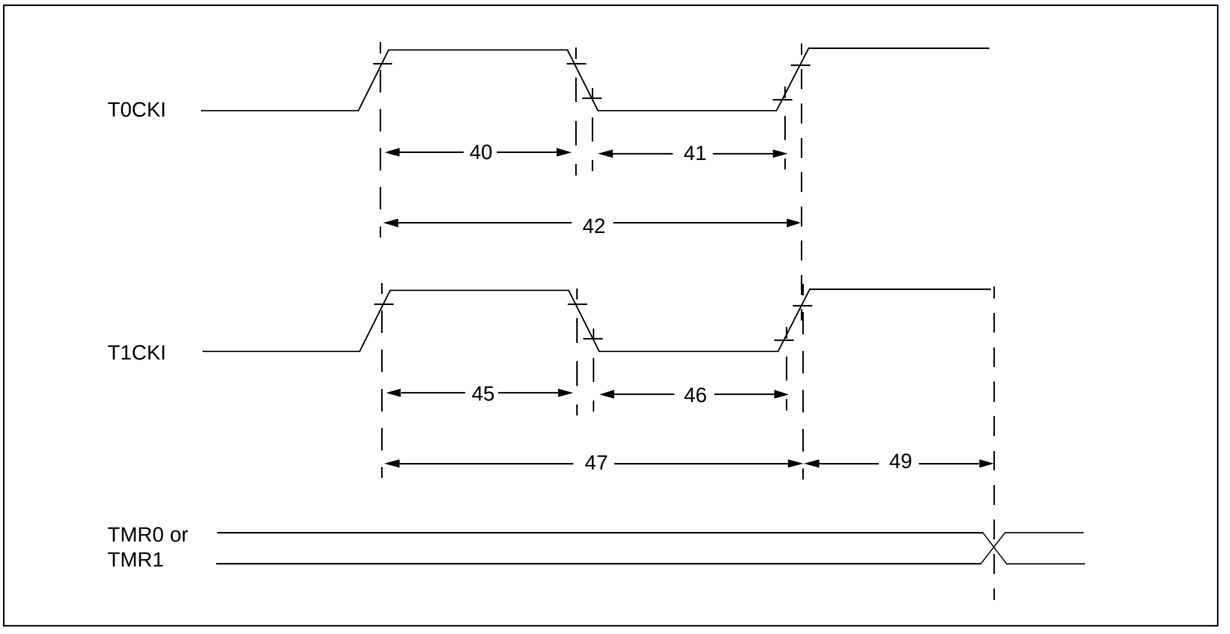


TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

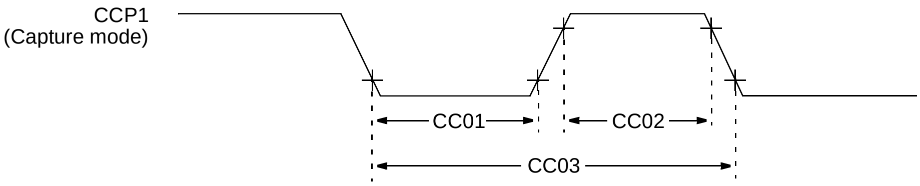
Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or $\frac{TCY + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{TCY + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-9: CAPTURE/COMPARE/PWM TIMINGS (ECCP)



Note: Refer to Figure 15-3 for load conditions.

TABLE 15-6: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ T_A ≤ +125°C								
Param No.	**Sym**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
CC01*	TccL	CCP1 Input Low Time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 15-7: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ T_A ≤ +125°C								
Param No.	**Sym**	**Characteristics**		**Min**	**Typ†**	**Max**	**Units**	**Comments**
CM01	V_{OS}	Input Offset Voltage		—	± 5.0	± 10	mV	(V_{DD} - 1.5)/2
CM02	V_{CM}	Input Common Mode Voltage		0	—	V_{DD} – 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	T_{RT}	Response Time	Falling	—	150	600	ns	**(NOTE 1)**
			Rising	—	200	1000	ns	
CM05*	T_{MC2COV}	Comparator Mode Change to Output Valid		—	—	10	µs	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (V_{DD} - 1.5)/2 - 100 mV to (V_{DD} - 1.5)/2 + 20 mV.

TABLE 15-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Comments**
CV01*	C_{LSB}	Step Size[(2)]	— —	V_{DD}/24 V_{DD}/32	— —	V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02*	C_{ACC}	Absolute Accuracy	— —	— —	± 1/2 ± 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03*	C_R	Unit Resistor Value (R)	—	2k	—	Ω	
CV04*	C_{ST}	Settling Time[(1)]	—	—	10	µs	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from ‘0000’ to ‘1111’.

2: See **Section 8.11 “Comparator Voltage Reference”** for more information.

TABLE 15-9: PIC12F683 A/D CONVERTER (ADC) CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	±1	LSb	VREF = 5.12V
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V
AD04	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.12V
AD07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.12V
AD06 AD06A	VREF	Reference Voltage(3)	2.2 2.7	—	— VDD	V	 Absolute minimum to ensure 1 LSb accuracy
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	IREF	VREF Input Current(3)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

TABLE 15-10: PIC12F683 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD130*	TAD	A/D Clock Period	1.6	—	9.0	µs	TOSC-based, VREF ≥ 3.0V
			3.0	—	9.0	µs	TOSC-based, VREF full range
		A/D Internal RC Oscillator Period	3.0	6.0	9.0	µs	ADCS<1:0> = 11 (ADRC mode) At VDD = 2.5V
			1.6	4.0	6.0	µs	At VDD = 5.0V
AD131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO/$\overline{\text{DONE}}$ bit to new data in A/D Result register.
AD132*	TACQ	Acquisition Time		11.5	—	µs	
AD133*	TAMP	Amplifier Settling Time	—	—	5	µs	
AD134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	
			—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

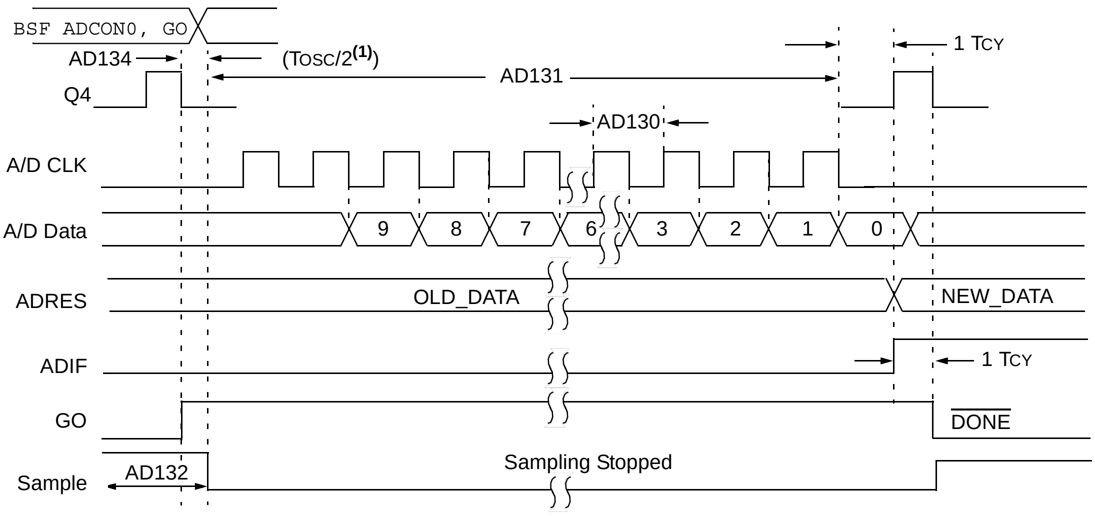
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

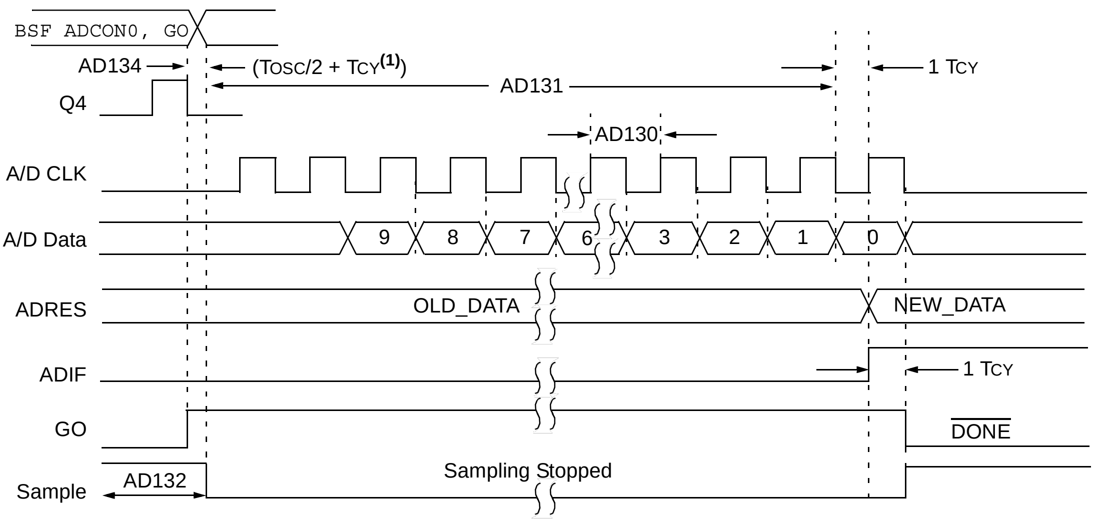
2: See **Section 9.3 "A/D Acquisition Requirements"** for minimum conditions.

FIGURE 15-10: PIC12F683 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

FIGURE 15-11: PIC12F683 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

NOTES:

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 16-1: TYPICAL IDD vs. FOSC OVER VDD (EC MODE)

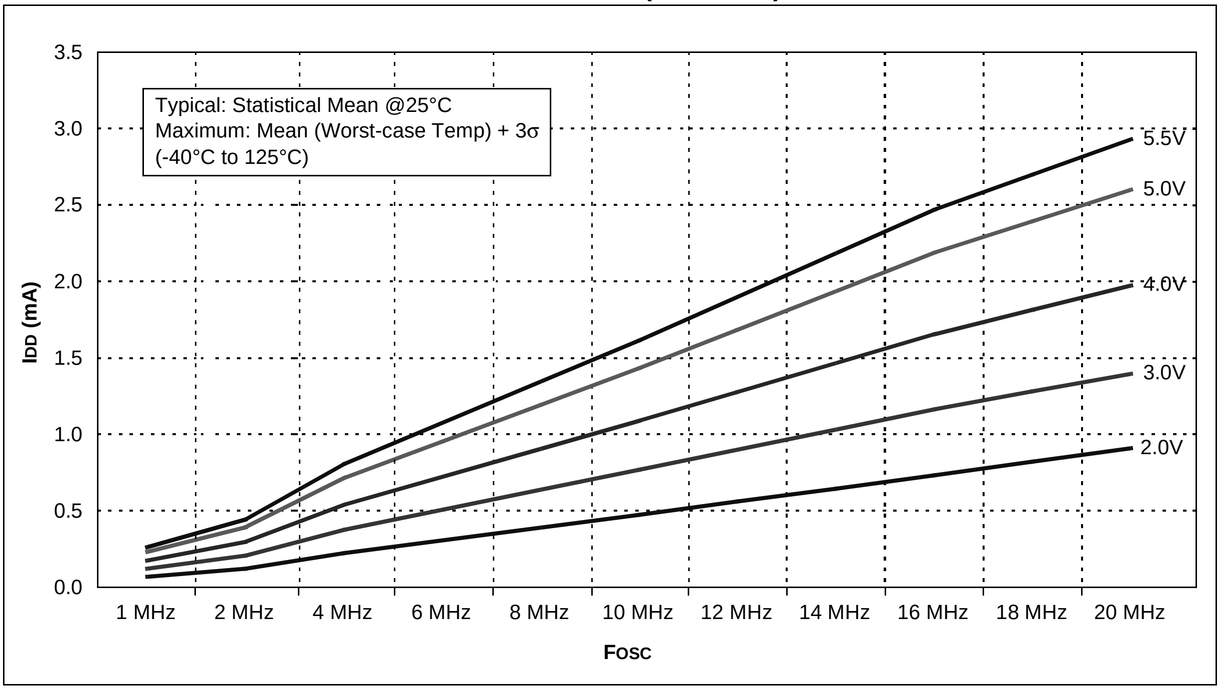


FIGURE 16-2: MAXIMUM IDD vs. FOSC OVER VDD (EC MODE)

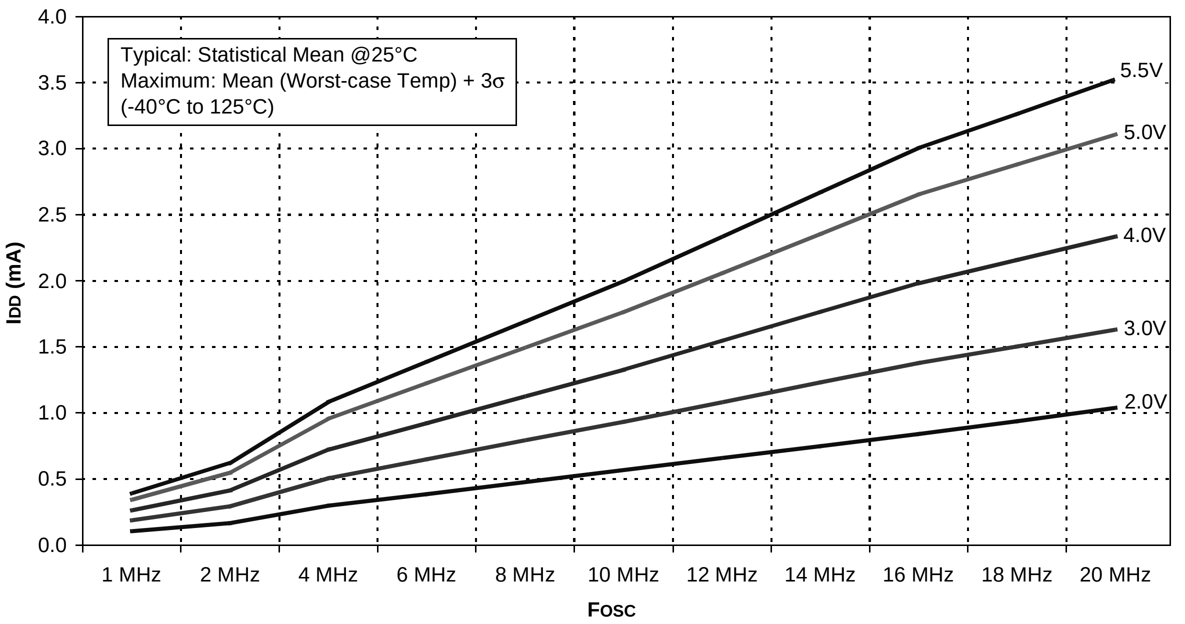


FIGURE 16-3: TYPICAL IDD vs. FOSC OVER VDD (HS MODE)

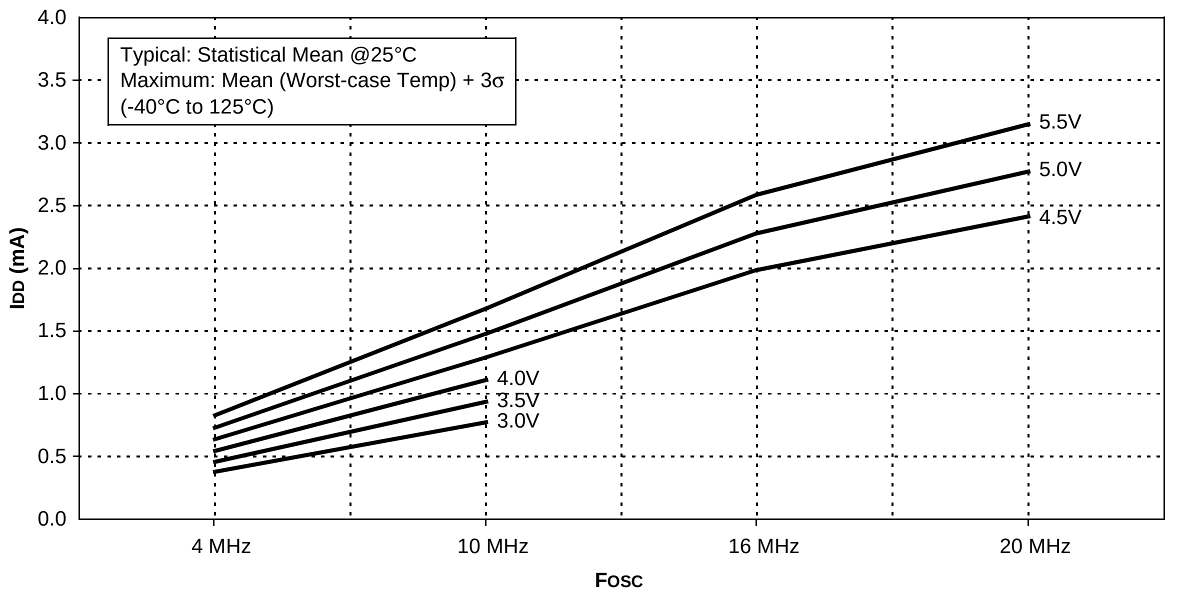


FIGURE 16-4: MAXIMUM IDD vs. FOSC OVER VDD (HS MODE)

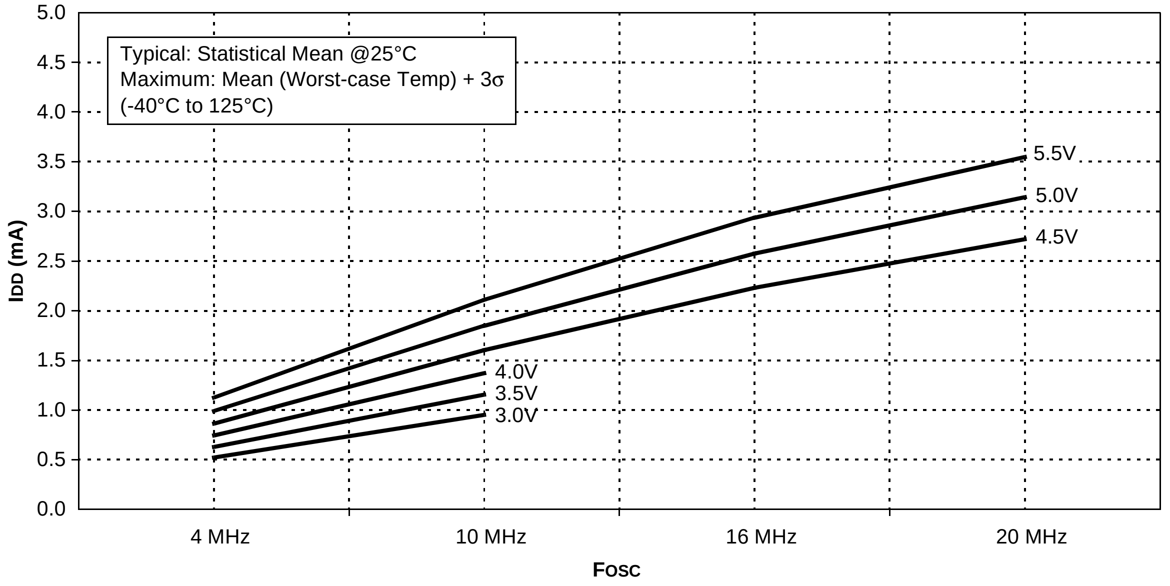


FIGURE 16-5: TYPICAL IDD vs. VDD OVER FOSC (XT MODE)

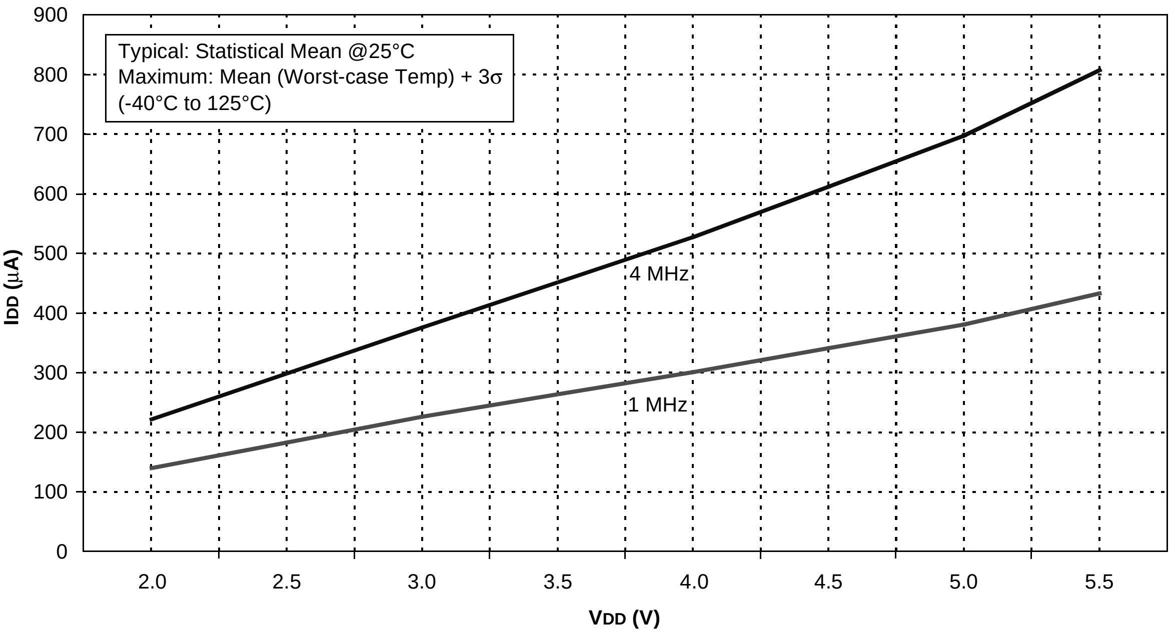


FIGURE 16-6: MAXIMUM IDD vs. VDD OVER FOSC (XT MODE)

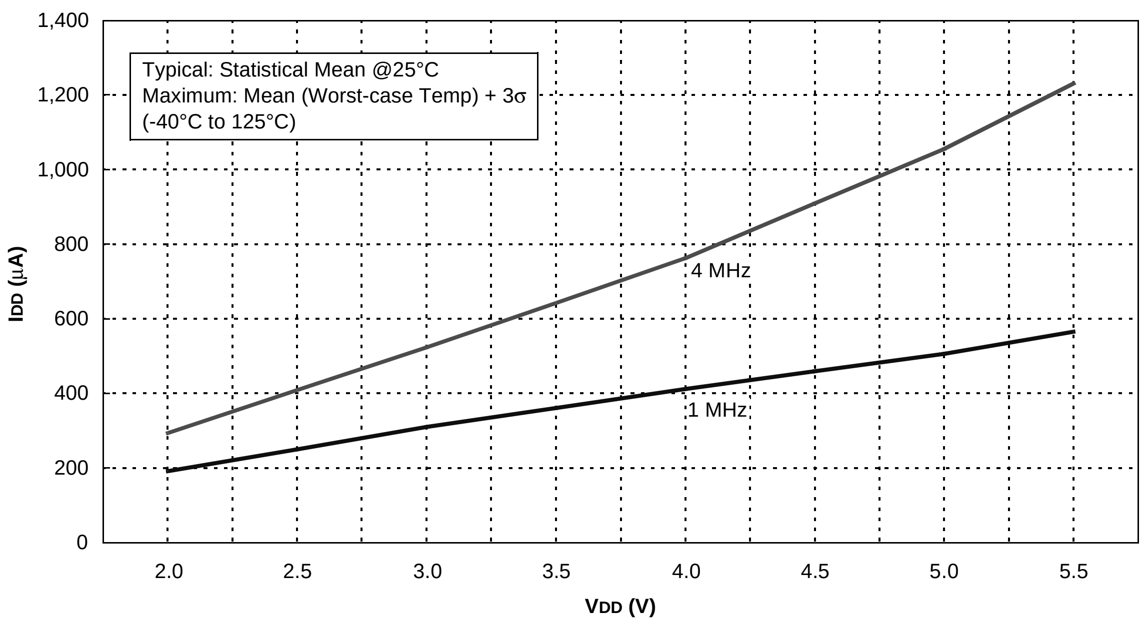


FIGURE 16-7: TYPICAL IDD vs. VDD OVER FOSC (EXTRC MODE)

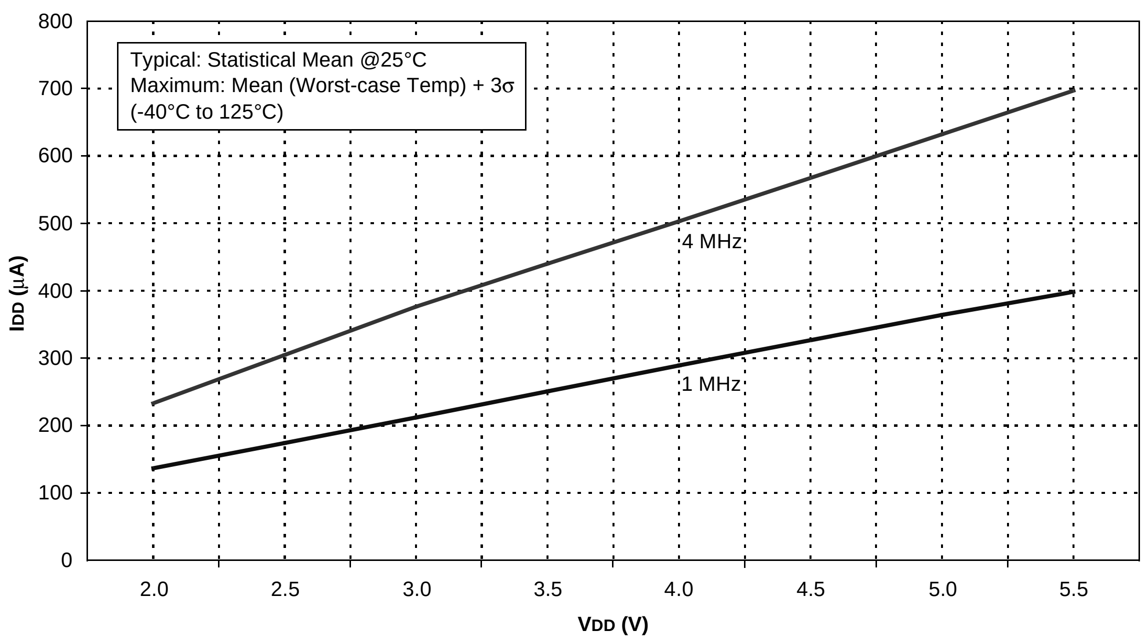


FIGURE 16-8: MAXIMUM IDD vs. VDD (EXTRC MODE)

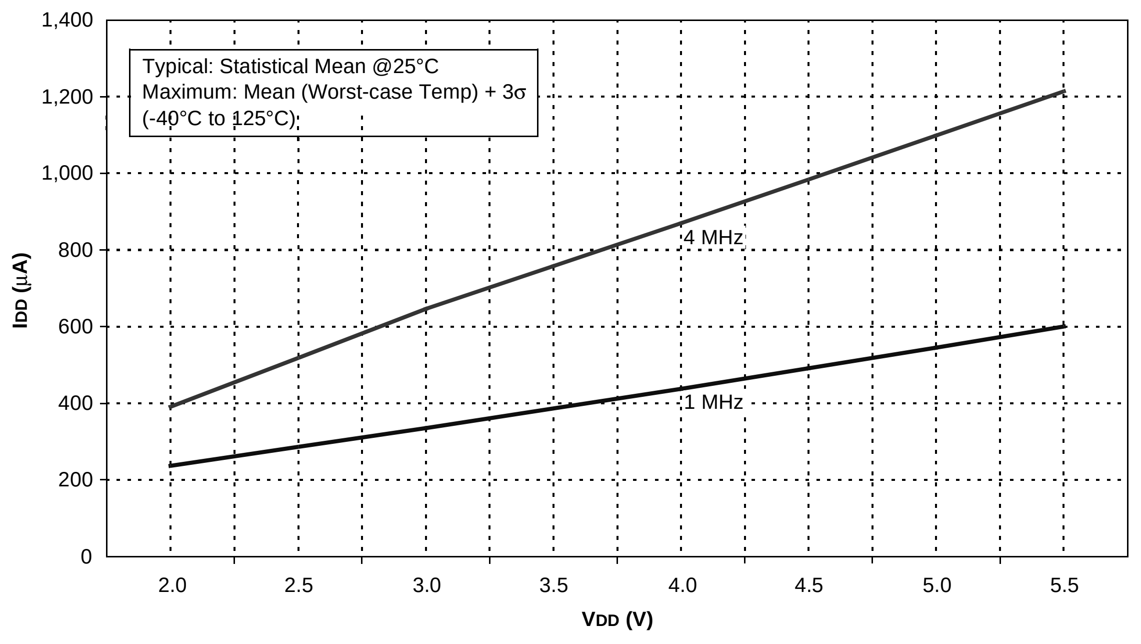


FIGURE 16-9: IDD vs. VDD OVER FOSC (LFINTOSC MODE, 31 kHz)

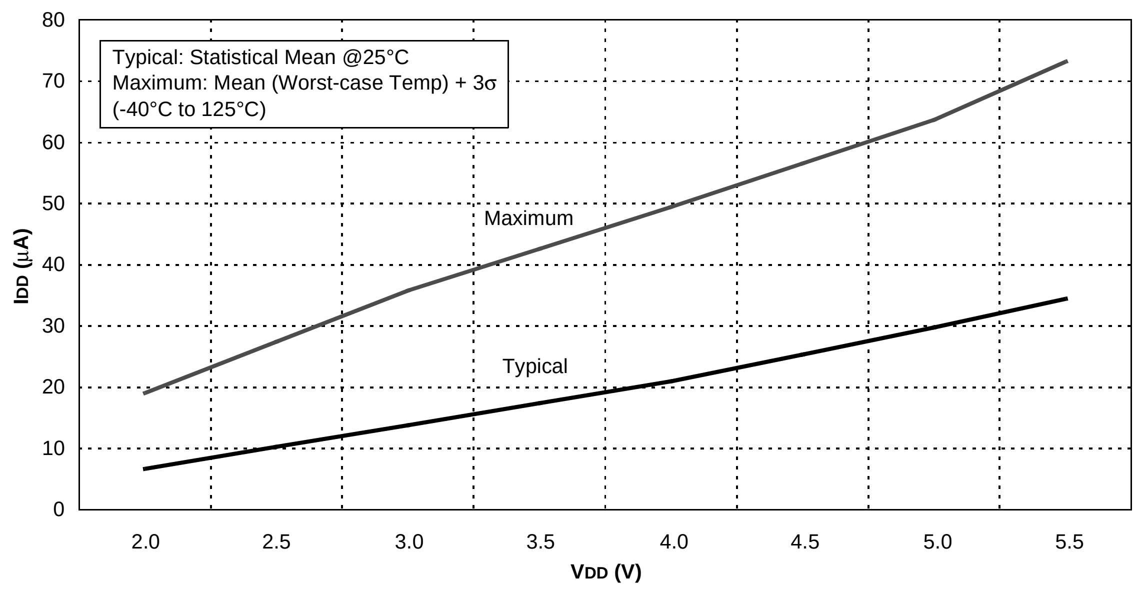


FIGURE 16-10: IDD VS. VDD (LP MODE)

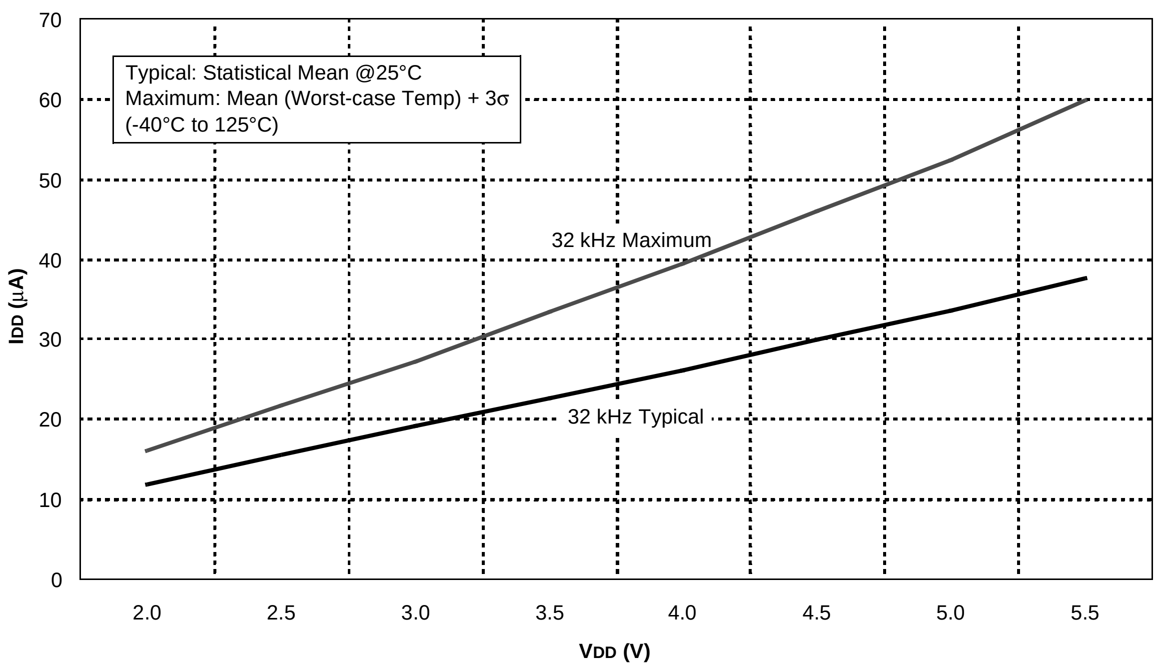


FIGURE 16-11: TYPICAL IDD VS. FOSC OVER VDD (HFINTOSC MODE)

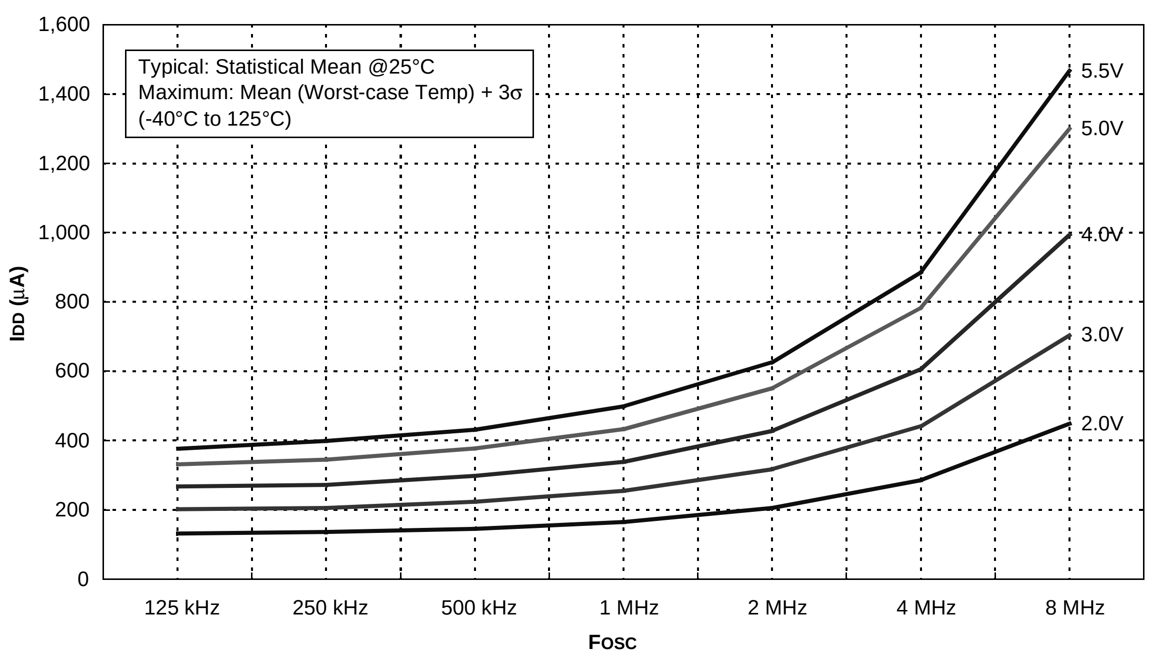


FIGURE 16-12: MAXIMUM IDD vs. FOSC OVER VDD (HFINTOSC MODE)

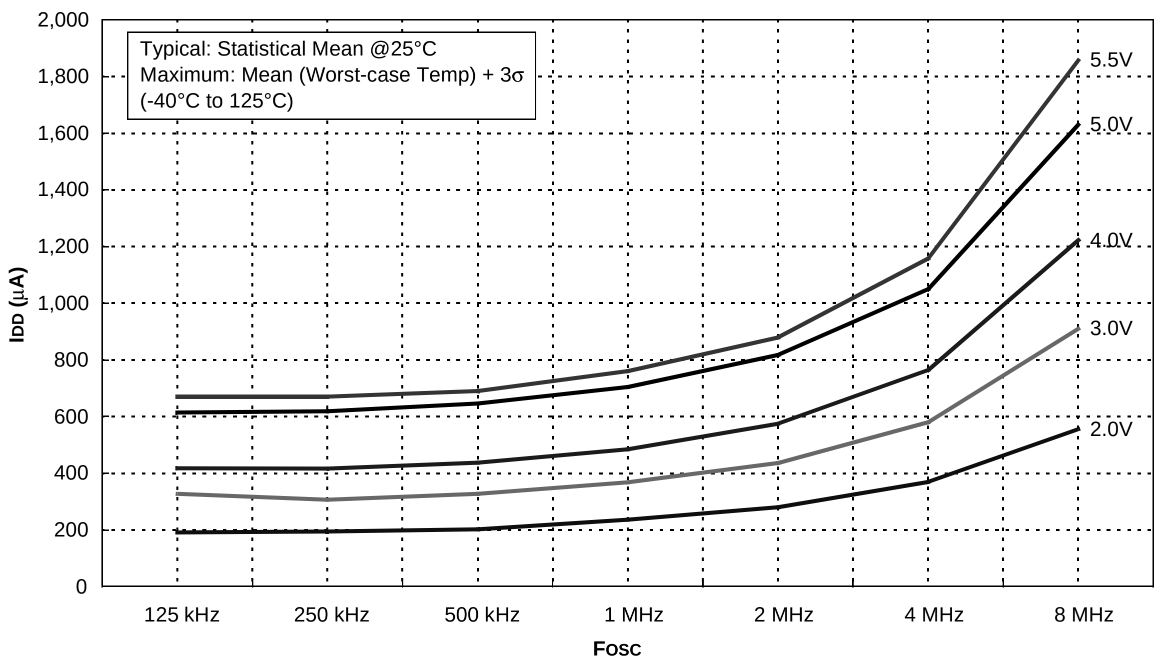


FIGURE 16-13: TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

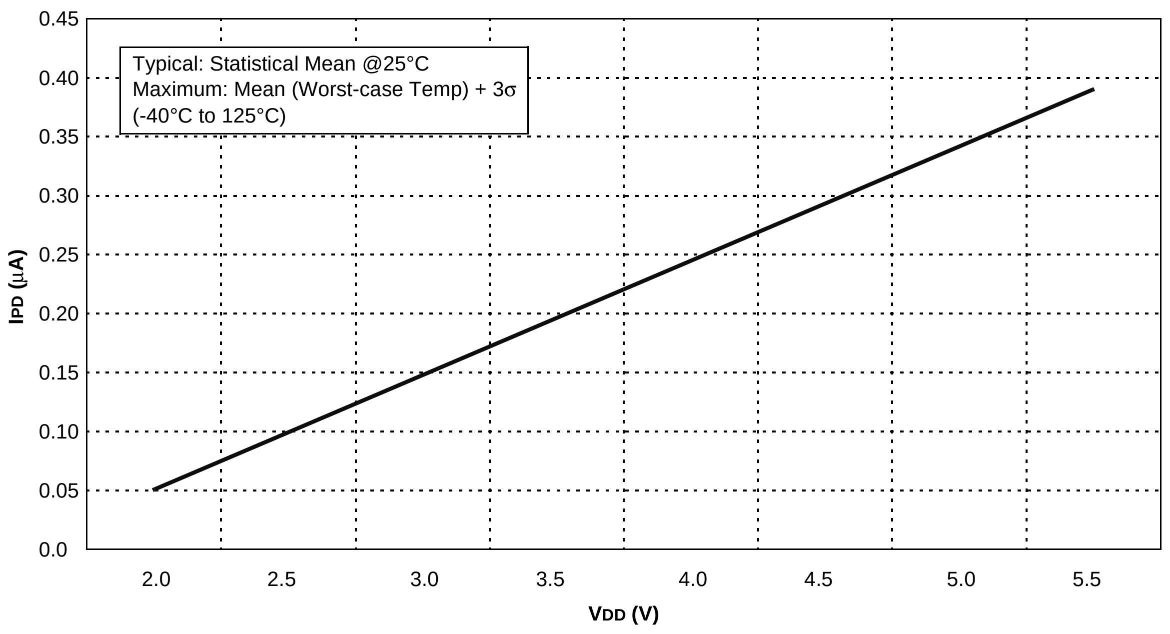


FIGURE 16-14: MAXIMUM IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

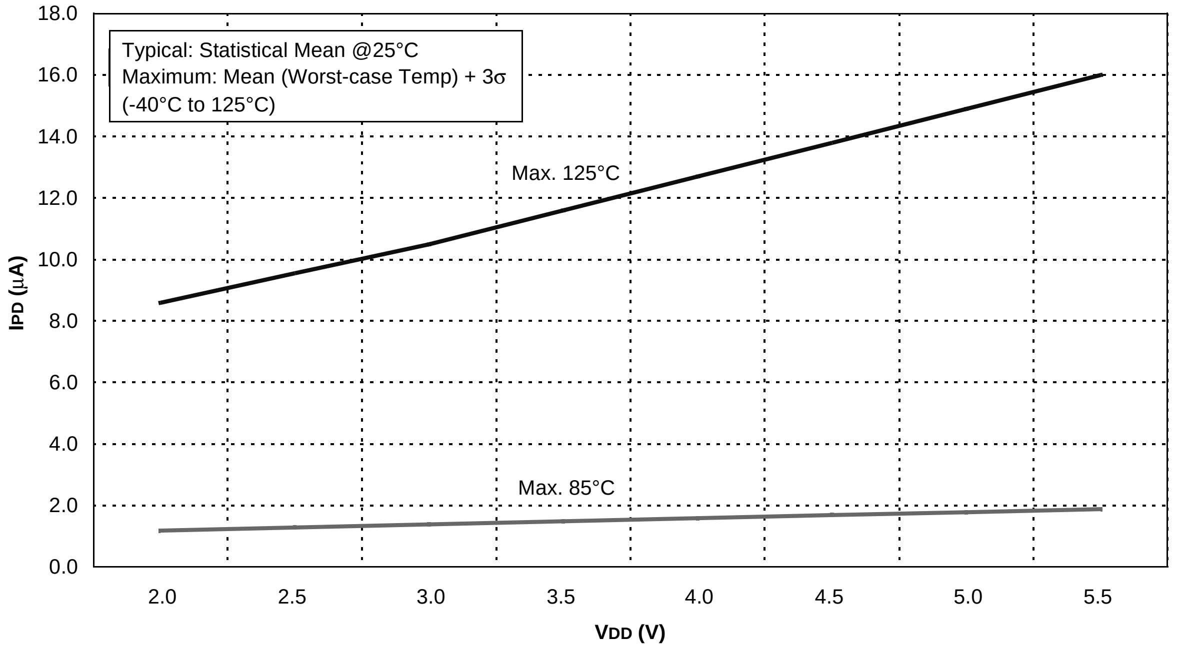


FIGURE 16-15: COMPARATOR IPD vs. VDD (BOTH COMPARATORS ENABLED)

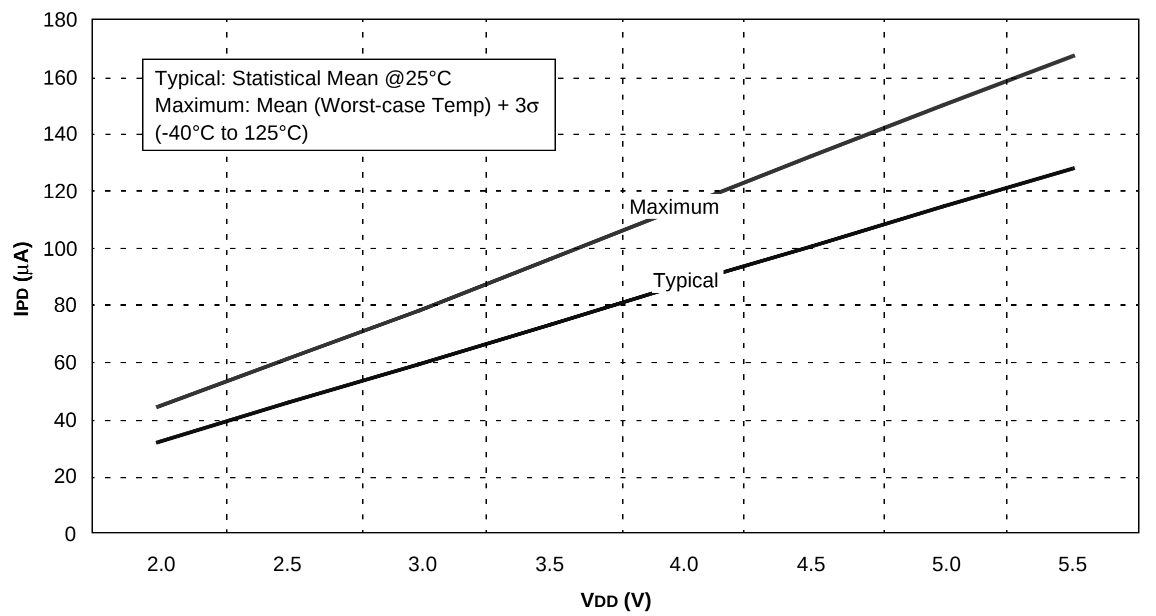


FIGURE 16-16: BOR IPD vs. VDD OVER TEMPERATURE

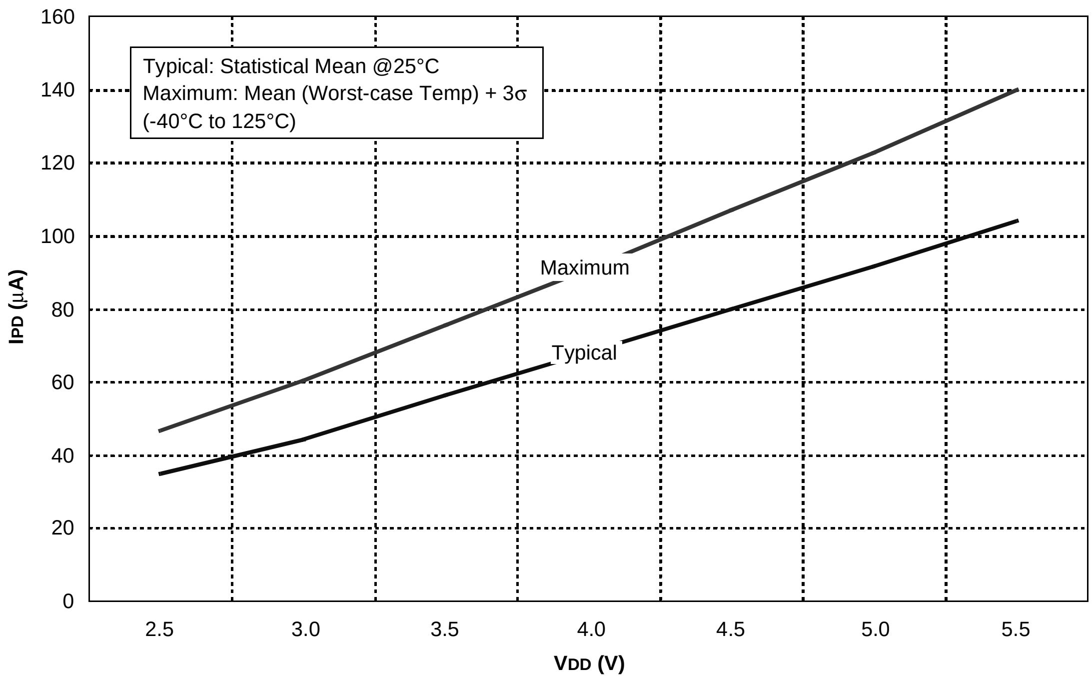


FIGURE 16-17: TYPICAL WDT IPD vs. VDD OVER TEMPERATURE

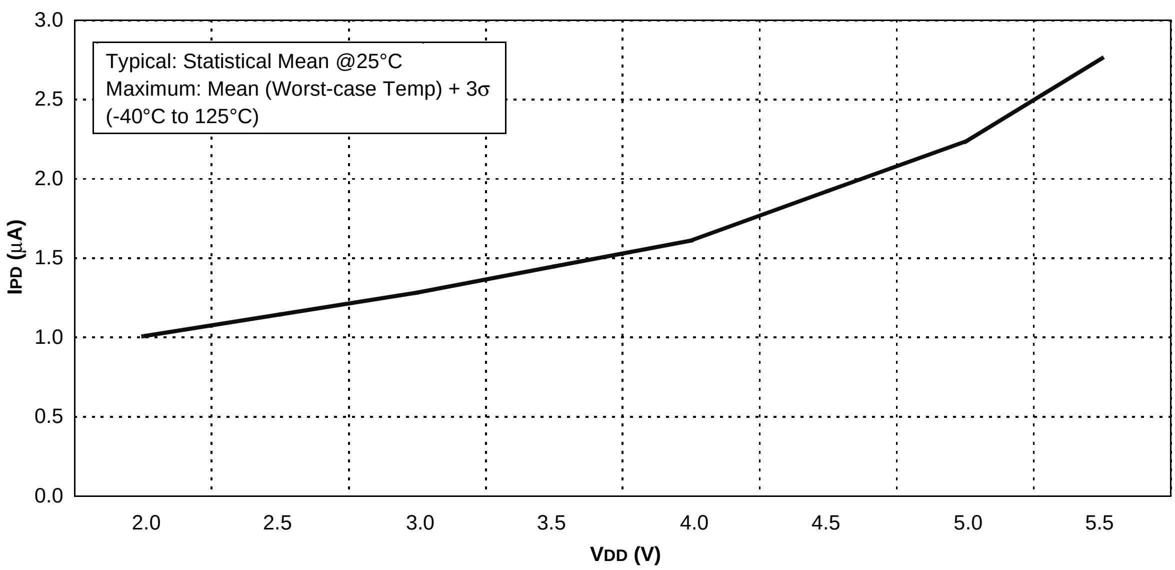


FIGURE 16-18: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE

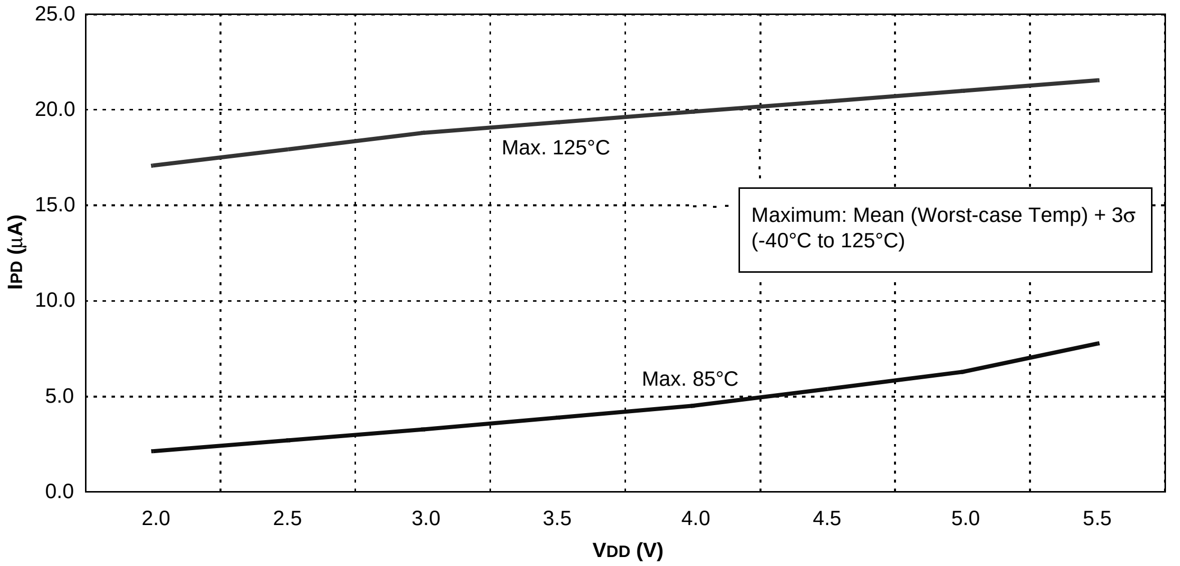


FIGURE 16-19: WDT PERIOD vs. VDD OVER TEMPERATURE

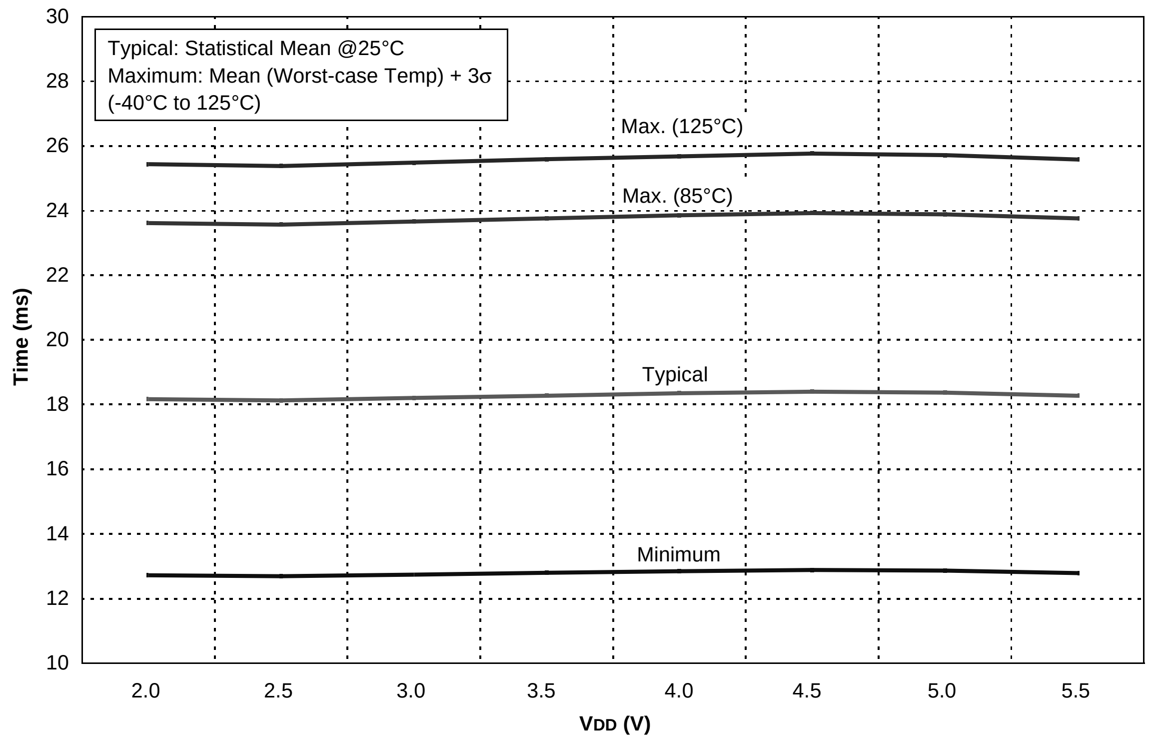


FIGURE 16-20: WDT PERIOD vs. TEMPERATURE OVER VDD (5.0V)

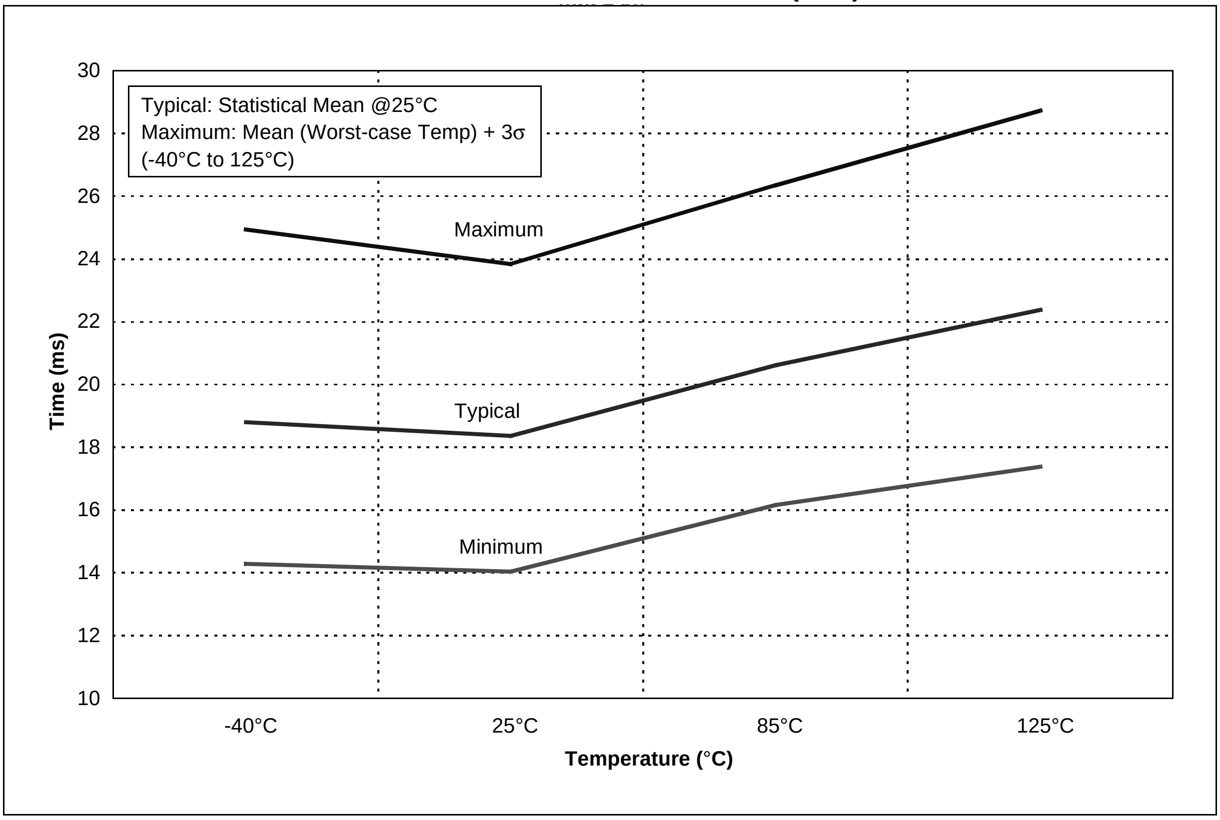


FIGURE 16-21: CVREF IPD vs. VDD OVER TEMPERATURE (HIGH RANGE)

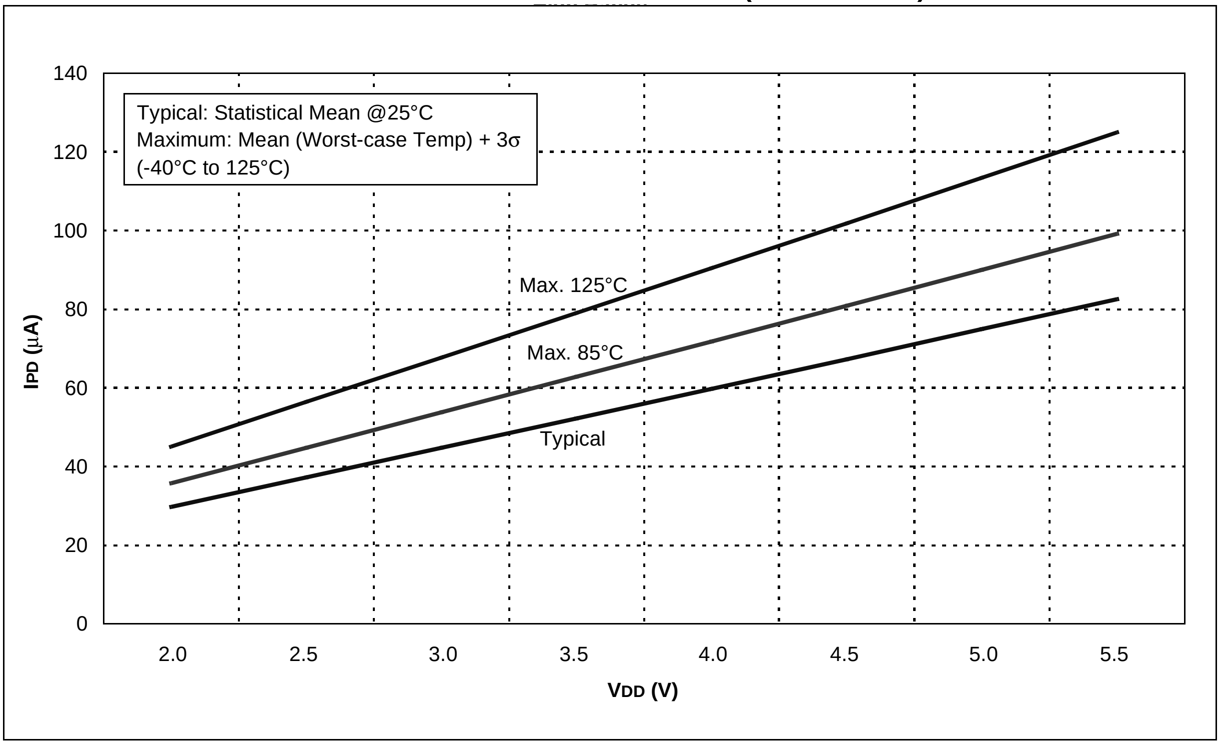


FIGURE 16-22: CVREF IPD vs. VDD OVER TEMPERATURE (LOW RANGE)

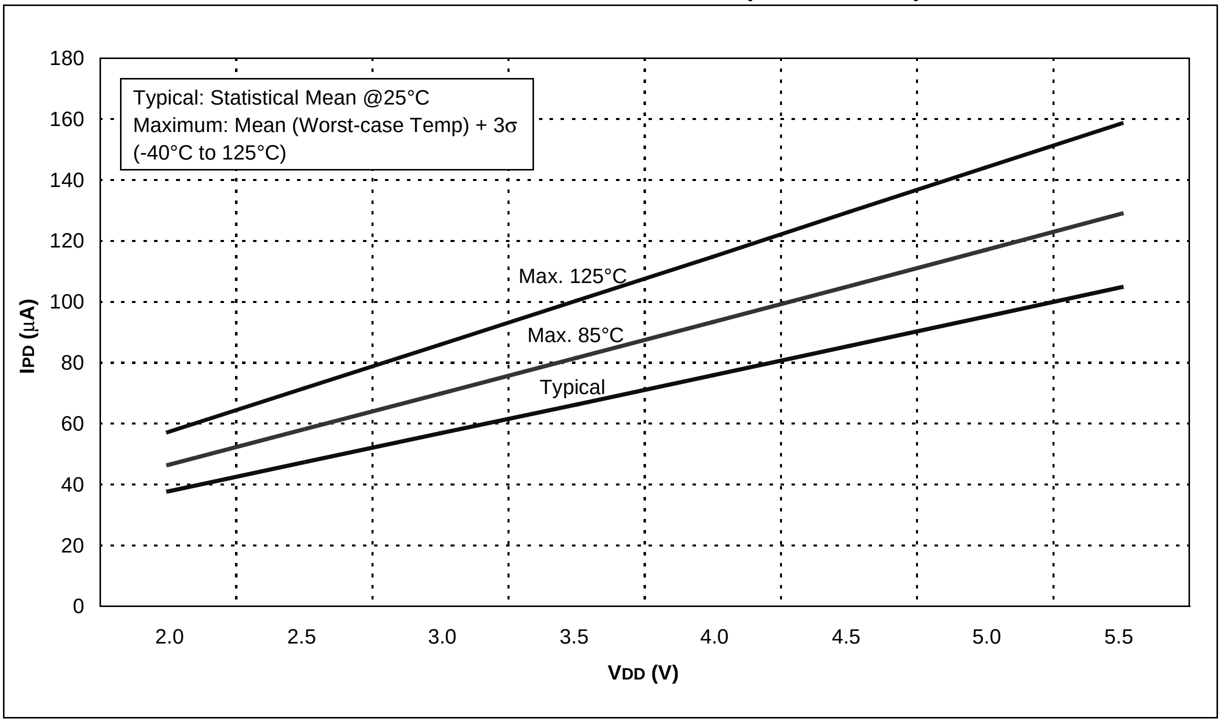


FIGURE 16-23: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

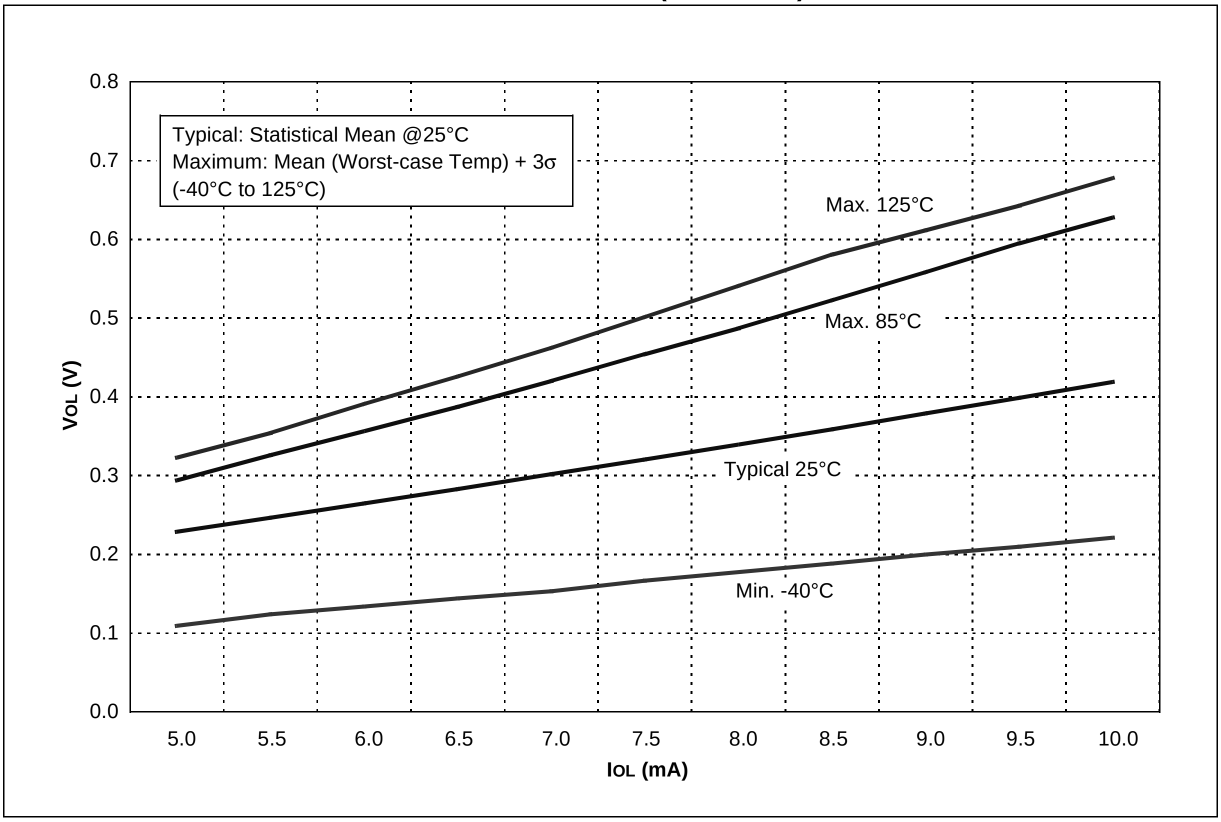


FIGURE 16-24: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

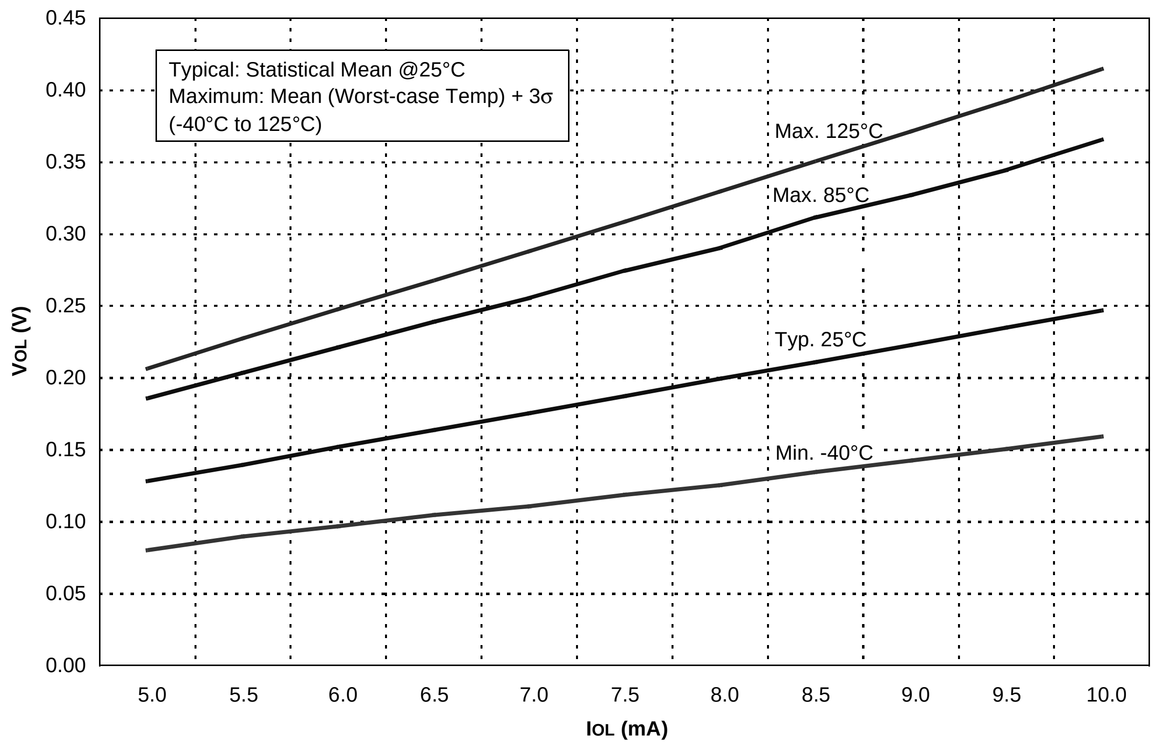


FIGURE 16-25: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

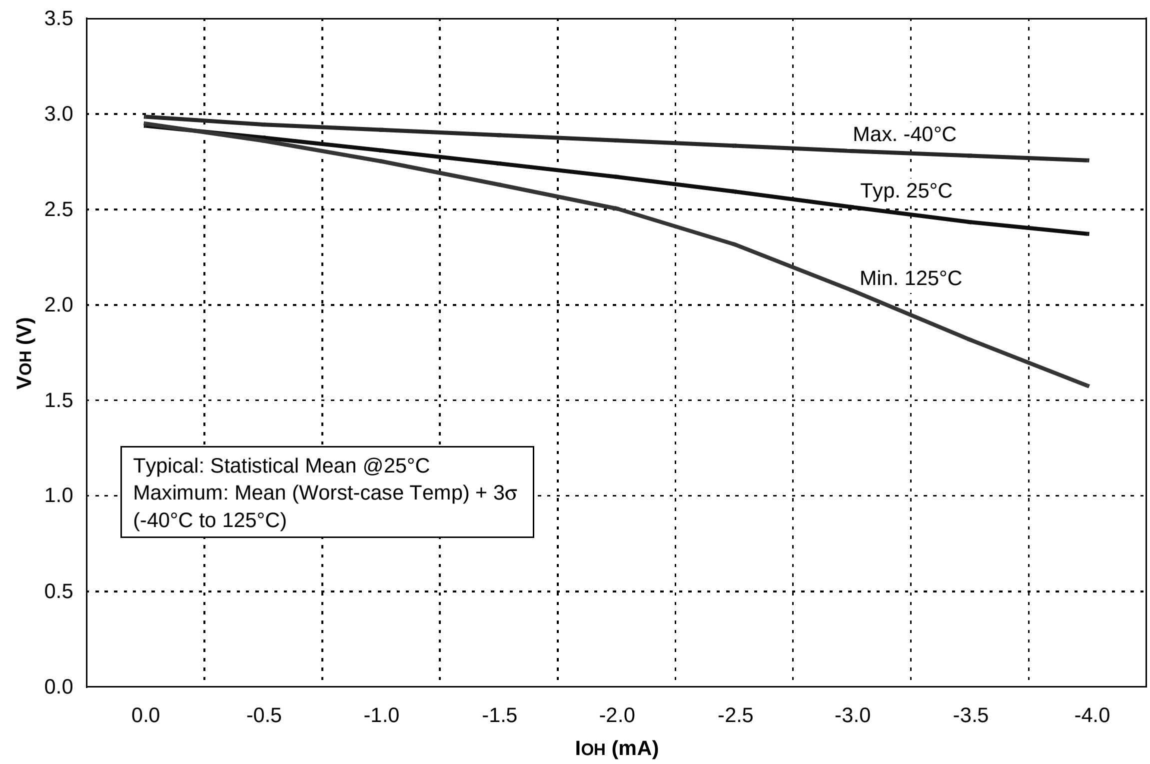


FIGURE 16-26: V_{OH} vs. I_{OH} OVER TEMPERATURE (V_{DD} = 5.0V)

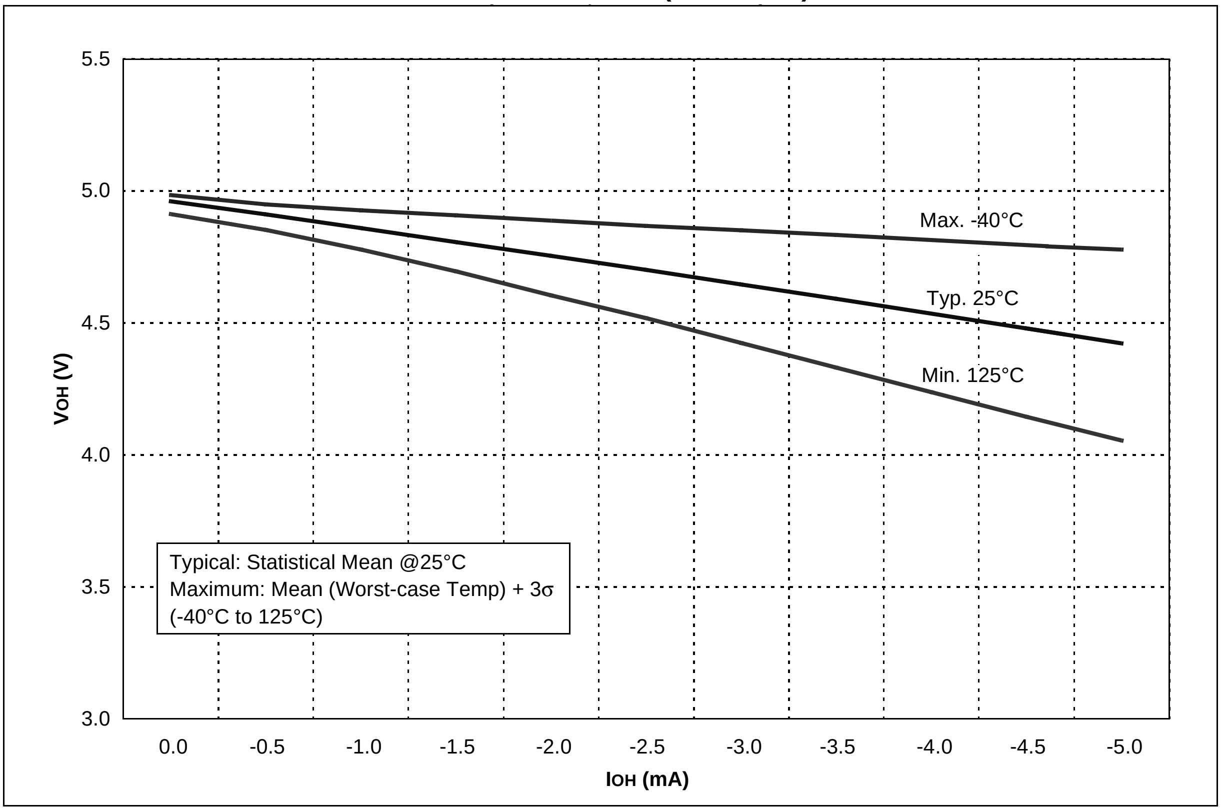


FIGURE 16-27: TTL INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

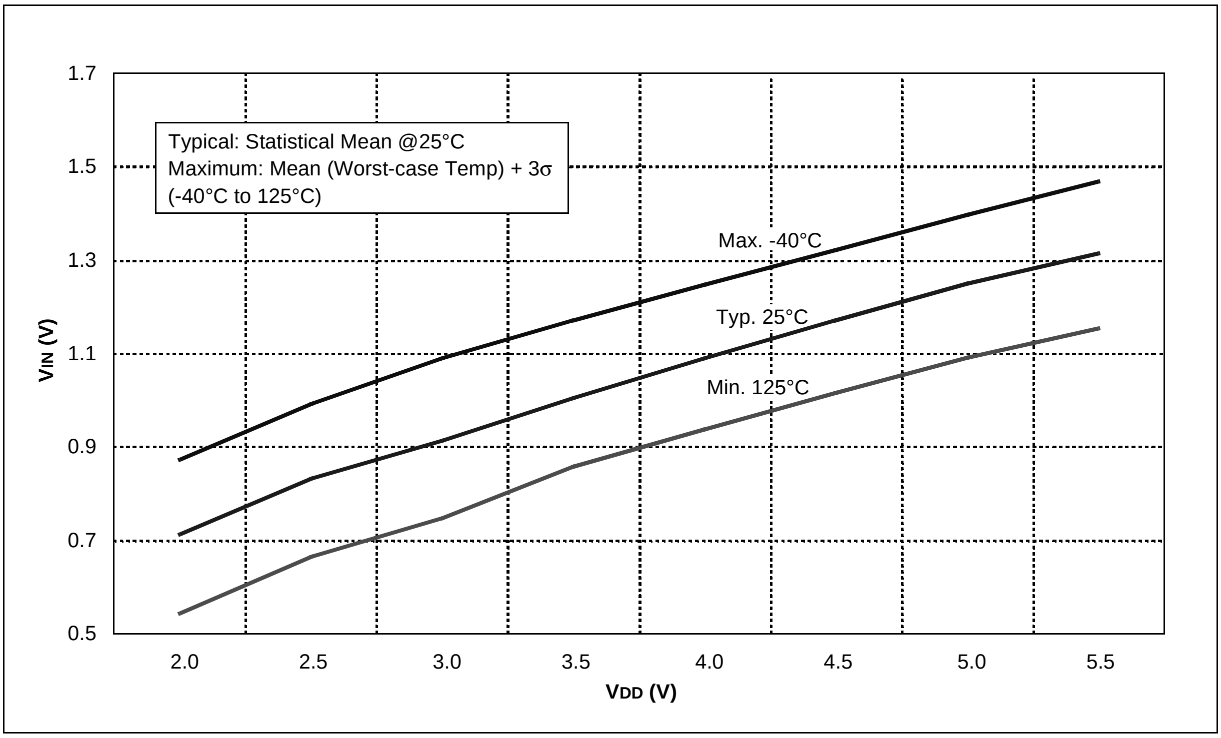


FIGURE 16-28: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD OVER TEMPERATURE

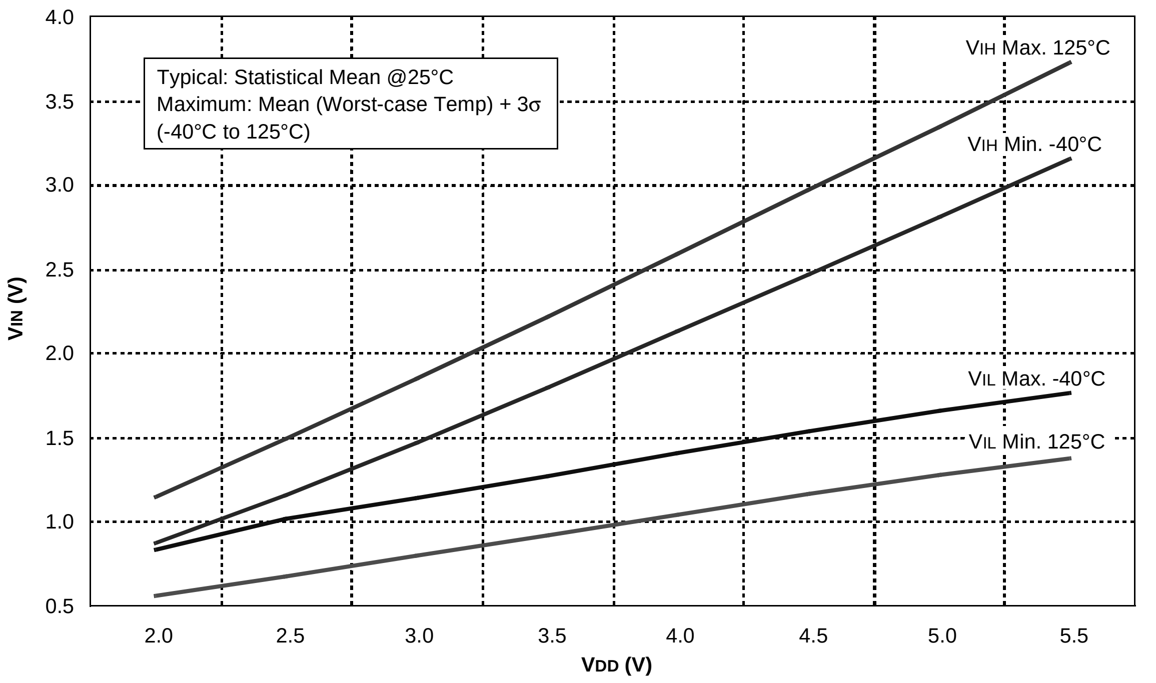


FIGURE 16-29: T1OSC IPD vs. VDD OVER TEMPERATURE (32 kHz)

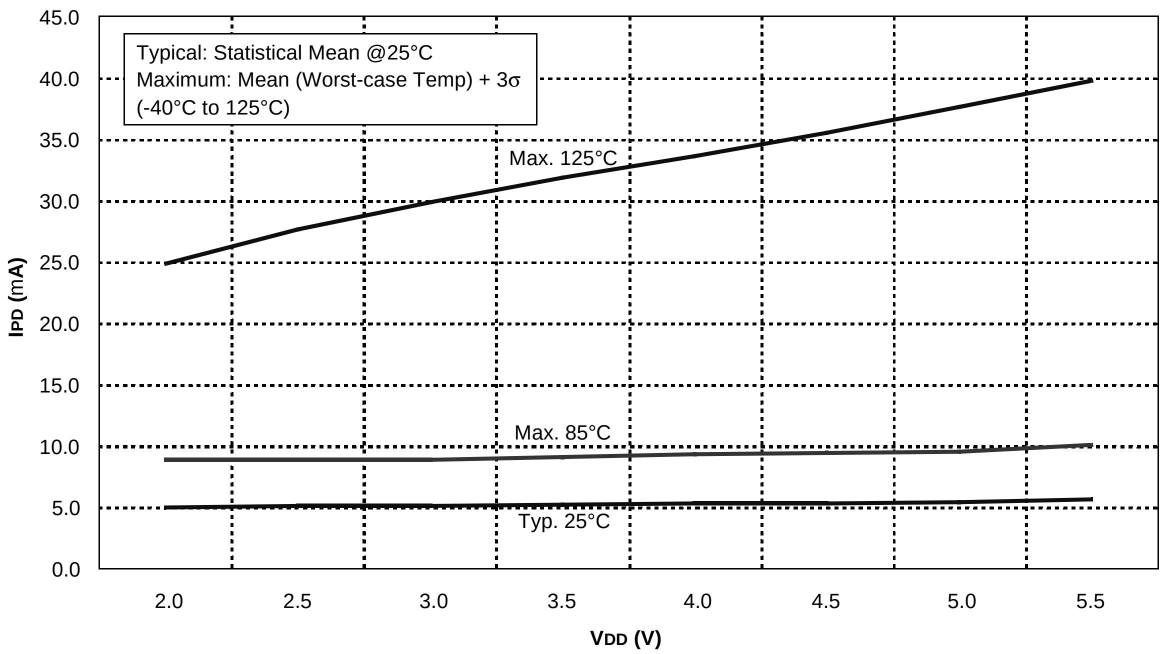


FIGURE 16-30: COMPARATOR RESPONSE TIME (RISING EDGE)

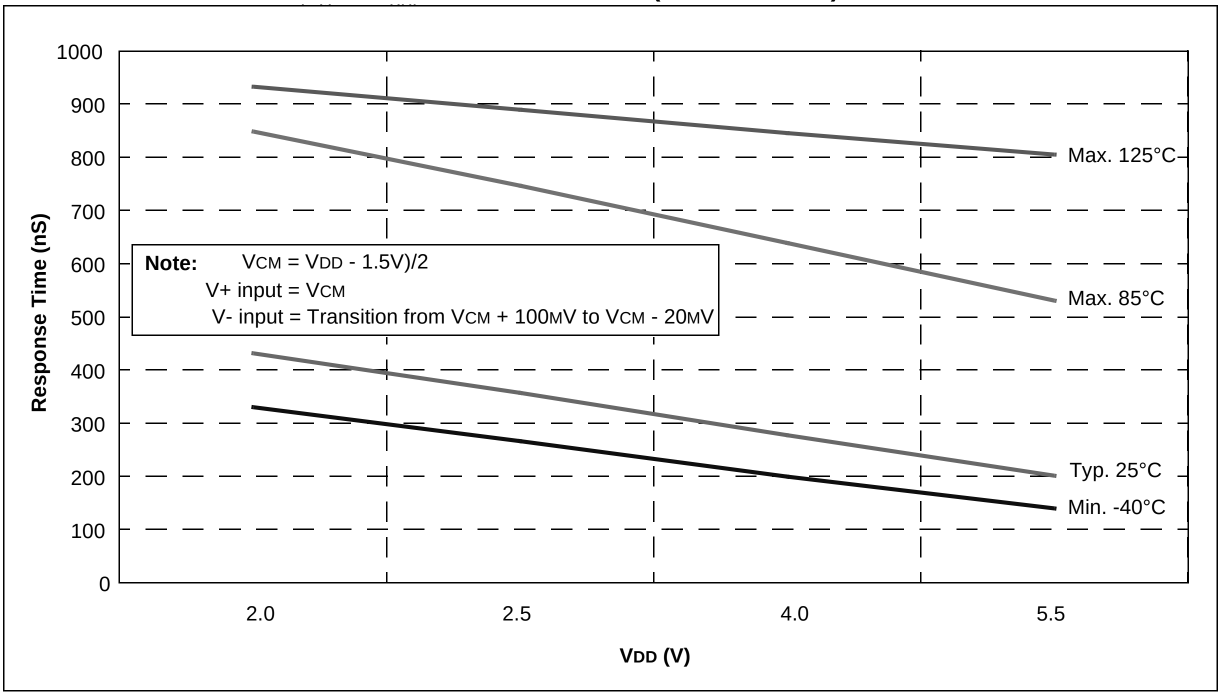


FIGURE 16-31: COMPARATOR RESPONSE TIME (FALLING EDGE)

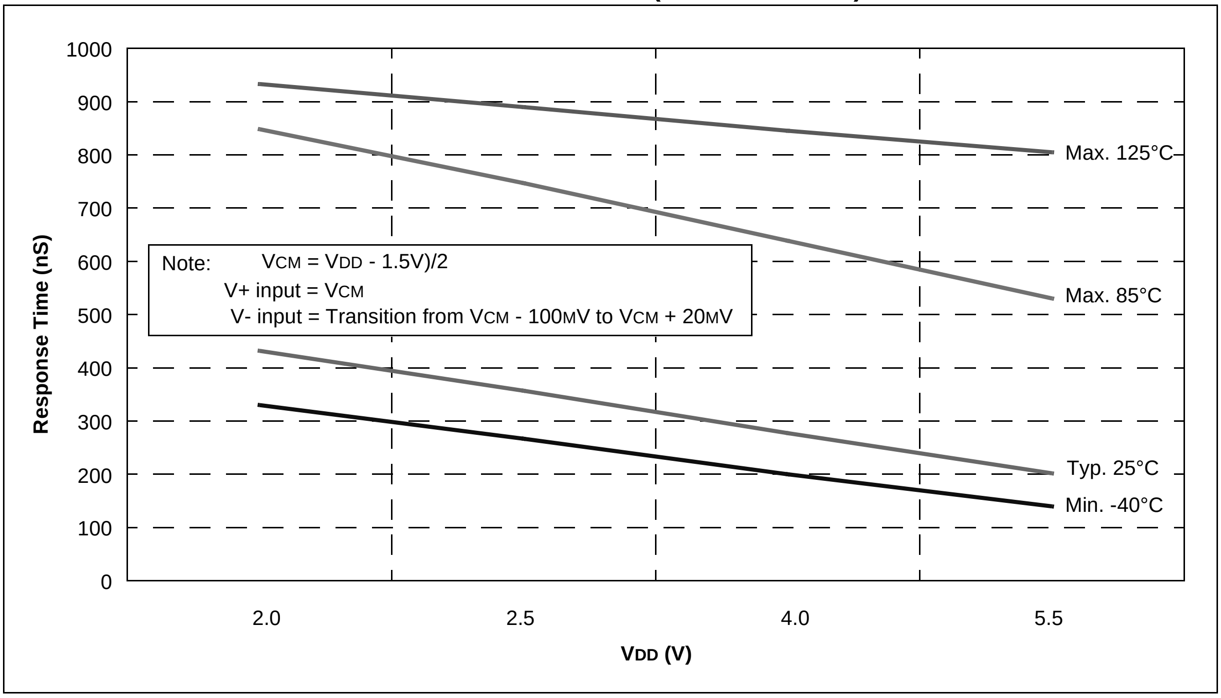


FIGURE 16-32: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)

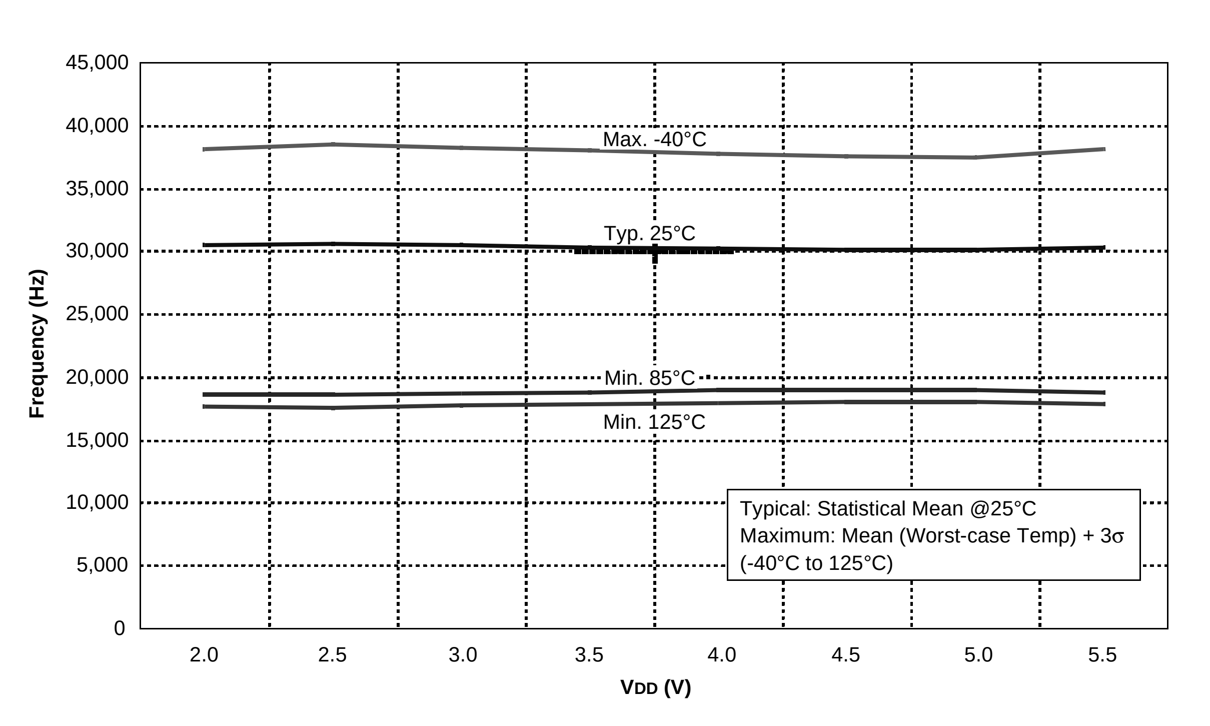


FIGURE 16-33: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE

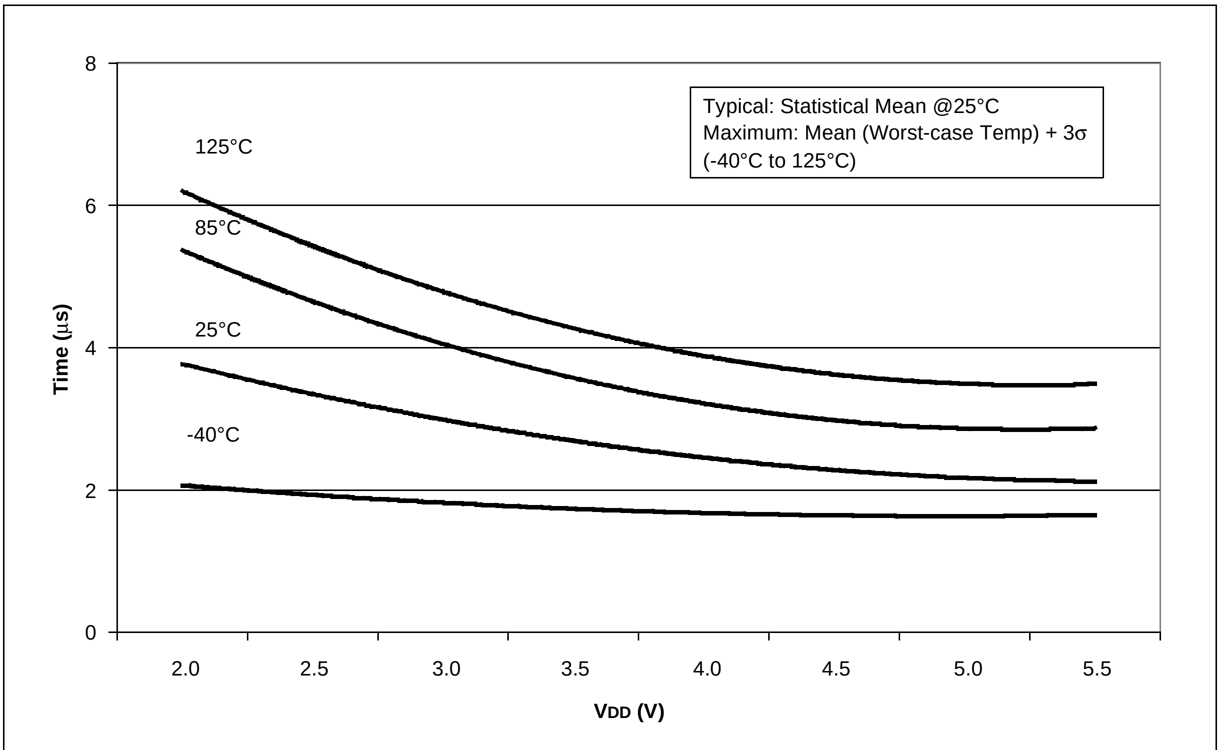


FIGURE 16-34: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

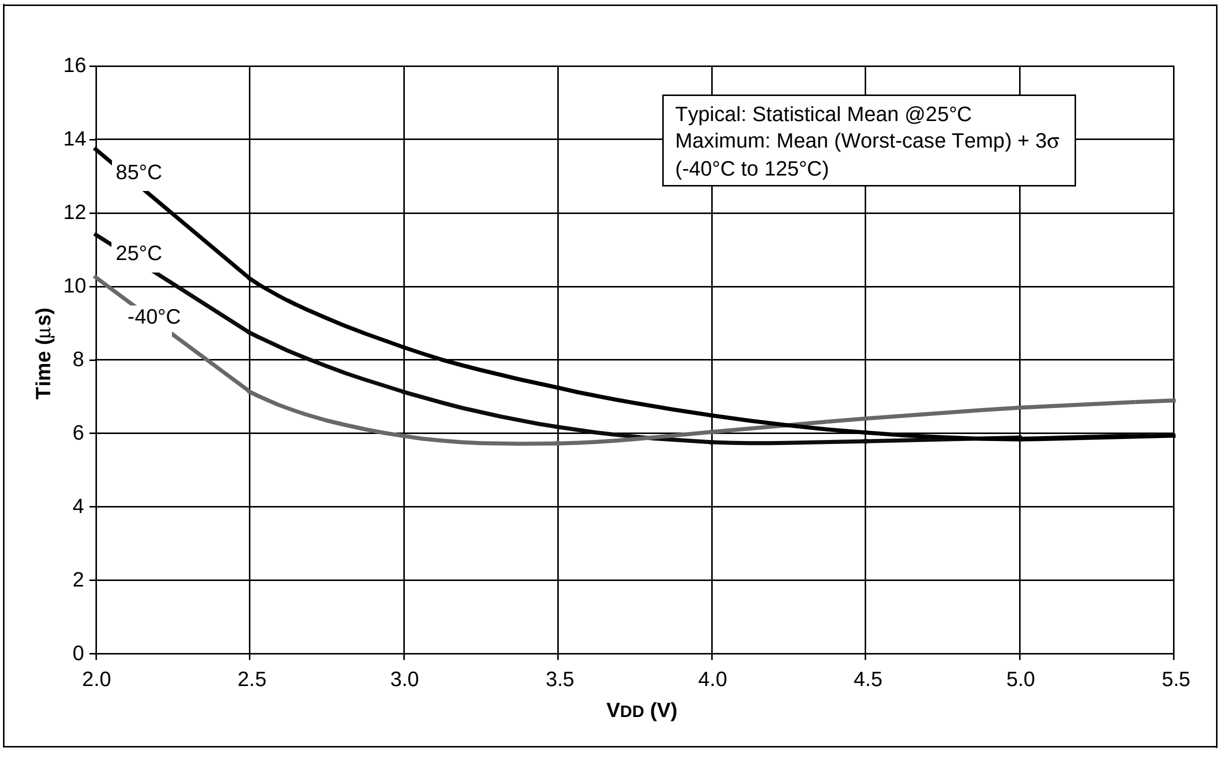


FIGURE 16-35: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

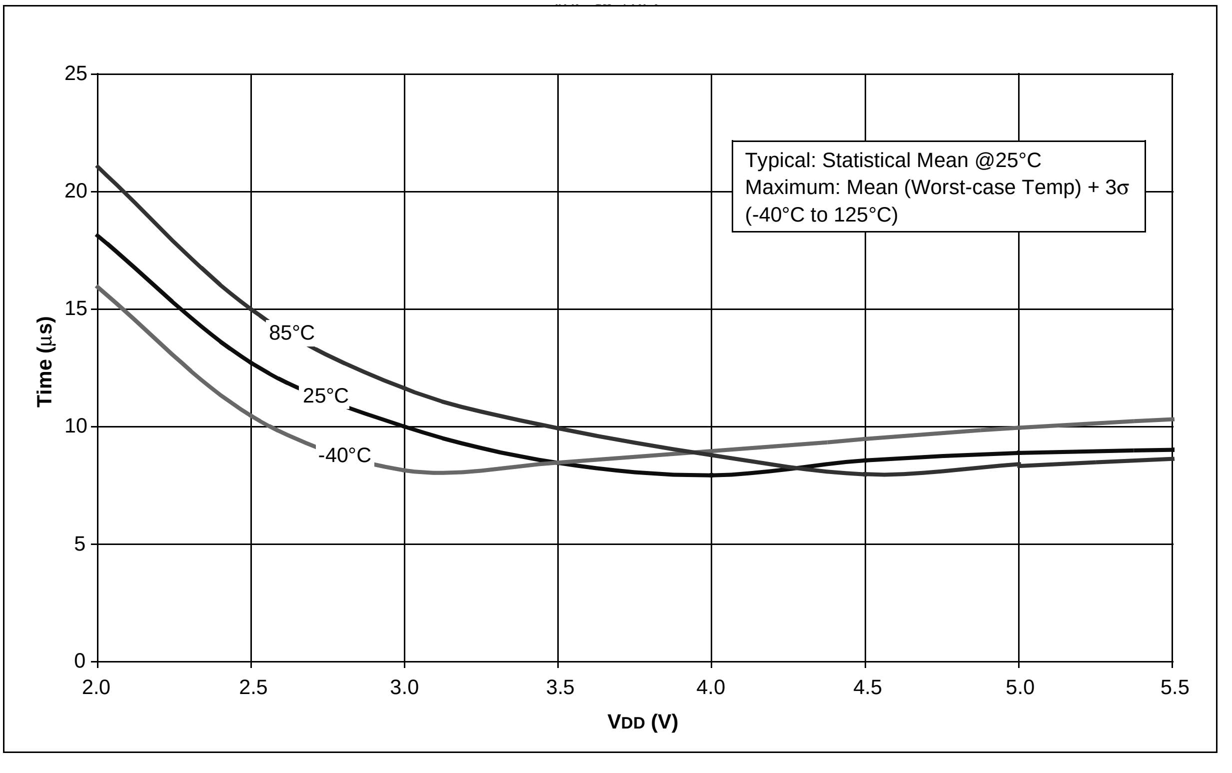


FIGURE 16-36: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

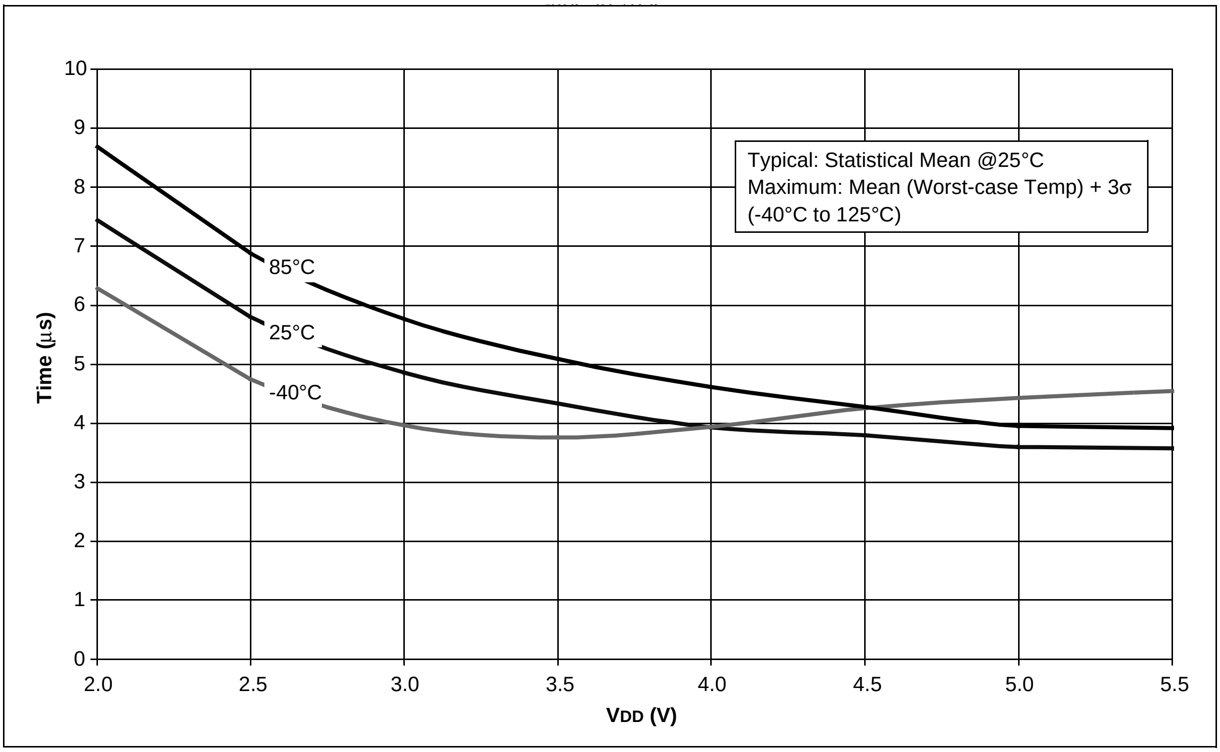


FIGURE 16-37: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)

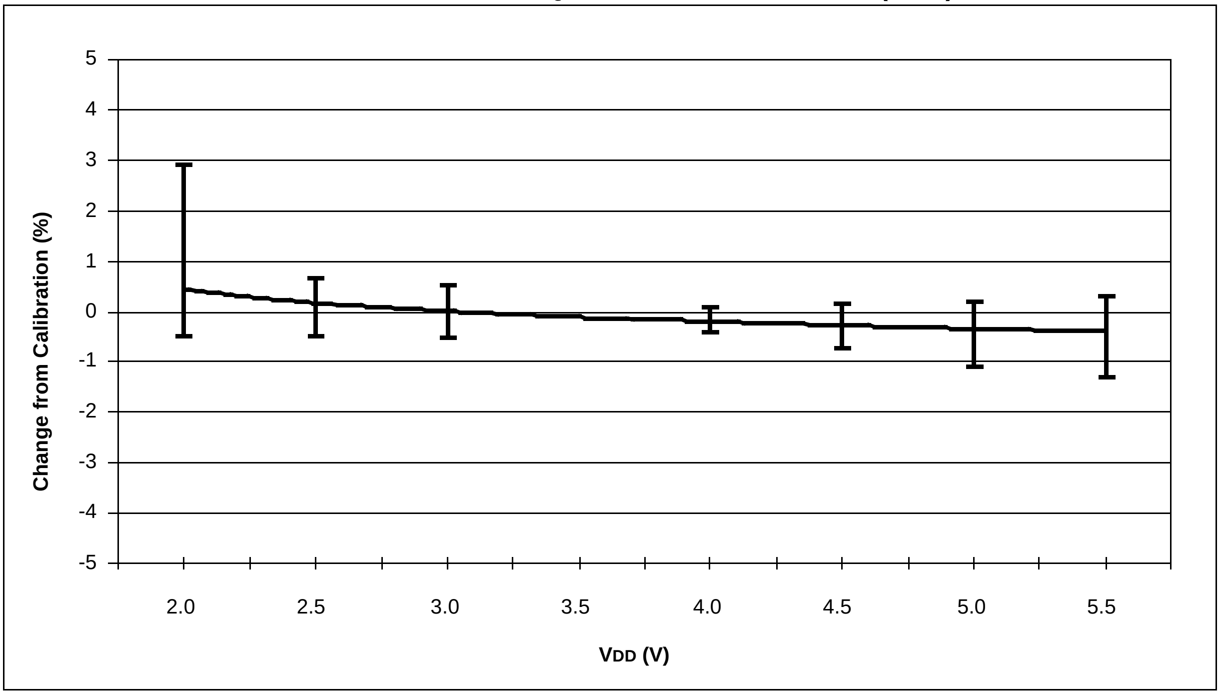


FIGURE 16-38: TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE VDD (85°C)

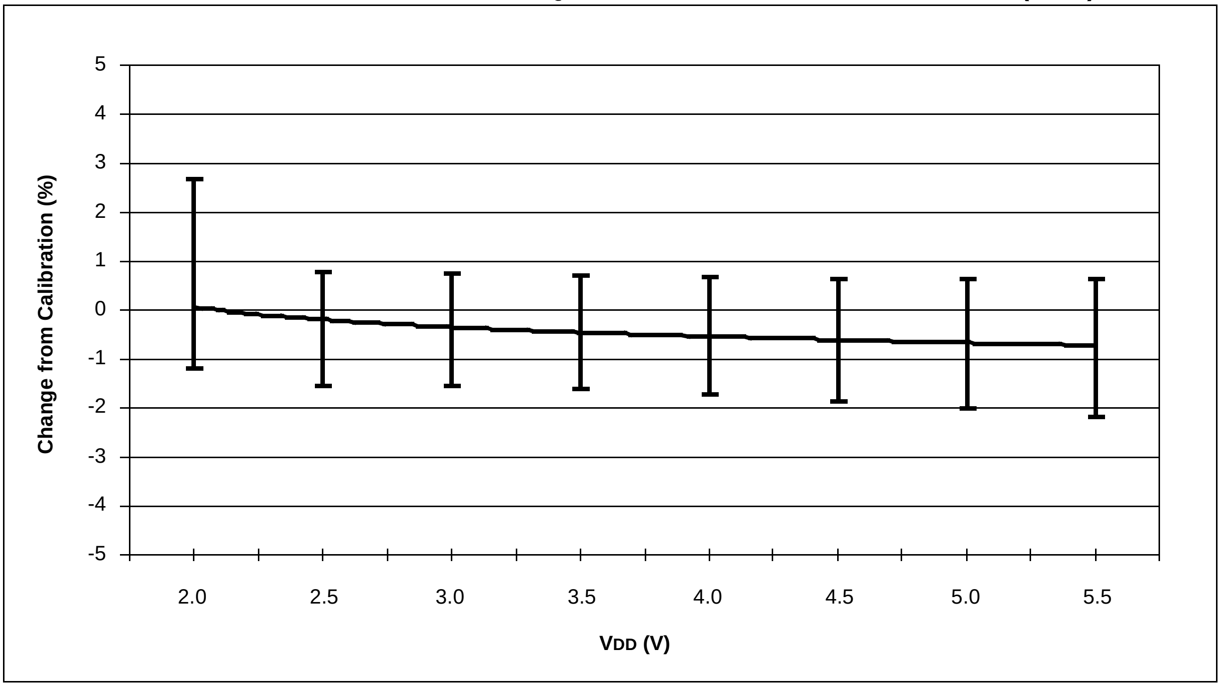


FIGURE 16-39: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (125°C)

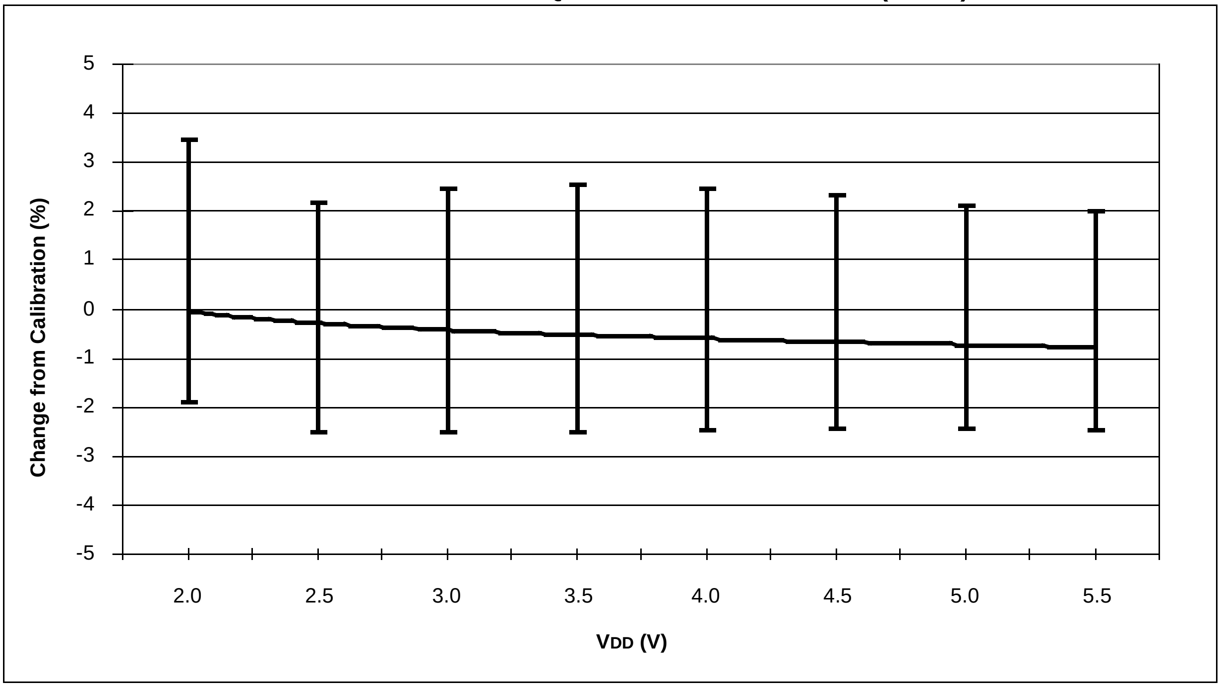
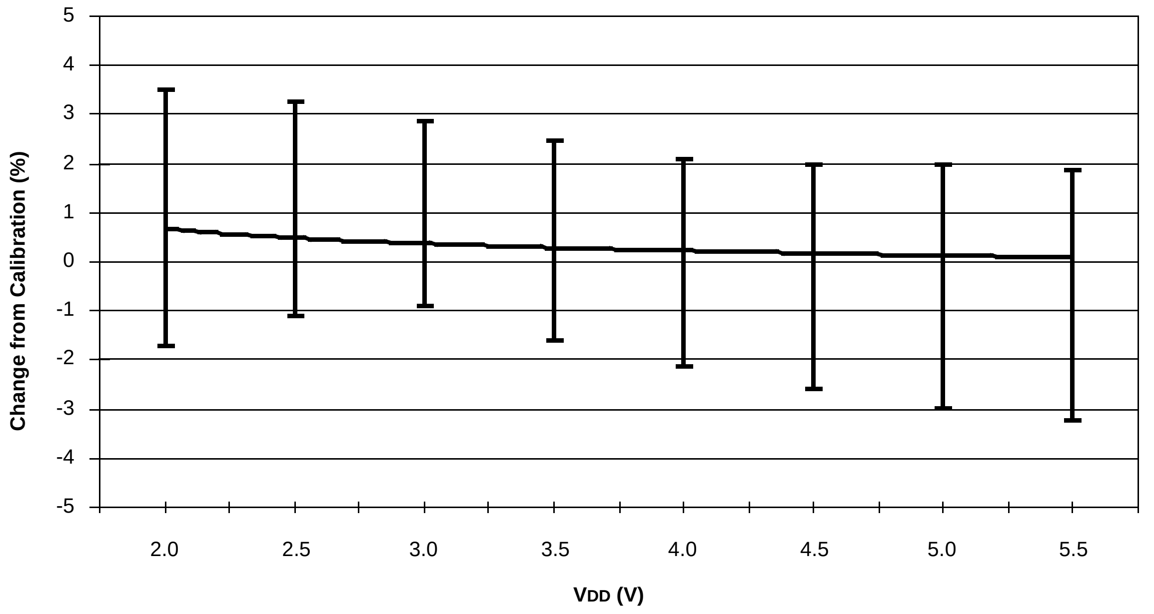


FIGURE 16-40: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)

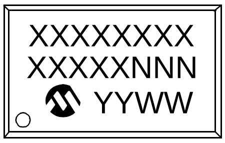


NOTES:

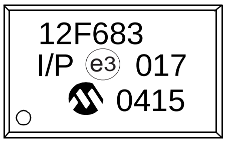
17.0 PACKAGING INFORMATION

17.1 Package Marking Information

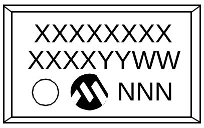
8-Lead PDIP



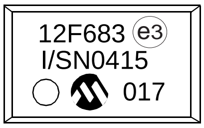
Example



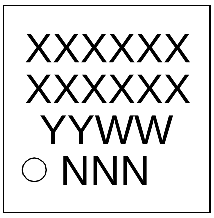
8-Lead SOIC (3.90 mm)



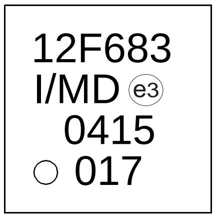
Example



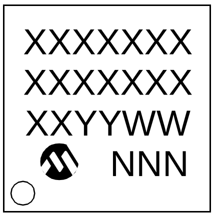
8-Lead DFN (4x4x0.9 mm)



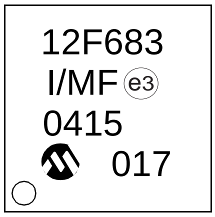
Example



8-Lead DFN-S (6x5 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

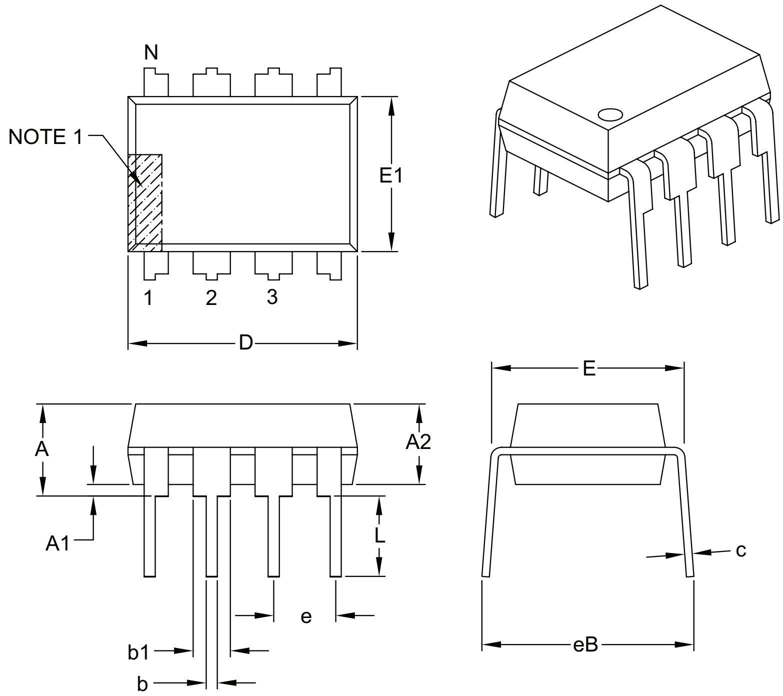
* Standard PIC® device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

17.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

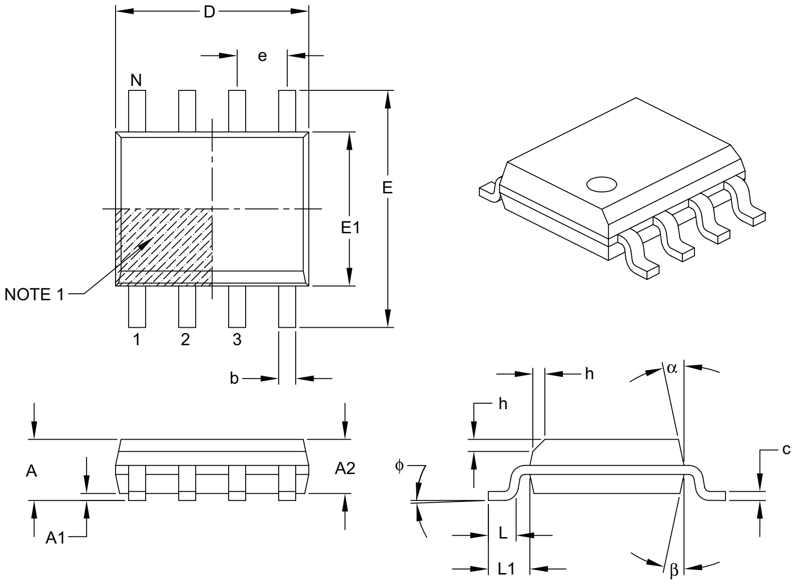
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

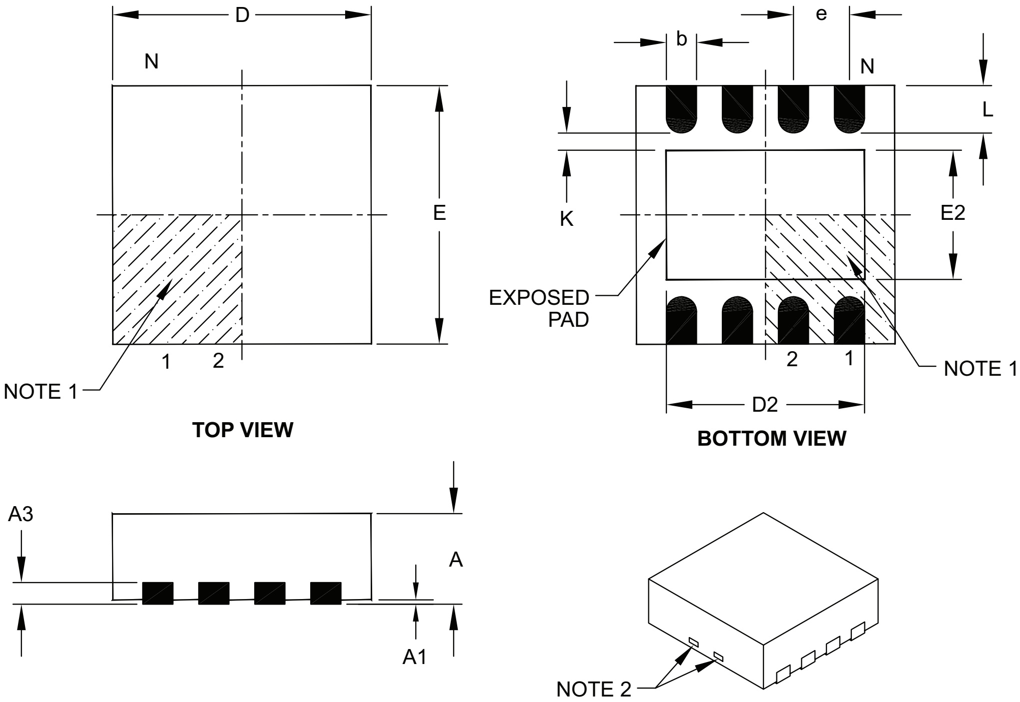
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



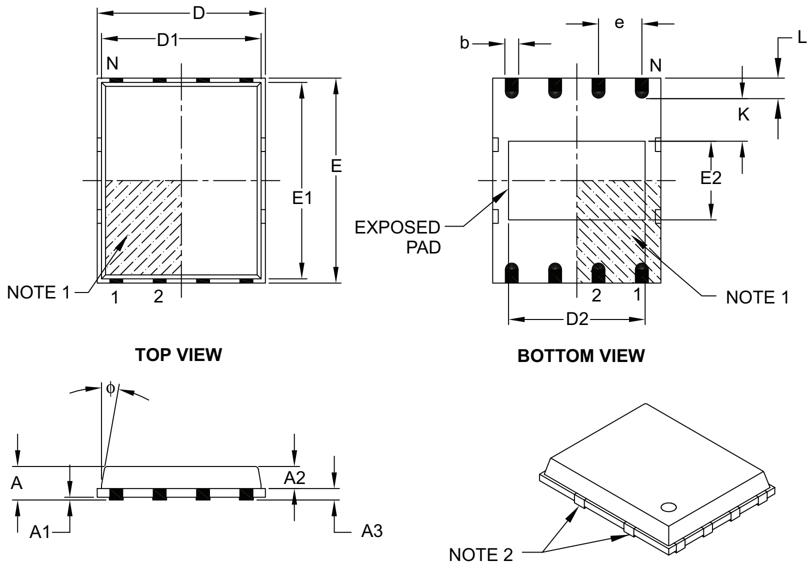
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	0.85	1.00
Molded Package Thickness	A2	–	0.65	0.80
Standoff	A1	0.00	0.01	0.05
Base Thickness	A3		0.20 REF	
Overall Length	D		4.92 BSC	
Molded Package Length	D1		4.67 BSC	
Exposed Pad Length	D2	3.85	4.00	4.15
Overall Width	E		5.99 BSC	
Molded Package Width	E1		5.74 BSC	
Exposed Pad Width	E2	2.16	2.31	2.46
Contact Width	b	0.35	0.40	0.47
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–
Model Draft Angle Top	φ	–	–	12°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Rewrites of the Oscillator and Special Features of the CPU sections. General corrections to Figures and formatting.

Revision C

Revisions throughout document. Incorporated Golden Chapters.

Revision D

Replaced Package Drawings; Revised Product ID Section (SN package to 3.90 mm); Replaced PICmicro with PIC; Replaced Dev Tool Section.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC12F683 device.

B.1 PIC16F676 to PIC12F683

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC12F683
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	2048
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Data EEPROM (Bytes)	128	256
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	GP0/1/2/4/5, $\overline{\text{MCLR}}$
Interrupt-on-change	RA0/1/2/3/4/5	GP0/1/2/3/4/5
Comparator	1	1
ECCP	N	N
Ultra Low-Power Wake-Up	N	Y
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	4 MHz	32 kHz-8 MHz
Clock Switching	N	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

NOTES:

INDEX

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager Total Pages Sent ________

RE: Reader Response

From: Name ____

Company ____

Address ____

City / State / ZIP / Country ____

Telephone: (_______) _________ - _________ FAX: (______) _________ - _________

Application (optional):

Would you like a reply?___Y ___N

Device: PIC12F683 Literature Number: DS41211D

Questions:

1. What are the best features of this document?

____

____

2. How does this document meet your hardware and software development needs?

____

____

3. Do you find the organization of this document easy to follow? If not, why?

____

____

4. What additions to the document do you think would enhance the structure and subject?

____

____

5. What deletions from the document could be made without affecting the overall usefulness?

____

____

6. Is there any incorrect or misleading information (what and where)?

____

____

7. How would you improve this document?

____

____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC12F683[1], PIC12F683T[2] VDD range 2.0V to 5.5V
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package:	P = Plastic DIP MD = Dual-Flat, No Leads (DFN-S, 4x4x0.9 mm) MF = Dual-Flat, No Leads (DFN-S, 6x5 mm) SN = 8-lead Small Outline (3.90 mm)
Pattern:	3-digit Pattern Code for QTP (blank otherwise)

Examples:

a) PIC12F683-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301

b) PIC12F683-I/SN = Industrial Temp., SOIC package, 20 MHz

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = in tape and reel PLCC, and TQFP packages only.

MICROCHIP

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Habour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Gumi
Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel: 60-4-646-8870
Fax: 60-4-646-5086

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

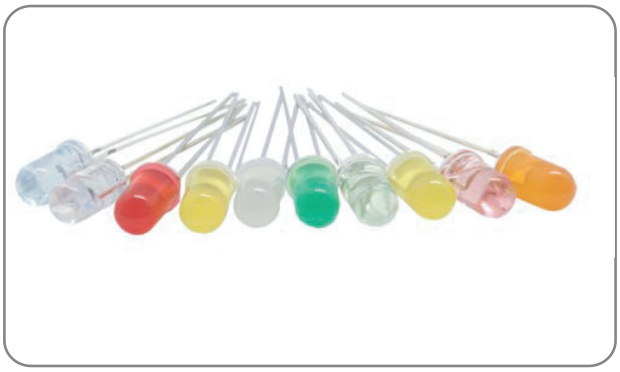
Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

12/08/06



LED DIP 5mm

LED-Y5D-PP-R30/S

- S: Característica Especial
- PP: Intensidad Luminosa
- Y: Color del LED

Especificaciones

Tipo de LED: DIP 5mm

Angulo de apertura: 15º a 30º

Encapsulado transparente y difuso

Temperatura de operación: - 40 a 70 °C

Corriente nominal: 20mA

Y Colores disponibles	Longitud de onda [nm] / TC[K]	Voltaje de Operación [V]		Consumo [mW]	**PP** Intensidad Luminosa [mcd]							
					AD	AC	B		SB		UB	
		Min	Max				Min	Max	Min	Max	Min	Max
R	600-650	1.8	2.2	40	***	***	2200	6000	3100	10000	6300	15 200
G	490-540	1.8	2.2	40	***	***	-	-	10600	13800	13800	22000
B	450-500	3.0	3.4	40	-	***	-	-	3700	6000	4900	9000
Y	550-600	1.8	2.2	40	***	***	2800	3700	4900	6300	6300	21300
O	600-650	1.8	2.2	40	***	***	-	-	-	-	2800	6000
W	5000 - 10000 K	3.0	3.4	40	-	***	10500	13800	18000	30000	20000	30000
PK	420-440	2.9	3.2	64	-	***	7000	10000	-	-	-	-
SP	380-420	3.0	3.4	40	-	***	-	-	-	-	-	-
RG	600-650 490-540	1.8	3.4	42	-	***	-	-	-	-	-	-
UV	400	3.0	4.5	60	-	***	-	-	-	-	-	-
RGB	630-525-475	3.0	3.4	60	-	***	-	-	-	-	-	-
LPK	430-440	3.0	3.4	40	-	***	-	-	-	-	-	-
LG	490-540	3.0	3.4	40	-	***	-	-	-	-	-	-
LB	450-500	3.0	3.4	60	-	***	-	-	-	-	-	-
CW	-	2.7	3.4	60	-	***	-	-	-	-	16000	18000

Los datos mostrados son unicamente de referencia, éstos pueden variar entre lotes diferentes.

*** LEDs de uso general como Indicadores

Características especiales

S=2P (2 pines)

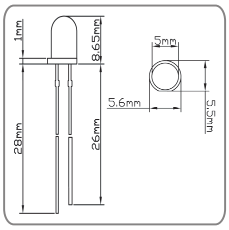
S=4P (4pines)

Aplican solo para LEDs RGB

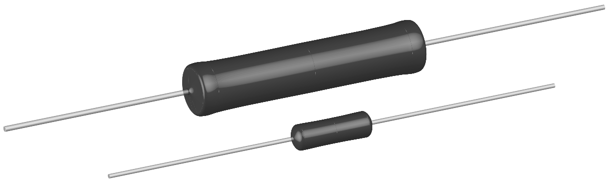
Acabado Difuso

Acabado Claro

Dimensiones



Wirewound Resistors, Commercial Power, Silicone Coated, Axial Lead



FEATURES

- High performance for low cost
- High temperature silicone coating
- Complete welded construction
- Excellent stability in operation
- High power to size ratio
- Compliant to RoHS Directive 2002/95/EC

Pb Pb-free Available
e3
RoHS* COMPLIANT
GREEN (5-2008)** Available

Notes
* Pb containing terminations are not RoHS compliant, exemptions may apply
** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

STANDARD ELECTRICAL SPECIFICATIONS

GLOBAL MODEL	HISTORICAL MODEL	POWER RATING [(1)] $P_{25\ °C}$ W CHARACTERISTIC U + 250 °C	POWER RATING [(1)] $P_{25\ °C}$ W CHARACTERISTIC V + 350 °C	RESISTANCE RANGE Ω	TOLERANCE ± % [(2)]	WEIGHT (max.) g
CW1/2	CW-1/2	0.5	-	0.1 to 1.77K	5, 10	0.21
CW001	CW-1	1.0	-	0.1 to 6.37K	5, 10	0.34
CW01M	CW-1M	1.0	-	0.1 to 3.3K	5, 10	0.3
CW002	CW-2	4.0	5.5	0.1 to 28.7K	5, 10	2.1
CW02M	CW-2M	3.0	3.75	0.1 to 12K	5, 10	0.65
CW02B	CW-2B	3.0	3.75	0.1 to 15K	5, 10	0.7
CW02B...13	CW-2B-13	4.0	6.0	0.1 to 10.89K [(3)]	5, 10	0.9
CW02C	CW-2C	2.5	3.25	0.1 to 19.9K	5, 10	1.8
CW02C...14	CW-2C-14	2.5	3.25	0.1 to 19.9K	5, 10	1.2
CW005	CW-5	5.0	6.5	0.1 to 58.5K	5, 10	4.2
CW005...2	CW-5-2	4.0	5.0	0.1 to 40.3K	5, 10	4.2
CW005...3	CW-5-3	5.0	6.5	0.1 to 58.5K	5, 10	4.2
CW007	CW-7	7.0	9.0	0.1 to 95.2K	5, 10	4.7
CW010	CW-10	10.0	13.0	0.1 to 167K	5, 10	9.0
CW010...3	CW-10-3	10.0	13.0	0.1 to 167K	5, 10	9.0

Notes
(1) Vishay Dale CW models have two power ratings, depending on operating temperature and stability requirements
(2) 3 % tolerance available
(3) Higher values available on request

TECHNICAL SPECIFICATIONS

PARAMETER	UNIT	CW RESISTOR CHARACTERISTICS
Temperature Coefficient	ppm/°C	± 30 for 10 Ω and above, ± 50 for 1.0 Ω to 9.9 Ω, ± 90 for 0.5 Ω to 0.99 Ω
Dielectric Withstanding Voltage	V_{AC}	1000
Short Time Overload	-	5 x rated power for 5 s for 3.75 W size and smaller, 10 x rated power for 5 s for 4 W size and greater
Terminal Strength	lb	10 minimum
Maximum Working Voltage	V	$(P \times R)^{1/2}$
Operating Temperature Range	°C	Characteristic U = - 65 to + 250, characteristic V = - 65 to + 350
Power Rating	-	Characteristic U = + 250 °C max. hot spot temperature, ± 0.5 % max. ΔR in 2000 h load life Characteristic V = + 350 °C max. hot spot temperature, ± 3.0 % max. ΔR in 2000 h load life

GLOBAL PART NUMBER INFORMATION

Global Part Numbering example: CW02C10K00JB1214

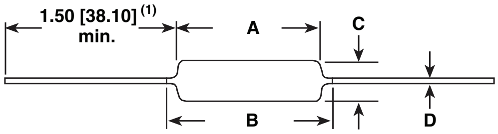
C	W	0	2	C	1	0	K	0	0	J	B	1	2	1	4	

GLOBAL MODEL	VALUE	TOLERANCE	PACKAGING	SPECIAL
(See Standard Electrical Specifications Global Model column for options)	**R** = Decimal **K** = Thousand **1R500** = 1.5 Ω **1K500** = 1.5 kΩ	**H** = ± 3.0 % **J** = ± 5.0 % **K** = ± 10.0 %	**E70** = Lead (Pb)-free, tape/reel, 1K pcs (smaller than CW005) **E73** = Lead (Pb)-free, tape/reel, 500 pcs **E12** = Lead (Pb)-free, bulk **D18** = Lead (Pb)-free, R1R80 tape/reel CW02B...13 pack code for Europe use only **S70** = Tin/lead, tape/reel, 1K pcs (smaller than CW005) **S73** = Tin/lead, tape/reel, 500 pcs **B12** = Tin/lead, bulk	(Dash Number) (up to 3 digits) From **1 to 999** as applicable

Historical Part Numbering example: CW-2C-14 10 kΩ 5 % B12

CW-2C-14	10 kΩ	5 %	B12
HISTORICAL MODEL	RESISTANCE VALUE	TOLERANCE CODE	PACKAGING

DIMENSIONS in inches (millimeters)



MODEL	DIMENSIONS in inches [millimeters]			
	A	B [MAXIMUM] (2)	C	D
CW1/2	0.250 ± 0.031 [6.35 ± 0.787]	0.281 [7.14]	0.085 ± 0.020 [2.16 ± 0.508]	0.020 ± 0.002 [0.508 ± 0.051]
CW001	0.406 ± 0.031 [10.31 ± 0.787]	0.437 [11.10]	0.094 ± 0.031 [2.39 ± 0.787]	0.020 ± 0.002 [0.508 ± 0.051]
CW01M	0.285 ± 0.025 [7.24 ± 0.635]	0.311 [7.90]	0.110 ± 0.015 [2.79 ± 0.381]	0.020 ± 0.002 [0.508 ± 0.051]
CW002	0.625 ± 0.062 [15.87 ± 1.57]	0.765 [19.43]	0.250 ± 0.032 [6.35 ± 0.813]	0.040 ± 0.002 [1.02 ± 0.051]
CW02M	0.500 ± 0.062 [12.70 ± 1.57]	0.562 [14.27]	0.185 ± 0.015 [4.70 ± 0.381]	0.032 ± 0.002 [0.813 ± 0.051]
CW02B	0.562 ± 0.062 [14.27 ± 1.57]	0.622 [15.80]	0.188 ± 0.032 [4.78 ± 0.813]	0.032 ± 0.002 [0.813 ± 0.051]
CW02B...13	0.500 ± 0.062 [12.70 ± 1.57]	0.563 [14.30]	0.188 ± 0.032 [4.78 ± 0.813]	0.032 ± 0.002 [0.813 ± 0.051]
CW02C	0.500 ± 0.062 [12.70 ± 1.57]	0.593 [15.06]	0.218 ± 0.032 [5.54 ± 0.813]	0.040 ± 0.002 [1.02 ± 0.051]
CW02C...14	0.500 ± 0.062 [12.70 ± 1.57]	0.593 [15.06]	0.218 ± 0.032 [5.54 ± 0.813]	0.032 ± 0.002 [0.813 ± 0.051]
CW005	0.875 ± 0.062 [22.22 ± 1.57]	1.0 [25.40]	0.312 ± 0.032 [7.92 ± 0.813]	0.040 ± 0.002 [1.02 ± 0.051]
CW005...2	0.875 ± 0.062 [22.22 ± 1.57]	1.0 [25.40]	0.250 ± 0.032 [6.35 ± 0.813]	0.032 ± 0.002 [0.813 ± 0.051]
CW005...3	0.875 ± 0.062 [22.22 ± 1.57]	1.0 [25.40]	0.312 ± 0.032 [7.92 ± 0.813]	0.032 ± 0.002 [0.813 ± 0.051]
CW007	1.218 ± 0.062 [30.94 ± 1.57]	1.281 [32.54]	0.312 ± 0.032 [7.92 ± 0.813]	0.040 ± 0.002 [1.02 ± 0.051]
CW010	1.781 ± 0.062 [45.24 ± 1.57]	1.875 [47.62]	0.375 ± 0.032 [9.52 ± 0.813]	0.040 ± 0.002 [1.02 ± 0.051]
CW010...3	1.781 ± 0.062 [45.24 ± 1.57]	1.875 [47.62]	0.375 ± 0.032 [9.52 ± 0.813]	0.032 ± 0.002 [0.813 ± 0.051]

Notes

(1) On some standard reel pack methods, the leads may be trimmed to a shorter length than shown

(2) B (maximum) dimension is clean lead to clean lead

MATERIAL SPECIFICATIONS

Element: Copper-nickel alloy or nickel-chrome alloy, depending on resistance value

Core: Ceramic: Steatite or alumina, depending on physical size

Coating: Special high temperature silicone

Standard Terminals: Tinned Copperweld®
(CW02B…13 is tinned copper)

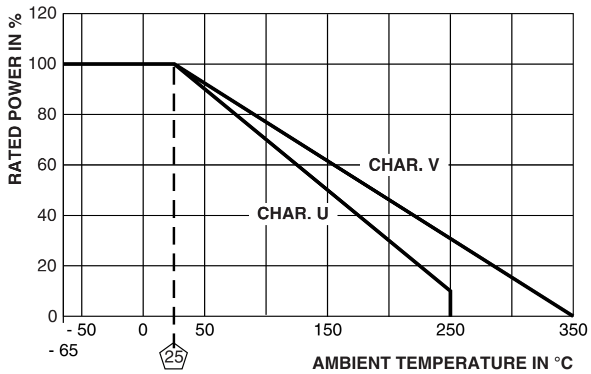
End Caps: Stainless steel

Part Marking: DALE, model, wattage (3), value, tolerance, date code

Note

(3) Wattage marked on resistor will be "V" characteristic, CW1/2 will not be marked with wattage

DERATING



PERFORMANCE

TEST	CONDITIONS OF TEST	TEST LIMITS (4) (CHARACTERISTIC V)
Thermal Shock	Rated power applied until thermally stable, then a minimum of 15 min at - 55 °C	± (2.0 % + 0.05 Ω) Δ*R*
Short Time Overload	5 x rated power (3.75 W and smaller), 10 x rated power (4 W and larger) for 5 s	± (2.0 % + 0.05 Ω) Δ*R*
Dielectric Withstanding Voltage	1000 V_{rms}, 1 min	± (0.1 % + 0.05 Ω) Δ*R*
Low Temperature Storage	- 65 °C for 24 h	± (2.0 % + 0.05 Ω) Δ*R*
High Temperature Exposure	250 h at + 350 °C	± (4.0 % + 0.05 Ω) Δ*R*
Moisture Resistance	MIL-STD-202 Method 106, 7b not applicable	± (2.0 % + 0.05 Ω) Δ*R*
Shock, Specified Pulse	MIL-STD-202 Method 213, 100 g's for 6 ms, 10 shocks	± (0.2 % + 0.05 Ω) Δ*R*
Vibration, High Frequency	Frequency varied 10 Hz to 2000 Hz, 20 g peak, 2 directions 6 h each	± (0.2 % + 0.05 Ω) Δ*R*
Load Life	2000 h at rated power, + 25 °C, 1.5 h "ON", 0.5 h "OFF"	± (3.0 % + 0.05 Ω) Δ*R*
Terminal Strength	5 s to 10 s 10 pound pull test; torsion test - 3 alternating directions, 360° each	± (1.0 % + 0.05 Ω) Δ*R*

Note

(4) All Δ*R* figures shown are maximum, based upon testing requirements per MIL-PRF-26 at a maximum operating temperature of + 350 °C. Δ*R* maximum figures are considerably lower when tested at a maximum operating temperature of + 250 °C.

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Carbon Film Fixed Resistors

Performance Specification

Temperature Coefficient	≤ 10Ω : ±350PPM/°C 11Ω ~99KΩ : 0 ~ -450PPM/°C 100KΩ ~ 1MΩ : 0 ~ -700PPM/°C 1.1MΩ ~ 10MΩ : 0 ~ -1500PPM/°C
Short Time Overload	±(1.0% + 0.05Ω)Max, with no evidence of mechanical damage.
Insulation Resistance	Min. 10,000 Mega Ohm
Dieiectric Withstanding Voltage	No evidence of flashover, mechanical damage, arcing or insulation breakdown.
Terminal Strength	No evidence of mechanical damage.
Resistance to Soldering Heat	±(1.0% + 0.05Ω)Max, with no evidence of mechanical damage.
Solderability	Min. 95% coverage.
Resistance to Solvent	No deterioration of protective coating and markings.
Temperature Cycling	±(1.0% + 0.05Ω)Max, with no evidence of mechanical damage.
Load Life in Humidity	Normal type: <100KΩ: ±(3.0% + 0.05Ω)Max ≥100KΩ: ±(5.0% + 0.05Ω)Max Non-Flame type: <100KΩ: ±(5.0% + 0.05Ω)Max ≥100KΩ: ±(10.0% + 0.05Ω)Max
Load Life	Normal type: <56KΩ: ±(2.0% + 0.05Ω)Max ≥56KΩ: ±(3.0% + 0.05Ω)Max Non-Flame type: <100KΩ: ±(5.0% + 0.05Ω)Max ≥100KΩ: ±(10.0% + 0.05Ω)Max

Ordering Procedure: Ex.: CFR 1/4W, +/-5%,10KΩ, T/B-5000

C F R 0 W 4 J 0 1 0 3 A 5 0

Type:
CFR = Carbon Film

Feature:
0 = Standard
F = Non-Flame
I = Non-Inductive

Wattage:

Normal size:
W8 = 1/8W
W4 = 1/4W
W2 = 1/2W
1W = 1W
2W = 2W

Small size:
S4 = 1/4W-S
S3 = 1/3W-S
S2 = 1/2W-S
1S = 1W-S
2S = 2W-S
3S = 3W-S

Extra small size:
U2 = 1/2W-SS
1U = 1W-SS

Tolerance:
F = ± 1%
G = ±2%
J = ±5%
K = ±10%

Resistance Value:

- E-24 series:
  1st digit is "0"
  2nd & 3rd digits are significant figures of the resistance
  4th indicates the number of zeros
  "J" ~0.1, "K" ~ 0.01
  Ex. 4.7Ω ~ 47J, 4.7KΩ ~ 472
- E-96 series:
  1st to 3rd digits are significant figures of the resistance
  4th digit indicates the number of zeros.
  Ex.: 1.33KΩ = 1331

Packing Type:
A = Tape/Box
T = Tape/Reel
B = Bulk/Box
P = Tape/Box of PT-26mm

Packing Qty:
1 = 1,000 pcs. 2 = 2,000 pcs.
4 = 4,000 pcs. 5 = 5,000 pcs.
A = 500 pcs. B = 2,500 pcs.
0 = Bulk/Box

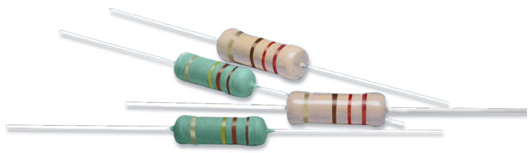
Additional Information:
P = Panasert type
1 = Avisert type
2 = Avisert type 2
3 = Avisert type 3
0 = PT-52mm, PT-26mm, Standard lead wire for Bulk/Box
8 = PT-58mm
9 = PT-64mm
7 = Lead wire (H) 38mm
C = PT-73mm

RoHS Compliant

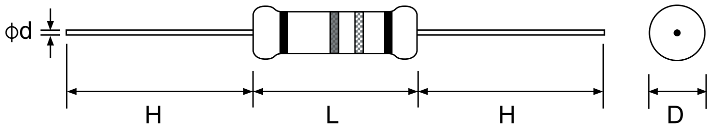
Carbon Film Fixed Resistors

Features

- Automatically insertable
- High quality performance
- Non-Flame type available
- Cost effective and commonly used
- Too low or too high values can be supplied on case to case basis



Standard : 2% ,5% ,10% -- E - 24 series
1% -- E - 96 series

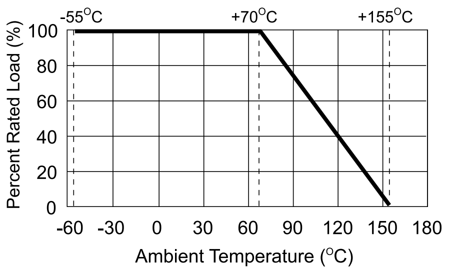


Part No.	Style	Power Rating at 70°C	Dimension (mm)					Resistance Range	Max Working Voltage	Max Overload Voltage	Dielectric Withstanding Voltage	Std Packing Qty
			D Max	L Max	H±3	d±0.05	PT					
Normal size												
CFR0W8	CFR 12	1/8W (0.125W)	1.85	3.5	28	0.45	52	1Ω ~ 1MΩ	200	400	400	5,000
CFR0W4	CFR 25	1/4W(0.25W)	2.5	6.8	28	0.54 (1)	52	1Ω ~ 10MΩ	250	500	500	5,000
CFR0W2	CFR 50	1/2W (0.50W)	3.5	10.0	28	0.54	52	1Ω ~ 10MΩ	350	700	700	1,000
CFR01W	CFR 100	1W	5.5	16.0	28	0.70	64	1Ω ~ 10MΩ	500	1,000	1,000	1,000
CFR02W	CFR 200	2W	6.5	17.5	28	0.75	64	1Ω ~ 10MΩ	500	1,000	1,000	500
Small size												
CFR0S4	CFR-25-S	1/4W(0.25W)	1.85	3.5	28	0.45	52	1Ω ~ 1MΩ	200	400	400	5,000
CFRFU2	CFR-50-SS	1/2W (0.50W)	2.5	6.8	28	0.54 (1)	52	1Ω ~ 10MΩ	250	500	250	5,000
CFR0S2	CFR-50-S	1/2W (0.50W)	3.0	9.0	28	0.54	52	1Ω ~ 10MΩ	350	700	700	4,000
CFRF1U	CFR-100-SS	1W	3.5	10.0	28	0.54	52	1Ω ~ 10MΩ	350	700	350	1,000
CFR01S	CFR-100-S	1W	5.0	12.0	25	0.70	52	1Ω ~ 10MΩ	500	1,000	1,000	1,000
CFR02S	CFR-200-S	2W	5.5	16.0	28	0.70	64	1Ω ~ 10MΩ	500	1,000	1,000	1,000
CFR03S	CFR-300-S	3W	6.5	17.5	28	0.75	64	1Ω ~ 10MΩ	500	1,000	1,000	500

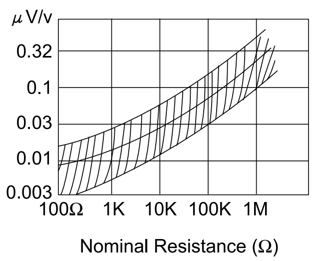
Note:

- Standard beige base color
- Standard grayish-green base color (Non-flammable coating) for CFRFU2 (CFR-50-SS) and CFRF1U (CFR-100.SS)
- (1) Lead diameter of CFR0W4 & CFRFU2 can be provided in 0.50mm, 0.54mm & 0.60mm
- Ohmic values outside the standard range available on a case to case basis

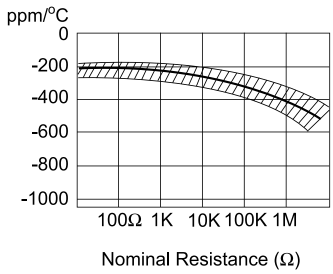
Derating Curve



Current Noise

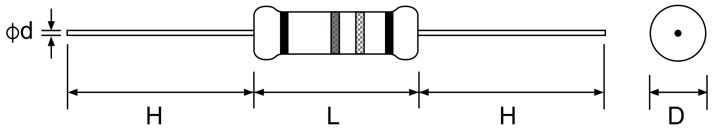


Temp. Coefficient



Carbon Film Fixed Resistors

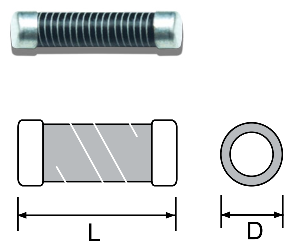
1) Copper Plated Steel Lead Wire Type
Copper Plated Wire (CP)
Tin Plated Copper Steel Lead Wire (CT)



Part No.	Style	Power Rating at 70°C	Dimension (mm)					Max Working Voltage	Max Overload Voltage	Dielectric Withstanding Voltage	Resistance Range	Std Packing Qty
			D Max	L Max	H±3	d±0.02	PT					
CPxxW8 / CTxxW8	CP/ CT 12	1/8W (0.125W)	1.85	3.5	28	0.50	52	200V	400V	400V	1Ω~1MΩ	5,000
CPxxW4 / CTxxW4	CP/ CT 25	1/4W(0.25W)	2.5	6.8	28/38	0.50	52	250V	500V	500V	1Ω ~ 10MΩ	5,000
CPxxS3 / CTxxS3	CP/ CT 33-S	1/3W (0.33W)	2.5	6.8	28/38	0.50	52	300V	600V	500V	1Ω ~ 10MΩ	5,000
CPxxW3 / CTxxW3	CP/ CT 33	1/3W (0.33W)	3.0	9.0	28	0.50	52	300V	600V	700V	1Ω ~ 10MΩ	2,000
CPxxS2 / CTxxS2	CP/ CT 50-S	1/2W (0.5W)	3.0	9.0	28	0.50	52	350V	700V	700V	1Ω ~ 10MΩ	2,000

2) Cutting (CO) Type

Part No.	Style	Power Rating at 70°C	Dimension (mm)		Resistance Range
			D	L	
CO..W8	CO 12	1/8W (0.125W)	1.6 +0.10 / - 0.00	3.2 ± 0.1	1Ω ~ 10MΩ
CO..W4	CO 25	1/4W (0.25W)	2.1 +0.09 / - 0.00	5.6 +0.10 / - 0.20	1Ω ~ 10MΩ
CO..W4-A	CO 25-A	1/4W (0.25W)	2.1 +0.09 / - 0.00	5.9 +0.10 / - 0.15	1Ω ~ 10MΩ



Cutting type resistors are produced without lead wire and without coating
"Cap plated : Tin plated (ROYALOHM std.)

Ordering Procedure: Ex.: CFO 1/4W, +/-5%,10Ω, T/B-5000

C P O 0 W 4 J 0 1 0 0 A 5 0

Type:
CPO =
Copper plated lead wire (H=28mm)
CPL =
Copper plated lead wire (H=38mm)
CTO =
Tin plated copper steel lead wire (H=28mm)
CTL =
Tin plated copper steel lead wire (H=38mm)
COT =
Cutting Type (Tin-Plated Cap)

Feature:
0 = Standard
F = Non-Flame
I = Non-Inductive

Wattage:
Normal
W8 = 1/8W
W4 = 1/4W
W3 = 1/3W

Small
S2 = 1/2W-S
S3 = 1/3W-S

Tolerance:
G = ±2%
J = ±5%
K = ±10%

Resistance Value:
- E-24 series:
  1st digit is "0"
  2nd & 3rd digits are significant figures of the resistance
  4th indicates the number of zeros
  "J" ~ 0.1, "K" ~ 0.01
  Ex. 4.7Ω ~ 47J, 4.7KΩ ~ 472

Packing Type:
A = Tape/Box
T = Tape/Reel
B = Bulk/Box

Packing Qty:
1 = 1,000 pcs. 2 = 2,000 pcs. 4 = 4,000 pcs.
5 = 5,000 pcs. A = 500 pcs. B = 2,500 pcs.
0 = Bulk/Box

Additional Information:
0 = CP/CT Type
A = Cutting type (CO-25-A)

RoHS Compliant

Little Rebel®

Carbon Film Resistors, 5% Tolerance
Available in E24 Ohmic values

Little Rebels are one of Ohmite's more economical lines of low wattage resistors. Constructed of a pure carbon film deposited on a high-grade ceramic body, these units offer better stability performance than comparable carbon composition resistors.
Little Rebels are designed for electrical and electronic applications that demand small sizes and small power ratings plus high performance and reliability.

FEATURES

- High stability, low noise level, long life.
- Ideal for applications requiring a steady low power drop.
- Available in Resistor Cabinet Assortments.
- 24 Values per decade.

SERIES SPECIFICATIONS

Series	Wattage	Ohms	Max. Working Voltage
OJ	0.125	1.0- 1M	200
OK	0.250	1.0-10M	250
OL	0.500	1.0-10M	350
OM	1.00	1.0-10M	500
ON	2.00	1.0-10M	500

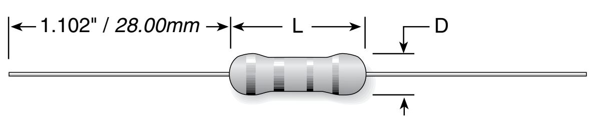
*Available in Cabinet Assortments

CHARACTERISTICS

Core	High-grade ceramic.
Terminals	Solder-coated copper lead.
Derating	Linearly from 100% @ +70°C to 0% @ 155°C.
Tolerance	±5%.
Temperature Coefficient	1Ω to 10: ±350 ppm/°C 11Ω to 91K: -450 ppm/°C 100K to 1M: -700 ppm/°C 1.1M to 10M: -800 to 1500 ppm/°C
Maximum Overload Voltage	OJ: 400 Volts OK: 500 Volts OL: 700 Volts OM: 1000 Volts ON: 1000 Volts
Quantity per reel	OJ: 5000 OK: 5000 OL: 4000 OM: 2500 ON: 1000

DIMENSIONS

(iin./mm)



Series	Wattage	Max. Length	Max. Diam.	Lead ga.
OJ	0.125	0.138 / 3.5	0.073 / 1.85	24
OK	0.250	0.268 / 6.8	0.099 / 2.5	22
OL	0.500	0.355 / 9.0	0.118 / 3.0	22
OM	1.00	0.473 /12.0	0.197 / 5.0	20
ON	2.00	0.630 / 16.0	0.217 / 5.5	20

(continued)

Little Rebel®

Carbon Film Resistors, 5% Tolerance
Available in E24 Ohmic values

ORDERING INFORMATION

Standard part numbers for standard resistance values

Ohmic value	Part No. Prefix ➤ Suffix ▼	Wattage OJ — 0.125	OK — 0.25	OL — 0.50	OM — 1.0	ON — 2.0
1	10G5	✔	✔	✔	✔	✔
1.1	11G5	✔	✔	✔	✔	✔
1.2	12G5	✔	✔	✔	✔	✔
1.3	13G5	✔	✔	✔	✔	✔
1.5	15G5	✔	✔	✔	✔	✔
1.6	16G5	✔	✔	✔	✔	✔
1.8	18G5	✔	✔	✔	✔	✔
2.0	20G5	✔	✔	✔	✔	✔
2.2	22G5	✔	✔	✔	✔	✔
2.4	24G5	✔	✔	✔	✔	✔
2.7	27G5	✔	✔	✔	✔	✔
3.0	30G5	✔	✔	✔	✔	✔
3.3	33G5	✔	✔	✔	✔	✔
3.6	36G5	✔	✔	✔	✔	✔
3.9	39G5	✔	✔	✔	✔	✔
4.3	43G5	✔	✔	✔	✔	✔
4.7	47G5	✔	✔	✔	✔	✔
5.1	51G5	✔	✔	✔	✔	✔
5.6	56G5	✔	✔	✔	✔	✔
6.2	62G5	✔	✔	✔	✔	✔
6.8	68G5	✔	✔	✔	✔	✔
7.5	75G5	✔	✔	✔	✔	✔
8.2	82G5	✔	✔	✔	✔	✔
9.1	91G5	✔	✔	✔	✔	✔
10	1005	✔	✔	✔	✔	✔
11	1105	✔	✔	✔	✔	✔
12	1205	✔	✔	✔	✔	✔
13	1305	✔	✔	✔	✔	✔
15	1505	✔	✔	✔	✔	✔
16	1605	✔	✔	✔	✔	✔
18	1805	✔	✔	✔	✔	✔
20	2005	✔	✔	✔	✔	✔
22	2205	✔	✔	✔	✔	✔
24	2405	✔	✔	✔	✔	✔
27	2705	✔	✔	✔	✔	✔
30	3005	✔	✔	✔	✔	✔
33	3305	✔	✔	✔	✔	✔
36	3605	✔	✔	✔	✔	✔
39	3905	✔	✔	✔	✔	✔
43	4305	✔	✔	✔	✔	✔
47	4705	✔	✔	✔	✔	✔
51	5105	✔	✔	✔	✔	✔
56	5605	✔	✔	✔	✔	✔

Ohmic value	Part No. Prefix ➤ Suffix ▼	Wattage OJ — 0.125	OK — 0.25	OL — 0.50	OM — 1.0	ON — 2.0
62	6205	✔	✔	✔	✔	✔
68	6805	✔	✔	✔	✔	✔
75	7505	✔	✔	✔	✔	✔
82	8205	✔	✔	✔	✔	✔
91	9105	✔	✔	✔	✔	✔
100	1015	✔	✔	✔	✔	✔
110	1115	✔	✔	✔	✔	✔
120	1215	✔	✔	✔	✔	✔
130	1315	✔	✔	✔	✔	✔
150	1515	✔	✔	✔	✔	✔
160	1615	✔	✔	✔	✔	✔
180	1815	✔	✔	✔	✔	✔
200	2015	✔	✔	✔	✔	✔
220	2215	✔	✔	✔	✔	✔
240	2415	✔	✔	✔	✔	✔
270	2715	✔	✔	✔	✔	✔
330	3315	✔	✔	✔	✔	✔
350	3515	✔	✔	✔	✔	✔
360	3615	✔	✔	✔	✔	✔
390	3915	✔	✔	✔	✔	✔
430	4315	✔	✔	✔	✔	✔
470	4715	✔	✔	✔	✔	✔
510	5115	✔	✔	✔	✔	✔
560	5615	✔	✔	✔	✔	✔
620	6215	✔	✔	✔	✔	✔
680	6815	✔	✔	✔	✔	✔
750	7515	✔	✔	✔	✔	✔
820	8215	✔	✔	✔	✔	✔
910	9115	✔	✔	✔	✔	✔
1,000	1025	✔	✔	✔	✔	✔
1,100	1125	✔	✔	✔	✔	✔
1,200	1225	✔	✔	✔	✔	✔
1,300	1325	✔	✔	✔	✔	✔
1,500	1525	✔	✔	✔	✔	✔
1,600	1625	✔	✔	✔	✔	✔
1,800	1825	✔	✔	✔	✔	✔
2,000	2025	✔	✔	✔	✔	✔
2,200	2225	✔	✔	✔	✔	✔
2,400	2425	✔	✔	✔	✔	✔
2,700	2725	✔	✔	✔	✔	✔
3,000	3025	✔	✔	✔	✔	✔
3,300	3325	✔	✔	✔	✔	✔
3,600	3625	✔	✔	✔	✔	✔

Ohmic value	Part No. Prefix ➤ Suffix ▼	Wattage OJ — 0.125	OK — 0.25	OL — 0.50	OM — 1.0	ON — 2.0
3,900	3925	✔	✔	✔	✔	✔
4,300	4325	✔	✔	✔	✔	✔
4,700	4725	✔	✔	✔	✔	✔
5,100	5125	✔	✔	✔	✔	✔
5,600	5625	✔	✔	✔	✔	✔
6,200	6225	✔	✔	✔	✔	✔
6,800	6825	✔	✔	✔	✔	✔
7,500	7525	✔	✔	✔	✔	✔
8,200	8225	✔	✔	✔	✔	✔
9,100	9125	✔	✔	✔	✔	✔
10,000	1035	✔	✔	✔	✔	✔
11,000	1135	✔	✔	✔	✔	✔
12,000	1235	✔	✔	✔	✔	✔
13,000	1335	✔	✔	✔	✔	✔
15,000	1535	✔	✔	✔	✔	✔
16,000	1635	✔	✔	✔	✔	✔
18,000	1835	✔	✔	✔	✔	✔
20,000	2035	✔	✔	✔	✔	✔
22,000	2235	✔	✔	✔	✔	✔
24,000	2435	✔	✔	✔	✔	✔
27,000	2735	✔	✔	✔	✔	✔
30,000	3035	✔	✔	✔	✔	✔
33,000	3335	✔	✔	✔	✔	✔
36,000	3635	✔	✔	✔	✔	✔
39,000	3935	✔	✔	✔	✔	✔
43,000	4335	✔	✔	✔	✔	✔
47,000	4735	✔	✔	✔	✔	✔
51,000	5135	✔	✔	✔	✔	✔
56,000	5635	✔	✔	✔	✔	✔
62,000	6235	✔	✔	✔	✔	✔
68,000	6835	✔	✔	✔	✔	✔
75,000	7535	✔	✔	✔	✔	✔
82,000	8235	✔	✔	✔	✔	✔
91,000	9135	✔	✔	✔	✔	✔
100,000	1045	✔	✔	✔	✔	✔
110,000	1145	✔	✔	✔	✔	✔
120,000	1245	✔	✔	✔	✔	✔
130,000	1345	✔	✔	✔	✔	✔
150,000	1545	✔	✔	✔	✔	✔
160,000	1645	✔	✔	✔	✔	✔
180,000	1845	✔	✔	✔	✔	✔
200,000	2045	✔	✔	✔	✔	✔
220,000	2245	✔	✔	✔	✔	✔

Ohmic value	Part No. Prefix ➤ Suffix ▼	Wattage OJ — 0.125	OK — 0.25	OL — 0.50	OM — 1.0	ON — 2.0
240,000	2445	✔	✔	✔	✔	✔
270,000	2745	✔	✔	✔	✔	✔
300,000	3045	✔	✔	✔	✔	✔
330,000	3345	✔	✔	✔	✔	✔
360,000	3645	✔	✔	✔	✔	✔
390,000	3945	✔	✔	✔	✔	✔
430,000	4345	✔	✔	✔	✔	✔
470,000	4745	✔	✔	✔	✔	✔
510,000	5145	✔	✔	✔	✔	✔
560,000	5645	✔	✔	✔	✔	✔
620,000	6245	✔	✔	✔	✔	✔
680,000	6845	✔	✔	✔	✔	✔
750,000	7545	✔	✔	✔	✔	✔
820,000	8245	✔	✔	✔	✔	✔
910,000	9145	✔	✔	✔	✔	✔
1 MEG	1055	✔	✔	✔	✔	✔
1.1 MEG	1155		✔	✔	✔	✔
1.2 MEG	1255		✔	✔	✔	✔
1.3 MEG	1355		✔	✔	✔	✔
1.5 MEG	1555		✔	✔	✔	✔
1.6 MEG	1655		✔	✔	✔	✔
1.8 MEG	1855		✔	✔	✔	✔
2.0 MEG	2055		✔	✔	✔	✔
2.2 MEG	2255		✔	✔	✔	✔
2.4 MEG	2455		✔	✔	✔	✔
2.7 MEG	2755		✔	✔	✔	✔
3.0 MEG	3055		✔	✔	✔	✔
3.3 MEG	3355		✔	✔	✔	✔
3.6 MEG	3655		✔	✔	✔	✔
3.9 MEG	3955		✔	✔	✔	✔
4.3 MEG	4355		✔	✔	✔	✔
4.7 MEG	4755		✔	✔	✔	✔
5.1 MEG	5155		✔	✔	✔	✔
5.6 MEG	5655		✔	✔	✔	✔
6.2 MEG	6255		✔	✔	✔	✔
6.8 MEG	6855		✔	✔	✔	✔
7.5 MEG	7555		✔	✔	✔	✔
8.2 MEG	8255		✔	✔	✔	✔
9.1 MEG	9155		✔	✔	✔	✔
10 MEG	1065		✔	✔	✔	✔

Tolerance
5 = 5% (Std.)
1 = 10%

RoHS Compliant

O J 1 0 3 5 E - R 5 2

Series
Selected from Specification Chart

Ohms
3 Digit IEC Code
("G" as 3rd digit = 0.1)
11G=1.1Ω
101=100Ω
102=1000Ω
103=10,000Ω
104=100,000Ω
105=1 MΩ
106=10 MΩ

Packaging Code
R52 = Tape & Reel 52mm
(except ON: R58 = Tape & Reel 58mm)
A52(26) = Ammo Pac 52mm (26mm)

Film capacitors

Metallized polypropylene film capacitors (MKP)

Series/Type: **B32774 ... B32778**

Date: December 2023

Typical applications

- Frequency converters
- Industrial and high-end power supplies
- Solar inverters

Climatic

- Max. operating temperature: 105 °C (case)
- Climatic category (IEC 60068-1:2013): 40/105/56

Construction

- Dielectric: polypropylene (MKP)
- Plastic case (UL 94 V-0)
- Epoxy resin sealing (UL 94 V-0)

Features

- Capacitance values up to 480 µF
- High CV product, compact
- Good self-healing properties
- Over-voltage capability
- Low losses with high current capability
- High reliability
- Long useful life
- RoHS-compatible

Terminals

- Parallel wire leads, lead-free tinned
- 2-pin, 4-pin and 12-pin versions
- Standard lead lengths: 6 –1 mm

Marking

Manufacturer's logo and lot number, date code, rated capacitance (coded), capacitance tolerance (code letter) and rated DC voltage

Delivery mode

Bulk (untaped)

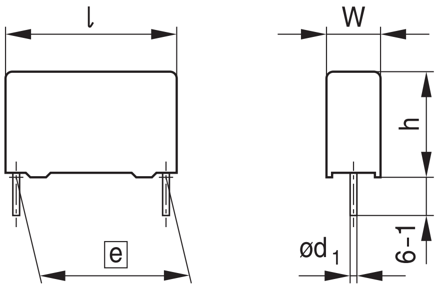
Dimensional drawings

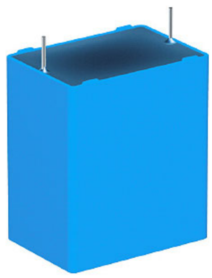
Number of wires	Lead spacing $\boxed{e}$ ±0.4	Lead diameter d_1 ±0.05	Type
2-pin	27.5	0.8	B32774D
2-pin	37.5	1.0	B32776E
2-pin	37.5	1.0	B32776T
4-pin	37.5	1.2	B32776G
4-pin	37.5	1.2	B32776T
4-pin	52.5	1.2	B32778T
4-pin	52.5	1.2	B32778G
12-pin	52.5	1.2	B32778J

Dimensions in mm

Dimensional drawings 2-pin versions

B32774D, B32776E

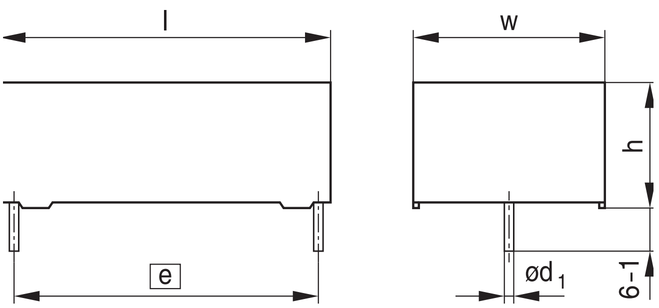


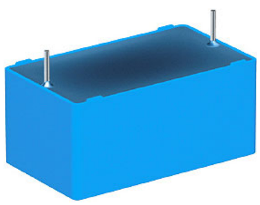


	B32774D	B32776E
Lead spacing $\boxed{e}$ ±0.4:	27.5	37.5
Lead diameter d_1:	0.8	1.0

Dimensions in mm

B32776T (low profile)



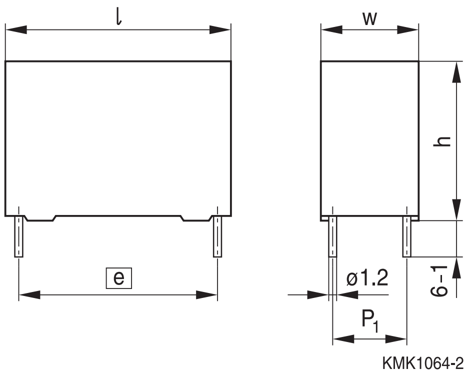


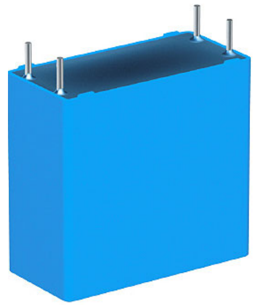
Lead spacing $\boxed{e}$ ±0.4:	37.5
Lead diameter d_1:	1.0

Dimensions in mm

Dimensional drawings 4-pin versions

B32776G, B32778G

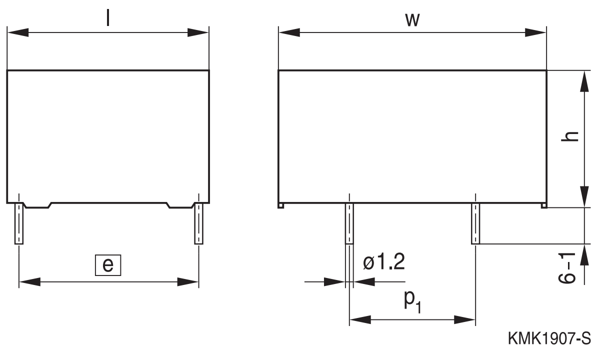


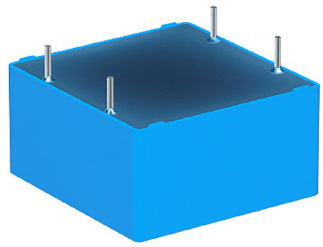


	B32776G	B32778G
Lead spacing $\boxed{e}$ ±0.4:	37.5	52.5
Lead diameter d_1:	1.2	1.2

Dimensions in mm

B32776T, B32778T (low profile)



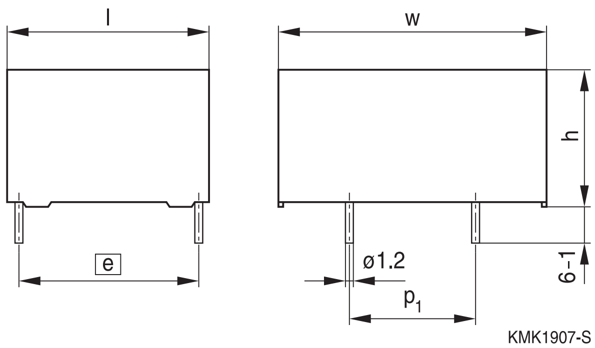


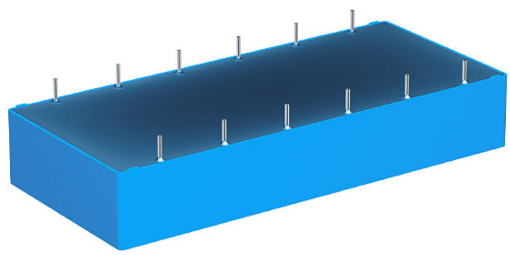
	B32776T	B32778T
Lead spacing $\boxed{e}$ ±0.4:	37.5	52.5
Lead diameter d_1:	1.2	1.2

Dimensions in mm

Dimensional drawing 12-pin version

B32778J





Lead spacing $\boxed{e}$ ±0.4:	52.5
Lead diameter d_1:	1.2

Dimensions in mm

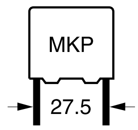
Overview of available types

Lead spacing	27.5 mm				37.5 mm					
Type	B32774				B32776					
Page	7				8					
V_R (V DC)	450	800	1100	1300	450	575	800	900	1100	1300
C_R (µF)										
1.5										
2.0										
2.7										
3.0										
3.3										
3.5										
3.9										
5.0										
6.8										
7.0										
7.5										
8.0										
8.5										
9.0										
10										
12										
13										
14										
15										
16										
20										
22										
25										
27										
30										
35										
40										
45										
50										
60										
65										

Overview of available types

Lead spacing	52.5 mm					
Type	B32778					
Page	11					
V_R (V DC)	450	575	800	900	1100	1300
C_R (µF)						
14						
20						
25						
27						
30						
35						
38						
40						
42						
45						
50						
55						
58						
60						
70						
75						
80						
90						
100						
110						
120						
130						
150						
170						
180						
200						
210						
270						
360						
480						

Ordering codes and packing units (lead spacing 27.5 mm)



C_R 1)	Max. dimensions w x h x l	Ordering code (composition see below)	$I_{RMS,max}$ 2) 70 °C 10 kHz	ESR_{typ} 70 °C 10 kHz	ESL_{typ} 3)	tan δ 1 kHz	tan δ 10 kHz	Un-taped pcs./
µF	mm		A	mΩ	nH	10^{-3}	10^{-3}	MOQ
$V_{R,70\,°C}$ = 450 V DC, $V_{op,85\,°C}$ = 450 V DC								
5.0	11.0 x 21.0 x 31.5	B32774D4505+000	5.0	21.1	19.0	1.2	10.7	2352
10.0	15.0 x 24.5 x 31.5	B32774D4106+000	8.0	10.9	24.0	1.2	11.0	1680
22.0	22.0 x 36.5 x 31.5	B32774D4226+000	14.5	5.4	30.0	1.3	12.1	784
$V_{R,70\,°C}$ = 800 V DC, $V_{op,85\,°C}$ = 700 V DC								
3.0	11.0 x 21.0 x 31.5	B32774D8305+000	4.5	24.8	19.0	0.9	7.6	2352
5.0	14.0 x 24.5 x 31.5	B32774D8505+000	6.5	15.3	23.0	0.9	7.7	1848
12.0	22.0 x 36.5 x 31.5	B32774D8126+000	13.0	6.8	34.0	1.0	8.3	784
$V_{R,70\,°C}$ = 1100 V DC, $V_{op,85\,°C}$ = 920 V DC								
2.0	12.5 x 21.5 x 31.5	B32774D0205+000	4.5	26.3	19.0	0.7	5.3	2100
3.3	18.0 x 27.5 x 31.5	B32774D0335+000	7.0	16.2	22.0	0.7	5.4	1428
5.0	19.0 x 30.0 x 31.5	B32774D0505+000	9.0	10.9	27.0	0.7	5.5	896
7.0	22.0 x 36.5 x 31.5	B32774D0705+000	12.0	8.1	30.0	0.7	5.8	784
$V_{R,70\,°C}$ = 1300 V DC, $V_{op,85\,°C}$ = 1100 V DC								
1.5	12.5 x 21.5 x 31.5	B32774D1155K000	4.4	31.3	20.0	0.6	4.8	2100
3.0	18.0 x 27.5 x 31.5	B32774D1305K000	7.0	16.0	24.0	0.6	4.9	1428
5.0	22.0 x 36.5 x 31.5	B32774D1505K000	10.5	9.8	33.0	0.7	5.1	784

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

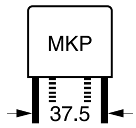
+ = Capacitance tolerance code:

J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for ΔT ≤20 °C at ΔESR_{typ} ≤±5%
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)

Ordering codes and packing units (lead spacing 37.5 mm)



C_R[1)] µF	Max. dimensions w x h x l mm	P_1 mm	Ordering code (composition see below)	$I_{RMS,max}$[2)] 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ}[3)] nH	tan δ 10^{-3}	tan δ 10^{-3}	Un-taped pcs./ MOQ
$V_{R,70\,°C}$ = 450 V DC, $V_{op,85\,°C}$ = 450 V DC									
12	24.0 x 15.0 x 41.5	–	B32776T4126K000	7.0	17.1	19.0	2.2	21.0	1040
16	24.0 x 19.0 x 41.5	–	B32776T4166K000	8.0	13.0	18.0	2.3	21.2	780
30	20.0 x 39.5 x 42.0	10.2	B32776G4306+000	14.0	7.0	11.0	2.3	21.3	640
30	20.0 x 39.5 x 42.0	–	B32776E4306+000	14.0	7.3	28.0	2.4	22.3	640
35	28.0 x 37.0 x 42.0	10.2	B32776G4356+000	16.5	6.0	10.0	2.3	21.4	440
35	28.0 x 37.0 x 42.0	–	B32776E4356+000	16.0	6.4	24.0	2.4	22.6	440
40	28.0 x 37.0 x 42.0	10.2	B32776G4406+000	17.5	5.3	11.0	2.3	21.4	440
40	28.0 x 37.0 x 42.0	–	B32776E4406+000	17.0	5.6	26.0	2.4	22.7	440
40	43.0 x 22.0 x 41.5	20.3	B32776T4406K000	17.0	5.2	13.0	2.3	21.2	280
50	28.0 x 42.5 x 42.0	10.2	B32776G4506+000	20.0	4.3	12.0	2.3	21.7	440
50	28.0 x 42.5 x 42.0	–	B32776E4506+000	19.0	4.7	30.0	2.5	23.8	440
60	30.0 x 45.0 x 42.0	20.3	B32776G4606+000	23.5	3.6	14.0	2.4	22.3	400
60	30.0 x 45.0 x 42.0	–	B32776E4606+000	22.0	4.0	32.0	2.5	24.2	400
65	33.0 x 48.0 x 42.0	20.3	B32776G4656+000	25.5	3.3	14.0	2.3	22.2	180
$V_{R,70\,°C}$ = 575 V DC, $V_{op,85\,°C}$ = 500 V DC									
8.5	24.0 x 15.0 x 41.5	–	B32776T5855+000	6.5	19.9	19.0	1.9	17.2	1040
12	24.0 x 19.0 x 41.5	–	B32776T5126K000	8.0	14.4	18.0	1.9	17.4	780
25	20.0 x 39.5 x 42.0	10.2	B32776G5256K000	14.0	7.0	12.0	1.9	17.5	640
25	20.0 x 39.5 x 42.0	–	B32776E5256K000	13.5	7.4	28.0	2.0	18.3	640
27	43.0 x 22.0 x 41.5	20.3	B32776T5276K000	15.5	6.4	14.0	1.9	17.5	280
30	28.0 x 37.0 x 42.0	10.2	B32776G5306K000	16.5	5.8	11.0	1.9	17.6	440
30	28.0 x 37.0 x 42.0	–	B32776E5306K000	16.5	6.1	26.0	2.0	18.5	440
35	28.0 x 42.5 x 42.0	10.2	B32776G5356+000	19.0	5.0	12.0	1.9	17.8	440
35	28.0 x 42.5 x 42.0	–	B32776E5356+000	18.0	5.3	29.0	2.0	19.0	440
45	30.0 x 45.0 x 42.0	20.3	B32776G5456K000	22.0	4.0	13.0	1.9	17.9	400
45	30.0 x 45.0 x 42.0	–	B32776E5456K000	21.0	4.4	32.0	2.1	19.7	400
50	33.0 x 48.0 x 42.0	20.3	B32776G5506K000	25.0	3.5	14.0	2.0	18.1	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

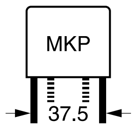
+ = Capacitance tolerance code:

J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for ΔT ≤20 °C at ΔESR_{typ} ≤±5%
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)

Ordering codes and packing units (lead spacing 37.5 mm)



C_R 1) µF	Max. dimensions w x h x l mm	P_1 mm	Ordering code (composition see below)	$I_{RMS,max}$ 2) 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ} 3) nH	tan δ 10^{-3}	tan δ 10^{-3}	Un-taped pcs./ MOQ
$V_{R,70\,°C}$ = 800 V DC, $V_{op,85\,°C}$ = 700 V DC									
6.8	24.0 x 15.0 x 41.5	–	B32776T8685+000	6.0	22.1	18.0	1.7	15.1	1040
8.5	24.0 x 19.0 x 41.5	–	B32776T8855+000	7.5	17.8	18.0	1.7	15.1	780
14	18.0 x 32.5 x 41.5	–	B32776E8146+000	10.0	11.5	23.0	1.8	16.3	720
15	20.0 x 39.5 x 42.0	10.2	B32776G8156+000	12.0	9.6	10.0	1.7	15.2	640
15	20.0 x 39.5 x 42.0	–	B32776E8156+000	11.5	10.3	24.0	1.7	15.7	640
20	28.0 x 37.0 x 42.0	10.2	B32776G8206+000	14.5	7.5	10.0	1.7	15.3	440
20	28.0 x 37.0 x 42.0	–	B32776E8206+000	14.5	7.8	24.0	1.7	15.9	440
20	43.0 x 22.0 x 41.5	20.3	B32776T8206K000*	14.5	7.2	9.0	1.7	15.1	280
22	28.0 x 37.0 x 42.0	10.2	B32776G8226+000	15.5	6.8	11.0	1.7	15.3	440
22	28.0 x 37.0 x 42.0	–	B32776E8226+000	15.0	7.1	25.0	1.7	16.0	440
25	28.0 x 42.5 x 42.0	10.2	B32776G8256+000	17.0	6.1	11.0	1.7	15.4	440
25	28.0 x 42.5 x 42.0	–	B32776E8256+000	16.5	6.4	28.0	1.8	16.3	440
30	30.0 x 45.0 x 42.0	20.3	B32776G8306+000	19.5	5.1	12.0	1.7	15.6	400
30	30.0 x 45.0 x 42.0	–	B32776E8306+000	19.0	5.5	30.0	1.8	16.7	400
35	33.0 x 48.0 x 42.0	20.3	B32776G8356+000	22.0	4.3	14.0	1.7	15.7	180
$V_{R,70\,°C}$ = 900 V DC, $V_{op,85\,°C}$ = 800 V DC									
5	24.0 x 15.0 x 41.5	–	B32776T9505+000	5.5	26.1	19.0	1.5	13.4	1040
7.5	24.0 x 19.0 x 41.5	–	B32776T9755K000	7.5	17.8	18.0	1.5	13.5	780
15	20.0 x 39.5 x 42.0	10.2	B32776G9156K000	12.5	9.1	12.0	1.5	13.6	640
15	20.0 x 39.5 x 42.0	–	B32776E9156K000	12.0	9.4	28.0	1.5	14.1	640
16	43.0 x 22.0 x 41.5	20.3	B32776T9166K000*	14.0	8.1	9.0	1.5	13.5	280
20	28.0 x 37.0 x 42.0	10.2	B32776G9206K000	15.0	7.0	11.0	1.5	13.6	440
20	28.0 x 37.0 x 42.0	–	B32776E9206K000	15.0	7.3	26.0	1.6	14.2	440
22	28.0 x 42.5 x 42.0	10.2	B32776G9226K000	17.0	6.3	12.0	1.5	13.7	440
22	28.0 x 42.5 x 42.0	–	B32776E9226K000	16.5	6.6	29.0	1.6	14.5	440
25	30.0 x 45.0 x 42.0	20.3	B32776G9256+000	19.0	5.5	13.0	1.5	13.8	400
25	30.0 x 45.0 x 42.0	–	B32776E9256+000	18.5	5.9	32.0	1.6	14.7	400
30	33.0 x 48.0 x 42.0	20.3	B32776G9306+000	21.5	4.7	14.0	1.5	13.9	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

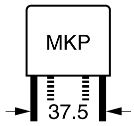
\+ = Capacitance tolerance code:

J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)
* This part is affected by "Dual Use" regulations according to the law of the country the production site is located in. Deliveries of such products are subject to prior approval of the respective local authorities based on customer declarations. The delivery to certain countries may be restricted.

Ordering codes and packing units (lead spacing 37.5 mm)



C_R 1) µF	Max. dimensions w x h x l mm	P_1 mm	Ordering code (composition see below)	$I_{RMS,max}$ 2) 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ} 3) nH	tan δ 10^{-3}	tan δ 10^{-3}	Un-taped pcs./ MOQ
$V_{R,70\ °C}$ = 1100 V DC, $V_{op,85\ °C}$ = 920 V DC									
3.9	24.0 x 15.0 x 41.5	–	B32776T0395+000	5.0	30.5	18.0	1.4	12.1	1040
5	24.0 x 19.0 x 41.5	–	B32776T0505+000	6.5	23.6	18.0	1.4	12.1	780
12	20.0 x 39.5 x 42.0	10.2	B32776G0126+000	12.0	10.2	12.0	1.4	12.2	640
12	20.0 x 39.5 x 42.0	–	B32776E0126+000	11.5	10.5	28.0	1.4	12.6	640
13	43.0 x 22.0 x 41.5	20.3	B32776T0136K000*	13.0	8.9	9.0	1.4	12.1	280
14	28.0 x 37.0 x 42.0	10.2	B32776G0146+000	13.5	8.7	21.0	1.4	12.2	440
14	28.0 x 37.0 x 42.0	–	B32776E0146+000	13.5	9.0	25.0	1.4	12.6	440
16	28.0 x 42.5 x 42.0	10.2	B32776G0166+000	15.5	7.4	12.0	1.4	12.3	440
16	28.0 x 42.5 x 42.0	–	B32776E0166+000	15.0	7.8	30.0	1.4	12.9	440
20	30.0 x 45.0 x 42.0	20.3	B32776G0206+000	18.0	6.0	14.0	1.4	12.4	400
20	30.0 x 45.0 x 42.0	–	B32776E0206+000	17.5	6.5	32.0	1.4	13.1	400
22	33.0 x 48.0 x 42.0	20.3	B32776G0226+000	21.0	4.9	15.0	1.3	11.4	180
$V_{R,70\ °C}$ = 1300 V DC, $V_{op,85\ °C}$ = 1100 V DC									
2.7	24.0 x 15.0 x 41.5	–	B32776T1275+000	5.0	34.7	19.0	1.1	9.6	1040
3.5	24.0 x 19.0 x 41.5	–	B32776T1355+000	6.0	27.4	18.0	1.1	9.7	780
8.0	20.0 x 39.5 x 42.0	10.2	B32776G1805+000	11.0	12.1	12.0	1.1	9.7	640
8.0	20.0 x 39.5 x 42.0	–	B32776E1805+000	10.5	12.4	24.0	1.2	10.0	640
9.0	43.0 x 22.0 x 41.5	20.3	B32776T1905K000*	12.0	10.7	9.0	1.1	9.7	280
10	28.0 x 37.0 x 42.0	10.2	B32776G1106+000	13.0	9.6	11.0	1.1	9.7	440
10	28.0 x 37.0 x 42.0	–	B32776E1106+000	12.5	9.9	26.0	1.2	10.0	440
12	28.0 x 42.5 x 42.0	10.2	B32776G1126+000	14.5	8.1	12.0	1.1	9.8	440
12	28.0 x 42.5 x 42.0	–	B32776E1126+000	14.0	8.5	28.0	1.2	10.1	440
14	30.0 x 45.0 x 42.0	20.3	B32776G1146+000	17.0	6.8	14.0	1.1	10.1	400
14	30.0 x 45.0 x 42.0	–	B32776E1146+000	16.5	7.3	32.0	1.2	10.4	400
16	33.0 x 48.0 x 42.0	20.3	B32776G1166+000	19.0	6.0	15.0	1.1	9.9	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

\+ = Capacitance tolerance code:

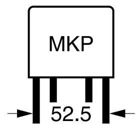
J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for ΔT ≤20 °C at ΔESR_{typ} ≤±5%
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)

* This part is affected by "Dual Use" regulations according to the law of the country the production site is located in. Deliveries of such products are subject to prior approval of the respective local authorities based on customer declarations. The delivery to certain countries may be restricted.

Ordering codes and packing units (lead spacing 52.5 mm, P_1 = 20.3 mm)



C_R[1)] µF	Max. dimensions w x h x l mm	Ordering code (composition see below)	$I_{RMS,max}$[2)] 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ}[3)] nH	tan δ 10^{-3}	tan δ 10^{-3}	Un-taped pcs./ MOQ
$V_{R,70\,°C}$ = 450 V DC, $V_{op,85\,°C}$ = 450 V DC								
55	43.0 x 24.0 x 57.5	B32778T4556K000	16.5	7.2	13.0	4.3	41.7	560
75	30.0 x 45.0 x 57.5	B32778G4756+000	21.0	5.6	12.0	4.4	42.6	280
80	30.0 x 45.0 x 57.5	B32778G4806+000	21.5	5.3	13.0	4.4	42.7	280
100	35.0 x 50.0 x 57.5	B32778G4107+000	26.0	4.3	14.0	4.5	43.3	108
110	35.0 x 50.0 x 57.5	B32778G4117K000	27.0	3.9	15.0	4.5	43.6	108
150	130.0 x 24.0 x 57.5	B32778J4157K000	43.5	2.7	4.0	4.4	42.1	80
170	45.0 x 57.0 x 57.5	B32778G4177+000	36.5	2.6	17.0	4.6	45.7	140
180	60.0 x 45.0 x 57.5	B32778G4187+000	39.0	2.5	19.0	4.6	44.6	200
480	130.0 x 58.0 x 57.5	B32778J4487K000	79.5	0.9	6.0	4.8	45.4	40
$V_{R,70\,°C}$ = 575 V DC, $V_{op,85\,°C}$ = 500 V DC								
40	43.0 x 24.0 x 57.5	B32778T5406K000	15.5	8.5	13.0	3.6	34.5	560
60	30.0 x 45.0 x 57.5	B32778G5606+000	20.5	5.8	13.0	3.7	35.3	280
80	35.0 x 50.0 x 57.5	B32778G5806+000	25.5	4.4	15.0	3.7	36.0	108
110	130.0 x 24.0 x 57.5	B32778J5117K000	40.5	3.0	5.0	3.6	34.5	80
120	45.0 x 57.0 x 57.5	B32778G5127+000	34.5	3.1	17.0	3.8	37.2	140
130	60.0 x 45.0 x 57.5	B32778G5137+000	36.5	2.8	19.0	3.8	36.7	200
360	130.0 x 58.0 x 57.5	B32778J5367K000	75.0	1.0	6.0	4.0	37.3	40

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

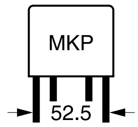
+ = Capacitance tolerance code:

J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)

Ordering codes and packing units (lead spacing 52.5 mm, P_1 = 20.3 mm)



C_R 1) µF	Max. dimensions w x h x l mm	Ordering code (composition see below)	$I_{RMS,max}$ 2) 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ} 3) nH	tan δ 10^{-3}	tan δ 10^{-3}	Un-taped pcs./ MOQ
$V_{R,70\,°C}$ = 800 V DC, $V_{op,85\,°C}$ = 700 V DC								
30	43.0 x 24.0 x 57.5	B32778T8306K000*	14.5	9.8	9.0	3.2	30.2	560
45	30.0 x 45.0 x 57.5	B32778G8456+000	19.5	6.6	14.0	3.2	30.9	280
50	30.0 x 45.0 x 57.5	B32778G8506+000	20.0	6.3	13.0	3.2	30.9	280
55	35.0 x 50.0 x 57.5	B32778G8556+000	23.0	5.6	14.0	3.2	31.1	108
60	35.0 x 50.0 x 57.5	B32778G8606+000	23.5	5.1	15.0	3.3	31.2	108
80	130.0 x 24.0 x 57.5	B32778J8806K000*	37.5	3.6	4.0	3.2	30.2	80
90	45.0 x 57.0 x 57.5	B32778G8906+000	32.5	3.5	17.0	3.3	32.2	140
100	60.0 x 45.0 x 57.5	B32778G8107+000	34.5	3.2	19.0	3.3	31.9	200
270	130.0 x 58.0 x 57.5	B32778J8277K000*	70.5	1.2	6.0	3.5	32.4	40
$V_{R,70\,°C}$ = 900 V DC, $V_{op,85\,°C}$ = 800 V DC								
25	43.0 x 24.0 x 57.5	B32778T9256K000*	13.5	10.7	9.0	2.8	26.8	560
35	30.0 x 45.0 x 57.5	B32778G9356+000	18.0	7.7	13.0	2.9	27.3	280
50	35.0 x 50.0 x 57.5	B32778G9506K000	22.5	5.6	15.0	2.9	27.7	108
70	45.0 x 57.0 x 57.5	B32778G9706+000	31.0	3.8	18.0	3.0	28.5	140
70	130.0 x 24.0 x 57.5	B32778J9706K000*	36.0	3.8	4.0	2.9	27.2	80
75	60.0 x 45.0 x 57.5	B32778G9756+000	32.5	3.6	20.0	2.9	28.2	200
210	130.0 x 58.0 x 57.5	B32778J9217K000*	66.0	1.3	6.0	3.1	28.6	40

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

+ = Capacitance tolerance code:

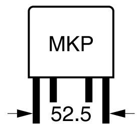
J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)

* This part is affected by "Dual Use" regulations according to the law of the country the production site is located in. Deliveries of such products are subject to prior approval of the respective local authorities based on customer declarations. The delivery to certain countries may be restricted.

Ordering codes and packing units (lead spacing 52.5 mm, P1 = 20.3 mm)



C_R[1] µF	Max. dimensions w x h x l mm	Ordering code (composition see below)	$I_{RMS,max}$[2] 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ}[3] nH	tan δ 10^{-3}	tan δ 10^{-3}	Un-taped pcs./ MOQ
$V_{R,70\,°C}$ = 1100 V DC, $V_{op,85\,°C}$ = 920 V DC								
20	43.0 x 24.0 x 57.5	B32778T0206K000*	13.0	11.9	9.0	2.6	24.1	560
30	30.0 x 45.0 x 57.5	B32778G0306+000	17.5	8.2	13.0	2.6	24.5	280
40	35.0 x 50.0 x 57.5	B32778G0406+000	21.5	6.2	15.0	2.7	25.9	108
58	45.0 x 57.0 x 57.5	B32778G0586+000	29.0	4.3	17.0	2.7	25.4	140
60	60.0 x 45.0 x 57.5	B32778G0606+000	30.5	4.0	19.0	2.7	25.2	200
60	130.0 x 24.0 x 57.5	B32778J0606K000*	34.5	4.1	4.0	2.7	25.1	80
200	130.0 x 58.0 x 57.5	B32778J0207K000*	66.0	1.4	6.0	3.0	26.8	40
$V_{R,70\,°C}$ = 1300 V DC, $V_{op,85\,°C}$ = 1100 V DC								
14	43.0 x 24.0 x 57.5	B32778T1146K000*	12.0	13.8	9.0	2.1	19.5	560
20	30.0 x 45.0 x 57.5	B32778G1206+000	16.0	9.7	13.0	2.1	19.8	280
25	35.0 x 50.0 x 57.5	B32778G1256+000	19.0	7.8	15.0	2.1	19.9	108
27	35.0 x 50.0 x 57.5	B32778G1276+000	19.5	7.3	15.0	2.1	20.0	108
38	130.0 x 24.0 x 57.5	B32778J1386K000*	31.5	5.1	4.0	2.1	19.5	80
40	45.0 x 57.0 x 57.5	B32778G1406+000	26.5	5.0	17.0	2.2	20.3	140
42	60.0 x 45.0 x 57.5	B32778G1426+000	28.0	4.7	19.0	2.2	20.2	200
120	130.0 x 58.0 x 57.5	B32778J1127K000*	58.5	1.7	6.0	2.3	20.5	40

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further intermediate capacitance values are available on request.

Composition of ordering code

+ = Capacitance tolerance code:

J = ±5%
K = ±10%

Packing code:
000 = untaped (lead length 6 –1 mm)

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z versus frequency)

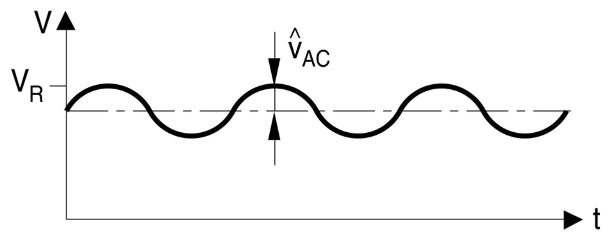
* This part is affected by "Dual Use" regulations according to the law of the country the production site is located in. Deliveries of such products are subject to prior approval of the respective local authorities based on customer declarations. The delivery to certain countries may be restricted.

Technical data

Reference standard: IEC 61071:2007. All data given at T = 20 °C, unless otherwise specified.

Operating temperature range (case)	Max. operating temperature, $T_{op,max}$ +105 °C Upper category temperature T_{max} +105 °C Lower category temperature T_{min} –40 °C					
Insulation resistance R_{ins} given as time constant $\tau = C_R \cdot R_{ins}$, rel. humidity ≤ 65% (minimum as-delivered values)	τ > 10 000 s (after 1 min) For V_R ≥500 V measured at 500 V For V_R <500 V measured at V_R					
DC test voltage between terminals (10 s)	$1.5 \cdot V_R$					
Voltage test terminal to case (10 s)	2110 V AC, 50 Hz					
Pulse Handling Capability (V/µs)	I_P (A) / C (µF)					
Reliability: Failure rate λ	10 fit (≤ $10 \cdot 10^{-9}$/h) at $0.5 \cdot V_R$, 40 °C For conversion to other operating conditions and temperatures, refer to chapter "Quality, 2 Reliability".					
Service life t_{SL}	100 000 h at V_R and 70 °C					
V_R (V DC)	450	575	800	900	1100	1300
Continuous operating voltage V_{op} (V DC) at 70 °C	450	575	800	900	1100	1300
Continuous operating voltage V_{op} (V DC) at 85 °C	450	500	700	800	920	1100
For temperatures between 85 °C and 105 °C	1.33%/°C of V_{op} derating compared to V_{op} at 85 °C					

Typical waveforms



KLK1635-E

KLK1267-S

Restrictions:
V_R: Maximum operating peak voltage of either polarity but of a non-reversing waveform, for which the capacitor has been designed for continuous operation.

$\hat{v}_{AC} \leq 0.2 \cdot V_R$

Overvoltage	Maximum duration within one day	Observation
$1.1 \cdot V_R$	30% of on-load duration	System regulation
$1.15 \cdot V_R$	30 min	System regulation
$1.2 \cdot V_R$	5 min	System regulation
$1.3 \cdot V_R$	1 min	System regulation

NOTE 1 An overvoltage equal to $1.5 \cdot V_R$ for 30 ms is permitted 1000 times during the life of the capacitor.

The amplitudes of the overvoltages that may be tolerated without significant reduction in the life time of the capacitor depend on their duration, the number of application and the capacitor temperature.

In addition these values assume that the overvoltages may appear when the internal temperature of the capacitor is less than 0 °C but within the temperature category.

NOTE 2 The average applied voltage must not be higher than the specified voltage.

Pulse handling capability

"dV/dt" represents the maximum permissible voltage change per unit of time for non-sinusoidal voltages, expressed in V/µs.

Note:

The values of dV/dt provided below must not be exceeded in order to avoid damaging the capacitor.

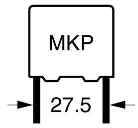
dV/dt values

Lead spacing	27.5 mm				37.5 mm					
Type	B32774				B32776					
V_R (V DC)	450	800	1100	1300	450	575	800	900	1100	1300
dV/dt in V/µs	30	40	75	100	21	22	22	35	54	73

Lead spacing	52.5 mm					
Type	B32778					
V_R (V DC)	450	575	800	900	1100	1300
dV/dt in V/µs	14	14	15	22	35	50

Characteristics curves

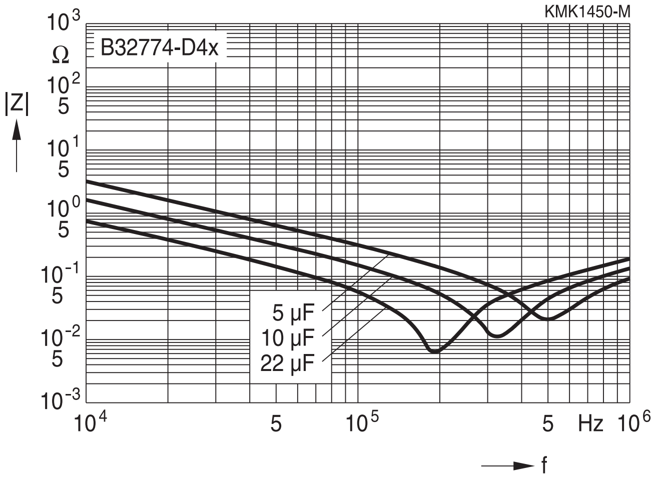
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 27.5 mm

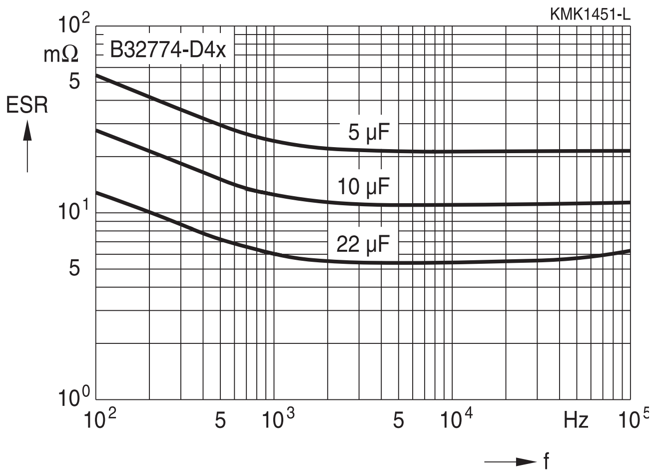
450 V DC



ESR versus frequency f
(typical values)

Lead spacing 27.5 mm

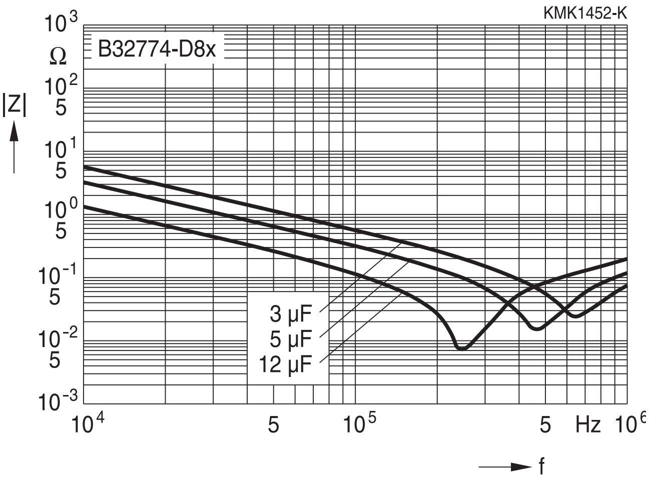
450 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 27.5 mm

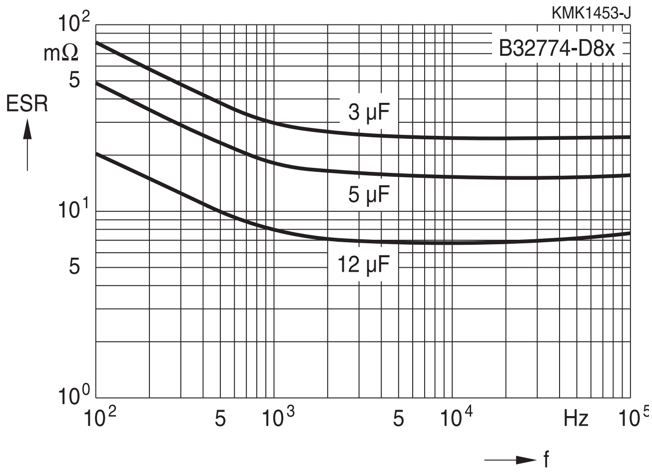
800 V DC



ESR versus frequency f
(typical values)

Lead spacing 27.5 mm

800 V DC



Characteristics curves

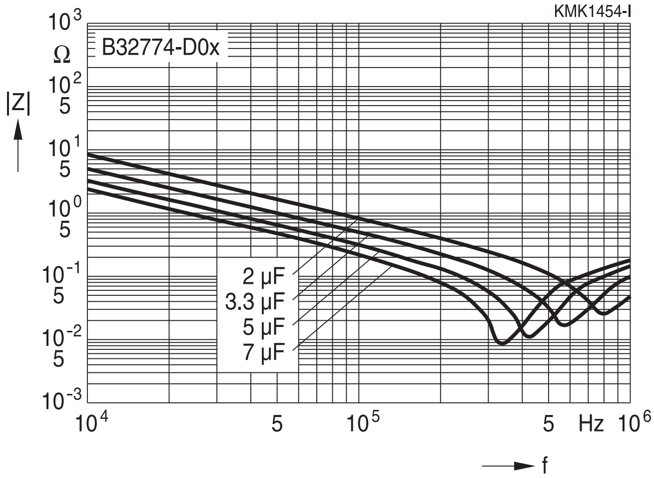
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.

MKP
27.5

Impedance Z versus frequency f
(typical values)

Lead spacing 27.5 mm

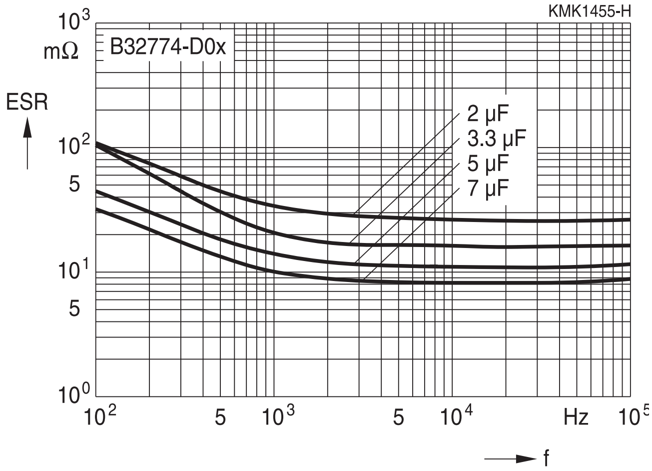
1100 V DC



ESR versus frequency f
(typical values)

Lead spacing 27.5 mm

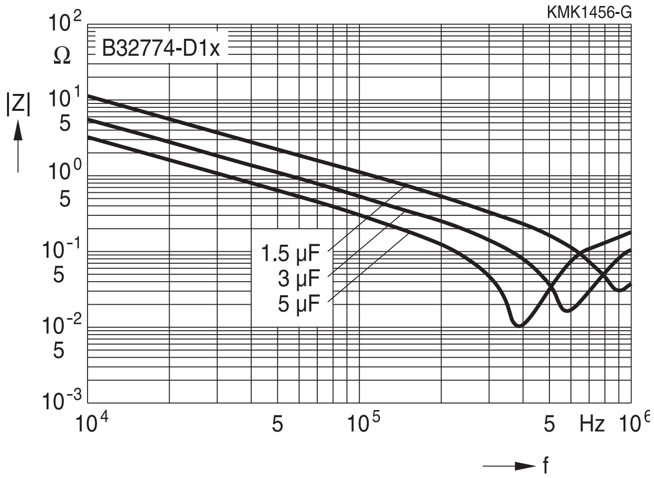
1100 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 27.5 mm

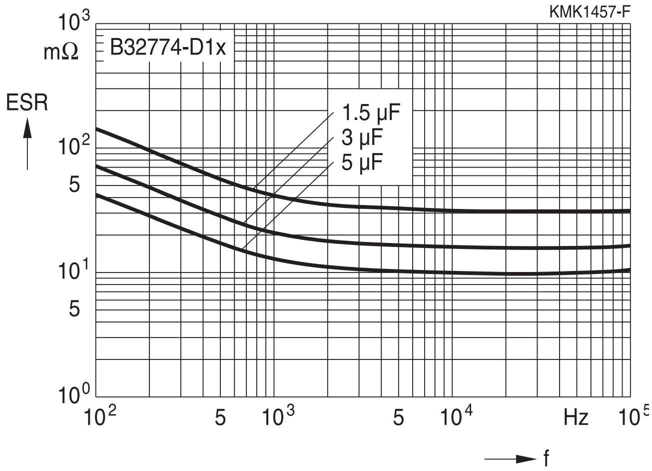
1300 V DC



ESR versus frequency f
(typical values)

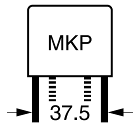
Lead spacing 27.5 mm

1300 V DC



Characteristics curves

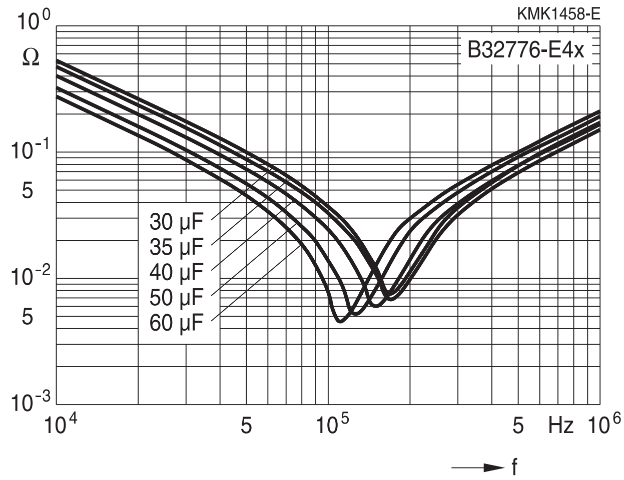
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

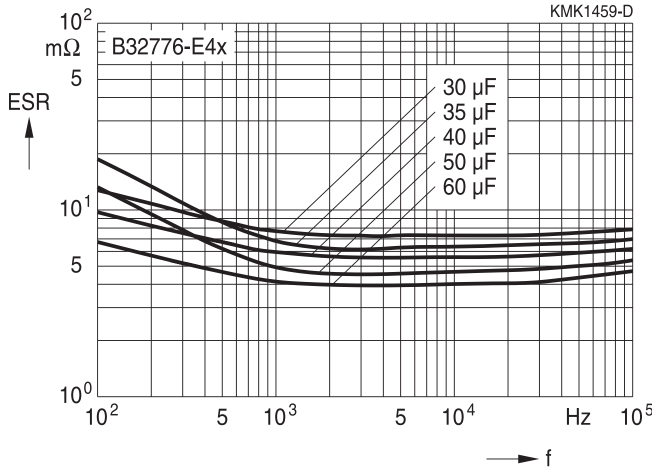
450 V DC



ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

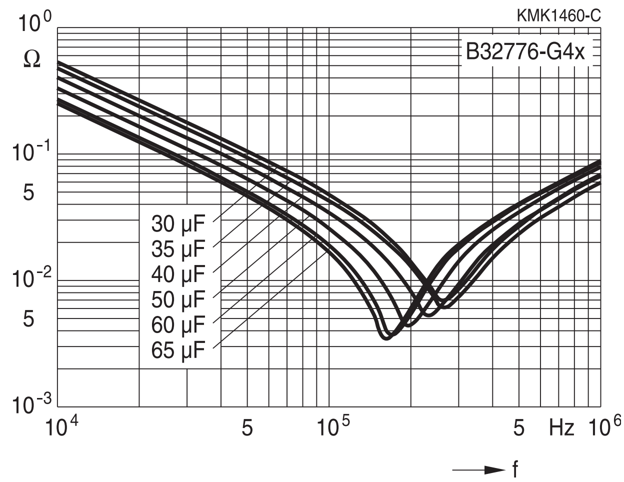
450 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

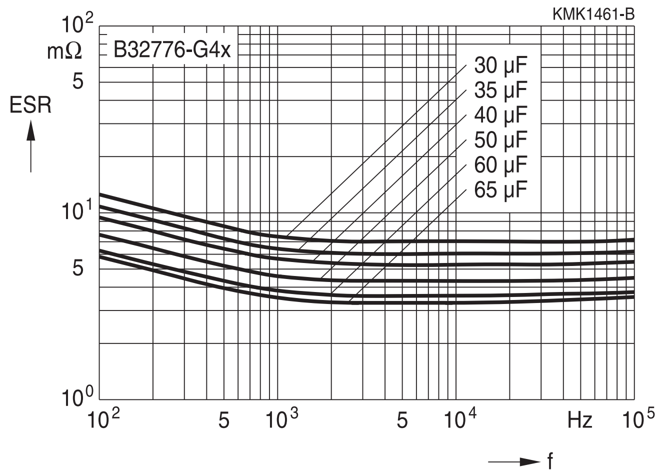
450 V DC



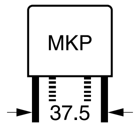
ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

450 V DC



Characteristics curves

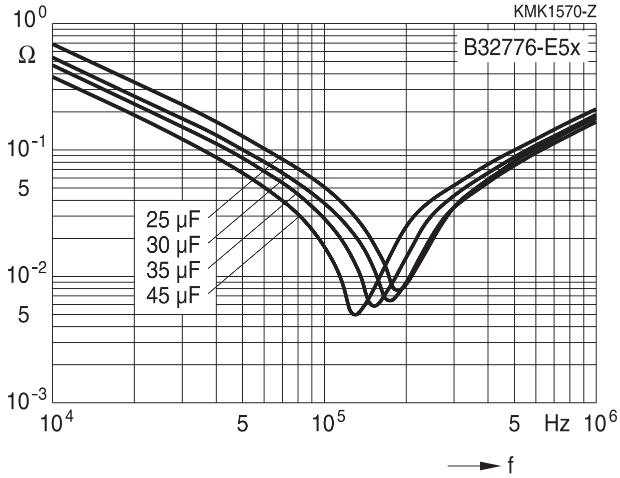


Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.

Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

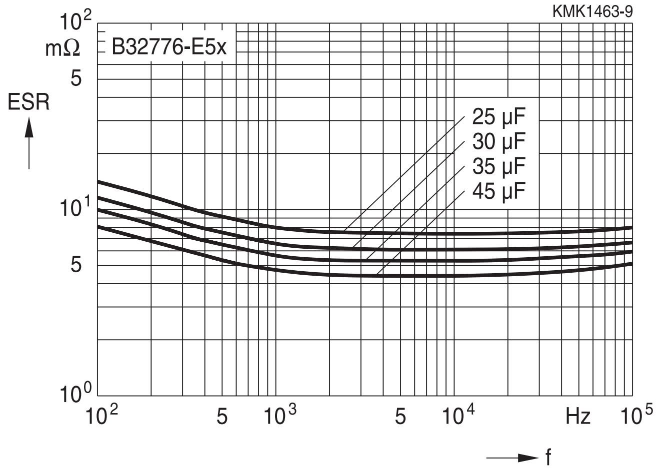
575 V DC



ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

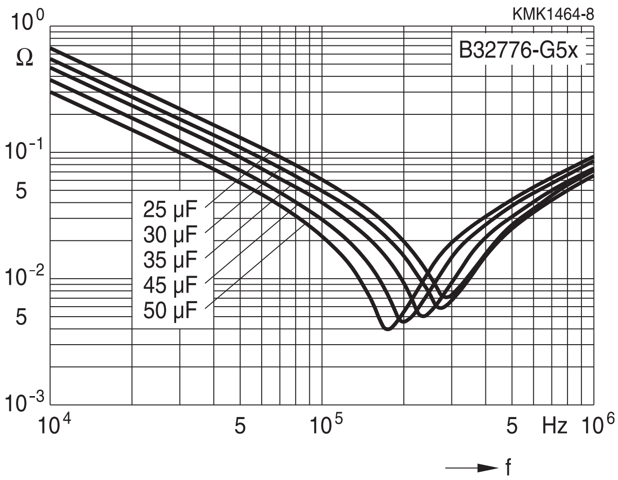
575 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

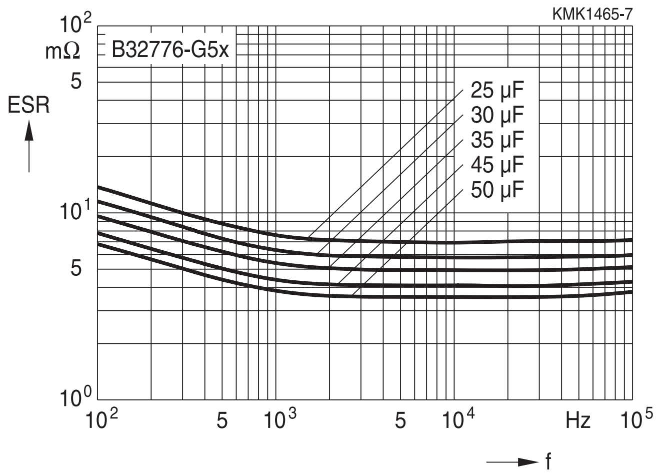
575 V DC



ESR versus frequency f
(typical values)

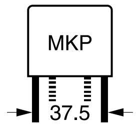
Lead spacing 37.5 mm

575 V DC



Characteristics curves

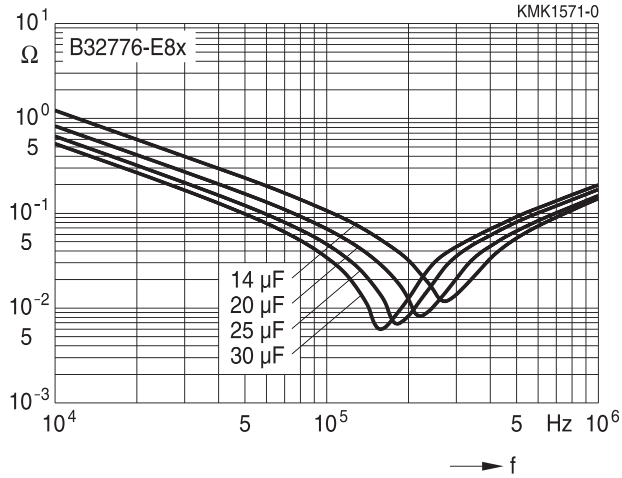
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

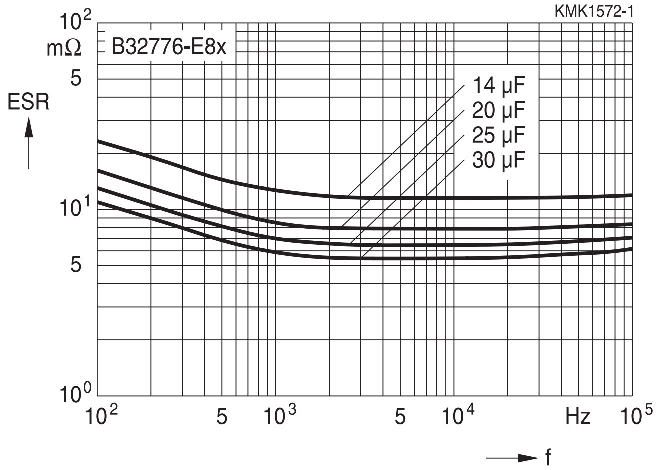
B32776E8*/800 V DC



ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

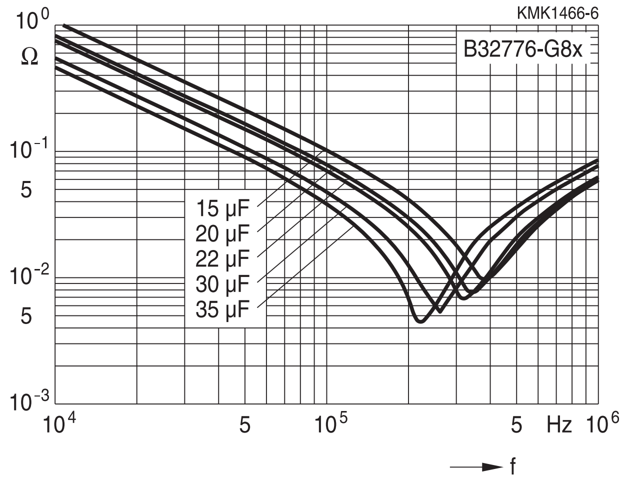
B32776E8*/800 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

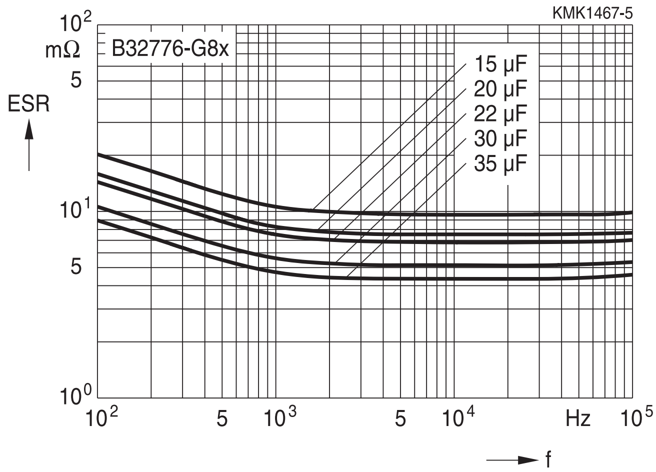
800 V DC



ESR versus frequency f
(typical values)

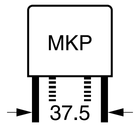
Lead spacing 37.5 mm

800 V DC



Characteristics curves

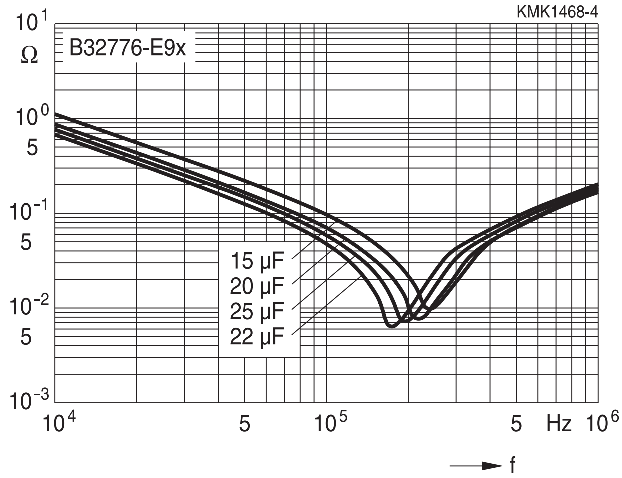
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

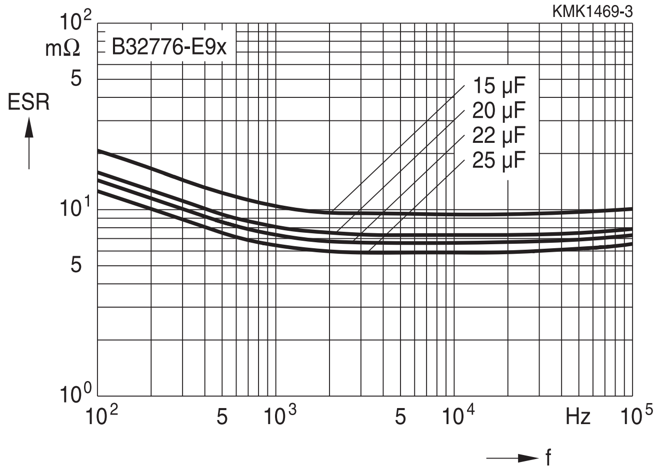
900 V DC



ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

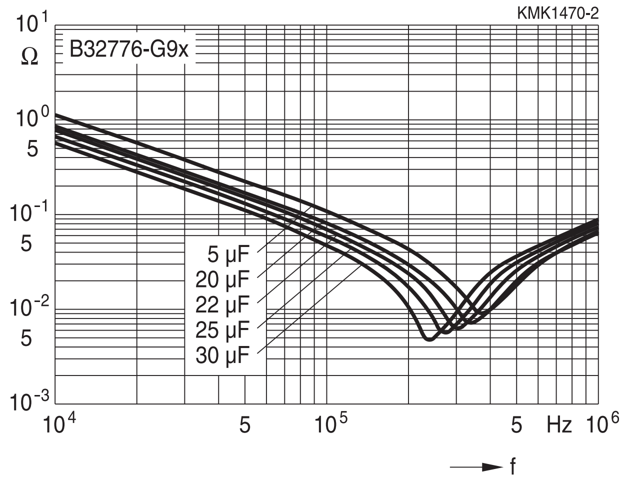
900 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

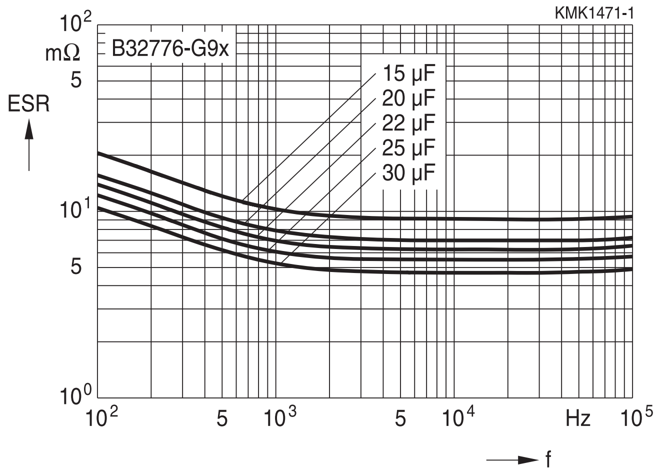
900 V DC



ESR versus frequency f
(typical values)

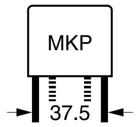
Lead spacing 37.5 mm

900 V DC



Characteristics curves

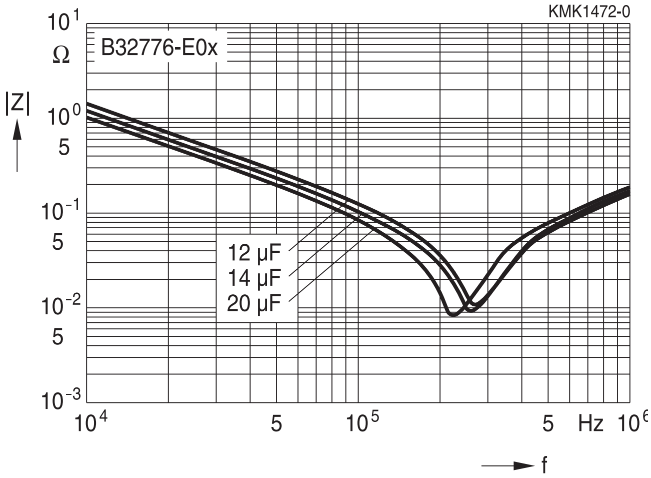
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

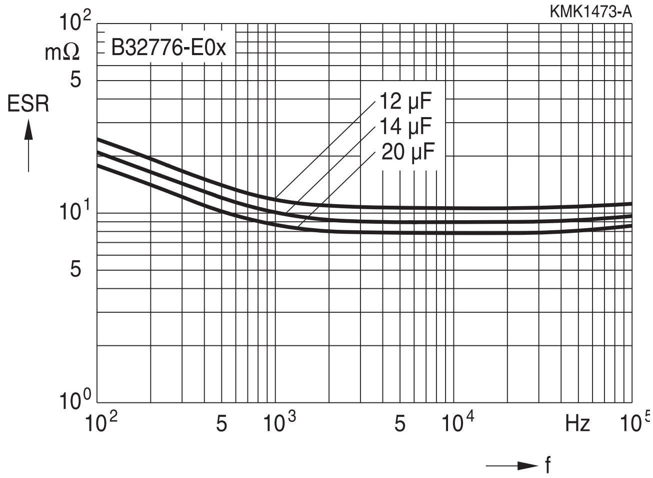
1100 V DC



ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

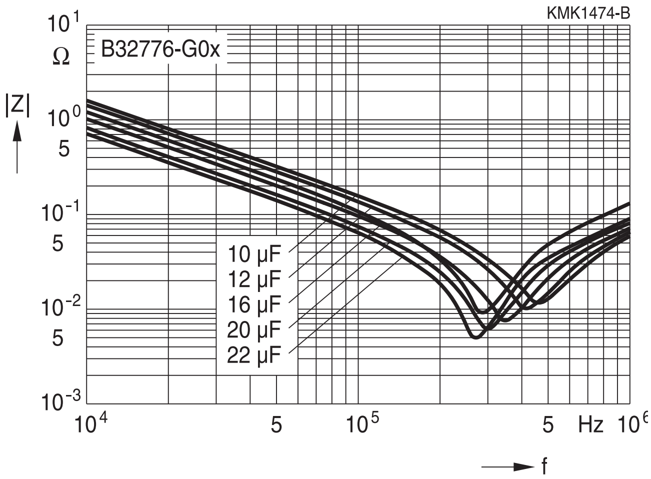
1100 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

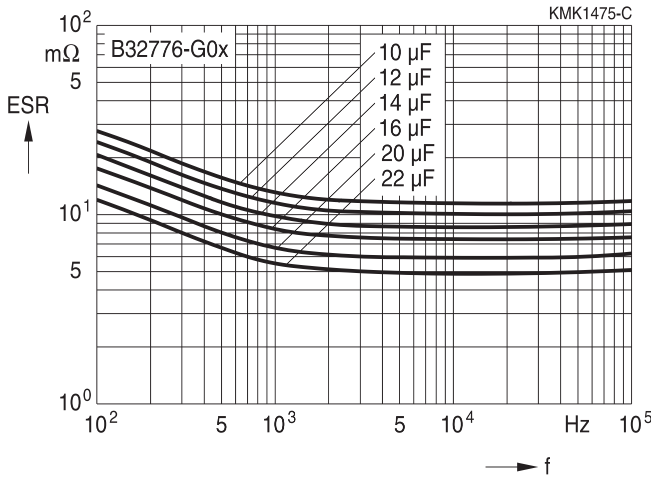
1100 V DC



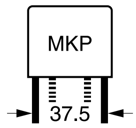
ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

1100 V DC



Characteristics curves

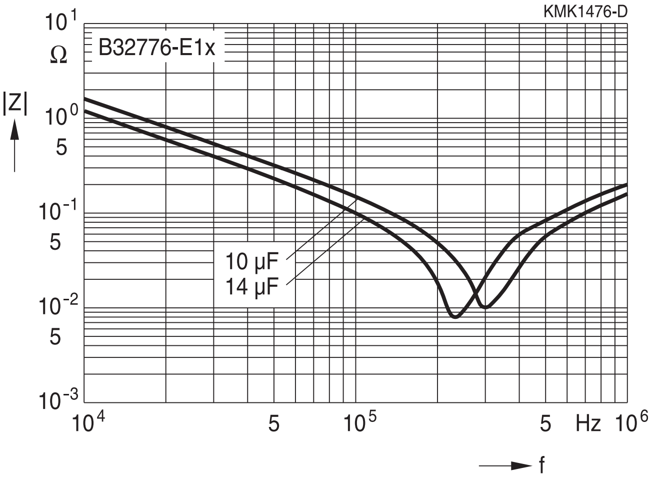


Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.

Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

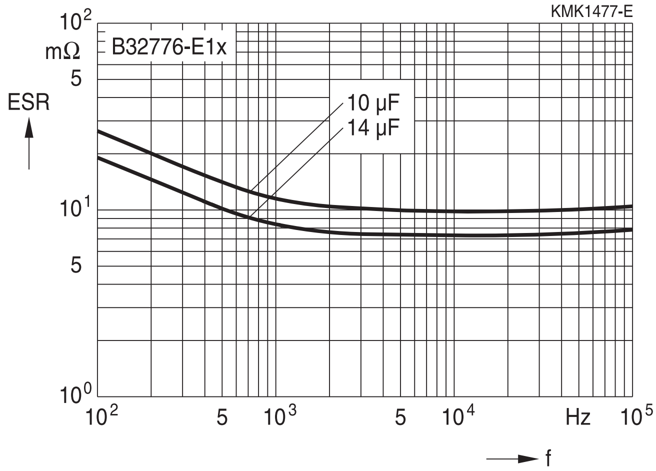
1300 V DC



ESR versus frequency f
(typical values)

Lead spacing 37.5 mm

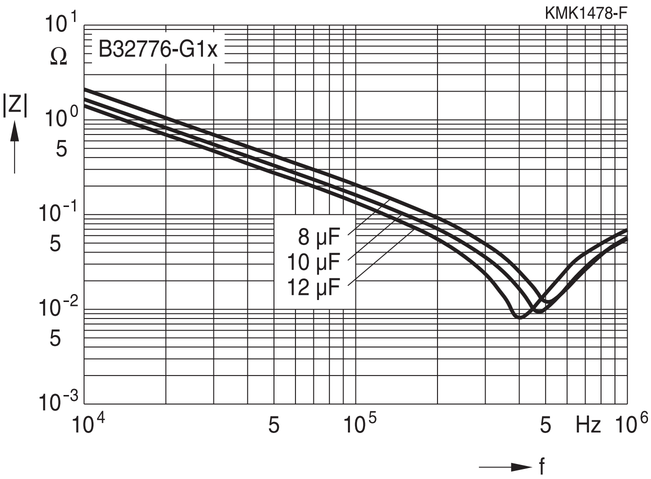
1300 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm

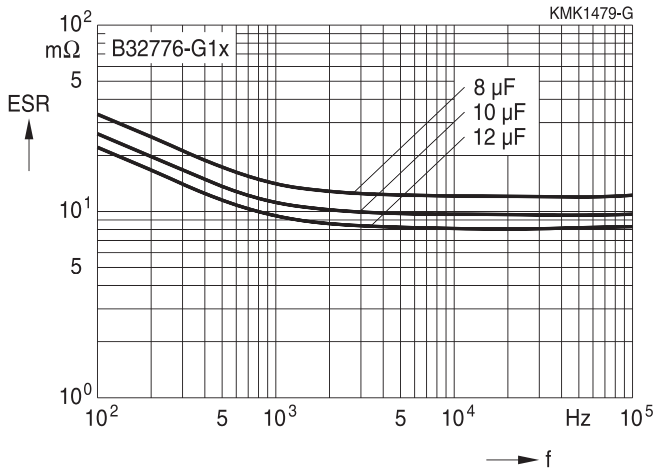
1300 V DC



ESR versus frequency f
(typical values)

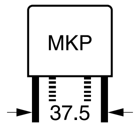
Lead spacing 37.5 mm

1300 V DC



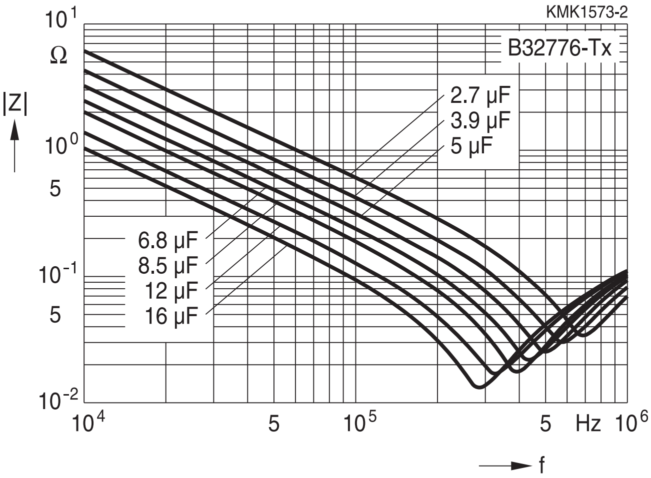
Characteristics curves

Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



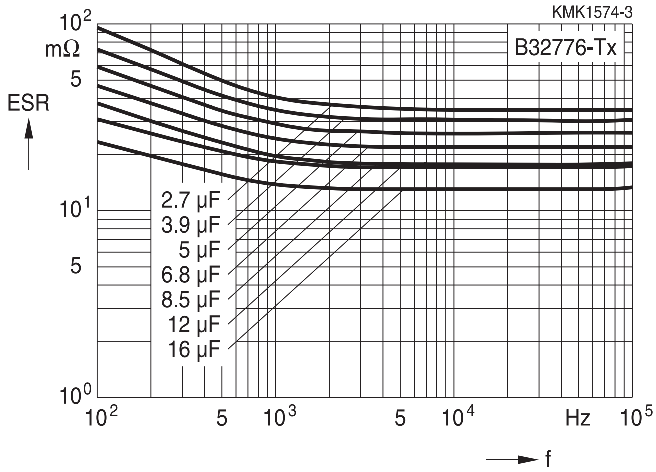
Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm (low profile, 2 pins)



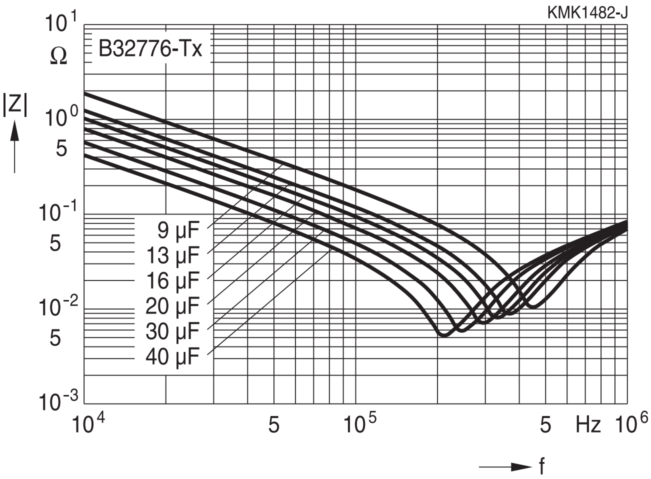
ESR versus frequency f
(typical values)

Lead spacing 37.5 mm (low profile, 2 pins)



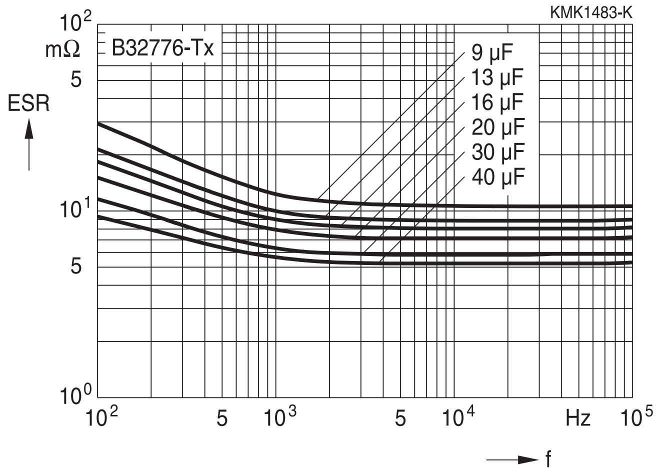
Impedance Z versus frequency f
(typical values)

Lead spacing 37.5 mm (low profile, 4 pins)

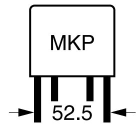


ESR versus frequency f
(typical values)

Lead spacing 37.5 mm (low profile, 4 pins)



Characteristics curves

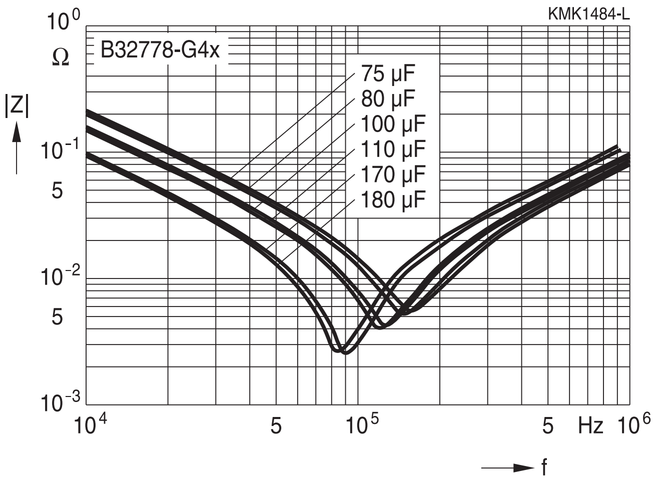


Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.

Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm

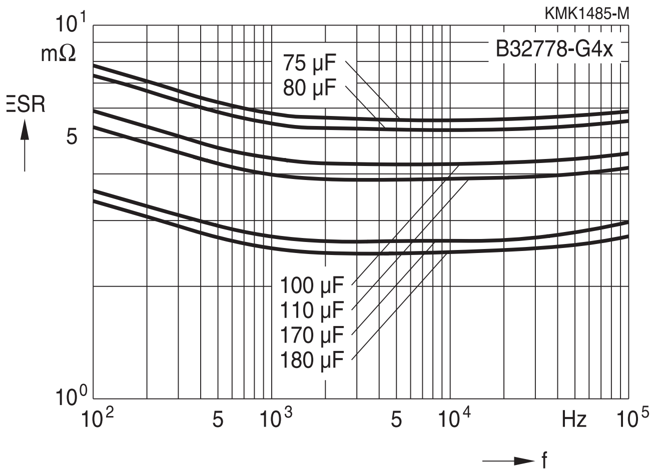
450 V DC



ESR versus frequency f
(typical values)

Lead spacing 52.5 mm

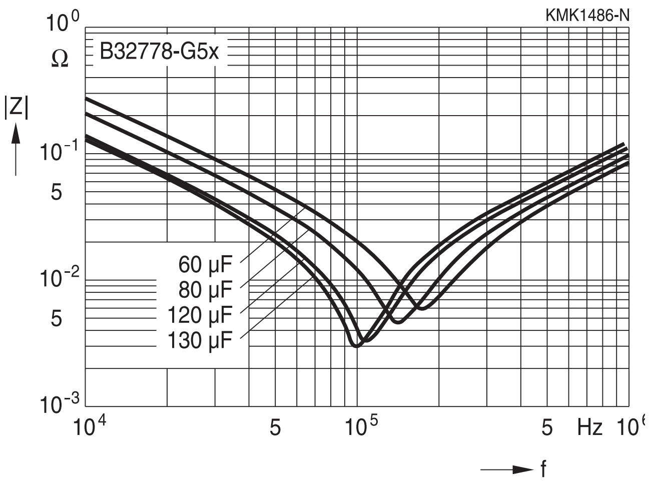
450 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm

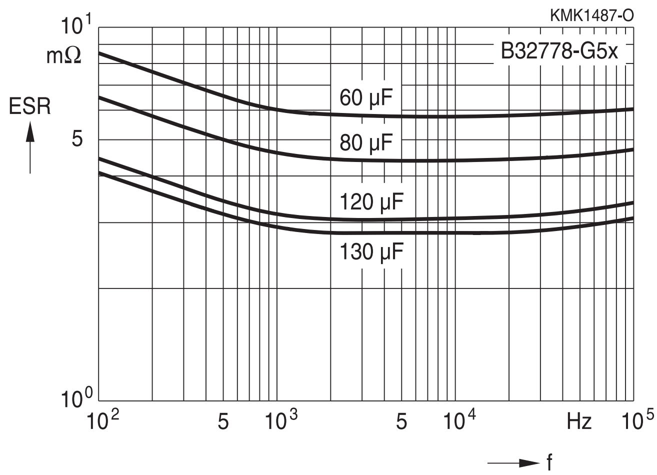
575 V DC



ESR versus frequency f
(typical values)

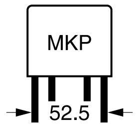
Lead spacing 52.5 mm

575 V DC



Characteristics curves

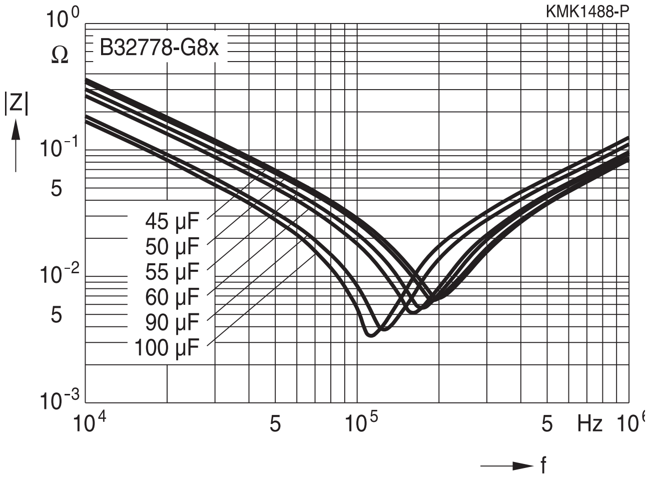
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm

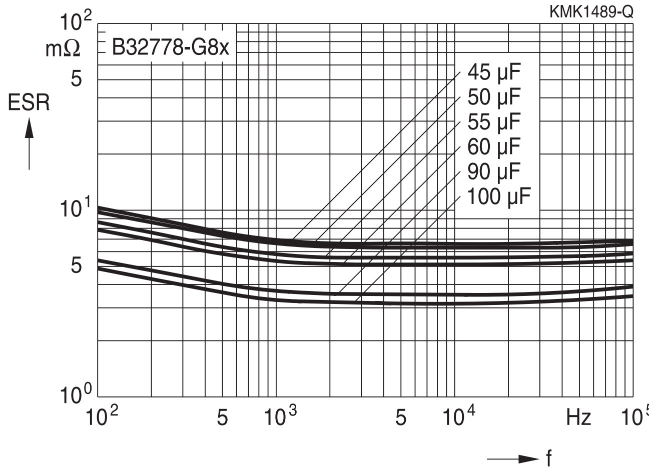
800 V DC



ESR versus frequency f
(typical values)

Lead spacing 52.5 mm

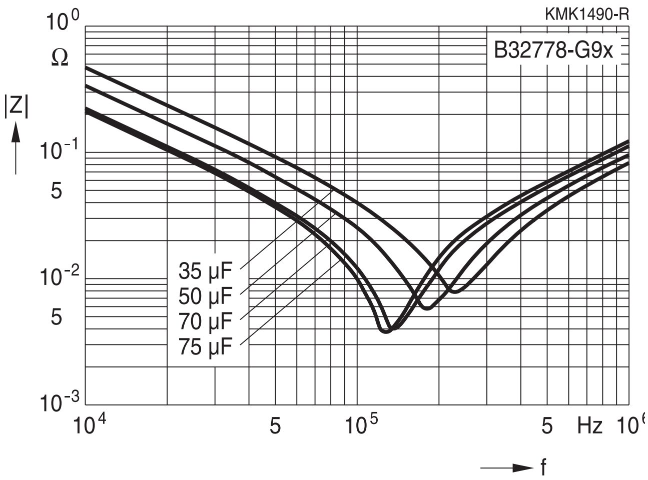
800 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm

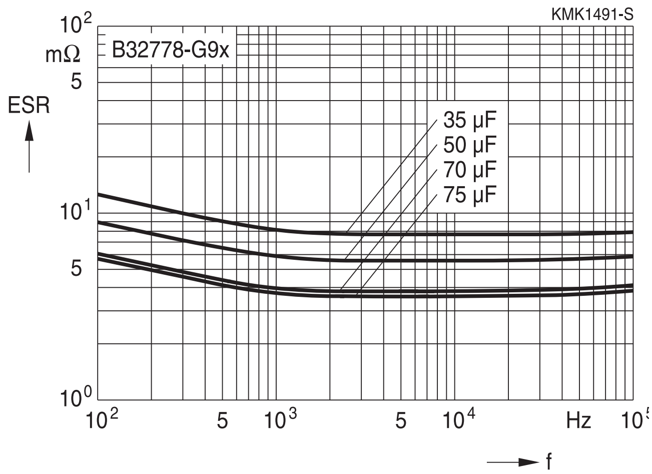
900 V DC



ESR versus frequency f
(typical values)

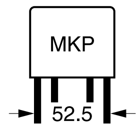
Lead spacing 52.5 mm

900 V DC



Characteristics curves

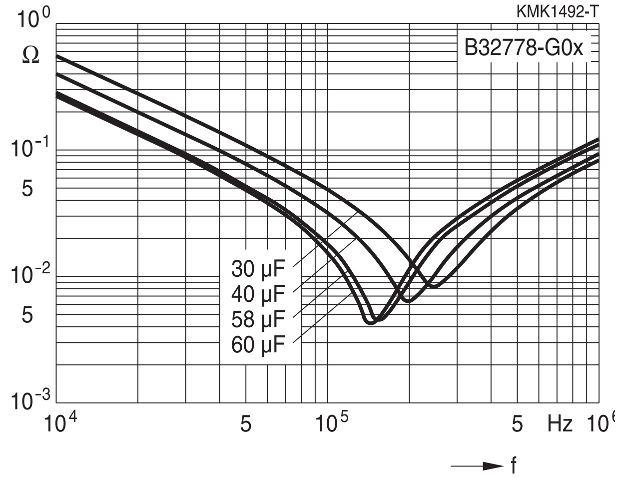
Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.



Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm

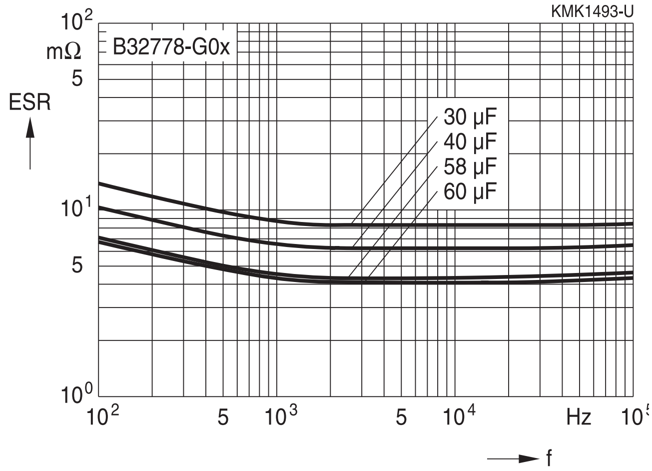
B32778G0*/1100 V DC



ESR versus frequency f
(typical values)

Lead spacing 52.5 mm

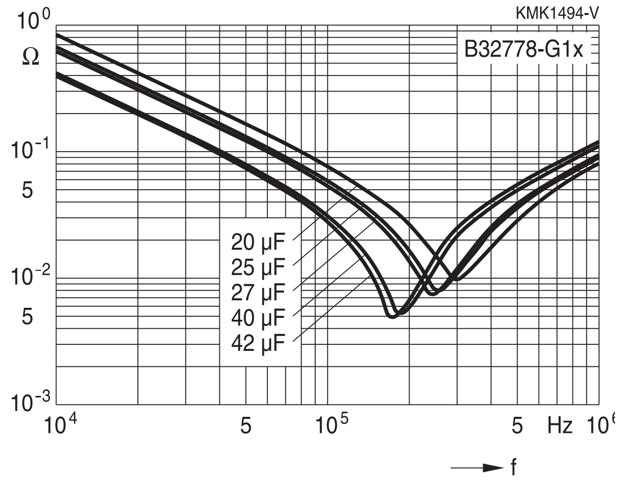
B32778G0*/1100 V DC



Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm

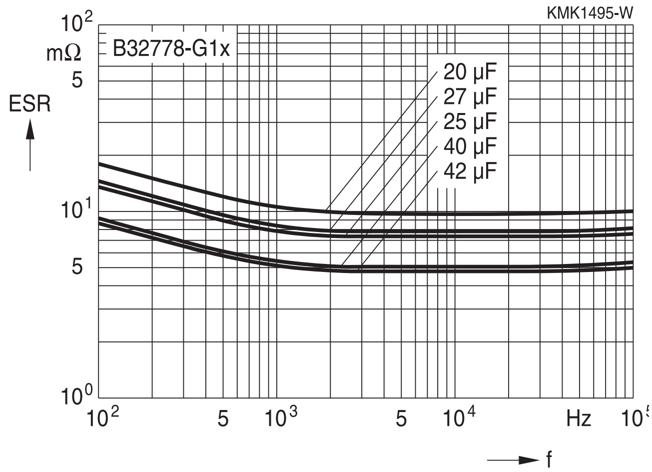
1300 V DC



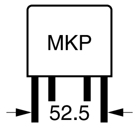
ESR versus frequency f
(typical values)

Lead spacing 52.5 mm

1300 V DC



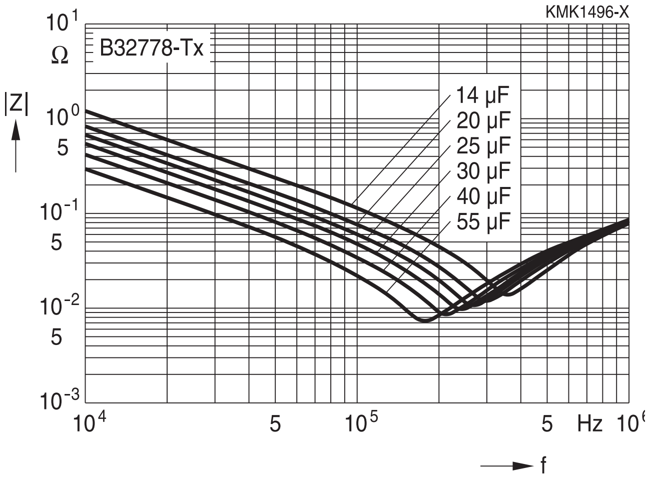
Characteristics curves



Additional technical information can be found under "Design support" on www.tdk-electronics.tdk.com.

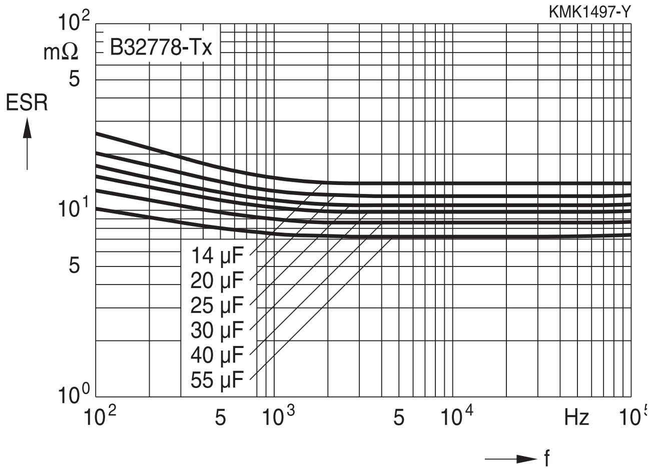
Impedance Z versus frequency f
(typical values)

Lead spacing 52.5 mm (low profile)



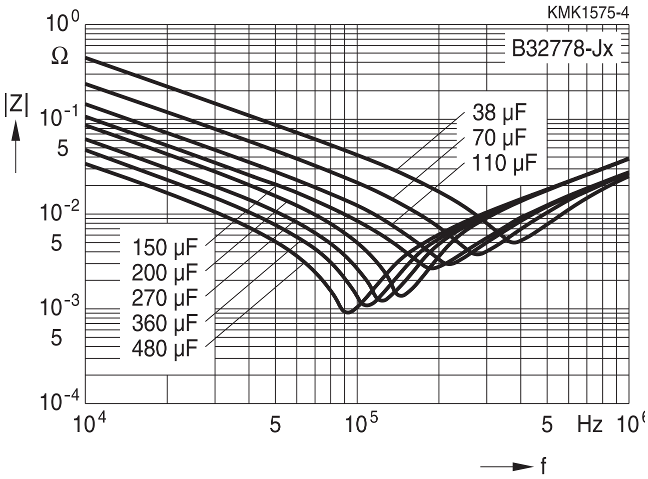
ESR versus frequency f
(typical values)

Lead spacing 52.5 mm (low profile)



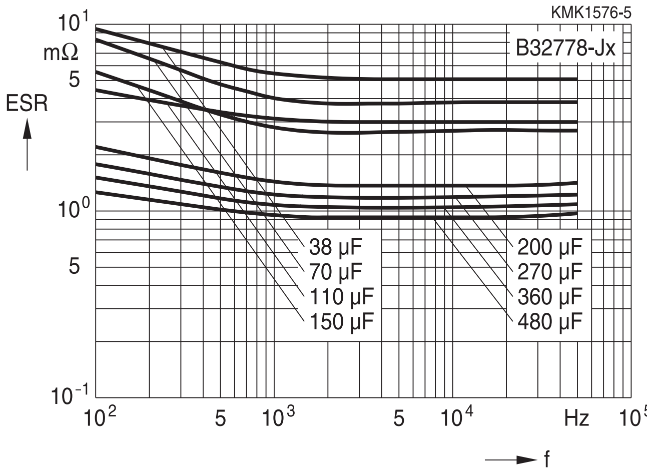
Impedance Z versus frequency f
(typical values)

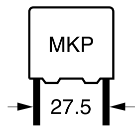
Lead spacing 52.5 mm (12 pins)



ESR versus frequency f
(typical values)

Lead spacing 52.5 mm (12 pins)



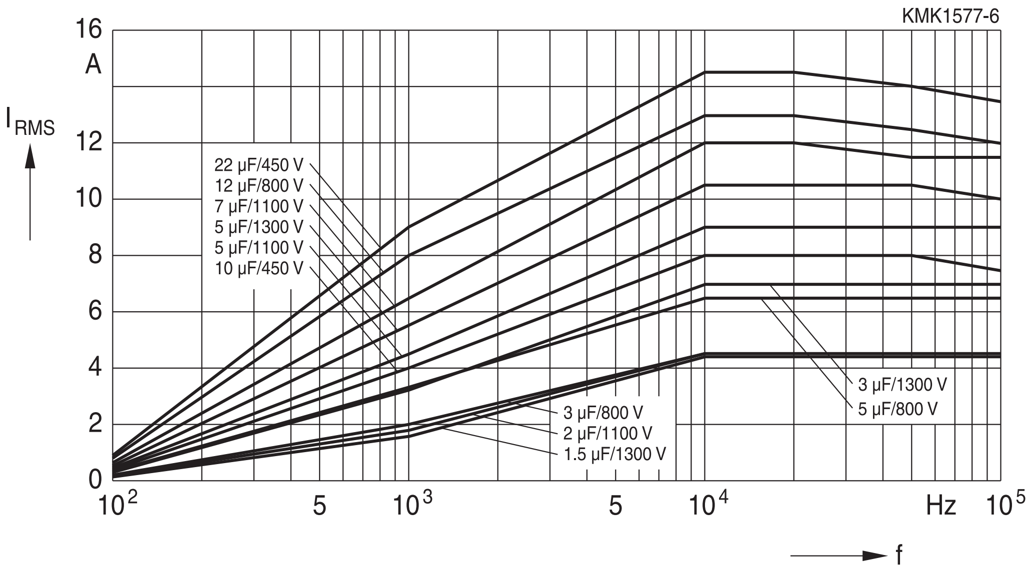


Characteristics curves

Permissible current I_{RMS} versus frequency f at 70 °C

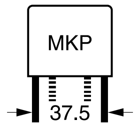
Lead spacing 27.5 mm

B32774D*



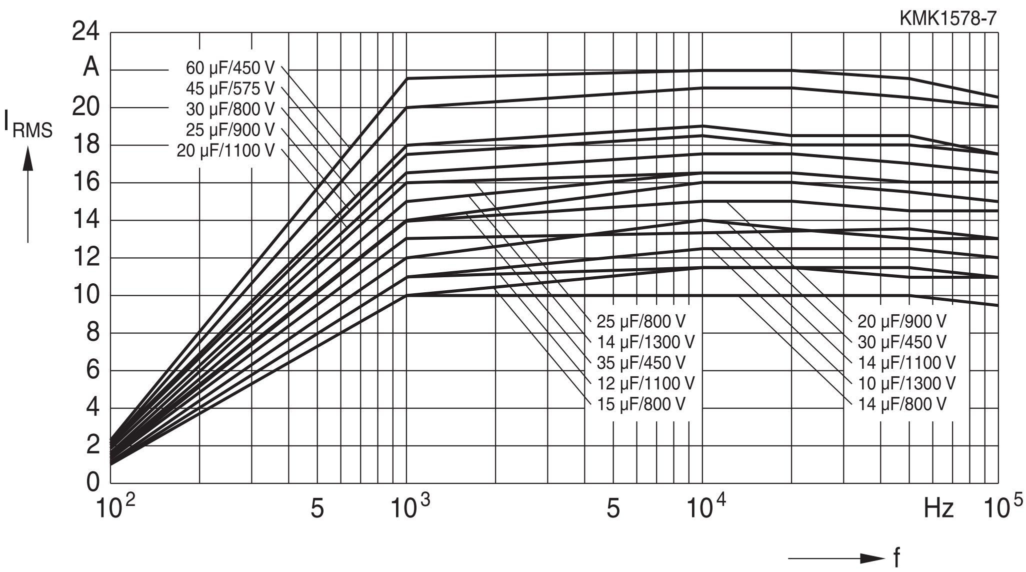
Characteristics curves

Permissible current I_{RMS} versus frequency f at 70 °C

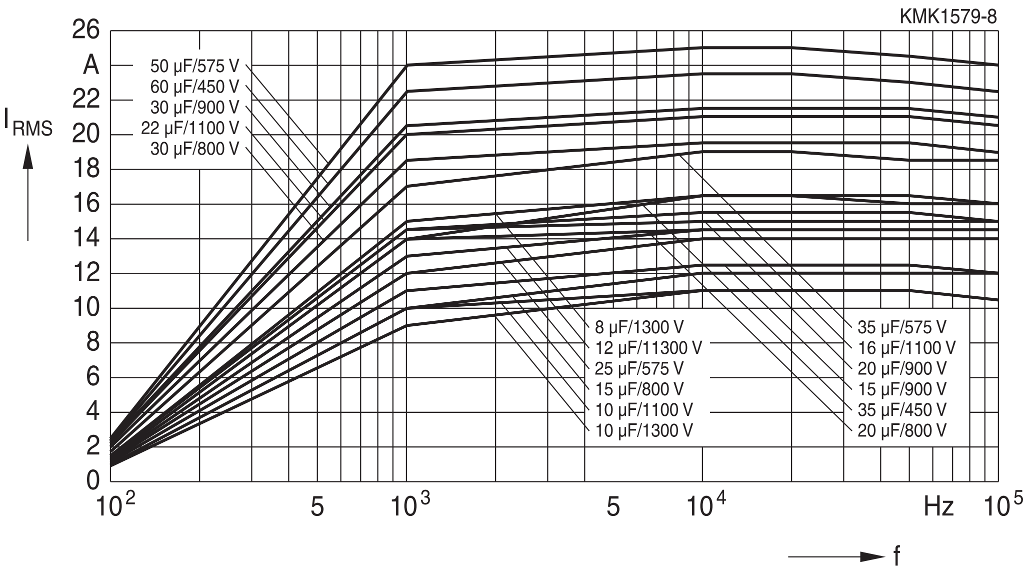


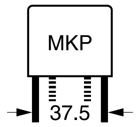
Lead spacing 37.5 mm

B32776E*



B32776G*



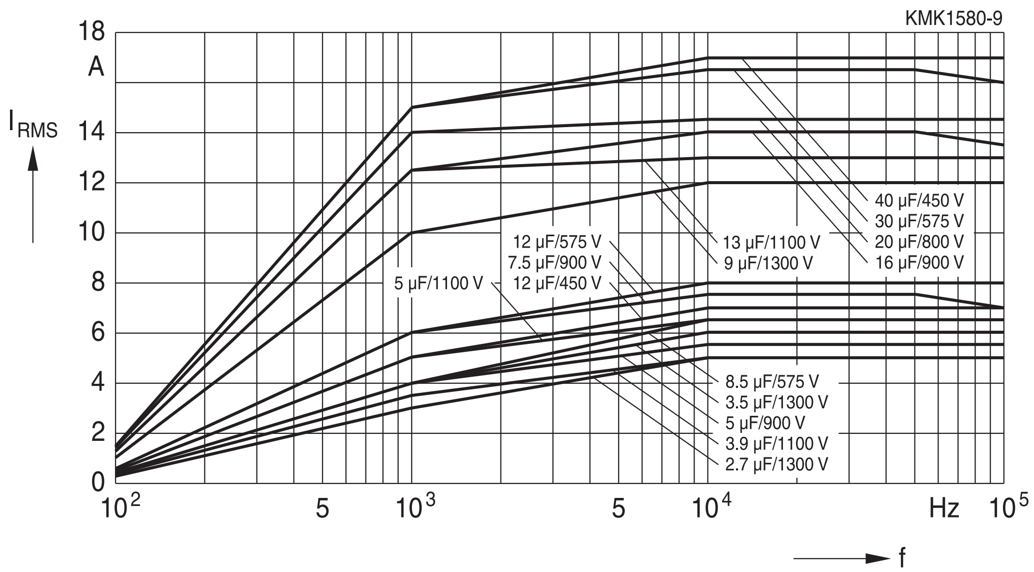


Characteristics curves

Permissible current I_{RMS} versus frequency f at 70 °C

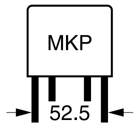
Lead spacing 37.5 mm

B32776T*



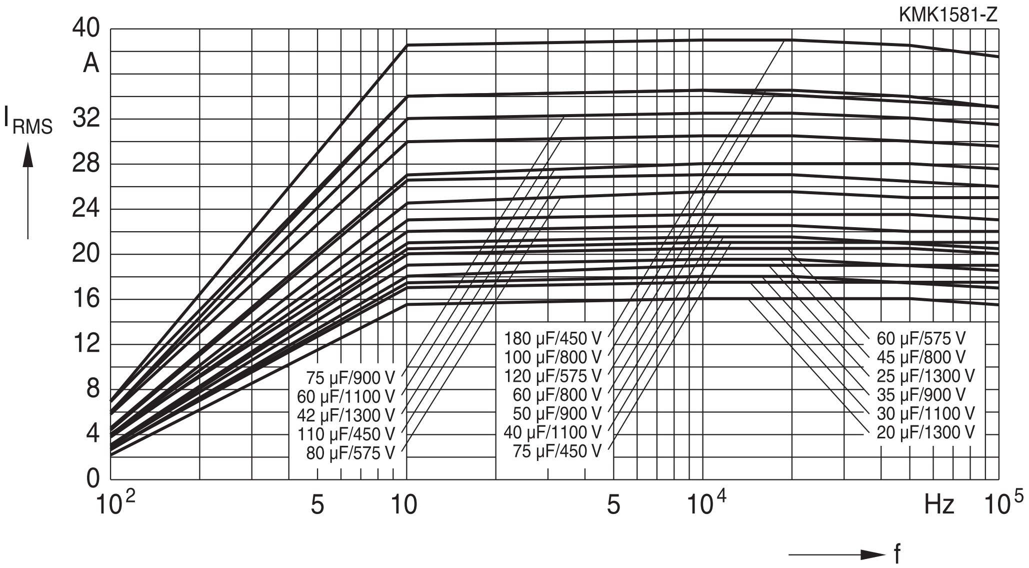
Characteristics curves

Permissible current I_{RMS} versus frequency f at 70 °C

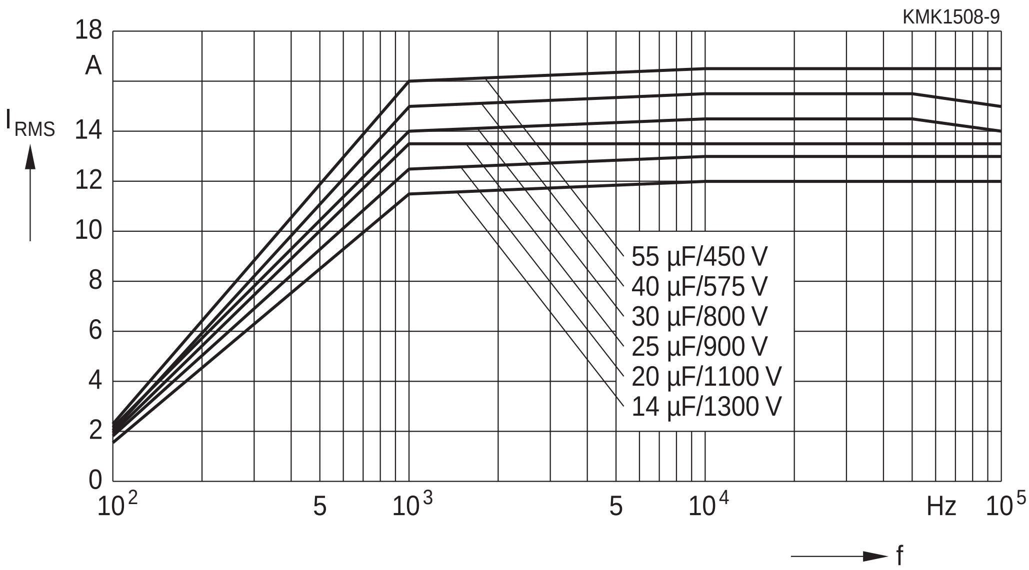


Lead spacing 52.5 mm

B32778G* (4 pins)

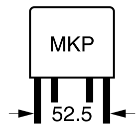


B32778T* (4 pins)



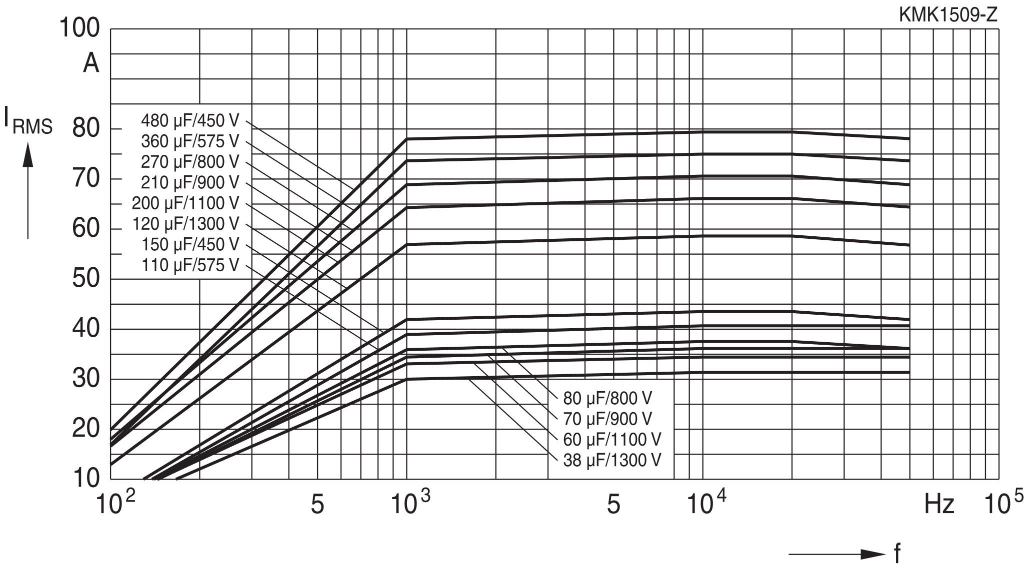
Characteristics curves

Permissible current I_{RMS} versus frequency f at 70 °C

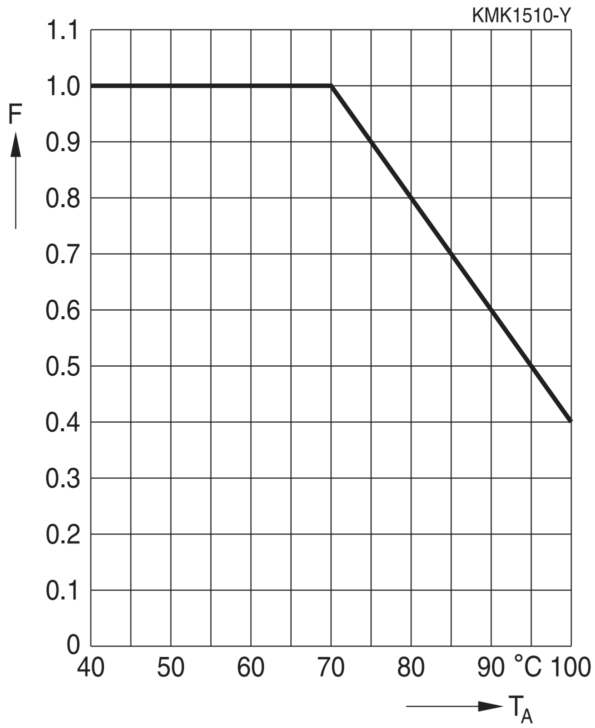


Lead spacing 52.5 mm

B32778J* (12 pins)



Curves characteristics (I_{RMS} derating versus temperature)



Maximum I_{RMS} current as function of the ambient temperature: I_{RMS} (T_A) = Factor x I_{RMS} (70 °C)

Heat transference for self heating calculation

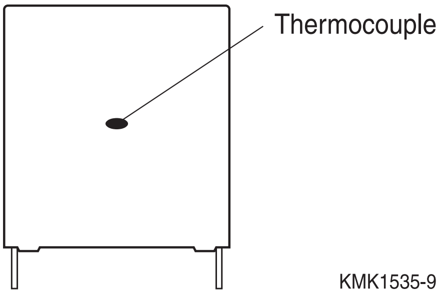


Figure 1

Box dimensions			Equivalent heat coefficient
w (mm)	h (mm)	l (mm)	G (mW/°C)
11.0	19.0	31.5	25
11.0	21.0	31.5	28
12.5	21.5	31.5	30
13.5	23.0	31.5	32
14.0	24.5	31.5	35
15.0	24.5	31.5	36
16.0	32.0	31.5	45
18.0	27.5	31.5	44
18.0	33.0	31.5	48
19.0	30.0	31.5	48
20.0	11.0	31.5	65
21.0	31.0	31.5	51
22.0	36.5	31.5	58
12.0	22.0	41.5	70
14.0	25.0	41.5	43
16.0	28.5	41.5	50
18.0	32.5	41.5	59
20.0	39.5	41.5	72
24.0	19.0	41.5	50
24.0	15.0	41.5	44
28.0	37.0	42.0	83
28.0	42.5	41.5	90
30.0	45.0	42.0	100
33.0	48.0	42.0	100
43.0	22.0	41.5	80
30.0	45.0	57.5	125
35.0	50.0	57.5	145
43.0	24.0	57.5	103
45.0	57.0	57.5	185
60.0	45.0	57.5	192
130.0	24.0	57.5	200
130.0	58.0	57.5	300

The equivalent heat coefficient **"G (mW/ºC)"** is given for measuring the temperature on the lateral surface of the plastic box as Figure 1 shows. By using a thermocouple and avoiding effect of radiation and convection the temperature measured during operation conditions should be a result of the dissipated power divided by the equivalent heat coefficient.

Self Heating by power dissipation & equivalent heat coefficient

The I_{RMS} and consequently the power dissipation must be limited during operation in order to not exceed the maximum limit of ΔT allowed for this series. ΔT_{max} given for this series is equal or lower than 20 °C at rated temperature (70 °C), for higher ambient temperatures ΔT_{max} (T) will have the same derating factor than I_{RMS} versus temperature and then an equivalent derating as per: ambient temperatures ΔT_{max} (T) will have the same derating factor than I_{RMS} versus temperature and then an equivalent derating as per:

$$\Delta T_{max} (T) = (Factor)^2 \times \Delta T (70\ °C).$$

For any particular I_{RMS} the ΔT may be calculated by:

$$\Delta T (°C) = P_{dis} (mW) / G(mW/°C).$$

Where ΔT (°C) is the difference between the temperature measured on the box (see Figure 1) and the ambient temperature when capacitor is working during normal operation;

$$\Delta T (°C) = T_{op} (°C) - T_A (°C).$$

It represents the increasing of temperature provoked by the I_{RMS} during operation.
G (mW/°C) is the equivalent heat coefficient described above and P_{dis} (mW) is the dissipated power defined by:

$$P_{dis} (mW) = ESR_{typ} (m\Omega) \times I_{RMS^2} (A_{RMS}).$$

Example for thermal calculation:

We will take as reference B32778G0306K (30 µF/1100 V) type for thermal calculation.
Considering the following load and capacitor characteristics:

I_{RMS} : 12 A_{RMS} at 20 kHz T_A: 85 °C 30 × 45 × 57.5 box

G (mW/°C): 125

Then we have to find the ESR_{typ} at 20 kHz what is approx . 8.2 mΩ.

So according to:

$$P_{dis} (mW) = ESR_{typ} (m\Omega) \times I_{RMS^2} (A_{RMS})$$

we have the following:

$$P_{dis} (mW) = 8.2\ m\Omega \times 12\ A_{RMS^2} = 1181\ mW$$

and as per:

$$\Delta T (°C) = P_{dis} (mW) / G (mW/°C)$$

we have the following:

$$\Delta T (°C) = 1181 (mW) / 125 (mW/°C) = 9.5\ °C.$$

What is below of the

$$\Delta T_{max} (85\ °C) = (Factor)^2 \times \Delta T (70\ °C) = (0.7)^2 \times 20\ °C = 9.8\ °C.$$

On the other hand we may confirm that max I_{RMS} at 20 kHz at 70 °C = 17.5 A_{RMS}

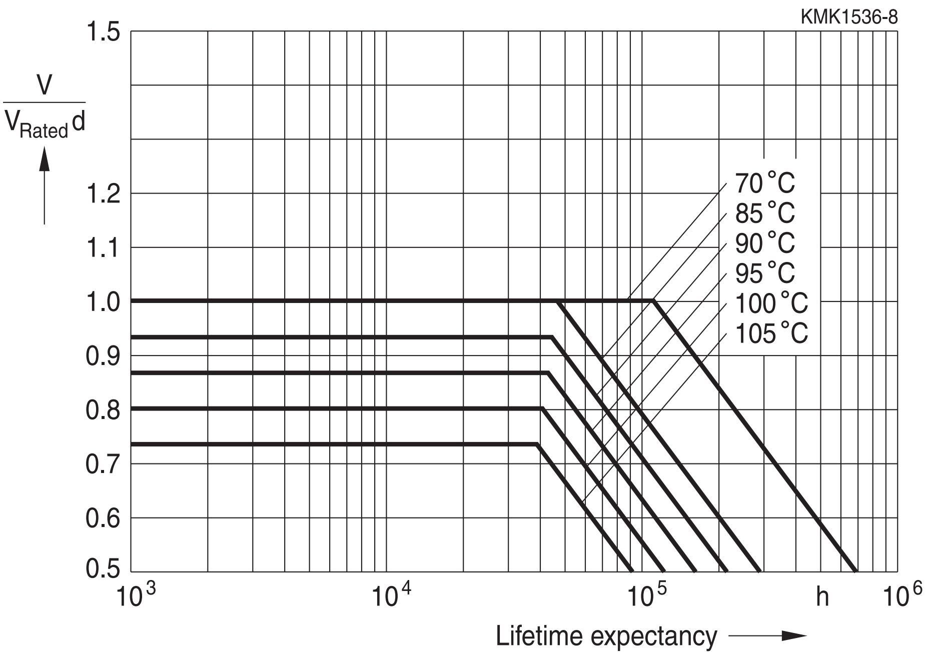
And then max I_{RMS} for 85 °C of ambient temperature is defined as follows:

$$I_{RMS} (85\ °C) = Factor \times I_{RMS} (70\ °C) = 0.7 \times 17.5\ A_{RMS} = 12.25\ A_{RMS}.$$

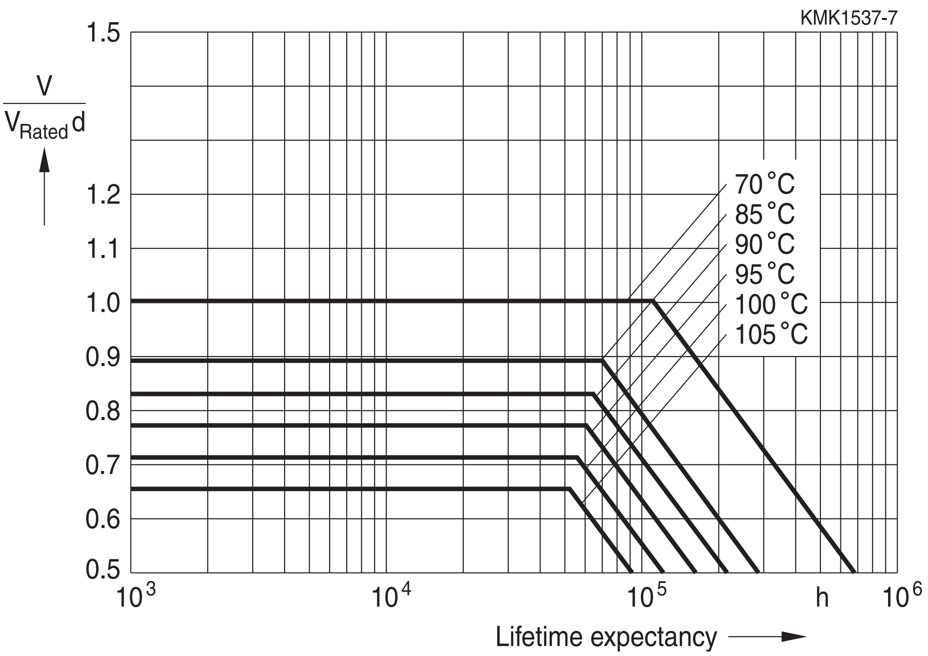
What confirms once again that I_{RMS} (12 A_{RMS} at 20 kHz) is below the max specified for such frequency and ambient temperature.

Life time expectancy - typical curves

B3277x-4 (450 V DC)



B3277x-5/8/9/0/1 (575 V DC / 800 V DC / 900 V DC / 1100 V DC / 1300 V DC)



Note: Confidence level of 95%

Testing and Standards

Test	Reference	Conditions of test	Performance requirements
Electrical parameters (Routine test)	IEC61071:2007	Voltage between terminals, 1.5 V_R, during 10 s Insulation resistance, R_{ins} at V_R if V_R <500 V or 500 V if V_R ≥500 V Capacitance, C at 1 kHz (room temperature) Dissipation factor, tan δ at 1/10 kHz (room temperature)	Within specified limits
Robustness of termina- tions (Type test)	IEC 60068-2-21-2006	Tensile strength (test Ua1) Wire diameter / Tensile force 0.5 <d_1 ≤0.8 mm / 10 N 0.8 <d_1 ≤1.25 mm / 20 N	Capacitance and tan δ within specified limits
Resistance to soldering heat (Type test)	IEC 60068-2-20:2008, test Tb, method 1A	Solder bath temperature at 260 ±5 °C, immersion for 10 seconds	$\Delta C/C_0$ ≤2% $\lvert\Delta \tan \delta\rvert$ ≤0.002
Rapid change of temperature (Type test)	IEC 60384-16:2005	T_A = lower category temperature T_B = upper category temperature Five cycles, duration t = 30 min	$\lvert\Delta C/C_0\rvert$ ≤2% $\lvert\Delta \tan \delta\rvert$ ≤0.002 R_{ins} ≥50% of initial limit
Vibration (Type test)	IEC 60384-16:2005	Test F_C: vibration sinusoidal Displacement: 0.75 mm Accleration: 98 m/s^2 Frequency: 10 Hz ... 500 Hz Test duration: 3 orthogonal axes, 2 hours each axe	No visible damage
Bump (Type test)	IEC 60384-16:2005	Test Eb: Total 4000 bumps with 390 m/s^2 mounted on PCB 6 ms duration	No visible damage $\lvert\Delta C/C_0\rvert$ ≤2% $\lvert\Delta \tan \delta\rvert$ ≤0.002 R_{ins} ≥50% of initial limit
Climatic se- quence (Type test)	IEC 60384-16:2005	Dry heat Tb / 16 h Damp heat cyclic, 1st cycle +55 °C / 24 h / 95% ... 100% RH Cold Ta / 2 h Damp heat cyclic, 5 cycles +55 °C / 24 h / 95% ... 100% RH	No visible damage $\lvert\Delta C/C_0\rvert$ ≤3% $\lvert\Delta \tan \delta\rvert$ ≤0.001 R_{ins} ≥50% of initial limit

Test	**Reference**	**Conditions of test**	**Performance requirements**
Damp heat, steady state (Type test)	IEC 60384-16:2005	Test Ca 40 °C / 93% RH / 56 days	No visible damage $\lvert\Delta C/C_0\rvert \leq 5\%$ $\lvert\Delta \tan \delta\rvert \leq 0.005$ $R_{ins} \geq 50\%$ of initial limit
Endurance (Type test)	IEC 60384-16:2005	70 °C / 1.25 V_R / 1000 hours or 85 °C / 1.25 V_{op} / 1000 hours or 100 °C / 1.25 V_{op} / 1000 hours	No visible damage $\lvert\Delta C/C_0\rvert \leq 5\%$ at 1 kHz $\lvert\Delta \tan \delta\rvert \leq 0.005$ $R_{ins} \geq 50\%$ of initial limit

Mounting guidelines

1 Soldering

1.1 Solderability of leads

The solderability of terminal leads is tested to IEC 60068-2-20:2008, test Ta, method 1.

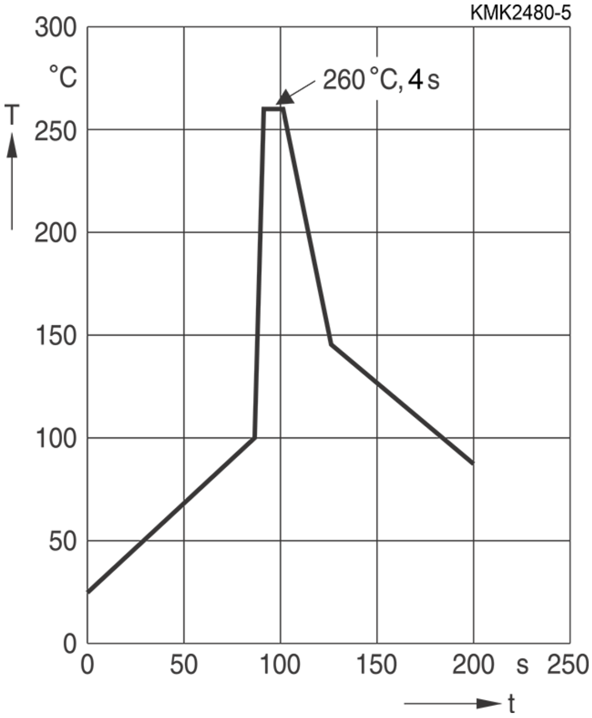
Before a solderability test is carried out, terminals are subjected to accelerated ageing (to IEC 60068-2-2:2007, test Ba: 4 h exposure to dry heat at 155 °C). Since the ageing temperature is far higher than the upper category temperature of the capacitors, the terminal wires should be cut off from the capacitor before the ageing procedure to prevent the solderability being impaired by the products of any capacitor decomposition that might occur.

Solder bath temperature	235 ±5 °C
Soldering time	2.0 ±0.5 s
Immersion depth	2.0 +0/–0.5 mm from capacitor body or seating plane
Evaluation criteria: Visual inspection	 Wetting of wire surface by new solder ≥90%, free-flowing solder

1.2 Resistance to soldering heat

Resistance to soldering heat is tested to IEC 60068-2-20:2008, test Tb, method 1. Conditions:

Series		Solder bath temperature	Soldering time
MKT	boxed (except 2.5 × 6.5 × 7.2 mm) coated uncoated (lead spacing >10 mm)	260 ±5 °C	10 ±1 s
MFP MKP	 (lead spacing >7.5 mm)		
MKT	boxed (case 2.5 × 6.5 × 7.2 mm)		5 ±1 s
MKP MKT	(lead spacing ≤7.5 mm) uncoated (lead spacing ≤10 mm) insulated (B32559)		<4 s recommended soldering profile for MKT uncoated (lead spacing ≤10 mm) and insulated (B32559)



Immersion depth	2.0 +0/–0.5 mm from capacitor body or seating plane
Shield	Heat-absorbing board, (1.5 ±0.5) mm thick, between capacitor body and liquid solder
Evaluation criteria:	
Visual inspection	No visible damage
$\Delta C/C_0$	2% for MKT/MKP/MFP 5% for EMI suppression capacitors
tan δ	As specified in sectional specification

1.3 General notes on soldering

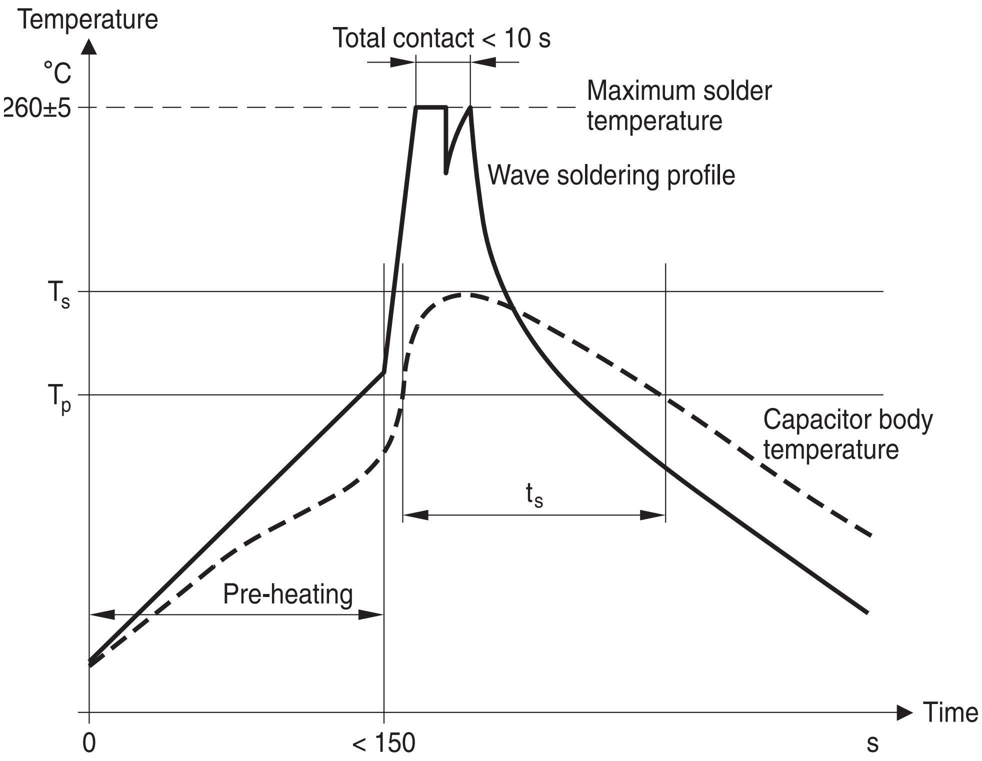
Permissible heat exposure loads on film capacitors are primarily characterized by the upper category temperature T_{max}. Long exposure to temperatures above this type-related temperature limit can lead to changes in the plastic dielectric and thus change irreversibly a capacitor's electrical characteristics. For short exposures (as in practical soldering processes) the heat load (and thus the possible effects on a capacitor) will also depend on other factors like:

- Pre-heating temperature and time
- Forced cooling immediately after soldering
- Terminal characteristics:
  diameter, length, thermal resistance, special configurations (e.g. crimping)
- Height of capacitor above solder bath
- Shadowing by neighboring components
- Additional heating due to heat dissipation by neighboring components
- Use of solder-resist coatings

The overheating associated with some of these factors can usually be reduced by suitable countermeasures. For example, if a pre-heating step cannot be avoided, an additional or reinforced cooling process may possibly have to be included.

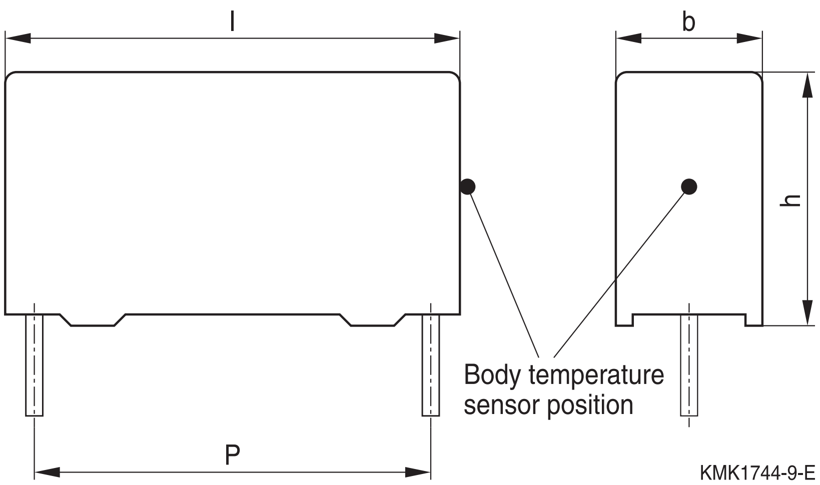
Recommendations

As a reference, the recommended wave soldering profile for our film capacitors is as follows:



T_s: Capacitor body maximum temperature at wave soldering
T_p: Capacitor body maximum temperature at pre-heating

KMK1745-A-E



KMK1744-9-E

Body temperature should follow the description below:

- MKP capacitor
  During pre-heating: $T_p \leq 110$ °C
  During soldering: $T_s \leq 120$ °C, $t_s \leq 45$ s
- MKT capacitor
  During pre-heating: $T_p \leq 125$ °C
  During soldering: $T_s \leq 160$ °C, $t_s \leq 45$ s

When SMD components are used together with leaded ones, the film capacitors should not pass into the SMD adhesive curing oven. The leaded components should be assembled after the SMD curing step.

Leaded film capacitors are not suitable for reflow soldering.

In order to ensure proper conditions for manual or selective soldering, the body temperature of the capacitor (T_s) must be ≤120 °C.

One recommended condition for manual soldering is that the tip of the soldering iron should be <360 °C and the soldering contact time should be no longer than 3 seconds.

For uncoated MKT capacitors with lead spacings ≤10 mm (B32560/B32561) the following measures are recommended:

- pre-heating to not more than 110 °C in the preheater phase
- rapid cooling after soldering

Please refer to our Film Capacitors Data Book in case more details are needed.

Cautions and warnings

- Do not exceed the upper category temperature (UCT).
- Do not apply any mechanical stress to the capacitor terminals.
- Avoid any compressive, tensile or flexural stress.
- Do not move the capacitor after it has been soldered to the PC board.
- Do not pick up the PC board by the soldered capacitor.
- Do not place the capacitor on a PC board whose PTH hole spacing differs from the specified lead spacing.
- Do not exceed the specified time or temperature limits during soldering.
- Avoid external energy inputs, such as fire or electricity.
- Avoid overload of the capacitors.
- Consult us if application is with severe temperature and humidity condition.
- There are no serviceable or repairable parts inside the capacitor. Opening the capacitor or any attempts to open or repair the capacitor will void the warranty and liability of TDK Electronics.
- Please note that the standards referred to in this publication may have been revised in the meantime.

The table below summarizes the safety instructions that must always be observed. A detailed description can be found in the relevant sections of the chapters "General technical information" and "Mounting guidelines".

Topic	Safety information	Reference chapter "General technical information"
Storage conditions	Make sure that capacitors are stored within the specified range of time, temperature and humidity conditions.	4.5 "Storage conditions"
Flammability	Avoid external energy, such as fire or electricity (passive flammability), avoid overload of the capacitors (active flammability) and consider the flammability of materials.	5.3 "Flammability"
Resistance to vibration	Do not exceed the tested ability to withstand vibration. The capacitors are tested to IEC 60068-2-6:2007. TDK Electronics offers film capacitors specially designed for operation under more severe vibration regimes such as those found in automotive applications. Consult our catalog "Film Capacitors for Automotive Electronics".	5.2 "Resistance to vibration"
Soldering	Do not exceed the specified time or temperature limits during soldering.	1 "Soldering"
Cleaning	Use only suitable solvents for cleaning capacitors.	2 "Cleaning"
Embedding of capacitors in finished assemblies	When embedding finished circuit assemblies in plastic resins, chemical and thermal influences must be taken into account. Caution: Consult us first, if you also wish to embed other uncoated component types!	3 "Embedding of capacitors in finished assemblies"

Display of ordering codes for TDK Electronics products

The ordering code for one and the same product can be represented differently in data sheets, data books, other publications, on the company website, or in order-related documents such as shipping notes, order confirmations and product labels. The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products.
Detailed information can be found on the Internet under www.tdk-electronics.tdk.com/orderingcodes.

Correlation of data sheet values and modelling tool outputs

Data sheet values and results of design tools may deviate as they have not been derived in the same context.

While data sheets show individual parameter statements without considering a possible dependency to other parameters. Tools model a complete given scenario as input and processed inside the tool.

Furthermore as we constantly strive to improve our models, the results of tools can change over time and be a non-binding indication only.

Symbols and terms

Symbol	English	German
α	Heat transfer coefficient	Wärmeübergangszahl
α_C	Temperature coefficient of capacitance	Temperaturkoeffizient der Kapazität
A	Capacitor surface area	Kondensatoroberfläche
β_C	Humidity coefficient of capacitance	Feuchtekoeffizient der Kapazität
C	Capacitance	Kapazität
C_R	Rated capacitance	Nennkapazität
ΔC	Absolute capacitance change	Absolute Kapazitätsänderung
$\Delta C/C$	Relative capacitance change (relative deviation of actual value)	Relative Kapazitätsänderung (relative Abweichung vom Ist-Wert)
$\Delta C/C_R$	Capacitance tolerance (relative deviation from rated capacitance)	Kapazitätstoleranz (relative Abweichung vom Nennwert)
dt	Time differential	Differentielle Zeit
Δt	Time interval	Zeitintervall
ΔT	Absolute temperature change (self-heating)	Absolute Temperaturänderung (Selbsterwärmung)
$\Delta \tan \delta$	Absolute change of dissipation factor	Absolute Änderung des Verlustfaktors
ΔV	Absolute voltage change	Absolute Spannungsänderung
dV/dt	Time differential of voltage function (rate of voltage rise)	Differentielle Spannungsänderung (Spannungsflankensteilheit)
$\Delta V/\Delta t$	Voltage change per time interval	Spannungsänderung pro Zeitintervall
E	Activation energy for diffusion	Aktivierungsenergie zur Diffusion
ESL	Self-inductance	Eigeninduktivität
ESR	Equivalent series resistance	Ersatz-Serienwiderstand
f	Frequency	Frequenz
f_1	Frequency limit for reducing permissible AC voltage due to thermal limits	Grenzfrequenz für thermisch bedingte Reduzierung der zulässigen Wechselspannung
f_2	Frequency limit for reducing permissible AC voltage due to current limit	Grenzfrequenz für strombedingte Reduzierung der zulässigen Wechselspannung
f_r	Resonant frequency	Resonanzfrequenz
F_D	Thermal acceleration factor for diffusion	Therm. Beschleunigungsfaktor zur Diffusion
F_T	Derating factor	Deratingfaktor
i	Current (peak)	Stromspitze
I_C	Category current (max. continuous current)	Kategoriestrom (max. Dauerstrom)
I_{RMS}	(Sinusoidal) alternating current, root-mean-square value	(Sinusförmiger) Wechselstrom
i_z	Capacitance drift	Inkonstanz der Kapazität
k_0	Pulse characteristic	Impulskennwert
L_S	Series inductance	Serieninduktivität
λ	Failure rate	Ausfallrate
λ_0	Constant failure rate during useful service life	Konstante Ausfallrate in der Nutzungsphase

Symbol	English	German
λ_{test}	Failure rate, determined by tests	Experimentell ermittelte Ausfallrate
P_{diss}	Dissipated power	Abgegebene Verlustleistung
P_{gen}	Generated power	Erzeugte Verlustleistung
Q	Heat energy	Wärmeenergie
ρ	Density of water vapor in air	Dichte von Wasserdampf in Luft
R	Universal molar constant for gases	Allg. Molarkonstante für Gas
R	Ohmic resistance of discharge circuit	Ohmscher Widerstand des Entladekreises
R_i	Internal resistance	Innenwiderstand
R_{ins}	Insulation resistance	Isolationswiderstand
R_P	Parallel resistance	Parallelwiderstand
R_S	Series resistance	Serienwiderstand
S	severity (humidity test)	Schärfegrad (Feuchtetest)
t	Time	Zeit
T	Temperature	Temperatur
τ	Time constant	Zeitkonstante
tan δ	Dissipation factor	Verlustfaktor
tan δ_D	Dielectric component of dissipation factor	Dielektrischer Anteil des Verlustfaktors
tan δ_P	Parallel component of dissipation factor	Parallelanteil des Verlfustfaktors
tan δ_S	Series component of dissipation factor	Serienanteil des Verlustfaktors
T_A	Temperature of the air surrounding the component	Temperatur der Luft, die das Bauteil umgibt
T_{max}	Upper category temperature	Obere Kategorietemperatur
T_{min}	Lower category temperature	Untere Kategorietemperatur
t_{OL}	Operating life at operating temperature and voltage	Betriebszeit bei Betriebstemperatur und -spannung
T_{op}	Operating temperature, $T_A + \Delta T$	Beriebstemperatur, $T_A + \Delta T$
T_R	Rated temperature	Nenntemperatur
T_{ref}	Reference temperature	Referenztemperatur
t_{SL}	Reference service life	Referenz-Lebensdauer
V_{AC}	AC voltage	Wechselspannung
V_C	Category voltage	Kategoriespannung
$V_{C,RMS}$	Category AC voltage	(Sinusförmige) Kategorie-Wechselspannung
V_{CD}	Corona-discharge onset voltage	Teilentlade-Einsatzspannung
V_{ch}	Charging voltage	Ladespannung
V_{DC}	DC voltage	Gleichspannung
V_{FB}	Fly-back capacitor voltage	Spannung (Flyback)
V_i	Input voltage	Eingangsspannung
V_o	Output voltage	Ausgangssspannung
V_{op}	Operating voltage	Betriebsspannung
V_p	Peak pulse voltage	Impuls-Spitzenspannung
V_{pp}	Peak-to-peak voltage Impedance	Spannungshub

Symbol	English	German
V_R	Rated voltage	Nennspannung
$\hat{V}_R$	Amplitude of rated AC voltage	Amplitude der Nenn-Wechselspannung
V_{RMS}	(Sinusoidal) alternating voltage, root-mean-square value	(Sinusförmige) Wechselspannung
V_{SC}	S-correction voltage	Spannung bei Anwendung "S-correction”
V_{sn}	Snubber capacitor voltage	Spannung bei Anwendung "Beschaltung"
Z	Impedance	Scheinwiderstand
$\boxed{e}$	Lead spacing	Rastermaß

Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule, we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.

2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.

3. **The warnings, cautions and product-specific notes must be observed**.

4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.tdk-electronics.tdk.com/material). Should you have any more detailed questions, please contact our sales offices.

5. We constantly strive to improve our products. Consequently, **the products described in this publication may change from time to time**. The same is true of the corresponding product specifications. Please check therefore to what extent product descriptions and specifications contained in this publication are still applicable before or when you place an order.
   We also **reserve the right to discontinue production and delivery of products**. Consequently, we cannot guarantee that all products named in this publication will always be available. The aforementioned does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

6. Unless otherwise agreed in individual contracts, **all orders are subject to our General Terms and Conditions of Supply**.

7. **Our manufacturing sites serving the automotive business apply the IATF 16949 standard**. The IATF certifications confirm our compliance with requirements regarding the quality management system in the automotive industry. Referring to customer requirements and customer specific requirements ("CSR") TDK always has and will continue to have the policy of respecting individual agreements. Even if IATF 16949 may appear to support the acceptance of unilateral requirements, we hereby like to emphasize that **only requirements mutually agreed upon can and will be implemented in our Quality Management System.** For clarification purposes we like to point out that obligations from IATF 16949 shall only become legally binding if individually agreed upon.
8. The trade names EPCOS, CarXield, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, FilterCap, FormFit, InsuGate, LeaXield, MediPlas, MiniBlue, MiniCell, MKD, MKK, ModCap, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PiezoBrush, PlasmaBrush, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, ThermoFuse, WindCap, XieldCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at www.tdk-electronics.tdk.com/trademarks.

Release 2023-08

PUSH-2/2P

PUSH MINI 2MM 2 PINES

DESCRIPCIÓN

Mini interruptor pulsador de dos terminales con botón de 2 mm, configuración SPST (por sus siglas en inglesque significan Single Pole Single Throw) o Polo Simple Corte Simple, donde polo se refiere al número de circuitos controlados por el interruptor y corte se refiere a la posición extrema del interruptor.

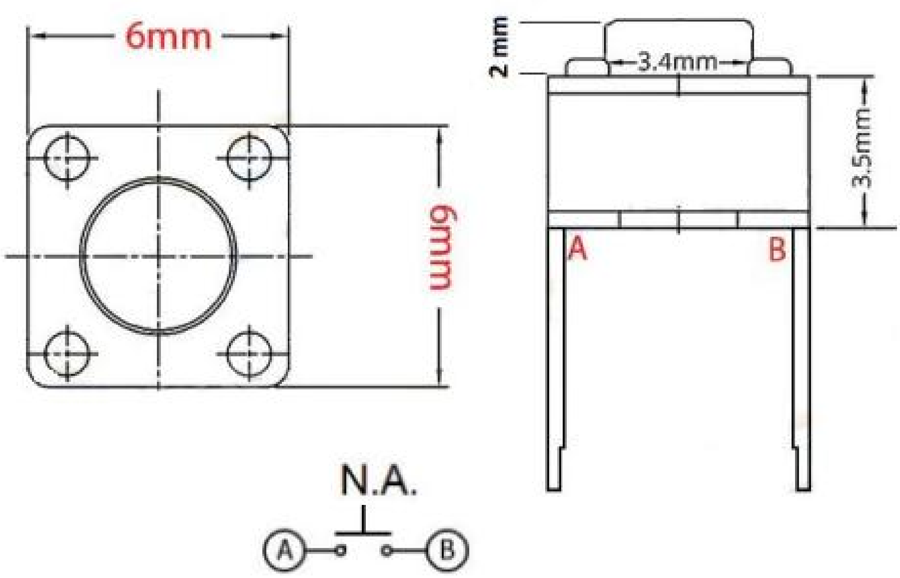
CARACTERÍSTICAS

- Permite el flujo de corriente solamente mientras es presionado.
- Permite desviar o interrumpir el curso de una corriente eléctrica.
- El push button se puede utilizar para la creación de circuitos electrónicos que requieran un interruptor para controlar el flujo de corriente y alimentar diferentes partes del circuito o elegir diferentes configuraciones de forma temporal, ya que al dejar de presionar el push button, se abre el circuito.

ESPECIFICACIONES

Parámetro	Descripción
Tipo de producto	Interruptor pulsador de 2 pines.
Voltaje máximo	12 VCD
Corriente máxima	50 mA
Altura	2 mm
Fuerza de presión	250±50gf
Vida útil	50000 ciclos
Resistencia de aislamiento	100mΩ
Resistencia de contacto	100mΩ

DIMENSIONES



APLICACIONES

- Practicas de electrónica
- Proyectos
- Prototipado