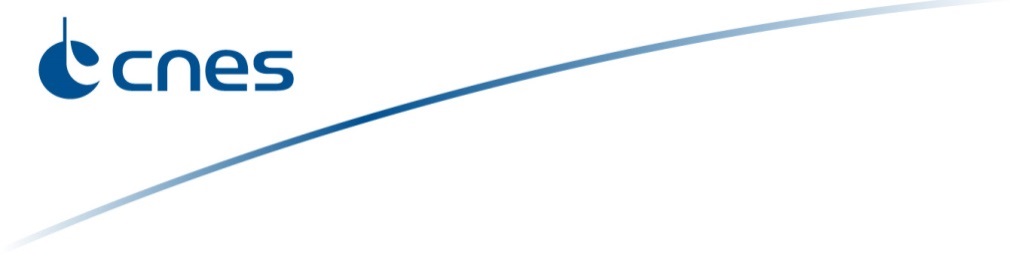
**VHDL Handbook:**

**CNES Edition**

**Indent:**

* Use a fixed number of **spaces**, no ~~tabs~~

**Lines:**

* One statement, port declaration or mapping per line.

**File:**

* Extension: “**.vhd**”
* Content: 1 entity + 1 architecture
* Max Size: **450 lines** (between architecture’s begin and end)
* Name: After the entity (**My\_Entity.vhd**)
* Header: Use the given header

**Libraries:**

* “**std\_logic\_1164**”
* “**numeric\_std**”
* That’s all (no Synopsis libraries if possible)

**RTL Design:**

* No “wait” or “after”
* No variables
* No functions or procedures

**Simulation:**

* Event starvation to stop simulation (or script with run + duration)
* Use “wait” and “after” keywords
* Use functions and procedures

**IP:**

* Naming rules do not apply to external IP
* Isolated in a wrapper entity

**Entity:**

* Name: 20 characters max
* Nested: No more than 10 times
* Suffix:
  + “**\_tb**” for testbenches
  + “**\_cfg**” for configuration

**Port:**

* Grouped by:
  + External interface
  + Direction
* Special port (clk, rst) first
* Comments on each port
* Unused output port: “open”
* No “buffer”
* No “record” for top level ports
* Prefix
  + “**i\_**” for input
  + “**o\_**” for output
  + “**b\_**” for bidirectional

**Component:**

* Instantiation made by name

**Architecture (name):**

* RTL, Behavioral or Simulation

**Process:**

* **Labeled**
* Sensitivity list:
  + Sync: only **clk** and **rst**
  + Async: **all read inputs**
* Label prefix: “**P\_**”

**Clock:**

* Name:
  + should include “**clk**” or “**clock**”
  + kept identical across hierarchy
  + no frequency values
* No gated clock
* Only **one edge** used

**Reset:**

* Name:
  + should include “**rst**”, “**reset**”, or “**clr**”
  + kept identical across hierarchy
* **One level** used
* Asserted: asynchronous
* Deasserted: synchronous

**Variables:**

* Prefix: “**v\_**”

**Signals:**

* Name:
  + Coherent with usage
  + No change → no renaming
  + No pin number
* Initialization: in reset sequence
* Suffix:
  + “**\_n**” if active low
  + “**\_re**” if representing a rising edge
  + “**\_fe**” if representing a falling edge
  + “**\_r**” if it registers another signal
  + “**\_rX**” for X registrations
* Prefix: “**sm\_**” for FSM signals

**Integers:**

* Constrain using “**range**”

**Arrays:**

* Max dimension: **2**
* Using “**to**” keyword

**Std\_logic\_vector:**

* Using “**downto**” keyword

**Constant:**

* Use them instead of hardcoded values, as much as possible
* Prefix: “**c\_**”

**Generic:**

* Prefix: “**g\_**”

**Custom type:**

* Prefix: “**t\_**”

**Package:**

* Nested: No more than 3 times
* Prefix: “**pkg\_**”

**FSM:**

* Use **enumerated** type
* Use “Case” coding style and do not forget “when others”
* Do not use the “if … elsif … else” coding style