Digital Logic Design
(EL-227)
LABORATORY MANUAL
Fall-2021

LAB 09
Multiplexer
&
Demultiplexer

Lab Session #9: Multiplexer & Demultiplexer

OBJECTIVES:

- To study the concept of multiplexers & demultiplexers
- To learn the implementation of Boolean function using multiplexer To learn
- how to implement large multiplexer using small size multiplexers
- Parallel Multiplexing using 74LS151

APPARATUS: Logic trainer, Logic probe

COMPONENTS: ICs 74LS08, 74LS32, 74LS04, 74LS86, 74LS02

Multiplexer:

A multiplexer is a device that allows data information from several sources to be routed onto a single line for transmission to a common destination. It has several input lines and a single output line. It also has data-select inputs, which permit digital data on any one of the inputs to be switched to the output line. A multiplexer is also called a data selector because of this ability to select which data input is connected o the output. Normally there are 2n input lines and n selection lines whose bit combination determine which input is selected.

A 74LS151 has eight inputs that can be individually selected by three select lines. The output is connected to the input line selected by the binary value on the three select lines. If the three select lines are all zeros, then input line "0" is selected and connected to the output line.

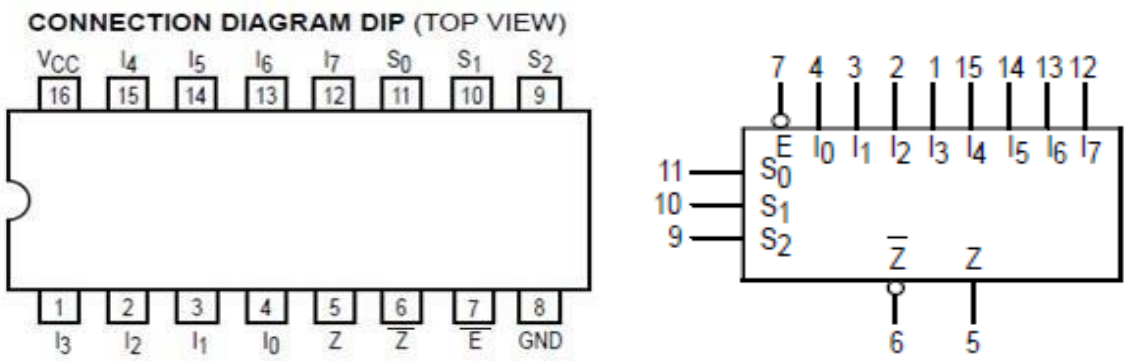


Fig 1: Pin's Description

2-to-1 multiplexer:

The truth table of the 2-to-1 multiplexer is shown below. Depending on the value of the select input, the inputs i.e., D0, D1 are produced at outputs. The output is D0 when Select value is S = 0 and the output is D1 when Select value is S = 1.

$$Y = \bar{S}D0 + SD1$$

S	D0	D1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Table#1: 2*1 Multiplexer

H= Logic High, L= Logic Low, X= Don't Care

4-to-1 multiplexer:

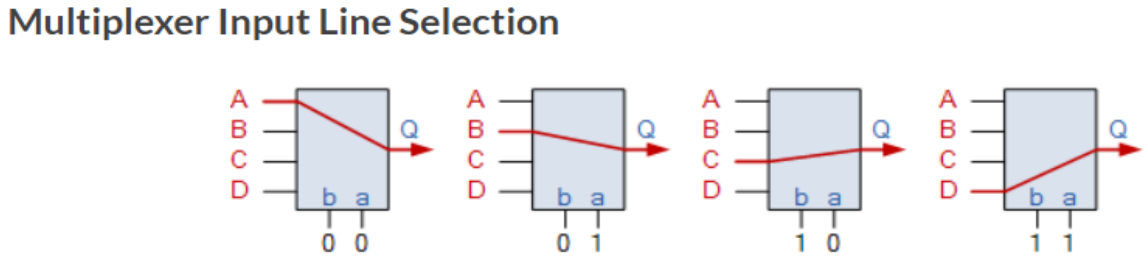
The truth table of a 4-to-1 multiplexer is shown below in which four input combinations 00, 10, 01 and 11 on the select lines respectively switches the inputs D0, D2, D1 and D3 to the output. That means when S0=0 and S1 =0, the output at Y is D0, similarly Y is D1 if the select inputs S0=0 and S1= 1 and so on.

$$Y = \overline{S0}\,\overline{S1}\,D0 + \overline{S0}\,S1\,D1 + S0\,\overline{S1}\,D2 + S0\,S1\,D3$$

S0	S1	D0	D1	D2	D3	Y
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Table#2: 4*1 Multiplexer

H= Logic High, L= Logic Low, X= Don"t Care



Logic Diagram 2:1 MUX using AND gates

From the above output expression, the logic circuit of 2-to-1 multiplexer can be implemented using logic gates as shown in figure. It consists of two AND gates, one NOT gate and one OR gate. When the select line, S=0, the output of the lower AND gate is zero, but the output of upper AND gate is D0. Thus, the output generated by the OR gate is equal to D0.

Similarly, when S=1, the output of the upper AND gate is zero, but the output of lower AND gate is D1. Therefore, the output of the OR gate is D1. Thus, the above given Boolean expression is satisfied by this circuit.

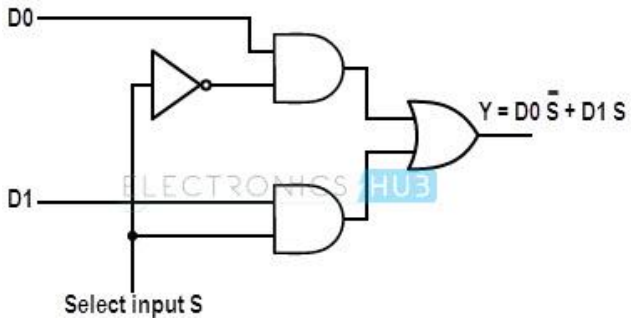


Fig 2: 2:1 MUX using AND gates

Logic Diagram 4:1 MUX using AND gate

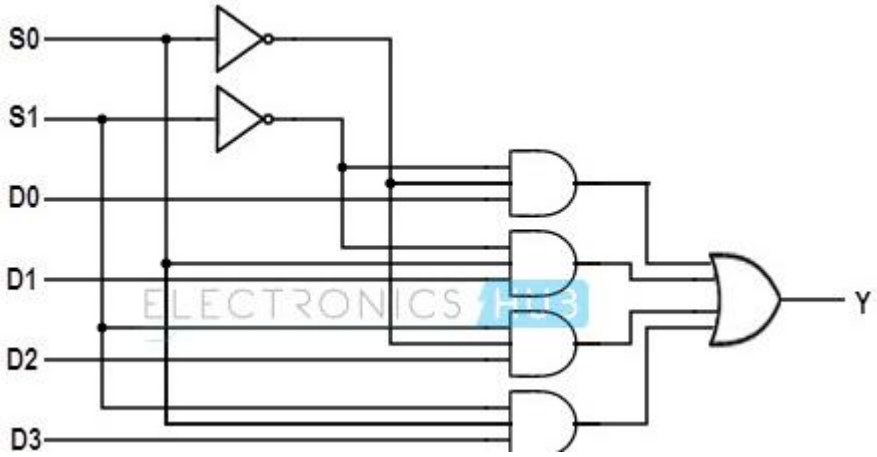


Fig 3: 4*1 Multiplexer using AND Gate

Applications of Multiplexer:

Multiplexer are used in various fields where multiple data need to be transmitted using a single line. Following are some of the applications of multiplexers.

1. **Communication System** – Communication system is a set of system that enable communication like transmission system, relay and tributary station, and communication network. The efficiency of communication system can be increased considerably using multiplexer. Multiplexer allow the process of transmitting different type of data such as audio, video at the same time using a single transmission line.

2. **Telephone Network –** In telephone network, multiple audio signals are integrated on a single line for transmission with the help of multiplexers. In this way, multiple audio signals can be isolated and eventually, the desire audio signals reach the intended recipients.

3. **Computer Memory** - Multiplexers are used to implement huge amount of memory into the computer, at the same time reduces the number of copper lines required to connect the memory to other parts of the computer circuit.

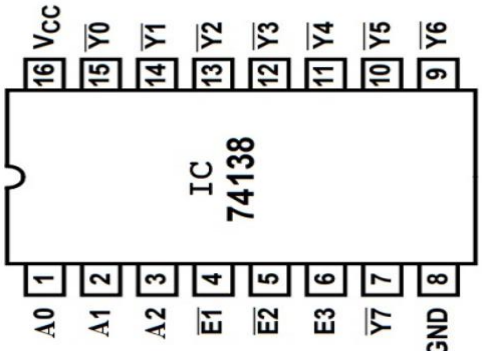
Demultiplexer:

The process of getting information from one input and transmitting the same over one of many outputs is called Demultiplexing. If you recall the Multiplexer, there we discussed the concept of Multiplexing. Demultiplexing is just the opposite of that.

A Demultiplexer is a combinational logic circuit that receives the information on a single input line and transmits the same information over one of 'n' possible output lines. If Multiplexers are called as Data Selectors, then Demultiplexers are called as Data Distributors, since they transmit the same data which is received at the input to different destinations. Thus, a demultiplexer is a 1-to-N device, whereas the multiplexer is an N-to-1 device.

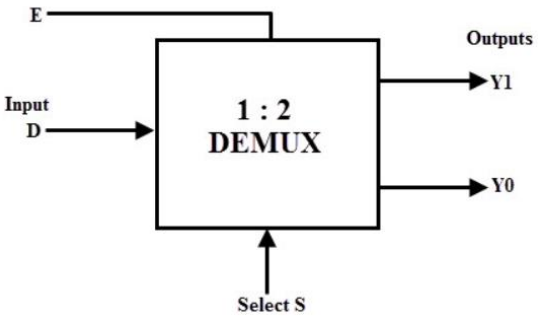
In order to select a particular output, we have to use a set of Select Lines and the bit combinations of these select lines control the selection of specific output line to be connected to the input at a given instant.

1-to-8 demultiplexer integrated circuits is the IC 74LS138. All the enable pins are normal enable pins – two are active LOW and one is active HIGH and the outputs are active LOW. The following image shows the pinout of 74LS138 IC.



1-to-2 demultiplexer

A 1-to-2 demultiplexer consists of one input line, two output lines and one select line. The signal on the select line helps to switch the input to one of the two outputs. The figure below shows the block diagram of a 1-to-2 demultiplexer with additional enable input.



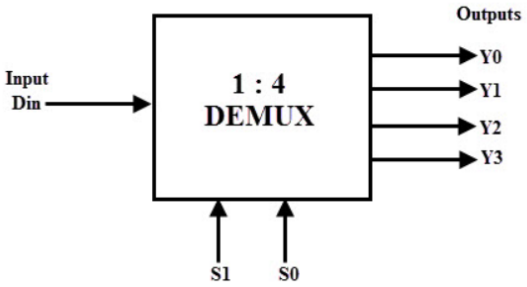
The truth table of a 1-to-2 demultiplexer is shown below, in which the input is routed to Y0 and Y1 depending on the value of select input S.

S	D	Y1	Y0
0	0	0	**0**
0	1	0	**1**
1	0	**0**	0
1	1	**1**	0

1-to-4 demultiplexer

A 1-to-4 demultiplexer has a single input (D), two selection lines (S1 and S0) and four outputs (Y0 to Y3). The input data goes to any one of the four outputs at a given time for a particular combination of select lines.

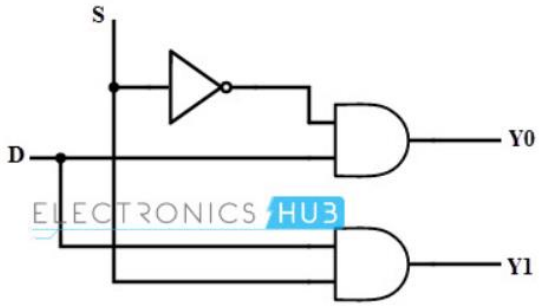
This demultiplexer is also called as a 2-to-4 Demultiplexer, which means that it has two select lines and 4 output lines. The block diagram of a 1:4 DEMUX is shown below.



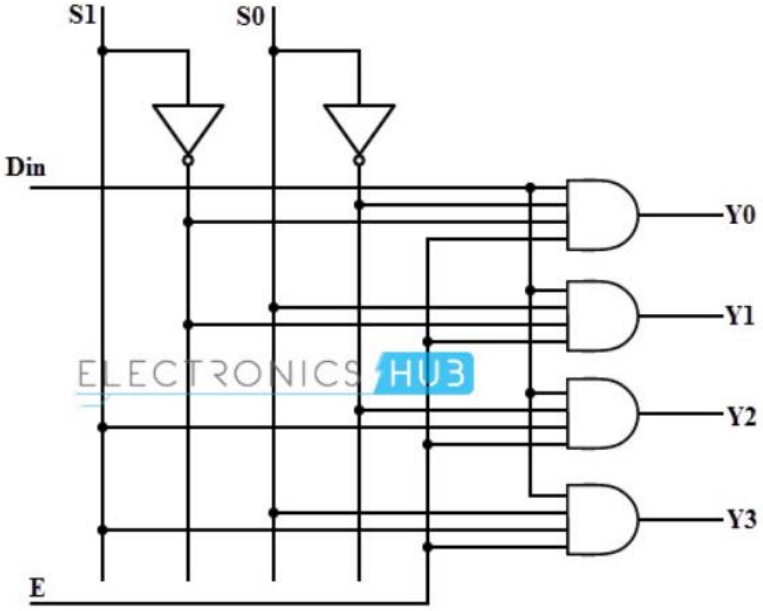
The truth table of this type of demultiplexer is given below. From the truth table it is clear that, when S0=0 and S1 = 0, the data input is connected to output Y0 and when S0 = 0 and s1=1, the data input is connected to output Y1.

S1	S0	D	Y3	Y2	Y1	Y0
0	0	0	0	0	0	**0**
0	0	1	0	0	0	**1**
0	1	0	0	0	**0**	0
0	1	1	0	0	**1**	0
1	0	0	0	**0**	0	0
1	0	1	0	**1**	0	0
1	1	0	**0**	0	0	0
1	1	1	**1**	0	0	0

Logic Diagram 1:2 DEMUX using AND gates



Logic Diagram 1:4 DEMUX using AND gates



Applications of Demultiplexer

Since the demultiplexers are used to select or enable the one signal out of many, these are extensively used in microprocessor or computer control systems such as:

- Selecting different IO devices for data transfer (Data Routing)
- Choosing different banks of memory (Memory Decoding)
- Depends on the address, enabling different rows of memory chips
- Enabling different functional units.

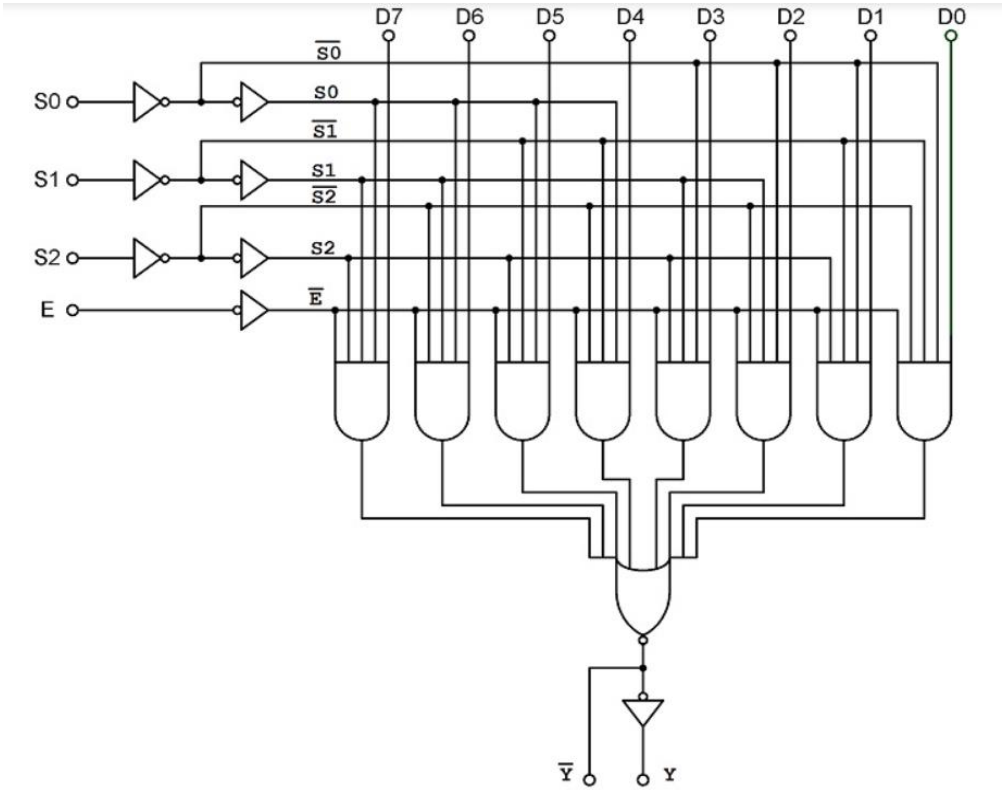
Other than these, demultiplexers can be found in a wide variety of application such as:

- Synchronous data transmission systems
- Boolean function implementation (as we discussed full subtractor function above)
- Data acquisition systems
- Combinational circuit design
- Automatic test equipment systems
- Security monitoring systems (for selecting a particular surveillance camera at a time), etc.

LAB TASKS

Lab Task #1

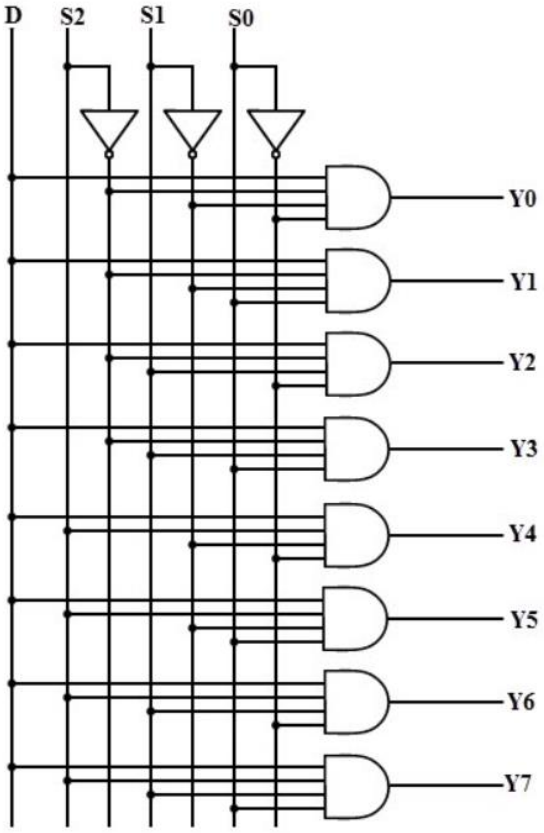
Fill up the Truth Table below given the enable input, select inputs and the multiplexer



$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z	$\overline{Z}$
H	X	X	X	X	X	X	X	X	X	X	X		
L	L	L	L	L	X	X	X	X	X	X	X		
L	L	L	L	H	X	X	X	X	X	X	X		
L	L	L	H	X	L	X	X	X	X	X	X		
L	L	L	H	X	H	X	X	X	X	X	X		
L	L	H	L	X	X	L	X	X	X	X	X		
L	L	H	L	X	X	H	X	X	X	X	X		
L	L	H	H	X	X	X	L	X	X	X	X		
L	L	H	H	X	X	X	H	X	X	X	X		
L	H	L	L	X	X	X	X	L	X	X	X		
L	H	L	L	X	X	X	X	H	X	X	X		
L	H	L	H	X	X	X	X	X	L	X	X		
L	H	L	H	X	X	X	X	X	H	X	X		
L	H	H	L	X	X	X	X	X	X	L	X		
L	H	H	L	X	X	X	X	X	X	H	X		
L	H	H	H	X	X	X	X	X	X	X	L		
L	H	H	H	X	X	X	X	X	X	X	H		

Lab Task #2

Fill up the Truth Table below given the enable input, select inputs and the demultiplexer



D	S0	S1	S2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
D	0	0	0								
D	0	0	1								
D	0	1	0								
D	0	1	1								
D	1	0	0								
D	1	0	1								
D	1	1	0								
D	1	1	1								

Lab Task #3

(I) Design NAND Logic Gate using 2:1 MUX.
(II) Design NOR Logic Gate using 2:1 MUX.
(III) Design 1:2 DEMUX using NAND Gate.
(IV) Design 1:4 DEMUX using NAND Gate.