PORT

Atmel SAM D21E / SAM D21G / SAM D21J
ARM Cortex M0+

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Overview

- PORT controls the I/O pins of the microcontroller.
- I/O pins are organized in a series of groups (port group)
- Each group = to 32 pins
- Configured and controlled individually or as a group
- Each pin may either be used for GPIO or assigned to an embedded device peripheral.
- For GPIO, each pin can be configured as input or output.

Features

- Selectable input and output configuration individually for each pin
- Software-controlled multiplexing of peripheral functions on I/O pins
- Flexible pin configuration through a dedicated Pin Configuration register
- Configurable output driver and pull settings
- Configurable input buffer and pull settings
- Read-modify-write support for pin configuration, output value and pin direction

I/O Lines

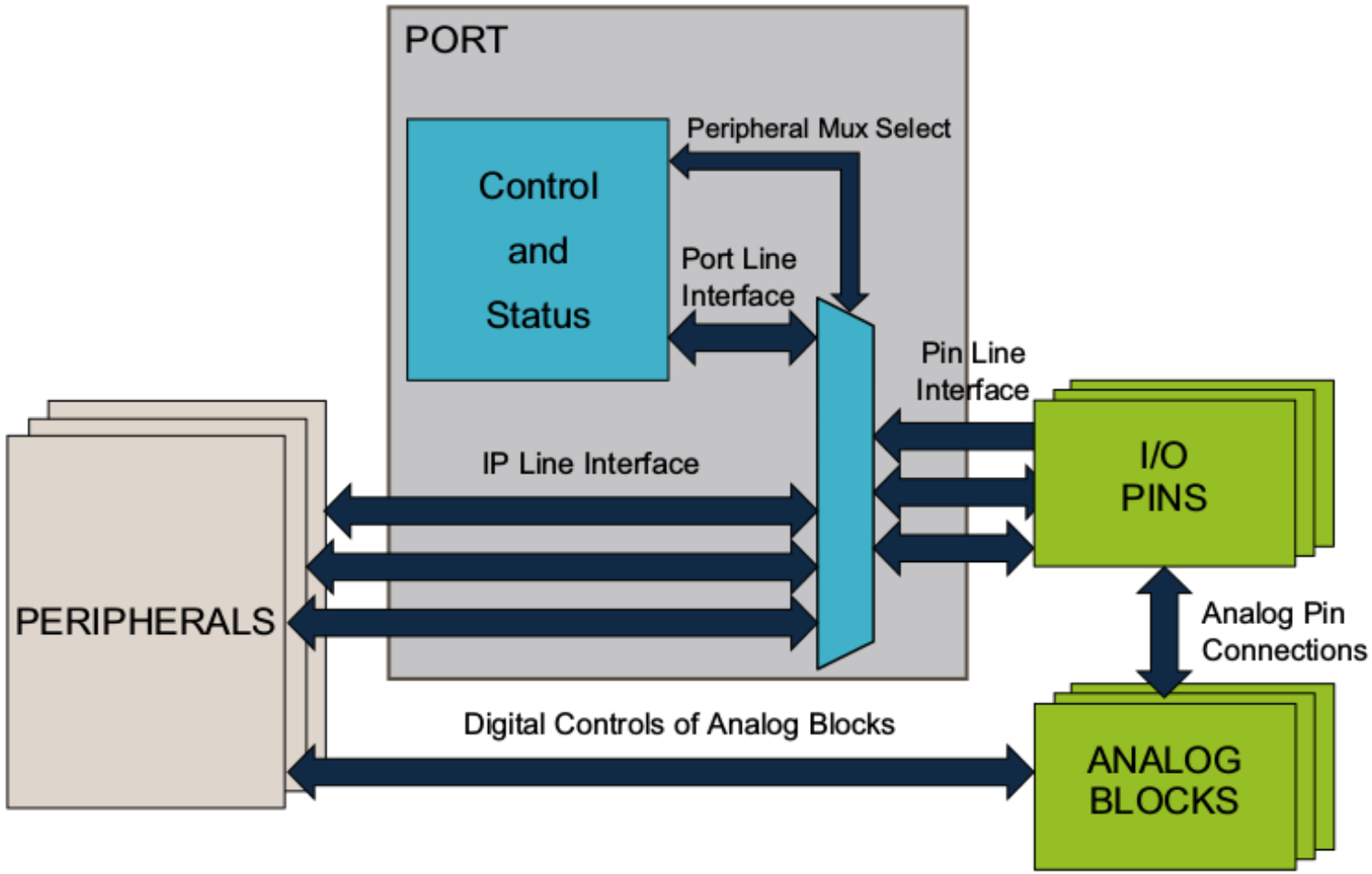
- Each group of 32 pins is assigned a letter id
  – A, B, ...
- With Each port group, each pin is assigned a numerical id
  – 00, 01, 02 ...
- PORT pins are mapped as: **Pxy**
  x = A, B, C, ... and y = 00, 01, ..., 31
- Each pin may have **one or more peripheral multiplexer settings**
- This allows the pin to be routed internally to a dedicated peripheral function
  - Refer to **I/O Multiplexing and Considerations on Atmel 42181 SAMD21 Datasheet on page 21**

Analog Connections

- Analog functions are connected directly between the analog blocks and I/O pins using analog buses
- Selecting an analog peripheral function for a given pin will disable the digital features of the pin

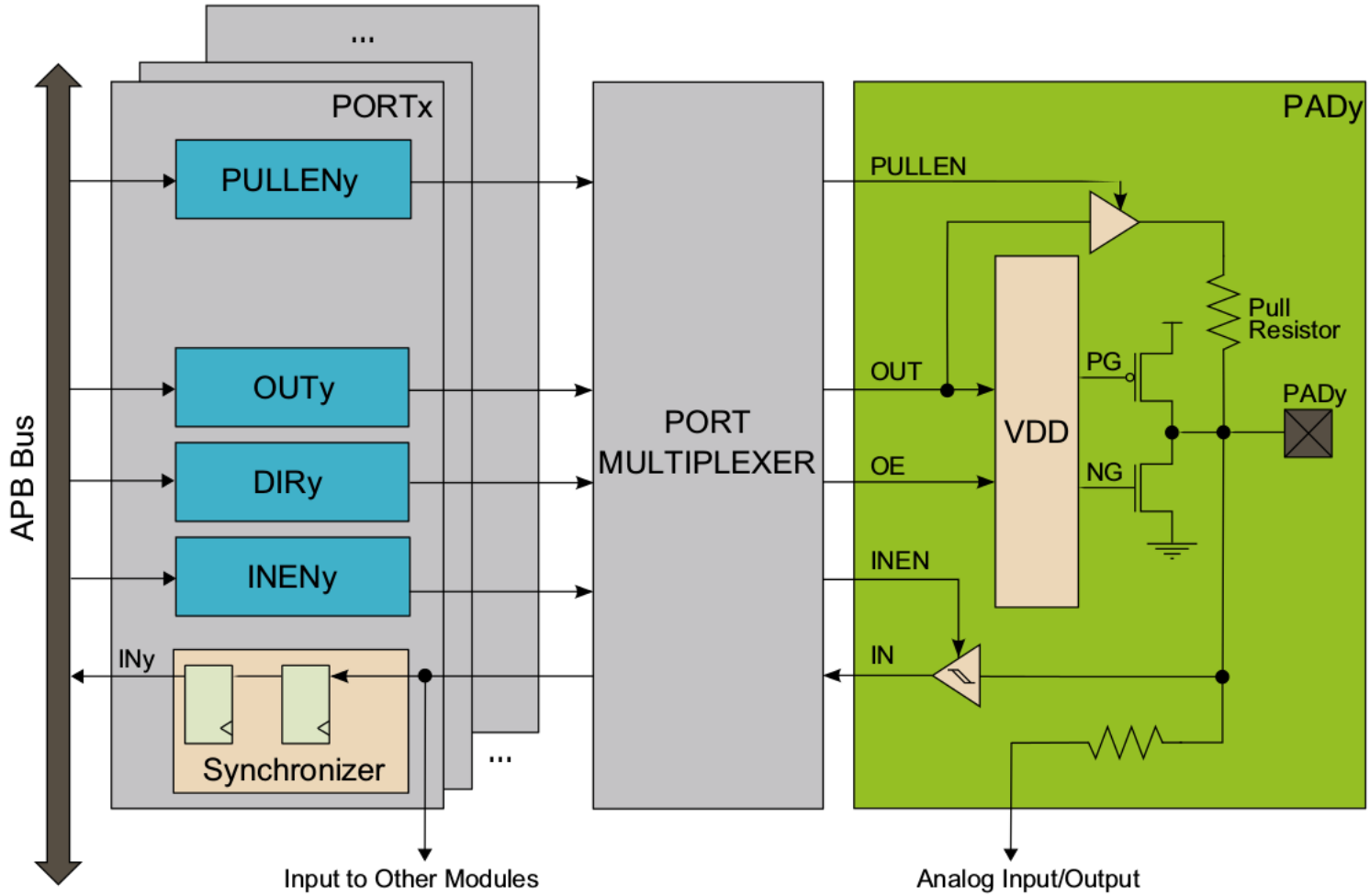
Port Block Diagram

Figure : PORT Block Diagram (Atmel 42181 SAMD21 Datasheet)



Overview of the PORT

Figure : PORT Overview (Atmel 42181 SAMD21 Datasheet)



Principle of Operation - 1

- Device I/O pins controlled by R/W of PORT peripheral registers
- To enable a pin as an output and to define the its Output State:
  – Enable de corresponding bit in **DIR** and **OUT** registers
- The directions of each pin is configured via **DIR** register
  – If a bit in **DIR** written to **1** – pin configured as **output**
  – if a bit in **DIR** written to **0** – pin configured as **input**

Principle of Operation - Output

- When Direction set as **output**:
- The corresponding bit int the **OUT** register is used to set the level of the pin
- If bit **y** of **OUT** is written **1**
  – Pin driven high
- If bit **y** of **OUT** is written **0**
  – Pin driven low

Principle of Operation - Input

- Bits from **IN** (Data Input Value) register are used to read the port pins
- Input value can always be read, whether the pin is configured as input or output
- Except if digital input is disabled i.e:
  – Write **0** to the **INEN** bit in **PINCFGy** registers

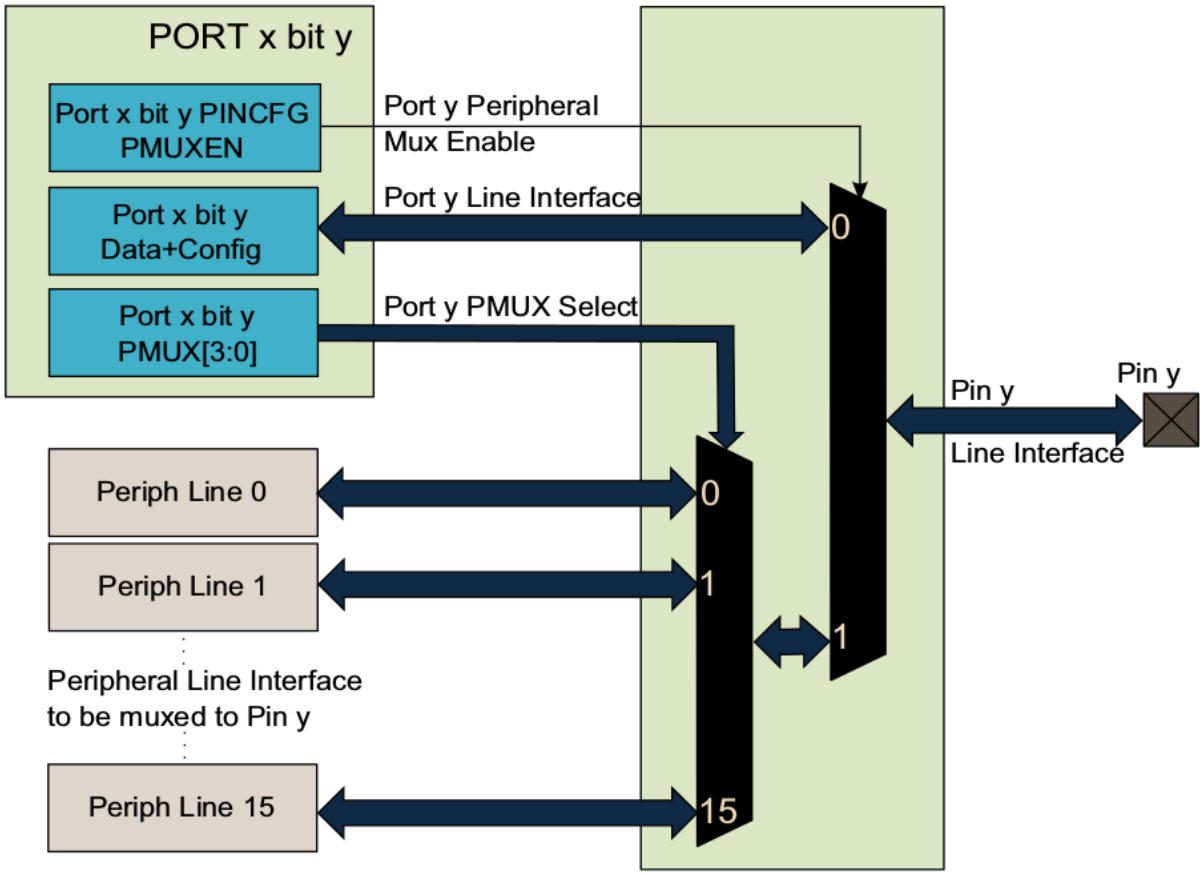
Register Description - Other Peripheral Functions

- PORT allows peripheral functions to be connected to individual I/O pins:
- Write **1** to **PMUXEN** bit in **PINCFGy** registers
- Write the chosen selection (**peripheral function**) in the corresponding nibble from the corresponding **PMUXn** (Peripheral Multiplexing) Register
- This will override the connection between PORT and the selected I/O pin
- The selected I/O pin will be connected to the chosen peripheral line interface

- For Peripheral functions Refer to **I/O Multiplexing and Considerations on Atmel 42181 SAMD21 Datasheet on page 21**

Overview Peripheral Functions Multiplexing

Figure : Peripheral Function Multiplexing(Atmel 42181 SAMD21 Datasheet)



PORT Registers


```
struct PORT{ //see [1] 23.7
 unsigned DIR;            //0x00
 unsigned DIRCLR;         //0x04
 unsigned DIRSET;         //0x08
 unsigned DIRTGL;         //0x0c
 unsigned OUT;            //0x10
 unsigned OUTCLR;         //0x14
 unsigned OUTSET;         //0x18
 unsigned OUTTGL;         //0x1c
 unsigned IN;             //0x20
 unsigned CTRL;           //0x24
 unsigned WRCONFIG;       //0x28
 unsigned RES;            //0x2c
 static const unsigned PMUXN=32/(2*4);
 unsigned PMUX[PMUXN];    //0x30
 static const unsigned PINCFGN=32/4;
 unsigned PINCFG[PINCFGN]; //0x40
```

Register Description - 1

- DIR - Data Direction (32 bit)
  - Set direction of each pin a port groups
- DIRCLR - Direction Clear (32 bit)
  - Set I/O pins as **input**
- DIRSET - Direction Set (32 bit)
  - Set I/O pins as **output**
- DIRTGL - Data Direction Toggle (32 bit)
  - Toggle the direction of one or more pins
- OUT - Data Output Value (32 bit)
  - Sets the data output drive value for I/O pins
- OUTCLR - Data Output Value Clear (32 bit)
  - Set pins drive level to **low**
- OUTSET - Data Output Value Set (32 bit)
  - Set pins drive level to **high**

Register Description - 2

- OUTTGL - Data Output Value Toggle (32 bit)
  - Toggle the drive level
- IN - Data Input Value (32 bit)
  - Read the port pin value
- CTRL - Control (32 bit)
  - Config the input sampling functionality from input pins
- WRCONFIG - Write Configuration (32 bit)
  - Used to configure several pins simultaneously with the same configuration and peripheral mux

Register Description - 3

- **PMUXn** - Peripheral Multiplexing n (8bit, 4 bit per pin) - 16 Peripheral Multiplexing Registers in each group

Figure : PMUXn Register(Atmel 42181 SAMD21 Datasheet)

Bit	7	6	5	4	3	2	1	0
	PMUXO[3:0]				PMUXE[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Register Description - 4

- **PINCFGn** - Pin Configuration Register n (8 bit)

Figure : PINCFGn Register(Atmel 42181 SAMD21 Datasheet)

Bit	7	6	5	4	3	2	1	0
		DRVSTR				PULLEN	INEN	PMUXEN
Access	R	R/W	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0