# LTSPICE PROJECT

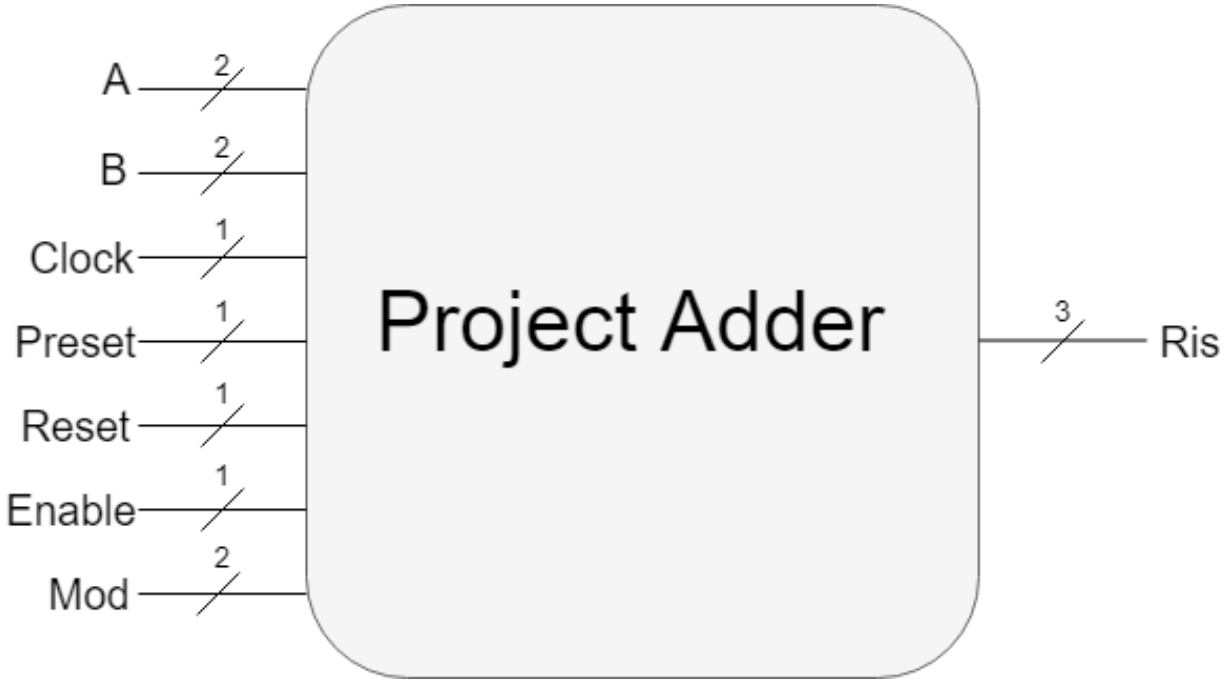
## INFORMATICA INDUSTRIALE

FABIO CIMMINO 807070
ROBERTO LOTTERIO 807500

# INTRO

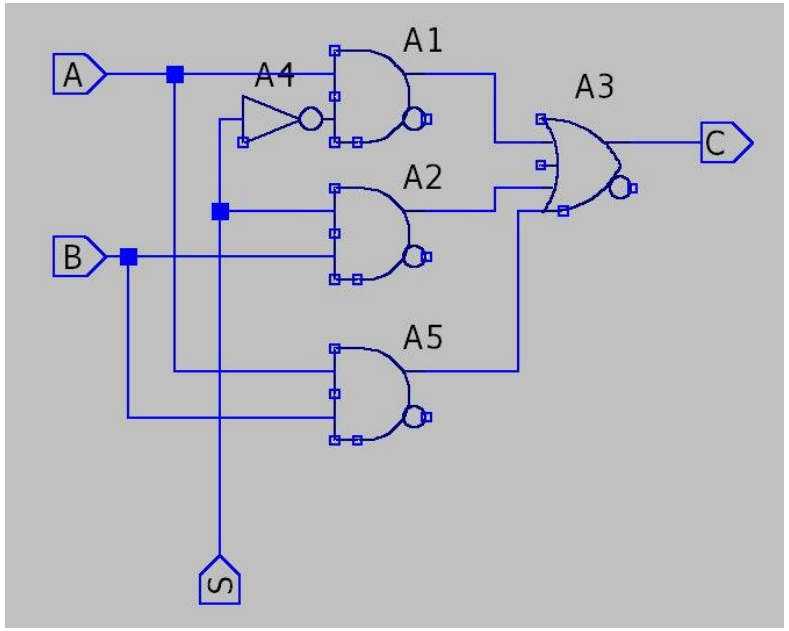
- L'obiettivo di questo progetto è realizzare un circuito sincrono che consente di sommare due numeri che verranno forniti da due registri sincroni.
- Il risultato finale della somma può essere salvato in un registro finale in base ad una delle seguenti modalità:
  - Il risultato viene sempre salvato nel registro d'uscita (MOD 0)
  - Il risultato viene salvato quando i numeri sommati sono uguali (MOD 1)
  - Il risultato viene salvato solo se l'operazione di somma genera un CarryOut (MOD 2)
- Il circuito è dotato dei segnali di Preset, Reset ed Enable.

# SPECIFICATIONS

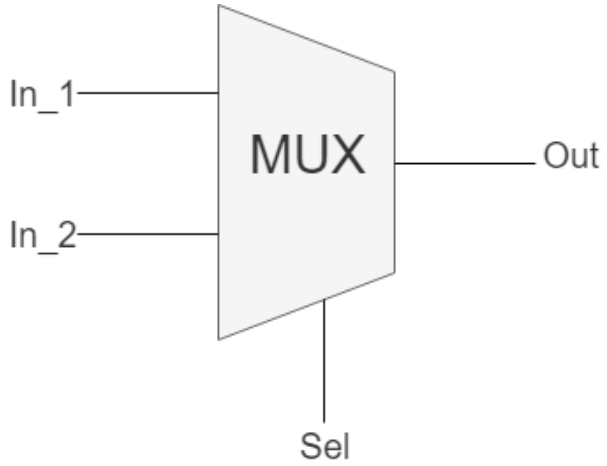



- Dato che l'Adder deve poter operare in 3 modalità abbiamo deciso che il segnale esterno «Mod» ha risoluzione di 2 bit. Abbiamo quindi associato ogni modalità al corrispettivo numero binario su 2 bit. La modalità inutilizzata (Mod = 11) è stata gestita mantenendo l'ultimo risultato calcolato.

- L'utilizzo di Preset e Reset deve essere mutualmente esclusivo; in caso contrario manteniamo i numeri presenti nei registri di ingresso.




| Signal | Direction | Resolution | Comments |
|---|---|---|---|
| In_1 | Input | 1 bit | Input data |
| In_2 | Input | 1 bit | Input data |
| Out | Output | 1 bit | Output data |
| Sel | Input | 1 bit | Selection |

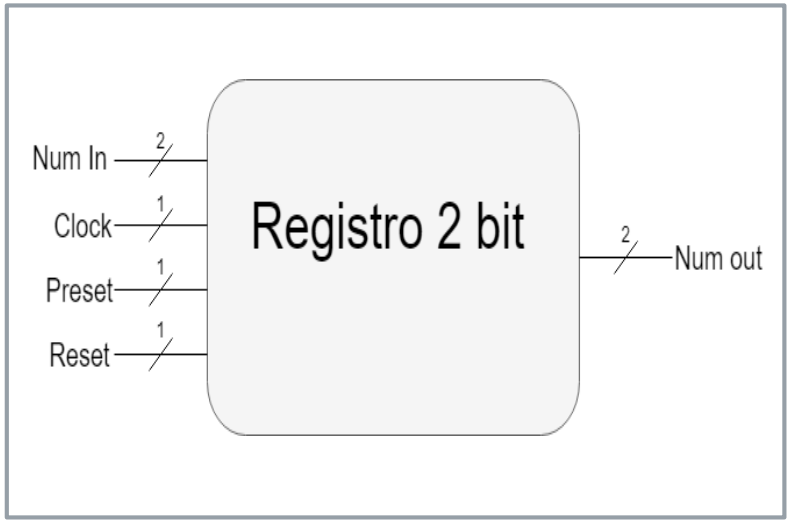


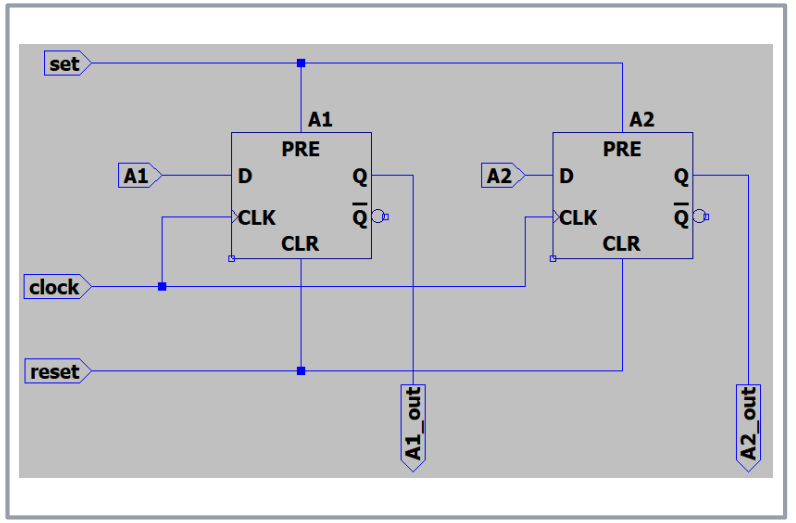

# COMPONENTI REALIZZATI

MULTIPLEXER

# COMPONENTI REALIZZATI

REGISTRO A 2 BIT



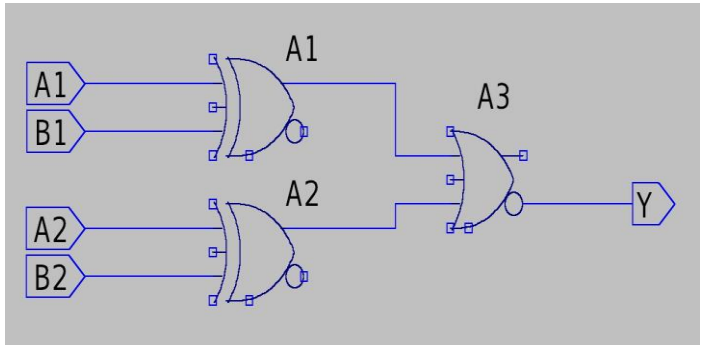




Pseudo-codice del registro a 2 bit

```
IF( (Preset = 0 AND Reset = 0) OR (Preset = 1 AND Reset = 1) )  then
        Num out = Num In
ELSIF (Preset = 1) then
        Num out = 1
ELSE
      Num out = 0
```

# COMPONENTI REALIZZATI

## DIGITAL COMPARATOR

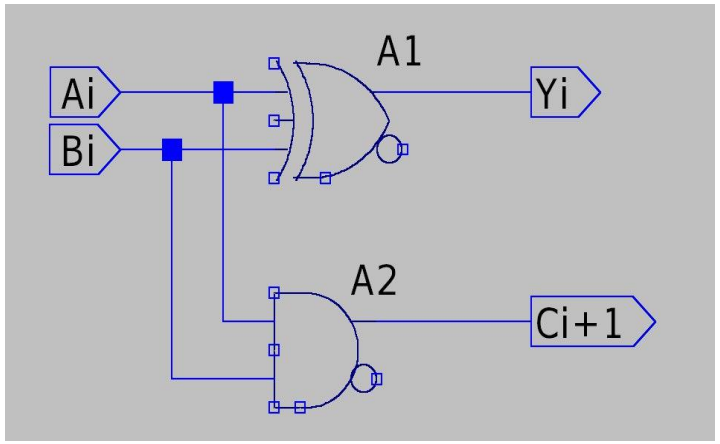


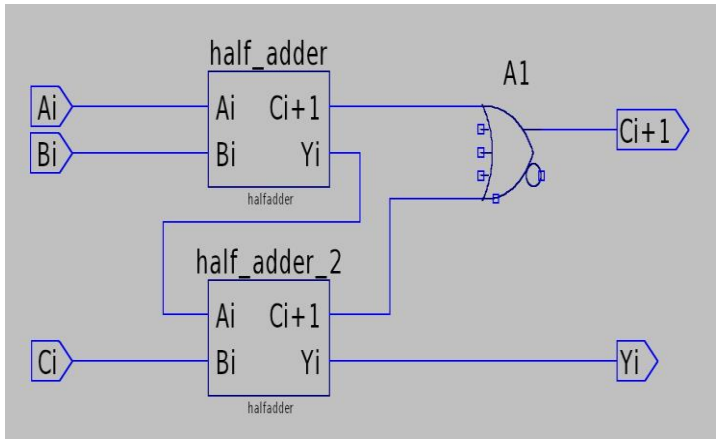


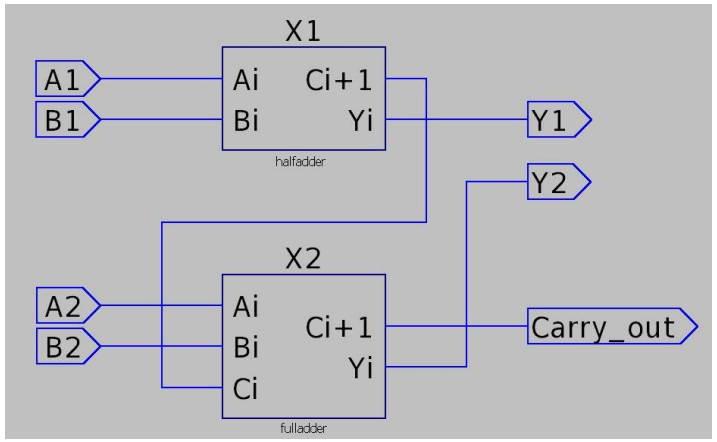
Pseudo-codice digital comparator

```
IF ( A = B ) then
  Y = 1
ELSE
  Y = 0
```

| Signal | Direction | Resolution | Comments |
|---|---|---|---|
| A | Input Number | 2 bit | Input data |
| B | Input Number | 2 bit | Input data |
| Y | Output | 1 bit | A=B |



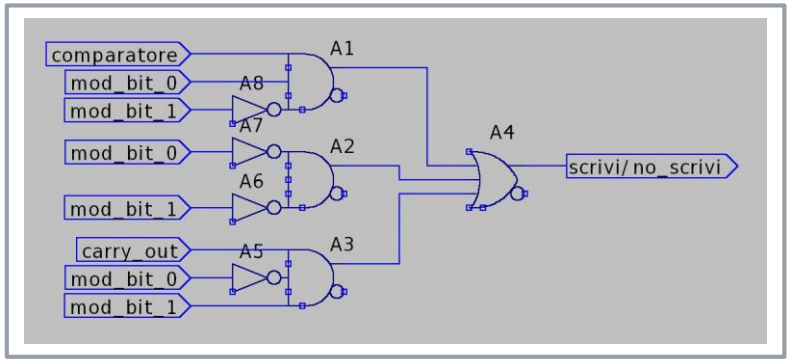



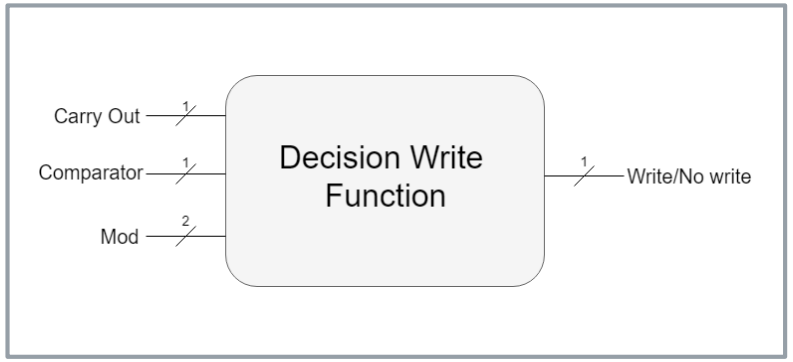

# COMPONENTI REALIZZATI

## FULL ADDER X2

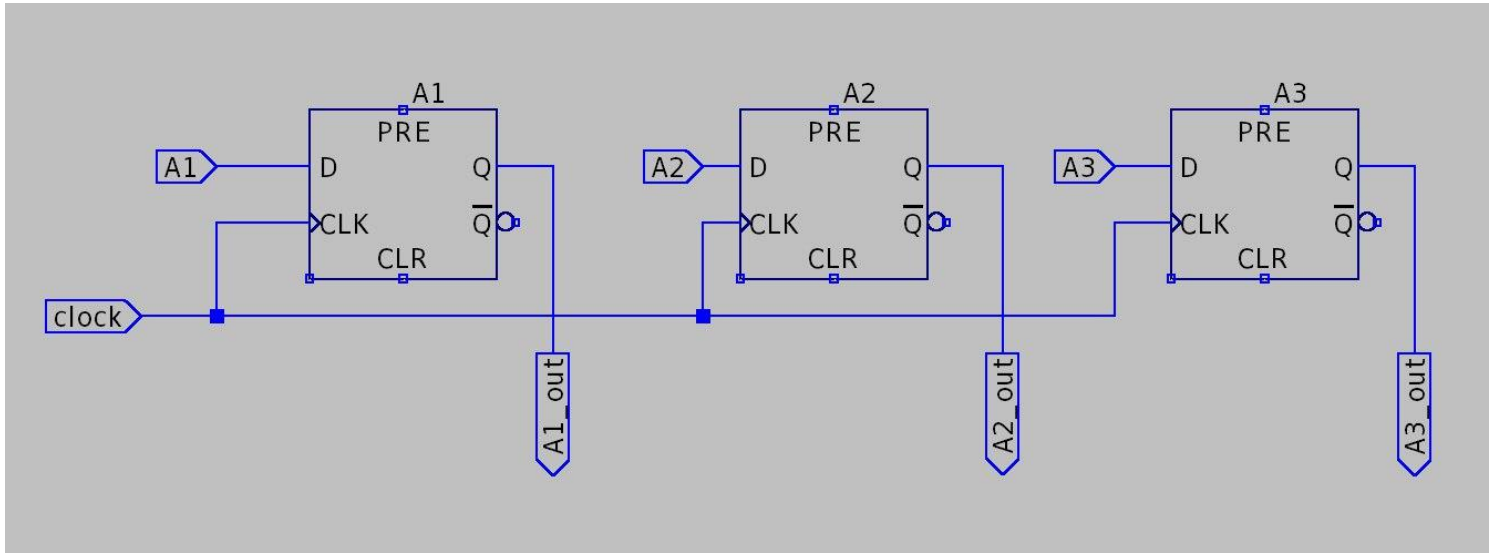
# COMPONENTI REALIZZATI

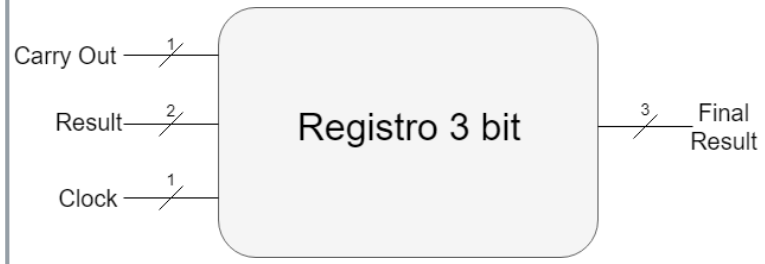
## DECISION WRITE FUNCTION




| Signal | Direction | Resolution | Comments |
|---|---|---|---|
| Carry out | Input | 1 bit | Input data |
| Comparator | Input | 1 bit | Input data |
| Mod | Input | 2 bit | Input data |
| Scrivi/no scrivi | Output | 1 bit | ( MOD=00)<br>OR (MOD=01 AND COMP=1)<br>OR (MOD=10 AND CARRY=1) |

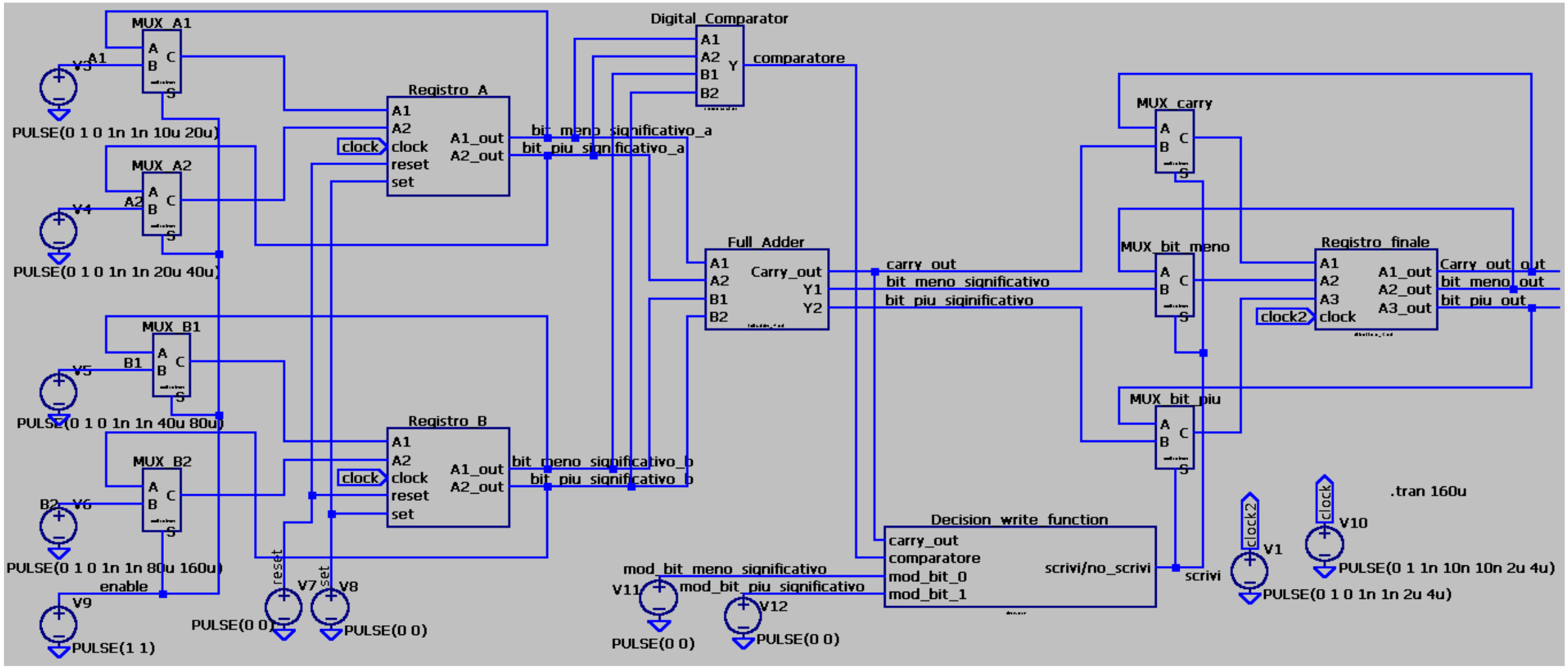


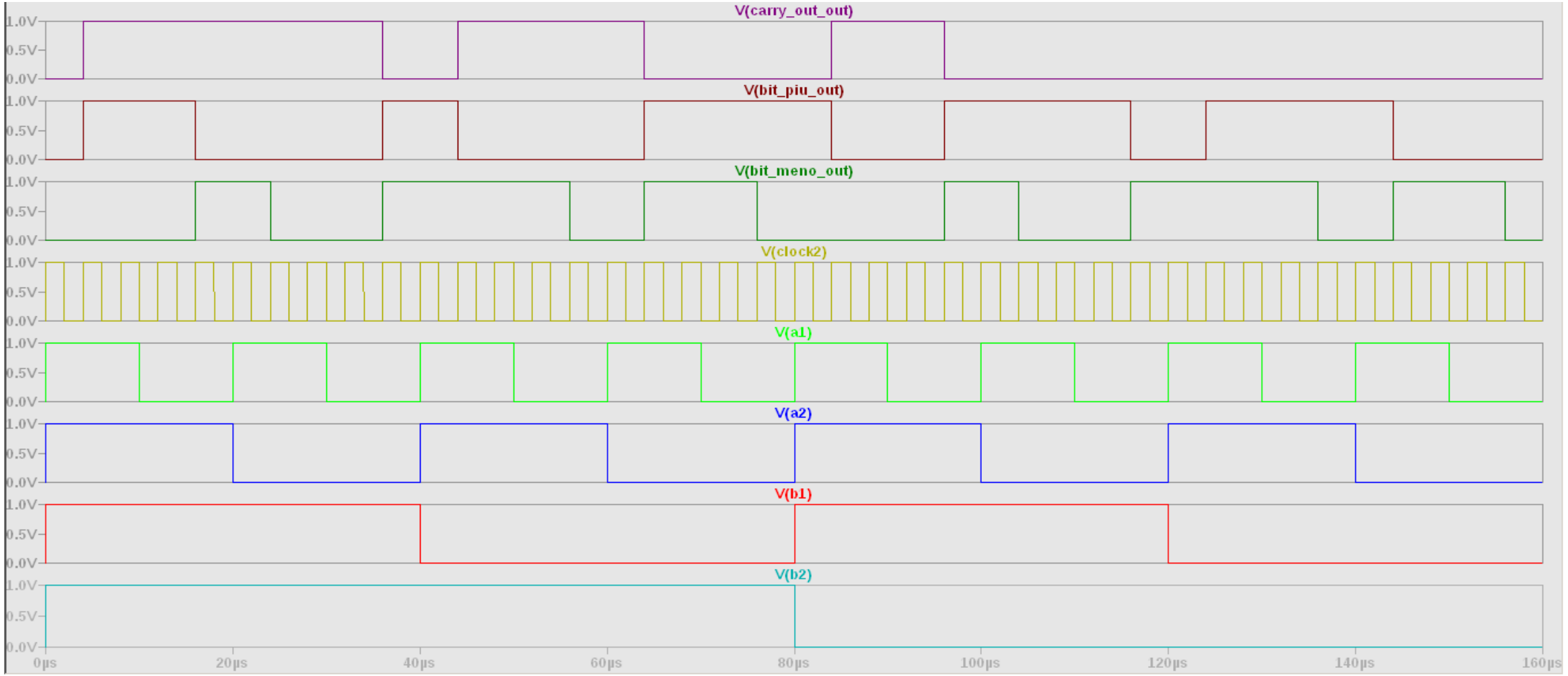

# COMPONENTI REALIZZATI

## REGISTRO A 3 BIT

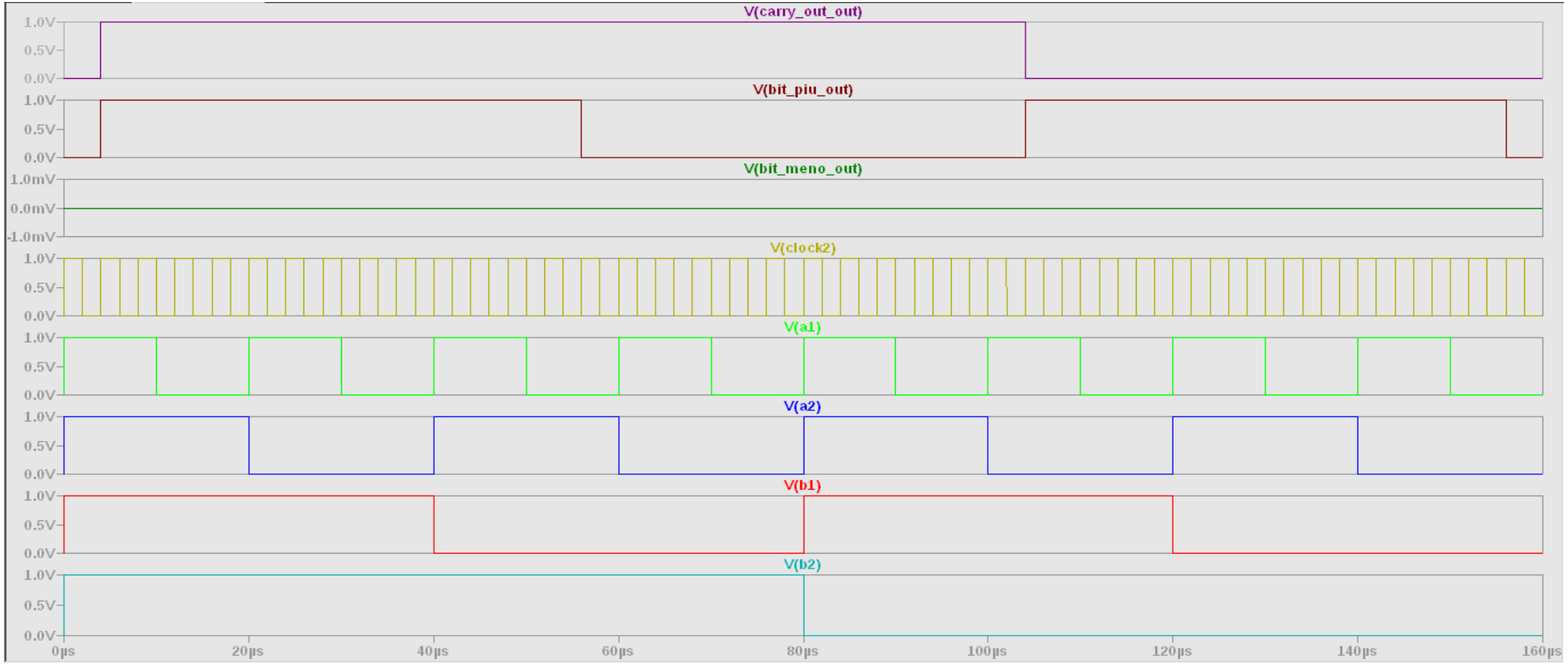
# TOP VIEW CIRCUITO



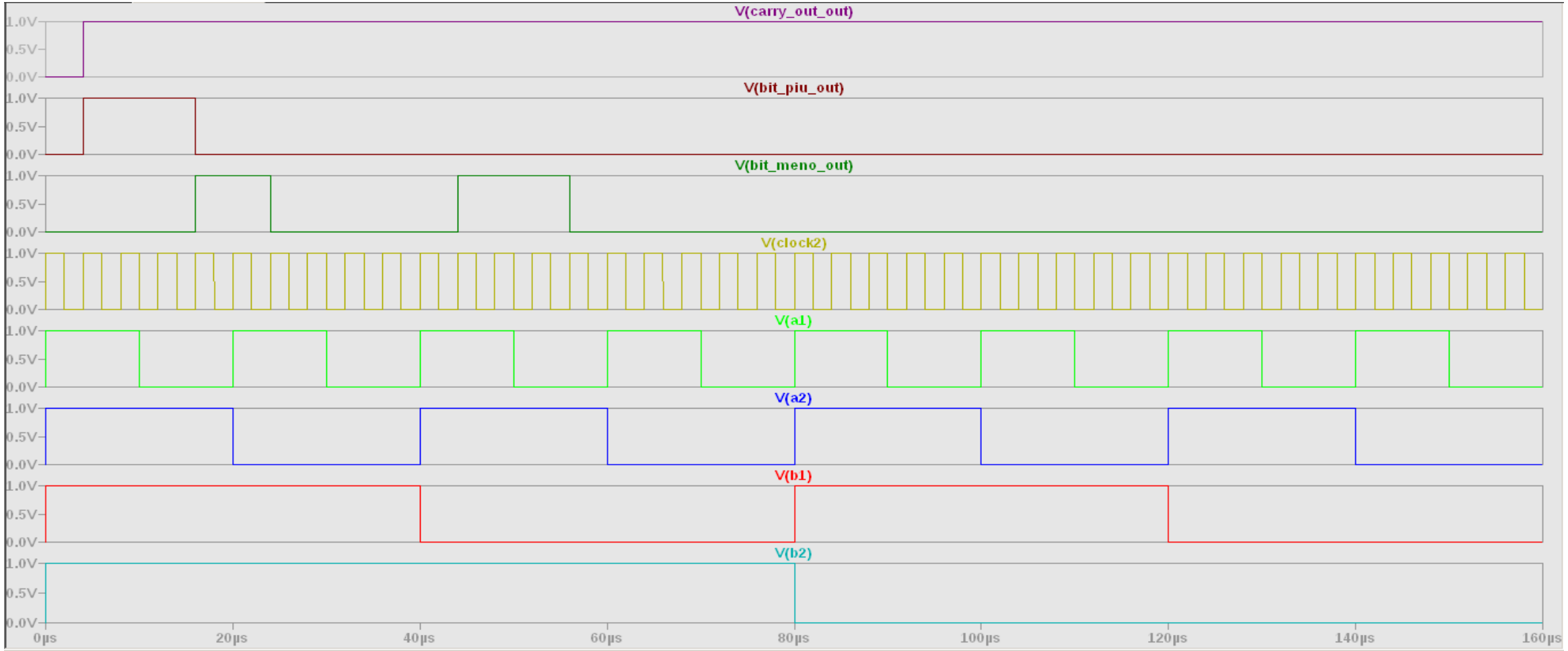
# TESTBENCH – MOD 0



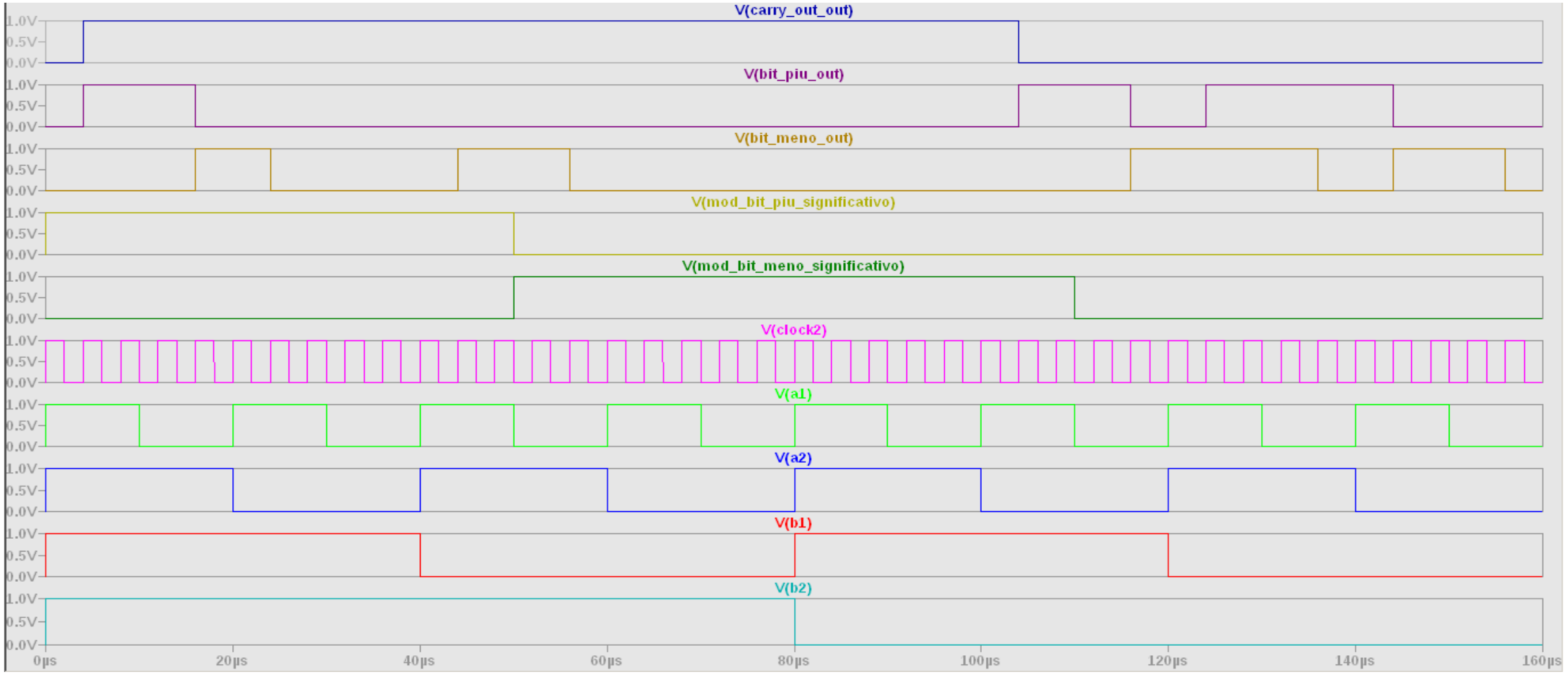
# TESTBENCH – MOD 1



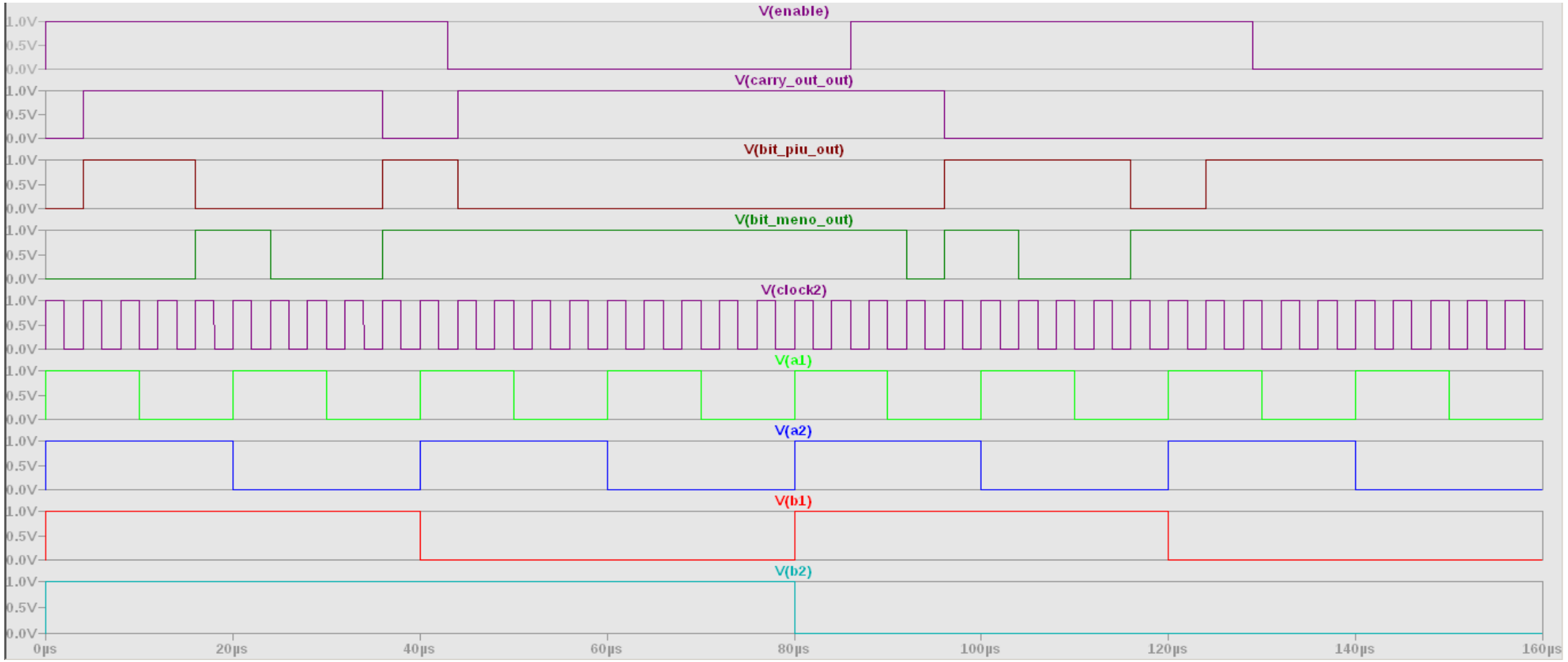
# TESTBENCH – MOD 2



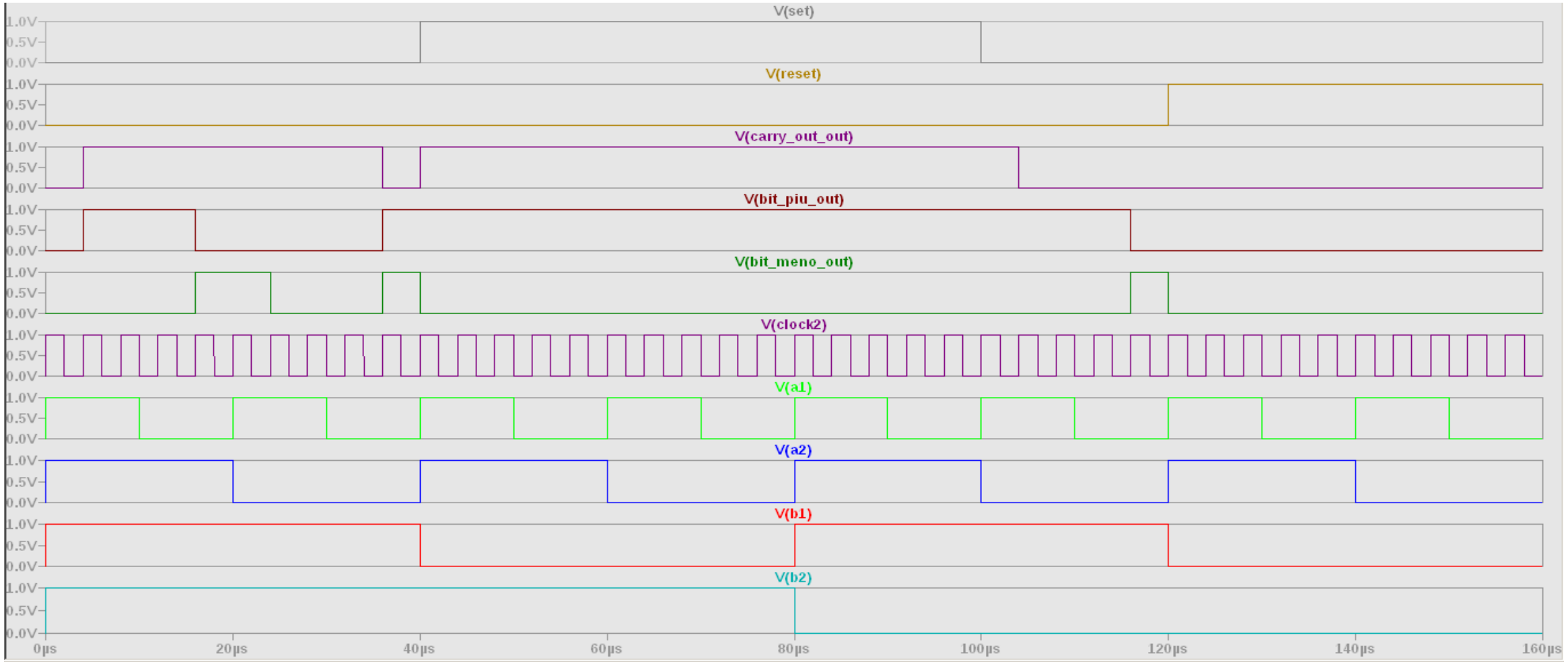
# TESTBENCH – RISULTATI AL VARIARE DI MOD



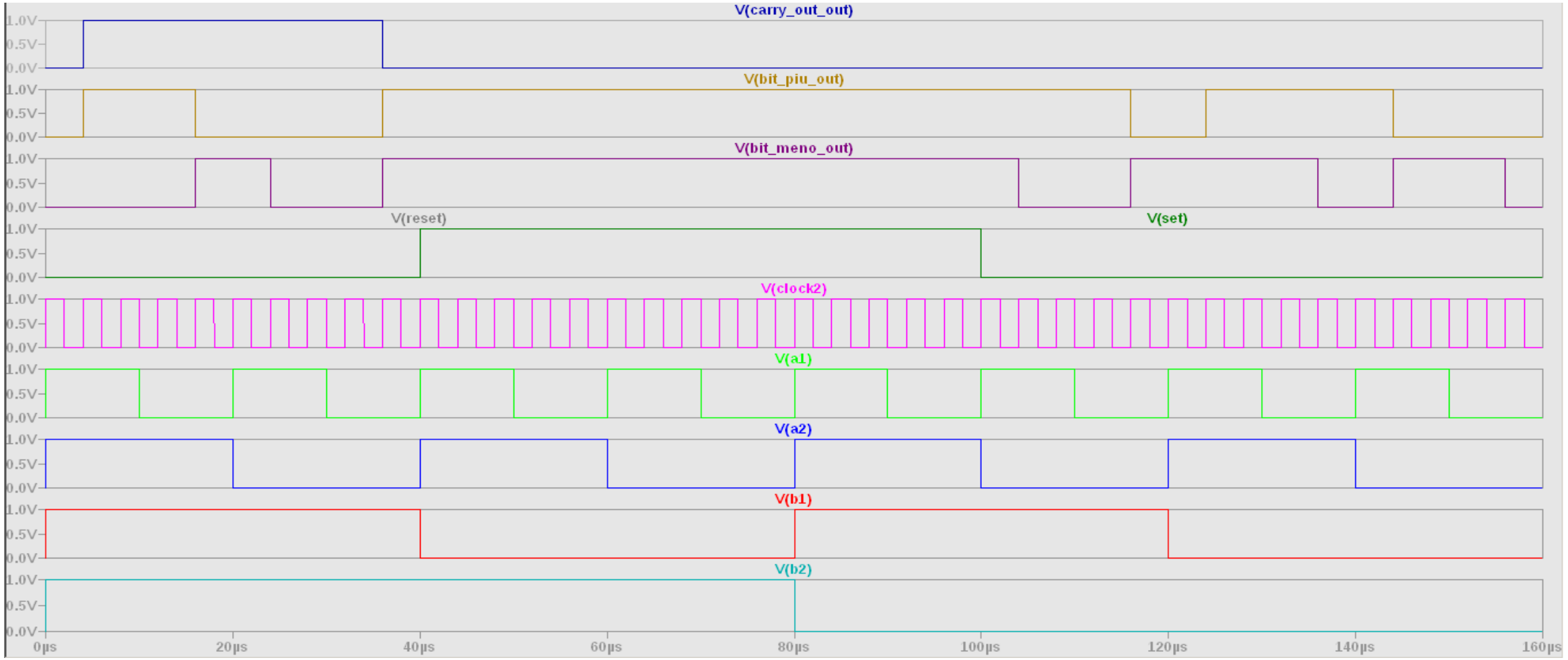
# TESTBENCH - ENABLE



# TESTBENCH – PRESET E RESET



# TESTBENCH – PRESET E RESET ATTIVI CONTEMPORANEAMENTE



# TESTBENCH – FAULT MANAGEMENT MOD 4 (MOD 11)