



Concordia University
**Engineering and
Computer Science**

COEN 313 PROJECT REPORT

Digital Systems Design II

Experiment Title: A Room Occupancy Monitoring System:
Design and Implementation

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**I certify that this submission is my original work and
meets the Faculty's Expectations of Originality**

Signature:

A handwritten signature in blue ink that reads "Fabio Binu Koshy".

Date: 2025 - 04 - 04

YYYY - MM - DD

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2. Direct quotations must not exceed 5% of the content of a report, must be enclosed in quotation marks, and must be attributed to the source by a numerical reference citation¹. Note that engineering reports rarely contain direct quotations.
3. Material paraphrased or taken from a source must be attributed to the source by a numerical reference citation.
4. Text that is inserted from a web site must be enclosed in quotation marks and attributed to the web site by numerical reference citation.
5. Drawings, diagrams, photos, maps or other visual material taken from a source must be attributed to that source by a numerical reference citation.
6. No part of any assignment, lab report or project report submitted for this course can be submitted for any other course.
7. In preparing your submissions, the work of other past or present students cannot be consulted, used, copied, paraphrased or relied upon in any manner whatsoever.
8. Your submissions must consist entirely of your own or your group's ideas, observations, calculations, information and conclusions, except for statements attributed to sources by numerical citation.
9. Your submissions cannot be edited or revised by any other student.
10. For lab reports, the data must be obtained from your own or your lab group's experimental work.
11. For software, the code must be composed by you or by the group submitting the work, except for code that is attributed to its sources by numerical reference.

You must write one of the following statements on each piece of work that you submit:

For individual work: **“I certify that this submission is my original work and meets the Faculty's Expectations of Originality”**, with your signature, I.D. #, and the date.

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A signed copy of this form must be submitted to the instructor at the beginning of the semester in each course.

I certify that I have read the requirements set out on this form, and that I am aware of these requirements. I certify that all the work I will submit for this course will comply with these requirements and with additional requirements stated in the course outline.

Course Number: COEN 313
Name: Fabio Binu Koshy
Signature: 

Instructor: Dr. Sébastien Le Beux
I.D. #: 40231803
Date: 2025-04-04

¹ Rules for reference citation can be found in “Form and Style” by Patrick MacDonagh and Jack Bordan, fourth edition, May, 2000, available at <http://www.encls.concordia.ca/scs/Forms/Form&Style.pdf>.

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Introduction

It has been made possible to determine and track the occupancy of any room to enhance the safety, comfort, and space efficiency in today's world with intelligent systems and automation. The current project being undertaken as part of the winter 2025 COEN313 Digital Design course is on designing and implementing a robust digital system that is capable of monitoring real-time room occupancy. This report will detail how the planning, development, and evaluation of a Room Occupancy Monitoring System that makes use of digital logic provides a dynamic, actionable solution adaptable for smart building applications.

The system employs two highly sensitive photocell sensors: the entrance and the exit. They are used to detect the presence of a person in the room. When a person passes through either doorway, the light will be interrupted, which will trigger a change in a binary signal, thus permitting the appropriate count to be increased or decreased. To ensure safety and adherence to the restrictions of the space, there are programmable maximum occupancy levels set via an 8-bit input signal. When this maximum occupancy is reached, the system asserts a dedicated `max_capacity` signal that effectively prevents any further entries until spaces are available.

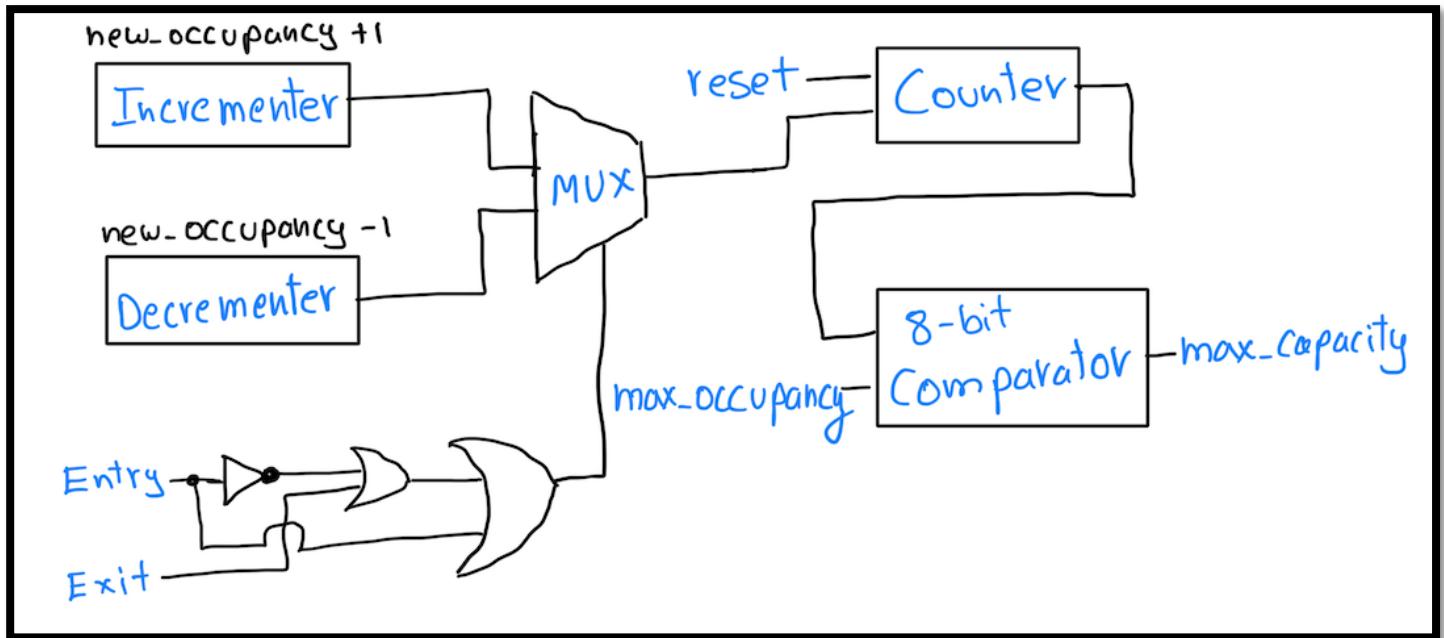
Moreover, the design consists of a reset function, which can also bring the system back to its initial state to allow accurate recounting from zero, if necessary. Therefore, the system guarantees flexibility and reliability across different use cases. The project is developed in Hardware Description Language (VHDL) and is simulated on Modelsim and synthesized and implemented on Xilinx Vivado. The report covers general descriptions of the system architecture, the VHDL implementation, simulation processes to validate the system's working and an analysis of the performance and resource usage of the system onto the FPGA platform.

Abstract

This project emphasizes on VHDL design and simulation of a digital system to monitor occupancy in a room. Two photocell binary inputs were utilized to detect entry and exit events at the doorways of the room while countering occupancy within. The maximum allowed occupancy is a programmable 8-bit input, which when reached by the counter-threshold, generates a signal to max_capacity, which disallows any further entries into the room until there is free space.

It has a reset that brings the system back to the original state for accurate tracking in multiple instances. The design encapsulates the increment/decrement logic, threshold check comparators, flip-flops to hold their states, and control logic signal handlers. The system is rigorously simulated in Modelsim to validate the entrance/exit sequence, threshold change, and reset. Design timing/logic utilization and efficiency targeting an FPGA have been determined by its synthesis in Xilinx Vivado.

Conceptual Diagram



Photocell Sensors:

Photocell Entrance: Entry

Photocell Exit: Exit

Occupancy Counter

- Tracks the number of people using an 8-bit unsigned signal (range: 0 to 255).
- Increments if Entry = '1' and Exit = '0', and occupancy < max_occupancy.
- Decrements if Entry = '1' and Exit = '1', and occupancy > 0.
- Resets occupancy count and max_capacity when reset = '1'.
- All operations are synchronized with the rising edge of the clk signal.
- Activates the max_capacity signal when occupancy equals max_occupancy.

Design Methodology

The system of monitoring room occupancy for logic is based on VHDL design, which directly counts the number of people entering and exiting the room in real-time. Identifying maximum room capacity is done through a programmable threshold, and the system is meant to be synthesized on Xilinx Nexys A7 FPGA. Edge detection and comparison mechanisms make the architecture feasible in counting people accurately.

Entity: room_occupancy_monitor

The system interface is defined in the room_occupancy_monitor entity. This includes input ports for the clock (clk), reset (reset), entry trigger (entrance_photocell), exit trigger (exit_photocell), and an 8-bit input, max_threshold, used to set the maximum number of people that can be allowed in the room. The outputs provide occupancy, representing the number of individuals inside, and max_capacity, a flag indicating the room has reached or exceeded the threshold.

Architecture: Behavioral

The functional logic of the system gets realized by the Behavioral architectures. It contains numerous internal signals including entrance_delay, exit_delay, entrance_pulse, and exit_pulse for edge detection-current_count, an unsigned 8-bit signal, stores the current room occupancy, along with a count that holds the threshold converted from max_threshold input. These signals form the basis for coordinating events of entering/leaving a room and updating the internal occupancy counter. The architecture, therefore, comprises three subprocesses: entrance edge detection, exit edge detection, and counting occupancy.

Occupancy Counter Process

This is the occupancy counter whose rising edge is clock sensitive and is made use of in incrementing or decrementing an occupancy value. Incrementing the counter happens in terms of entering with an entrance_pulse before the current occupancy reaches maximum threshold (max_count) or decrementing it via exiting through an exit_pulse when occupancy is more than zero. This logic keeps the correct recording of the individuals in the room while shielding the device against going beyond its upper or lower limits. The continuously available occupancy value is fed into the occupancy output that visualizes this by 8 LEDs.

Reset Condition

This system incorporates an asynchronous reset condition to ensure that a safe initialization can be ensured. Asserting the reset signal results in the clearing of current_count to zero immediately. Furthermore, the entrance_delay, exit_delay, entrance_pulse, and exit_pulse signals can also be returned to their default values, thus avoiding any possibility of creating a false triggering after the release of the reset. This condition guarantees that the system will always commence operation from an initialized, well-defined state that eliminates any undefined behaviors during simulation or deployment.

Comparator Logic

The comparator would always check for its existing occupancy status with respect to the defined max_threshold. This whole process is being done by comparing internal current_count signal against max_count. If the current_count is greater than or equals max_count, the max_capacity is '1', declaring the room is full. If it is lower than the mentioned threshold, it remains '0'. This can be used to drive a red LED that will signal immediately to users when maximum capacity is reached, immediately visualising this for them.

Output Behavior

System outputs measure the 8-bit occupancy signal, which is mapped to eight LEDs to show the current count in binary format, and max_capacity signal, which can be connected to an indicator LED. Thus monitoring room status in real-time and ensuring the system does not go above the configured occupancy limits.

Codes:

VHDL code: room_occupancy_code.vhd

```
-- COEN313 Digital Design Project
-- room_occupancy_monitor.vhd
-- Student Name: Fabio BInu Koshy
-- ID : 40231803
-- Date: Winter 2025

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity room_occupancy_monitor is
    Port (
        clk           : in STD_LOGIC;
        reset         : in STD_LOGIC;
        entrance_photocell: in STD_LOGIC;
        exit_photocell   : in STD_LOGIC;
        max_threshold  : in STD_LOGIC_VECTOR(7 downto 0);
        max_capacity   : out STD_LOGIC;
        occupancy      : out STD_LOGIC_VECTOR(7 downto 0)
    );
end room_occupancy_monitor;

architecture Behavioral of room_occupancy_monitor is

    signal entrance_delay  : STD_LOGIC := '0';
    signal exit_delay       : STD_LOGIC := '0';
    signal entrance_pulse  : STD_LOGIC;
    signal exit_pulse       : STD_LOGIC;
    signal current_count   : UNSIGNED(7 downto 0) := (others => '0');
    signal max_count        : UNSIGNED(7 downto 0);

begin

    max_count <= UNSIGNED(max_threshold);

    entrance_edge_detect: process(clk, reset)
    begin
        if reset = '1' then
            entrance_delay <= '0';
            entrance_pulse <= '0';
        elsif rising_edge(clk) then
            entrance_delay <= entrance_photocell;
            entrance_pulse <= '0';
            if entrance_delay = '1' and entrance_photocell = '0' then
                entrance_pulse <= '1';
            end if;
        end if;
    end process;
```

```

exit_edge_detect: process(clk, reset)
begin
    if reset = '1' then
        exit_delay <= '0';
        exit_pulse <= '0';
    elsif rising_edge(clk) then
        exit_delay <= exit_photocell;
        exit_pulse <= '0';
        if exit_delay = '1' and exit_photocell = '0' then
            exit_pulse <= '1';
        end if;
    end if;
end process;

counter: process(clk, reset)
begin
    if reset = '1' then
        current_count <= (others => '0');
    elsif rising_edge(clk) then
        if entrance_pulse = '1' and current_count < max_count then
            current_count <= current_count + 1;
        elsif exit_pulse = '1' and current_count > 0 then
            current_count <= current_count - 1;
        end if;
    end if;
end process;

max_capacity <= '1' when current_count >= max_count else '0';
occupancy <= STD_LOGIC_VECTOR(current_count);

end Behavioral;

```

Testbench code: tb_room_occupancy_monitor.vhd

```
-- COEN313 Digital Design Project
-- tb_room_occupancy_moitor.vhd
-- Student Name: Fabio Binu Koshy
-- ID : 40231803
-- Date: Winter 2025

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity tb_room_occupancy_monitor is
end tb_room_occupancy_monitor;

architecture Behavioral of tb_room_occupancy_monitor is
component room_occupancy_monitor
    Port (
        clk           : in STD_LOGIC;
        reset         : in STD_LOGIC;
        entrance_photocell: in STD_LOGIC;
        exit_photocell   : in STD_LOGIC;
        max_threshold  : in STD_LOGIC_VECTOR(7 downto 0);
        max_capacity   : out STD_LOGIC;
        occupancy      : out STD_LOGIC_VECTOR(7 downto 0)
    );
end component;

signal clk           : STD_LOGIC := '0';
signal reset         : STD_LOGIC := '0';
signal entrance_photocell: STD_LOGIC := '1';
signal exit_photocell   : STD_LOGIC := '1';
signal max_threshold  : STD_LOGIC_VECTOR(7 downto 0) := "000000101";

signal max_capacity   : STD_LOGIC;
signal occupancy      : STD_LOGIC_VECTOR(7 downto 0);

constant clk_period     : time := 10 ns;

begin
    uut: room_occupancy_monitor
        Port map (
            clk           => clk,
            reset         => reset,
            entrance_photocell => entrance_photocell,
            exit_photocell   => exit_photocell,
            max_threshold  => max_threshold,
            max_capacity   => max_capacity,
            occupancy      => occupancy
        );

```

```

clk_process: process
begin
    clk <= '0';
    wait for clk_period/2;
    clk <= '1';
    wait for clk_period/2;
end process;

stim_proc: process

procedure person_enters is
begin
    entrance_photocell <= '0';
    wait for 30 ns;
    entrance_photocell <= '1';
    wait for 30 ns;
end procedure;

procedure person_exits is
begin
    exit_photocell <= '0';
    wait for 30 ns;
    exit_photocell <= '1';
    wait for 30 ns;
end procedure;

begin
    report "Test Case 0: Initial reset";
    reset <= '1';
    wait for 100 ns;
    reset <= '0';
    wait for 100 ns;

    -- Test Case 1: People entering the room one by one until max capacity
    report "Test Case 1: People entering the room until max capacity";

    -- Person 1 enters
    person_enters;
    wait for 20 ns;
    assert unsigned(occupancy) = 1
        report "Failed: Count should be 1 after first person enters"
        severity note;
    -- Person 2 enters
    person_enters;
    wait for 20 ns;
    assert unsigned(occupancy) = 2
        report "Failed: Count should be 2 after second person enters"
        severity note;

    -- Person 3 enters
    person_enters;
    wait for 20 ns;
    assert unsigned(occupancy) = 3
        report "Failed: Count should be 3 after third person enters"
        severity note;

    -- Person 4 enters
    person_enters;
    wait for 20 ns;
    assert unsigned(occupancy) = 4
        report "Failed: Count should be 4 after fourth person enters"
        severity note;

    -- Person 5 enters (should reach max capacity)
    person_enters;
    wait for 20 ns;
    assert unsigned(occupancy) = 5
        report "Failed: Count should be 5 after fifth person enters"
        severity note;
    assert max_capacity = '1'
        report "Failed: Max capacity signal should be asserted"
        severity note;

```

```

-- Test Case 2: Attempt to enter when full
report "Test Case 2: Attempt to enter when full";
person_enters;
wait for 20 ns;
assert unsigned(occupancy) = 5
    report "Failed: Count should remain 5 when full"
    severity note;

-- Test Case 3: People exiting the room one by one
report "Test Case 3: People exiting the room one by one";

-- Person 1 exits
person_exits;
wait for 20 ns;
assert unsigned(occupancy) = 4
    report "Failed: Count should be 4 after one person exits"
    severity note;
assert max_capacity = '0'
    report "Failed: Max capacity signal should be deasserted"
    severity note;

-- Person 2 exits
person_exits;
wait for 20 ns;
assert unsigned(occupancy) = 3
    report "Failed: Count should be 3 after second person exits"
    severity note;

-- Test Case 4: Simultaneous entry and exit (should cancel out)
report "Test Case 4: Simultaneous entry and exit";
entrance_photocell <= '0';
exit_photocell <= '0';
wait for 30 ns;
entrance_photocell <= '1';
exit_photocell <= '1';
wait for 30 ns;
assert unsigned(occupancy) = 3
    report "Failed: Count should remain 3 after simultaneous entry/exit"
    severity note;

-- Test Case 5: Multiple entries followed by reset
report "Test Case 5: Multiple entries followed by reset";
for i in 1 to 2 loop
    person_enters;
    wait for 20 ns;
end loop;
assert unsigned(occupancy) = 5
    report "Failed: Count should be 5 after two more people enter"
    severity note;
assert max_capacity = '1'
    report "Failed: Max capacity signal should be asserted again"
    severity note;

```

```

reset <= '1';
wait for 50 ns;
reset <= '0';
wait for 50 ns;
assert unsigned(occupancy) = 0
    report "Failed: Count should be 0 after reset"
    severity note;
assert max_capacity = '0'
    report "Failed: Max capacity signal should be deasserted after reset"
    severity note;

-- Test Case 6: Testing with different max threshold
report "Test Case 6: Testing with different max threshold";

-- Add 2 people
for i in 1 to 2 loop
    person_enters;
    wait for 20 ns;
end loop;

-- Change threshold to 2
max_threshold <= "00000010"; -- Change max to 2
wait for 50 ns;

-- Should now be at max capacity with 2 people
assert max_capacity = '1'
    report "Failed: Max capacity should be asserted with new threshold of 2"
    severity note;

-- Test Case 7: Try to decrement below zero
report "Test Case 7: Try to decrement below zero";
reset <= '1';
wait for 50 ns;
reset <= '0';
wait for 50 ns;

```

```

-- Try exiting when count is already zero
person_exits;
wait for 20 ns;
assert unsigned(occupancy) = 0
    report "Failed: Count should remain 0 when trying to go below zero"
    severity note;

-- Test Case 8: Rapid succession of entries and exits
report "Test Case 8: Rapid succession of entries and exits";

-- Quick succession of 3 entries
for i in 1 to 3 loop
    entrance_photocell <= '0';
    wait for 20 ns;
    entrance_photocell <= '1';
    wait for 20 ns;
end loop;

wait for 20 ns;
assert unsigned(occupancy) = 3
    report "Failed: Count should be 3 after rapid entries"
    severity note;
assert max_capacity = '1'
    report "Failed: Max capacity should be asserted (3 > 2)"
    severity note;

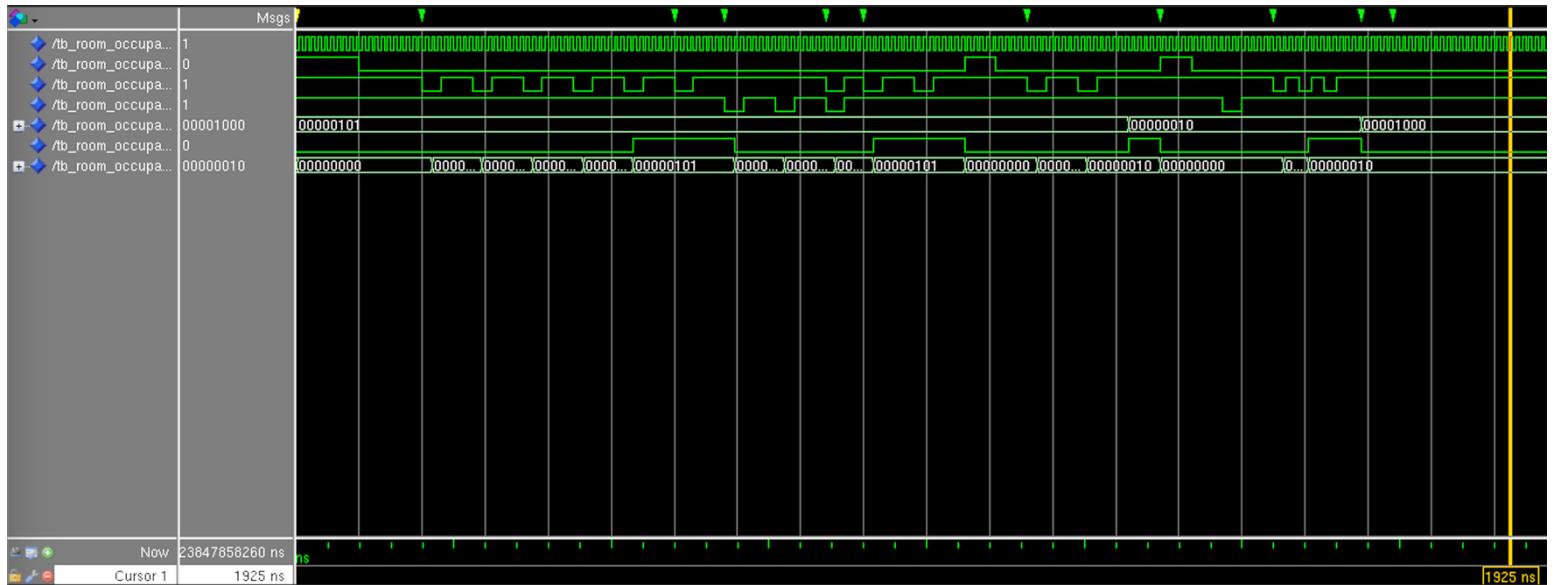
-- Change max threshold to higher value
report "Test Case 9: Change threshold to higher value";
max_threshold <= "00001000"; -- Change max to 8
wait for 50 ns;

assert max_capacity = '0'
    report "Failed: Max capacity should be deasserted with new threshold of 8"
    severity note;

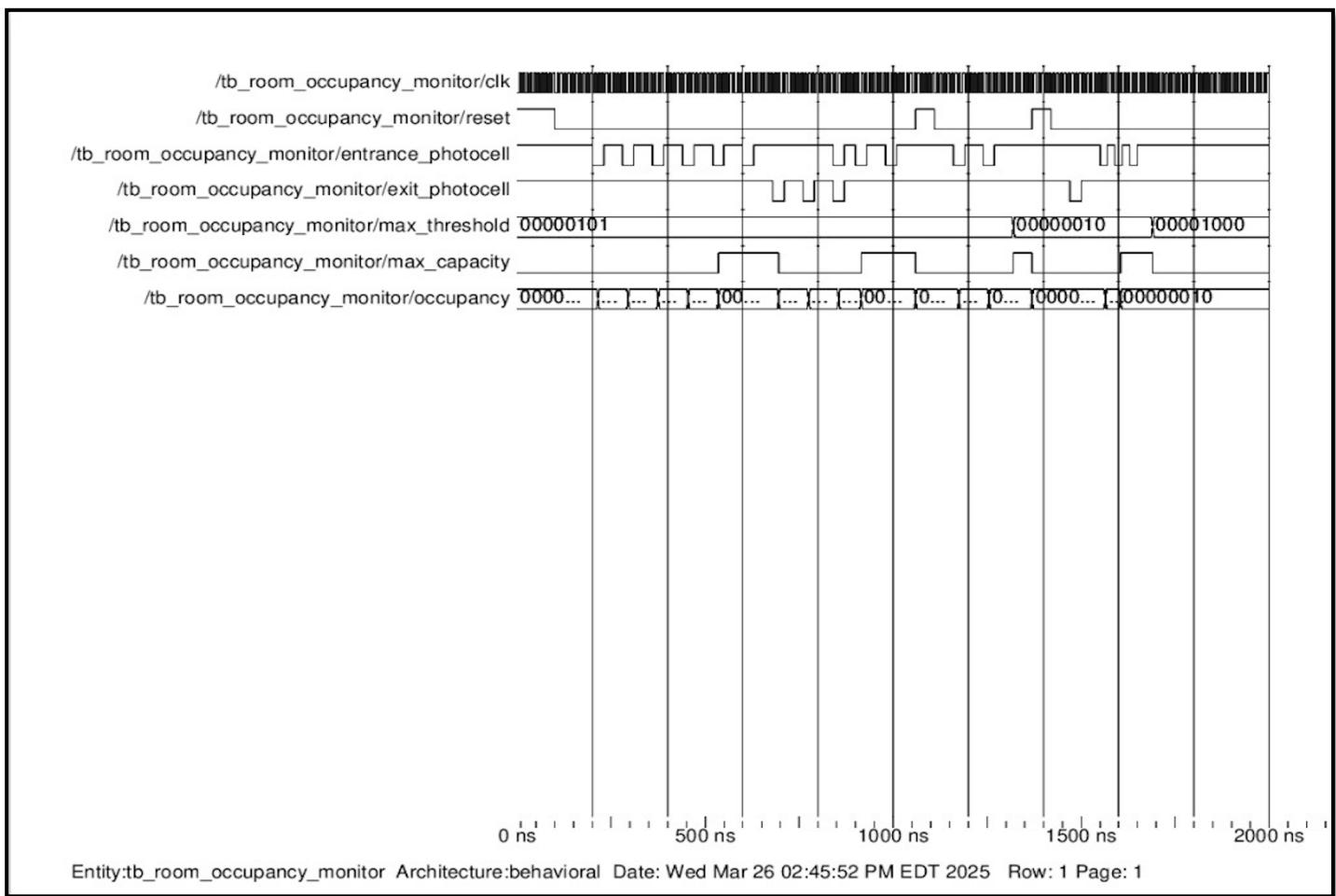
report "Test completed successfully";
wait;
end process;
end Behavioral;

```

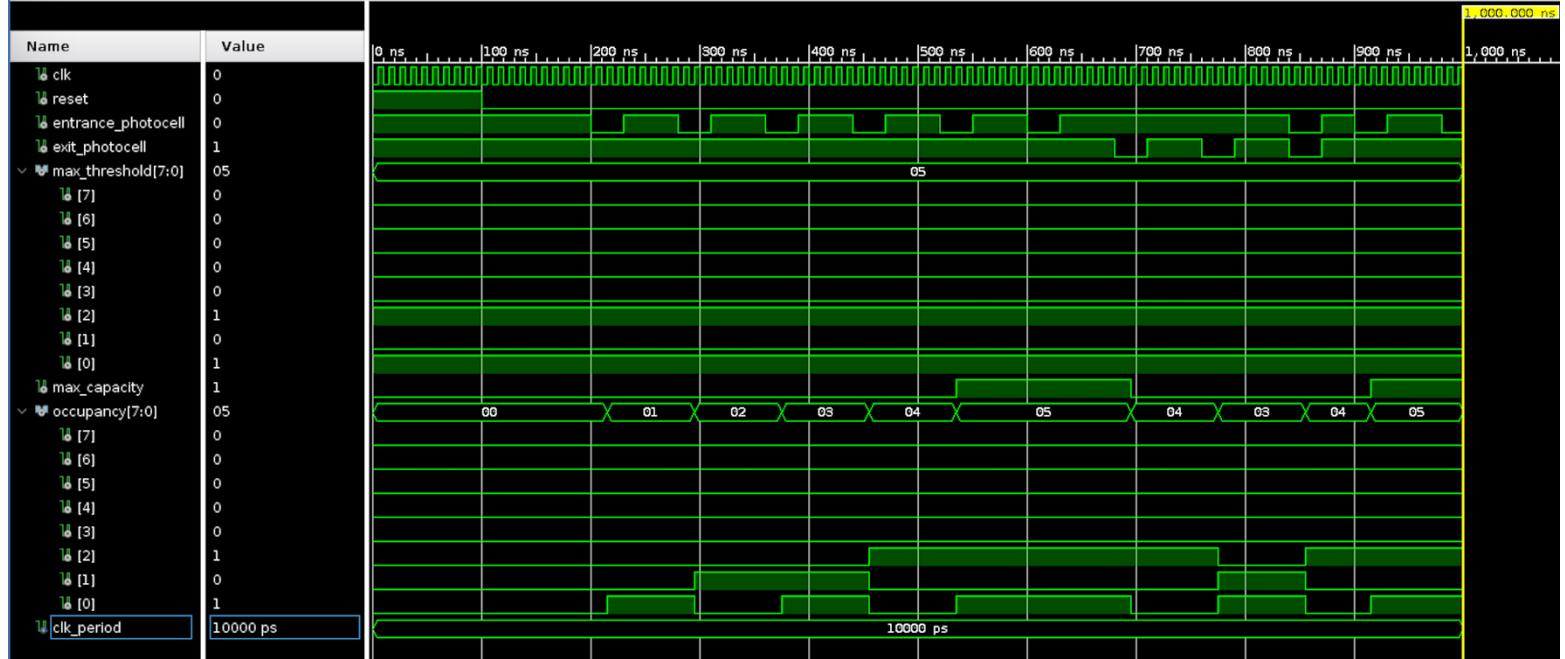
Simulation and Synthesis Results



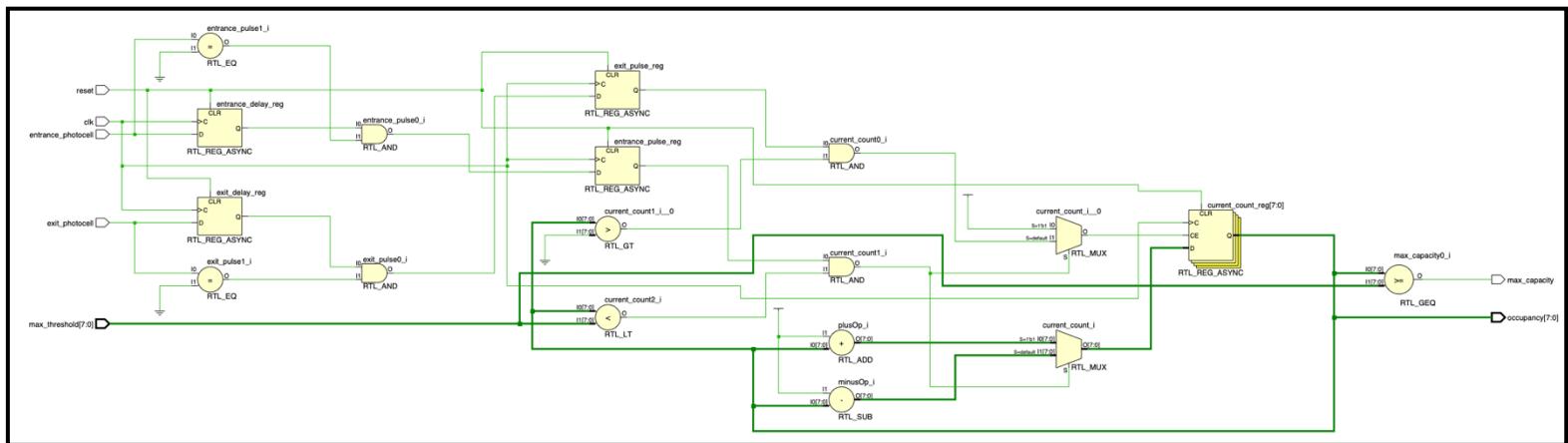
ModelSim Simulation(Above:Image, Below:Postscript)



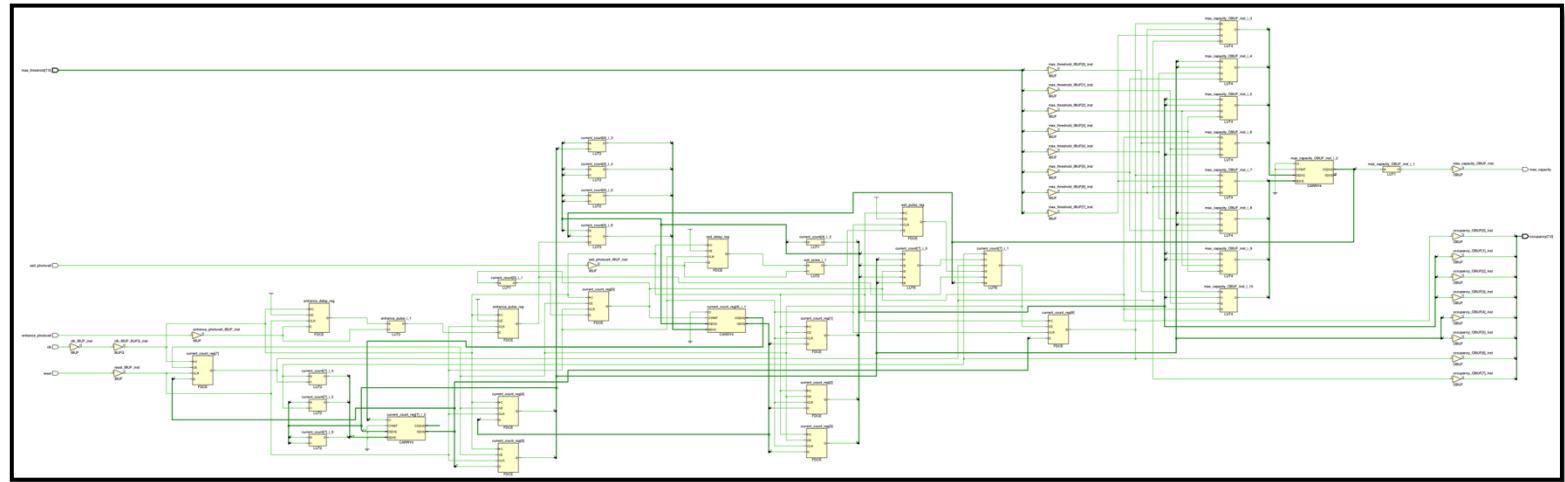
Vivado Simulation Run



Elaborated RTL Design



Elaborated Synthesis Design



Quality of the VHDL code

The module `room_occupancy_monitor` offers a neat and expandable VHDL design for the occupancy of a room. It has clean process separation between its edge detection and counting logic, which modularizes and clarifies things. The support for occupancy and `max_threshold` in 8 bits makes it more flexible than smaller-width designs. Also, clock and reset signals are handled well in the testbench, which has clear procedures to simulate real-world situations. The code is readable and synthesizable, but there are some improvements regarding descriptive comments. Great VHDL practice and deployment on FPGA are best shown by such a design.

Vivado Log Files:

runme.log(Implementation)

*** Running vivado

with args -log room_occupancy_monitor.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source room_occupancy_monitor.tcl -notrace

***** Vivado v2018.2 (64-bit)

**** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

**** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source room_occupancy_monitor.tcl -notrace

Command: link_design -top room_occupancy_monitor -part xc7a100tcsg324-1

Design is defaulting to srcset: sources_1

Design is defaulting to constrset: constrs_1

INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

6 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link_design completed successfully

link_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:14 . Memory (MB): peak = 1591.355 ; gain = 283.215 ; free physical = 12260 ; free virtual = 23487

Command: opt_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1683.383 ; gain = 92.027 ; free physical = 12252 ; free virtual = 23479

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: e9e104da

Time (s): cpu = 00:00:07 ; elapsed = 00:00:19 . Memory (MB): peak = 2109.879 ; gain = 426.496 ; free physical = 11807 ; free virtual = 23061

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: e9e104da

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: e9e104da

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: edeb45e3

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: edeb45e3

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 1115d28f5

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 1115d28f5

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2109.883 ; gain = 0.000 ; free physical = 11846 ; free virtual = 23100

Ending Logic Optimization Task | Checksum: 1115d28f5

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.05 . Memory (MB): peak = 2109.883 ; gain = 0.004 ; free physical = 11846 ; free virtual = 23100

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 1115d28f5

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2109.883 ; gain = 0.000 ; free physical = 11846 ; free virtual = 23100

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 1115d28f5

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2109.883 ; gain = 0.000 ; free physical = 11846 ; free virtual = 23100

INFO: [Common 17-83] Releasing license: Implementation

22 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt_design completed successfully

opt_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:21 . Memory (MB): peak = 2109.883 ; gain = 518.527 ; free physical = 11846 ; free virtual = 23100

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint
'/nfs/home/f/f_koshy/p/project/project.runs/impl_1/room_occupancy_monitor_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report_drc -file
room_occupancy_monitor_drc_opted.rpt -pb
room_occupancy_monitor_drc_opted.pb -rpx
room_occupancy_monitor_drc_opted.rpx

Command: report_drc -file room_occupancy_monitor_drc_opted.rpt -pb
room_occupancy_monitor_drc_opted.pb -rpx
room_occupancy_monitor_drc_opted.rpx

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file
'/nfs/home/f/f_koshy/p/project/project.runs/impl_1/room_occupancy_monitor_drc_opted.rpt'.

report_drc completed successfully

Command: place_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Running DRC as a precondition to command place_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2173.914 ; gain = 0.000 ; free physical = 11803 ; free virtual = 23057

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 2e19ba64

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2173.914 ; gain = 0.000 ; free physical = 11803 ; free virtual = 23057

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2173.914 ; gain = 0.000 ; free physical = 11803 ; free virtual = 23057

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 612d865a

Time (s): cpu = 00:00:00.82 ; elapsed = 00:00:00.40 . Memory (MB): peak = 2220.926 ; gain = 47.012 ; free physical = 11789 ; free virtual = 23046

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: e6936028

Time (s): cpu = 00:00:00.87 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2220.926 ; gain = 47.012 ; free physical = 11791 ; free virtual = 23048

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: e6936028

Time (s): cpu = 00:00:00.87 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2220.926 ; gain = 47.012 ; free physical = 11791 ; free virtual = 23048

Phase 1 Placer Initialization | Checksum: e6936028

Time (s): cpu = 00:00:00.87 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2220.926 ; gain = 47.012 ; free physical = 11791 ; free virtual = 23048

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: e6936028

Time (s): cpu = 00:00:00.90 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2220.926 ; gain = 47.012 ; free physical = 11789 ; free virtual = 23046

WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 119f466db

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.70 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11762 ; free virtual = 23020

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 119f466db

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.70 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11762 ; free virtual = 23020

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 92c5d556

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.71 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11763 ; free virtual = 23020

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 145619bed

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.72 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11763 ; free virtual = 23020

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 145619bed

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.72 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11763 ; free virtual = 23020

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11759 ; free virtual = 23017

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11759 ; free virtual = 23017

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11759 ; free virtual = 23017

Phase 3 Detail Placement | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11759 ; free virtual = 23017

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.79 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11759 ; free virtual = 23017

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.80 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11761 ; free virtual = 23018

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: d0b813fb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.80 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11761 ; free virtual = 23018

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: cc59832e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.80 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11761 ; free virtual = 23018

Phase 4 Post Placement Optimization and Clean-Up | Checksum: cc59832e

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.80 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11761 ; free virtual = 23018

Ending Placer Task | Checksum: b7756f2f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.80 . Memory (MB): peak = 2360.988 ; gain = 187.074 ; free physical = 11778 ; free virtual = 23035

INFO: [Common 17-83] Releasing license: Implementation

39 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

place_design completed successfully

WARNING: [Constraints 18-5210] No constraint will be written out.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.27 .

Memory (MB): peak = 2360.988 ; gain = 0.000 ; free physical = 11776 ; free virtual = 23034

INFO: [Common 17-1381] The checkpoint

'/nfs/home/f/f_koshy/p/project/project.runs/impl_1/room_occupancy_monitor_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report_io -file
room_occupancy_monitor_io_placed.rpt

report_io: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.08 . Memory (MB):
peak = 2360.988 ; gain = 0.000 ; free physical = 11770 ; free virtual = 23027

INFO: [runtcl-4] Executing : report_utilization -file
room_occupancy_monitor_utilization_placed.rpt -pb
room_occupancy_monitor_utilization_placed.pb

report_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory
(MB): peak = 2360.988 ; gain = 0.000 ; free physical = 11778 ; free virtual =
23036

INFO: [runtcl-4] Executing : report_control_sets -verbose -file
room_occupancy_monitor_control_sets_placed.rpt

report_control_sets: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.07 . Memory
(MB): peak = 2360.988 ; gain = 0.000 ; free physical = 11787 ; free virtual =
23044

Command: route_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'

Running DRC as a precondition to command route_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs

Checksum: PlaceDB: 895bb4cb ConstDB: 0 ShapeSum: 2e19ba64 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 107c2f1ee

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2389.984 ; gain = 28.996 ; free physical = 11629 ; free virtual = 22887

Post Restoration Checksum: NetGraph: 9142e0d4 NumContArr: 7680111a
Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 107c2f1ee

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2395.973 ; gain = 34.984 ; free physical = 11597 ; free virtual = 22854

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 107c2f1ee

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2395.973 ; gain = 34.984 ; free physical = 11597 ; free virtual = 22854

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 8f1425c5

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ;
gain = 44.250 ; free physical = 11588 ; free virtual = 22846

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 5d2a3410

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ;
gain = 44.250 ; free physical = 11589 ; free virtual = 22846

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ;
gain = 44.250 ; free physical = 11590 ; free virtual = 22848

Phase 4 Rip-up And Reroute | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ;
gain = 44.250 ; free physical = 11590 ; free virtual = 22848

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ; gain = 44.250 ; free physical = 11590 ; free virtual = 22848

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ; gain = 44.250 ; free physical = 11590 ; free virtual = 22848

Phase 6 Post Hold Fix | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ; gain = 44.250 ; free physical = 11590 ; free virtual = 22848

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.00570135 %

Global Horizontal Routing Utilization = 0.00341006 %

Routable Net Status*

*Does not include unroutable nets such as driverless and loadless.

Run report_route_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 10.8108%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 9.90991%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 10.2941%, No Congested Regions.

Reporting congestion hotspots

Direction: North

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2405.238 ; gain = 44.250 ; free physical = 11590 ; free virtual = 22848

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 12a4a7742

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2407.238 ; gain = 46.250 ; free physical = 11589 ; free virtual = 22847

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 11d4aebcd

Time (s): cpu = 00:00:13 ; elapsed = 00:00:10 . Memory (MB): peak = 2407.238 ; gain = 46.250 ; free physical = 11589 ; free virtual = 22847

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:14 ; elapsed = 00:00:10 . Memory (MB): peak = 2407.238 ; gain = 46.250 ; free physical = 11624 ; free virtual = 22882

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

51 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

route_design completed successfully

route_design: Time (s): cpu = 00:00:15 ; elapsed = 00:00:12 . Memory (MB): peak = 2407.242 ; gain = 46.254 ; free physical = 11624 ; free virtual = 22882

WARNING: [Constraints 18-5210] No constraint will be written out.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.11 .
Memory (MB): peak = 2407.242 ; gain = 0.000 ; free physical = 11620 ; free virtual = 22879

INFO: [Common 17-1381] The checkpoint
'/nfs/home/f/f_koshy/p/project/project.runs/impl_1/room_occupancy_monitor_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report_drc -file
room_occupancy_monitor_drc_routed.rpt -pb
room_occupancy_monitor_drc_routed.pb -rpx
room_occupancy_monitor_drc_routed.rpx

Command: report_drc -file room_occupancy_monitor_drc_routed.rpt -pb
room_occupancy_monitor_drc_routed.pb -rpx
room_occupancy_monitor_drc_routed.rpx

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file
/nfs/home/f/f_koshy/p/project/project.runs/impl_1/room_occupancy_monitor_drc_routed.rpt.

report_drc completed successfully

INFO: [runtcl-4] Executing : report_methodology -file
room_occupancy_monitor_methodology_drc_routed.rpt -pb
room_occupancy_monitor_methodology_drc_routed.pb -rpx
room_occupancy_monitor_methodology_drc_routed.rpx

Command: report_methodology -file
room_occupancy_monitor_methodology_drc_routed.rpt -pb
room_occupancy_monitor_methodology_drc_routed.pb -rpx
room_occupancy_monitor_methodology_drc_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 8 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file
/nfs/home/f/f_koshy/p/project/project.runs/impl_1/room_occupancy_monitor_methodology_drc_routed.rpt.

report_methodology completed successfully

INFO: [runtcl-4] Executing : report_power -file
room_occupancy_monitor_power_routed.rpt -pb
room_occupancy_monitor_power_summary_routed.pb -rpx
room_occupancy_monitor_power_routed.rpx

Command: report_power -file room_occupancy_monitor_power_routed.rpt -pb
room_occupancy_monitor_power_summary_routed.pb -rpx
room_occupancy_monitor_power_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

62 Infos, 5 Warnings, 0 Critical Warnings and 0 Errors encountered.

report_power completed successfully

INFO: [runtcl-4] Executing : report_route_status -file
room_occupancy_monitor_route_status.rpt -pb
room_occupancy_monitor_route_status.pb

INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file
room_occupancy_monitor_timing_summary_routed.rpt -pb
room_occupancy_monitor_timing_summary_routed.pb -rpx
room_occupancy_monitor_timing_summary_routed.rpx -warn_onViolation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type:
min_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a
maximum of 8 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints.
Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report_incremental_reuse -file
room_occupancy_monitor_incremental_reuse_routed.rpt

INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental
placement and routing data was found.

INFO: [runtcl-4] Executing : report_clock_utilization -file
room_occupancy_monitor_clock_utilization_routed.rpt

INFO: [runtcl-4] Executing : report_bus_skew -warn_onViolation -file
room_occupancy_monitor_bus_skew_routed.rpt -pb
room_occupancy_monitor_bus_skew_routed.pb -rpx
room_occupancy_monitor_bus_skew_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

INFO: [Common 17-206] Exiting Vivado at Fri Apr 4 18:48:36 2025...

*** Running vivado

with args -log room_occupancy_monitor.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source room_occupancy_monitor.tcl -notrace

***** Vivado v2018.2 (64-bit)

**** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

**** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source room_occupancy_monitor.tcl -notrace

Command: open_checkpoint room_occupancy_monitor_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1277.117 ; gain = 0.000 ; free physical = 12535 ; free virtual = 23793

INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcs324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1596.383 ; gain = 5.000 ; free physical = 12213 ; free virtual = 23471

Restored from archive | CPU: 0.110000 secs | Memory: 0.976776 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1596.383 ; gain = 5.000 ; free physical = 12213 ; free virtual = 23471

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

open_checkpoint: Time (s): cpu = 00:00:06 ; elapsed = 00:00:16 . Memory (MB): peak = 1596.383 ; gain = 319.270 ; free physical = 12213 ; free virtual = 23471

Command: write_bitstream -force room_occupancy_monitor.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write_bitstream

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

ERROR: [DRC NSTD-1] Unspecified I/O Standard: 21 out of 21 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all I/O standards. This design will fail to generate a bitstream unless all logical ports have a user specified I/O standard value defined. To allow bitstream creation with unspecified I/O standard values (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks NSTD-1].

NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports:

max_threshold[7:0], occupancy[7:0], clk, entrance_photocell, exit_photocell, max_capacity, and reset.

ERROR: [DRC UCIO-1] Unconstrained Logical Port: 21 out of 21 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all pin locations. This design will fail to generate a bitstream unless all logical ports have a user specified site LOC constraint defined. To allow bitstream creation with unspecified pin locations (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: max_threshold[7:0], occupancy[7:0], clk, entrance_photocell, exit_photocell, max_capacity, and reset.

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set

to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

```
set_property CFGBVS value1 [current_design]
```

#where value1 is either VCCO or GND

```
set_property CONFIG_VOLTAGE value2 [current_design]
```

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 2 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.

ERROR: [Vivado 12-1345] Error(s) found during DRC. Bitgen not run.

INFO: [Common 17-83] Releasing license: Implementation

15 Infos, 1 Warnings, 0 Critical Warnings and 3 Errors encountered.

write_bitstream failed

ERROR: [Common 17-39] 'write_bitstream' failed due to earlier errors.

INFO: [Common 17-206] Exiting Vivado at Fri Apr 4 18:49:19 2025...

runme.log(Synthesis)

*** Running vivado

with args -log room_occupancy_monitor.vds -m64 -product Vivado -mode batch
-messageDb vivado.pb -notrace -source room_occupancy_monitor.tcl

***** Vivado v2018.2 (64-bit)

**** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

**** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source room_occupancy_monitor.tcl -notrace

Command: synth_design -top room_occupancy_monitor -part xc7a100tcsg324-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 3898

Starting Synthesize : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.586 ; gain = 85.801 ; free physical = 12461 ; free virtual = 23655

INFO: [Synth 8-638] synthesizing module 'room_occupancy_monitor'
[/nfs/home/f/f_koshy/p/project/project.srcs/sources_1/imports/p/room_occupancy_ monitor.vhd:25]

INFO: [Synth 8-256] done synthesizing module 'room_occupancy_monitor' (1#1)
[/nfs/home/f/f_koshy/p/project/project.srcs/sources_1/imports/p/room_occupancy_ monitor.vhd:25]

Finished Synthesize : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory
(MB): peak = 1446.227 ; gain = 130.441 ; free physical = 12469 ; free virtual =
23665

Finished Constraint Validation : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 .
Memory (MB): peak = 1446.227 ; gain = 130.441 ; free physical = 12468 ; free
virtual = 23665

Start Loading Part and Timing Information

Loading part: xc7a100tcs324-1

INFO: [Device 21-403] Loading part xc7a100tcs324-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:02 ; elapsed
= 00:00:04 . Memory (MB): peak = 1454.223 ; gain = 138.438 ; free physical =
12468 ; free virtual = 23664

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared.
To prevent sharing consider applying a KEEP on the output of the operator

[/nfs/home/f/f_koshy/p/project/project.srcs/sources_1/imports/p/room_occupancy_monitor.vhd:71]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1462.227 ; gain = 146.441 ; free physical = 12459 ; free virtual = 23656

Report RTL Partitions:

RTL Partition	Replication	Instances
++-----+-----+		
++-----+-----+		

No constraint files found.

Start RTL Component Statistics

Detailed RTL Component Info :

+---Adders :

2 Input 8 Bit Adders := 1

+---Registers :

8 Bit Registers := 1

1 Bit Registers := 4

+---Muxes :

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

Finished RTL Component Statistics

Start RTL Hierarchical Component Statistics

Hierarchical RTL Component report

Module room_occupancy_monitor

Detailed RTL Component Info :

+---Adders :

 2 Input 8 Bit Adders := 1

+---Registers :

 8 Bit Registers := 1

 1 Bit Registers := 4

+---Muxes :

 2 Input 2 Bit Muxes := 1

 2 Input 1 Bit Muxes := 1

Finished RTL Hierarchical Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

Finished Part Resource Summary

No constraint files found.

Start Cross Boundary and Area Optimization

Warning: Parallel synthesis criteria is not met

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12272 ; free virtual = 23489

Report RTL Partitions:

RTL Partition	Replication	Instances

No constraint files found.

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 .
Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12272 ; free
virtual = 23488

Report RTL Partitions:

RTL Partition	Replication	Instances

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:06 ; elapsed = 00:00:19 .
Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free
virtual = 23487

Report RTL Partitions:

RTL Partition	Replication	Instances

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free virtual = 23488

Report Check Netlist:

+-----+-----+-----+-----+-----+	Item Errors Warnings Status Description	+-----+-----+-----+-----+-----+
+-----+-----+-----+-----+-----+		+-----+-----+-----+-----+-----+
1 multi_driven_nets 0 0 Passed Multi driven nets		+-----+-----+-----+-----+-----+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free virtual = 23488

Report RTL Partitions:

RTL Partition	Replication	Instances

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free virtual = 23488

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free virtual = 23488

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free virtual = 23488

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 . Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free virtual = 23488

Start Writing Synthesis Report

Report BlackBoxes:

++-----+-----+

| |BlackBox name |Instances |

```
+-----+-----+
+-----+-----+
```

Report Cell Usage:

```
+-----+-----+
```

	Cell	Count
--	------	-------

```
+-----+-----+
```

1	BUFG	1
---	------	---

2	CARRY4	3
---	--------	---

3	LUT1	3
---	------	---

4	LUT2	8
---	------	---

5	LUT3	1
---	------	---

6	LUT4	8
---	------	---

7	LUT6	2
---	------	---

8	FDCE	12
---	------	----

9	IBUF	12
---	------	----

10	OBUF	9
----	------	---

```
+-----+-----+
```

Report Instance Areas:

```
+-----+-----+-----+
```

	Instance	Module	Cells
--	----------	--------	-------

```
+-----+-----+-----+
```

1	top	59
---	-----	----

```
+-----+-----+-----+
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 .
Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12271 ; free
virtual = 23488

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 .
Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12273 ; free
virtual = 23489

Synthesis Optimization Complete : Time (s): cpu = 00:00:06 ; elapsed = 00:00:20 .
Memory (MB): peak = 1596.059 ; gain = 280.273 ; free physical = 12284 ; free
virtual = 23500

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

12 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:23 . Memory (MB): peak
= 1691.004 ; gain = 387.871 ; free physical = 12225 ; free virtual = 23452

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint
'/nfs/home/f/f_koshy/p/project/project.runs/synth_1/room_occupancy_monitor.dcp'
has been generated.

INFO: [runtcl-4] Executing : report_utilization -file
room_occupancy_monitor_utilization_synth.rpt -pb
room_occupancy_monitor_utilization_synth.pb

report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.11 . Memory
(MB): peak = 1715.023 ; gain = 0.000 ; free physical = 12226 ; free virtual =
23453

INFO: [Common 17-206] Exiting Vivado at Fri Apr 4 18:47:16 2025...