Transputer versions

MIKE's Technical Note 2

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Contents

Introduction

This technical note lists the differences of the various transputer versions. It covers only the first-generation transputers known collectively as the Txxx series.

There are three main types of first generation transputers; the 32 bit transputers with a floating point unit (known as the T8 or T8xx), the 32 bit transputers without a floating point unit (known as the T4 or T4xx) and the 16 bit transputers (known as the T2 or T2xx).

The **T212** is a 16-bit processor with 2K of on-chip RAM and a 64K address range (using separate address and data buses).

The **M212** is a T212 with a ST506/ST412, SA400/450 compatible interface and 4K of on-chip ROM.

The **T222** is an updated T212 with 4K of on-chip RAM and links with overlapped acknowledge.

The **T225** is an updated T222 with additional instructions for program debugging and double buffered links. The T225 also has some additional instructions found on T800 series transputers.

The **T414** is a 32-bit processor with 2K of on-chip RAM and a 4G address range (using multiplexed address and data lines).

The **T425** is an updated version of the T414 with additional instructions for program debugging. The T425 also has the (two-dimensional) block move instructions and some other instructions found on T800 series transputers.

The **T426** is a T425 with a new external memory interface which has built in support for parity checking of memory.

The **T400** is a cut-down, low-cost version of the T425 with only 2 links and only 2K of on-chip RAM.

The **T800** is a superset of the T414 in that it is a 32-bit processor with a floating point coprocessor on-chip, additional instructions, and 4K of on-chip RAM.

The **T801** is an updated T800 with separate address and data buses, thus speeding up memory accesses and additional instructions for program debugging.

The **T805** is an updated T800 with additional instructions for program debugging.

There are several variations of each of these but all first-generation trans-

puters have the same architecture, essential similar instruction sets and fully compatible communication links.

References

[1] Transputer Hardware and System Design
Jeremy Hinton & Alan Pinder (1993)
ISBN-10 0-13-953001-0

[2] Transputer Assembler Language Programming
John Roberts (1992)
ISBN-10 0-442-00872-4

[3] Transputer Databook - Third Edition
INMOS Limited (1992)
72-TRN-203-02

[4] Transputer Databook - Second Edition
INMOS Limited (1989)
72-TRN-203-01

[5] Transputer Databook - First Edition
INMOS Limited (1989)
72-TRN-203-00

[6] The Transputer Handbook
Ian Graham & Tim King (1990)
ISBN-10 0-13-929134-2

	T212	M212	T222	T225	T414	T400	T425	T426	T800	T801	T805
Word length (bits)	16	16	16	16	32	32	32	32	32	32	32
Floating point hardware	-	-	-	-	-	-	-	-	✓	✓	✓
On-chip memory (bytes)	2k	2k	4k	4k	2k	2k	4k	4k	4k	4k	4k
Number of links	4	2	4	4	4	2	4	4	4	4	4
Overlapped acknowledge	-	-	✓	✓	-	✓	✓	✓	✓	✓	✓
Double-buffered link output	-	-	-	✓	-	✓	✓	✓	✓	✓	✓
Programmable DRAM controller	-	-	-	-	✓	✓	✓	✓	✓	-	✓
Memory Parity	-	-	-	-	-	-	-	✓	-	-	-
External data bus width	16	8	16	16	32	32	32	32	32	32	32
Minimum external cycles	2	2	2	2	3	3	3	3	3	2	3
Disk interface	-	✓	-	-	-	-	-	-	-	-	-
In production 1992	-	-	-	✓	-	✓	✓	✓	-	✓	✓

Table 1: Transputer major differences

Table 2: Transputer pin differences

	T212	M212	T222	T225	T414	T400	T425	T426	T800	T801	T805
Number of pins (PGA)	68	68	68	68	84	84	84	100	84	100	84
Separate address and data	✓	-	✓	✓	-	-	-	-	-	✓	-
Multiplexed address and data	-	-/✓	-	-	✓	✓	✓	✓	✓	-	✓
Parity pins	-	-	-	-	-	-	-	✓	-	-	-
Disk interface	-	✓	-	-	-	-	-	-	-	-	-
ErrorIn	-	-	-	-	-	✓	✓	✓	✓	-	✓
RefreshPending	-	-	-	-	-	✓	✓	✓	-	-	✓
EventWaiting	-	-	-	-	-	✓	✓	✓	-	✓	✓
ProcSpeedSelect	-	-	✓	✓	-	✓	✓	✓	✓	✓	✓
DisableIntRam	-	-	-	✓	-	-	-	-	✓	-	-
MemBAcc	✓	-	✓	✓	-	-	-	-	-	-	-

Table 2: Transputer pin differences

	T212	M212	T222	T225	T414	T400	T425	T426	T800	T801	T805
Floating point unit (52)	-	-	-	-	-	-	-	-	✓	✓	✓
fptesterror (1)	-	-	-	-	-	✓	✓	✓	✓	✓	✓
Floating point support (5)	-	-	-	-	✓	✓	✓	✓	-	-	-
fmul (1)	-	-	-	-	✓	✓	✓	✓	✓	✓	✓
2D block moves (4)	-	-	-	-	-	✓	✓	✓	✓	✓	✓
CRC operations (2)	-	-	-	✓	-	✓	✓	✓	✓	✓	✓
Bit operations (3)	-	-	-	✓	-	✓	✓	✓	✓	✓	✓
Break-point debugging (8)	-	-	-	✓	-	✓	✓	✓	-	✓	✓
Fast negative prod	-	-	-	✓	-	✓	✓	✓	✓	✓	✓
dup (1)	-	-	-	✓	-	✓	✓	✓	✓	✓	✓
pop (1)	-	-	-	✓	-	✓	✓	✓	-	✓	✓
wsubdb (1)	-	-	-	-	-	✓	✓	✓	✓	✓	✓
lddevid (1)	-	-	-	✓	-	✓	✓	✓	-	✓	✓
Device identity numbers	-	-	-	40-49	-	50-59	00-09	30-39	-	20-29	10-19
ldmemstartval (1)	-	-	-	✓	-	✓	✓	✓	-	✓	✓
Memstart (byteoffset)	24	24	24	24	48	70	70	70	70	70	70

Table 3: Transputer instruction set differences

	T212	M212	T222	T225	T414	T400	T425	T426	T800	T801	T805
PGA - 15MHz (G17)	68	68	-	-	84	-	-	-	-	-	-
PGA - 17MHz (G17)	68	-	68	-	-	-	84	-	84	-	-
PGA - 20MHz (G20)	68	68	68	68	84	84	84	-	84	100	84
PGA - 25MHz (G25)	-	-	-	68	-	84	84	-	84	100	84
PGA - 30MHz (G30)	-	-	-	-	-	-	84	-	-	-	84
PLCC - 15MHz (J15)	-	68	68	-	84	-	-	-	-	-	-
PLCC - 17MHz (J17)	-	-	68	-	-	-	84	-	-	-	-
PLCC - 20MHz (J20)	-	68	68	68	-	84	84	-	-	-	84
PLCC - 25MHz (J25)	-	-	-	68	-	84	84	-	-	-	84
PLCC - 30MHz (J30)	-	-	-	-	-	-	-	-	-	-	84
CQFP - 20MHz (F20)	-	-	-	100	-	100	100	100	-	-	100
CQFP - 25MHz (F25)	-	-	-	100	-	-	100	100	-	-	100
CQFP - 30MHz (F30)	-	-	-	-	-	-	-	-	-	-	100
PQFP - 20MHz (X20)	-	-	-	-	-	100	-	-	-	-	-
PQFP - 25MHz (X25)	-	-	-	-	-	-	100	-	-	-	-

Table 4: Transputer package options