

Radio Shack®

Service Manual

25-1000

TANDY® 1000 COMPUTER



CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK, A DIVISION OF TANDY CORPORATION

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1 / INTRODUCTION TO THE TANDY 1000 COMPUTER

The Tandy 1000 Computer is modular in design to allow maximum flexibility in system configuration. The computer consists of a Main Unit, a detachable keyboard with coiled cable, and a monitor. The Main Unit is supplied with one internal floppy disk drive. (A second floppy disk drive is optional.) The standard types of monitors used with the Tandy 1000 are the monochrome composite and the color RGB monitor. Since these units are modular, they may be placed on top of the Main Unit or at any convenient location.

Internal storage is expanded by adding a second 5 $\frac{1}{4}$ " floppy disk drive. Each disk drive has a capacity of 360K bytes formatted.

The Tandy 1000 has a standard 128K of system RAM. An optional DMA/RAM board allows the Tandy 1000 to be expanded in increments of 128K of RAM. This board will fit into one of the expansion slots. With two fully populated RAM boards installed, the Tandy 1000 will have 640K bytes of maximum RAM allowed by the system memory map.

Other features include a parallel printer port, two built-in joystick interfaces, a speaker for audio feedback, and a light pen interface.

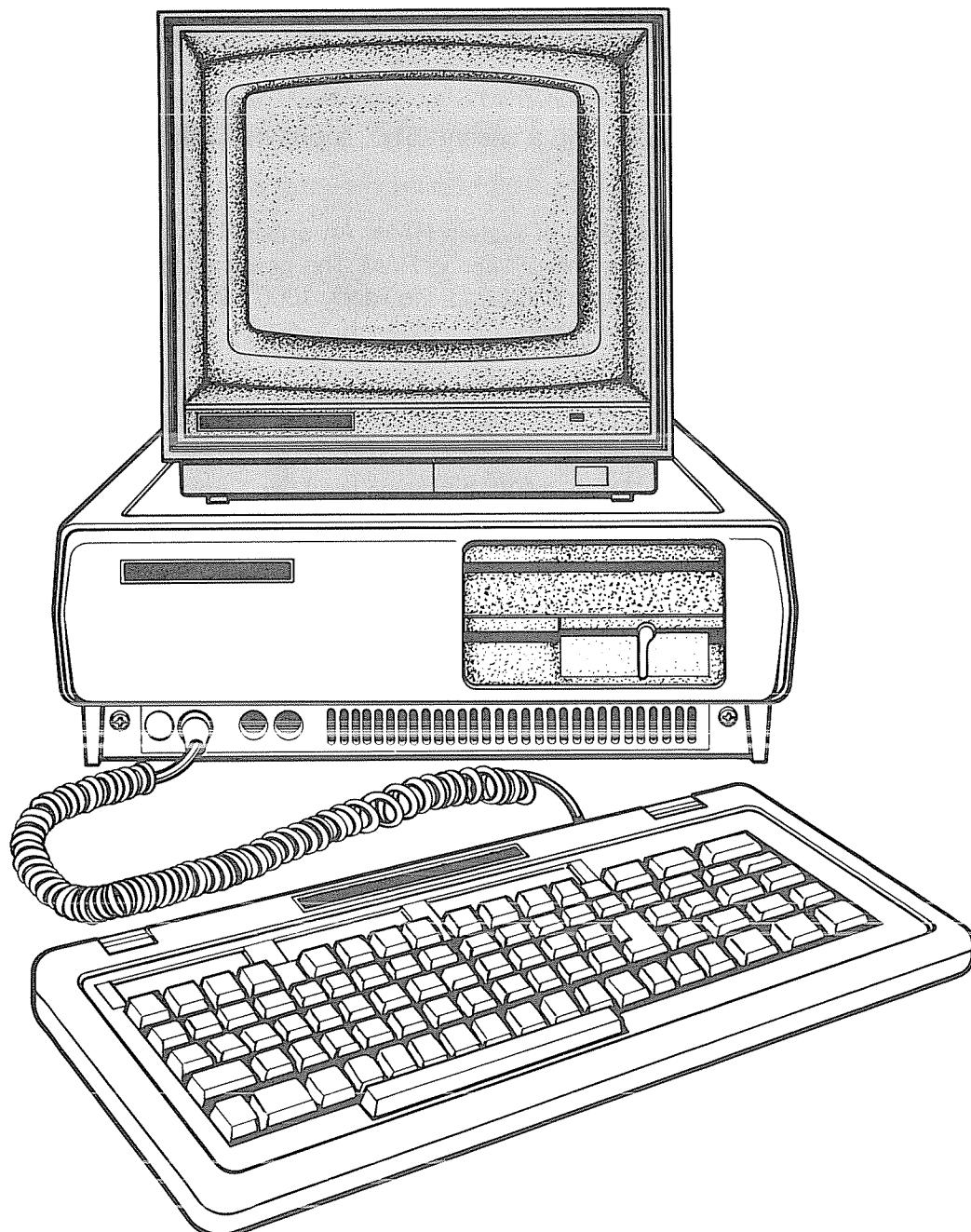
The Main Unit is the heart of the Tandy 1000. It houses the Main Logic Assembly, system power supply, and floppy disk drives.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, and disk drives by a series of cables. The illustration in Figure 1 shows the major components of a Tandy 1000 system.

The Power Supply is a 54W switching regulator type, designed to provide adequate power capacity for a fully configured system using all the option slots.

The Floppy Disk Drive uses 5 $\frac{1}{4}$ " double-sided, double-density diskettes to read, write, or store data. These are soft sector diskettes. The Disk Drive assembly is installed in the standard unit. The floppy disk stores approximately 360K bytes (formatted) of data. All system programs, with the exception of the system startup sequence, are stored on disk.

Either a monochrome or a color display may be used with the Tandy 1000. The monochrome monitor is a high-resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface. Each display is capable of 25 lines of 80 characters. The character matrix is 8 wide x 9 high.



**Tandy 1000 System
Figure 1**

2 / SPECIFICATIONS

Processor: Intel 8088

Dimensions:

6 x 17 x 13 $\frac{3}{8}$ inches (HWD)

Weight:

17 lbs. 4 oz. with 1 Disk Drive

Power Requirements:

120 VAC, 60 Hz, 1 Amp maximum

With 2 Floppy Disk Drives, 2 Memory Cards, and RS-232:

AC Current: 0.7 – 0.8 Amps with Floppy doing R/W tests.

Leakage Current: 0.5 mA

Disk Drive:

Idle + 5 VDC	0.23 Amps	+ 12 VDC 0.106 Amps
R/W	0.286 Amps	0.295 Amps
R/W	0.2 Minimum	0.550 Max.

Main Logic Board: + 5 VDC 4.07 Amps + 12 VDC 0.056 Amps

Main Logic Board Option Cards: – 12 VDC 0.032 Amps

Environment:

Air Temperature

System ON: 60 to 90 degrees F (15.6 to 32.2 degrees C)

System OFF: 50 to 110 degrees F (10 to 43 degrees C)

Humidity

System ON-OFF: 8% to 80%

Disk Drive Specifications

Power:

Supply Voltage	+ 5 VDC Input	+ 12 VDC Input
Ripple	100 mV	100 mV
Tolerance	+/- 5%	+/- 5%
Including Ripple		
Standby Current		
Nominal	600 mA	400 mA
Worst Case	700 mA	500 mA
Operating Current		
Nominal	600 mA	900 mA
Worst Case	700 mA	2400 mA

Environment:

Temperature	
Operating	50 to 122 degrees F (10 to 44 C)
Nonoperating	- 40 to 140 degrees F (- 40 to 60 C)
Relative Humidity	
Operating	20% to 80% (noncondensing)
Nonoperating	5% to 95% (noncondensing)

3 / Disassembly-Assembly

Since the Tandy 1000 is modular in its construction, disassembly/assembly procedures are simplified. The modules which make up the Tandy 1000 are the Main Unit, the keyboard, and the display monitor. These three units may be supplemented by various I/O devices such as printers, modems, memory devices or additional monitors. Disassembly of each module will be described in the following paragraphs. Exercise caution when handling the modules to prevent damage to internal components or exterior surfaces. See Figure 2.

Disassembly of the Main Unit

1. To remove the case, remove the 2 screws from the lower front of the case, slide the case forward until it clears the rear panel and remove.
2. To remove the rear panel, remove the 3 screws in the back of the unit and lift up slightly.
3. To remove the disk drive assembly, remove the 2 screws nearest the cooling fan on the rear of the chassis, the 1 screw on the right side of the drive structure which attaches it to the base of the chassis and the 3 screws on the front of the chassis. Disconnect the DC power and signal cables from the rear of the drive(s). Lift the drive upward to remove.
4. To remove the power supply, disconnect the DC power cable from the main board. Disconnect the fan cable on the left side of the drive structure. Remove the 4 screws on the rear of the chassis.
5. To remove an option board, locate the screw on the top of the option board panel. Remove the screw and pull up to separate it from the main logic circuit board.
6. To remove the main logic circuit board, disconnect the speaker cable and remove the 11 screws holding the board to the chassis.

Power Supply

The 54W main power supply is located at the right side of the Main Unit and is accessible when you remove the cover and rear panel from the Main Unit as noted above. See Figure 3.

1. Unplug the AC power cable from the power supply and lay it aside.
2. Disconnect the power cable and floppy drive cable from the circuit board.
3. Remove the 4 mounting screws on the power supply circuit board.
4. Disconnect the AC fan cable on the power supply circuit board and remove the power supply through the open end of the enclosure.

Assemble the power supply in the reverse order of disassembly. Ensure that all cables and wires are connected correctly.

Keyboard

The keyboard assembly is connected by a coiled cable attached to the left side of the front plate of the Main Unit. Disassemble the keyboard as noted below. See Figure 28 in the Keyboard Section.

Disassembly

1. After removing the connector from the Main Unit, turn the keyboard assembly upside down on a soft surface to prevent scratching the surface of keys. Be sure the cable is extended away from you.
2. Remove the 3 screws nearest the front of the keyboard. Keep these separate so that you can replace them in their correct locations.
3. Remove the remaining 6 screws from the sides and back of the keyboard assembly.
4. Hold the top and bottom of the keyboard assembly together and turn the assembly right side up.
5. Lift the top cover off the assembly, exposing the keyboard printed circuit board.
6. The keyboard cable is restrained by a labyrinth-shaped form. Carefully lift the cable from each bend, and when the cable is free of the restraint, disconnect the cable connector from the right rear of the keyboard assembly and remove the keyboard circuit board.

Assembly

Assemble the keyboard in the reverse order of disassembly. Be sure that the keyboard supports are properly positioned on the support springs before installing the top cover. Also be sure that the shorter mounting screws are used at the front positions of the keyboard assembly (to prevent damage to the keyboard plastic).

Display Unit

For more information on the display units, refer to the manual(s) available for the model you have.

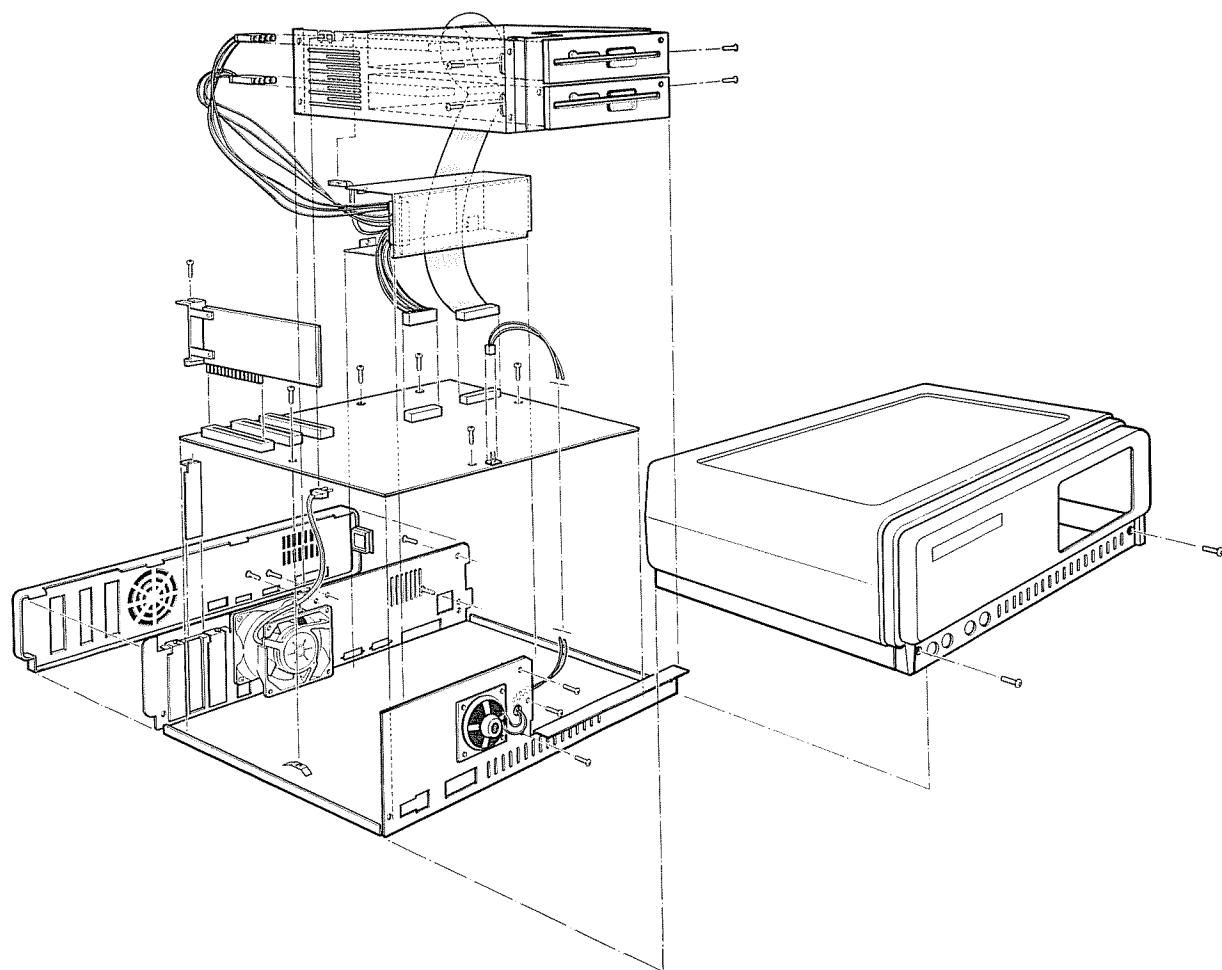


Figure 2
Tandy 1000 Exploded View

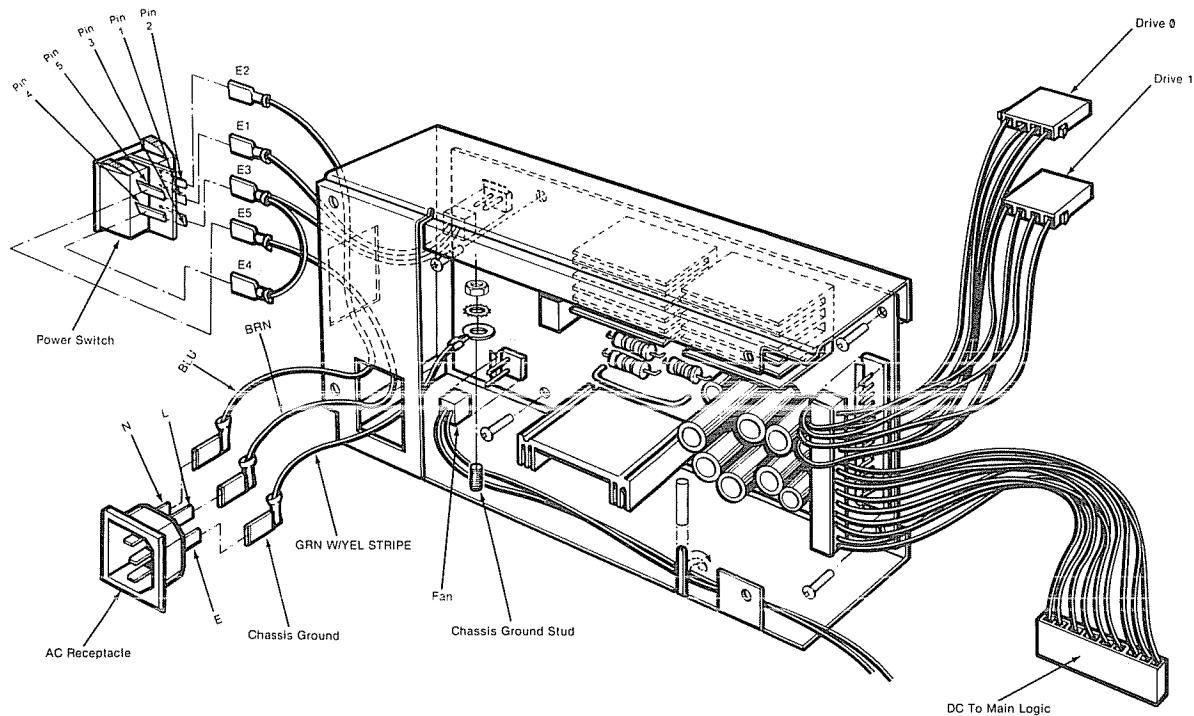


Figure 3
54 Watt Power Supply Exploded View

4 / CABLING DIAGRAMS AND PINOUT CONNECTIONS

This section of the manual provides connector diagrams and pin descriptions of the connectors used in the Tandy 1000. Figure 4 shows an interconnecting wiring diagram and identifies the connectors by symbol number and/or cable number. The drawings of each connector with their pin designations are in Section 12.

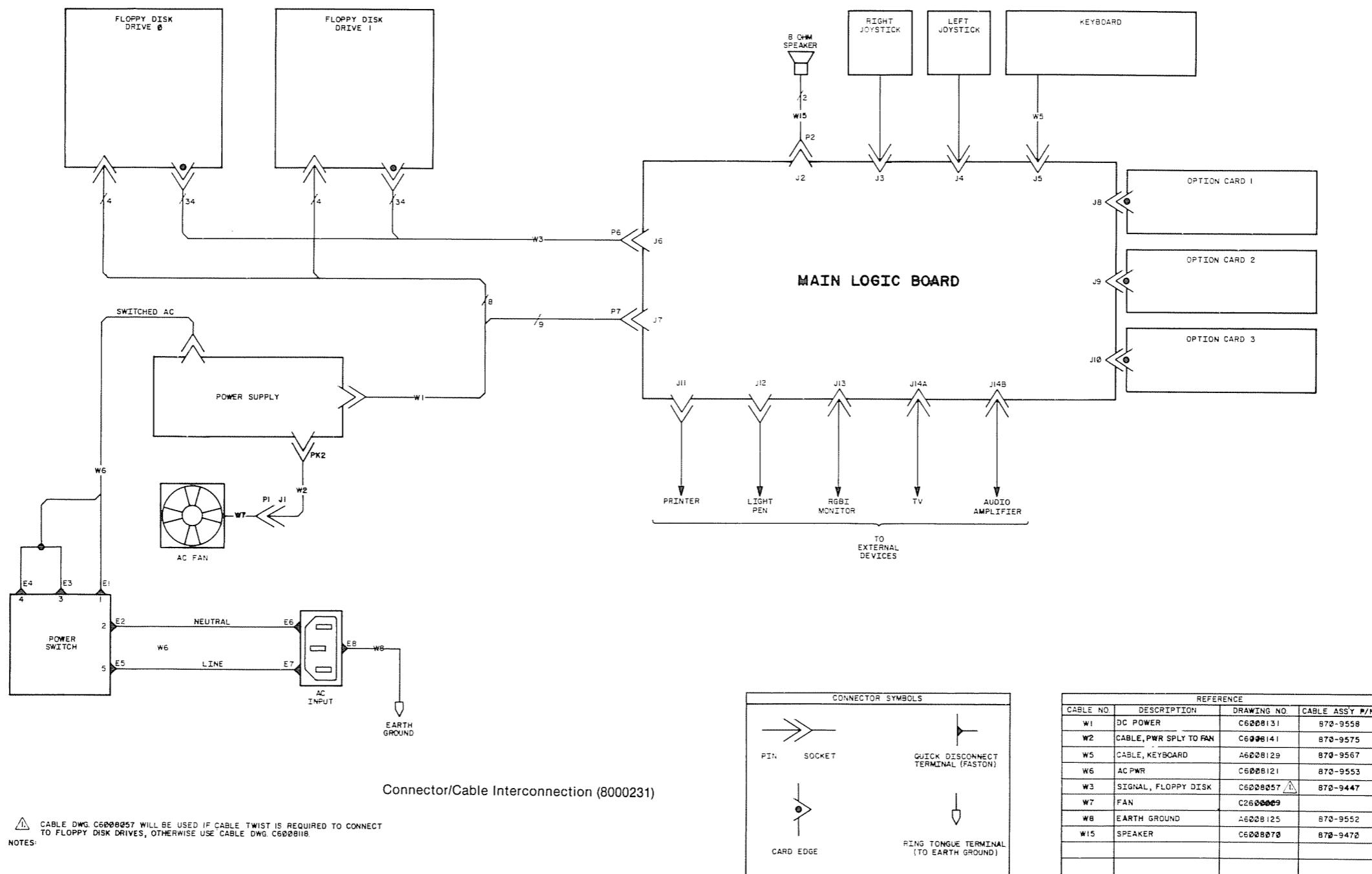


Figure 4
Interconnecting Wiring Diagram

Connector Pin Assignments

J2 — Speaker Interface
(2-Pin Vertical Header)

1 — Sound 2 — Ground

J3 — Right Joystick
(6-Pin Rt. Angle Circular Din)

1 — Y Axis	2 — X Axis
3 — Ground	4 — Switch 1
5 — +5 VDC	6 — Switch 2

J4 — Left Joystick
(6-Pin Rt. Angle Circular Din)

1 — Y Axis	2 — X Axis
3 — Ground	4 — Switch 1
5 — +5 VDC	6 — Switch 2

J5 — Keyboard Interface
(8-Pin Rt. Angle Circular Din)

1 — KBDDATA	2 — KBDBUSY*
3 — Ground	4 — KBDCLK
5 — +5 VDC	6 — KBDRST
7 — MULTIDATA	8 — MULTICLK

J6 — Floppy Disk Interface
(Dual 17-Pin Vertical Header)

1 — Ground	2 — NC
3 — Ground	4 — NC
5 — Ground	6 — NC
7 — Ground	8 — INDEX*
9 — Ground	10 — DS0*
11 — Ground	12 — DS1
13 — Ground	14 — NC
15 — Ground	16 — MTRON*
17 — Ground	18 — DIR*
19 — Ground	20 — STEP*
21 — Ground	22 — WRDATA*
23 — Ground	24 — WEN*
25 — Ground	26 — TRK0*
27 — Ground	28 — WRPRT*
29 — Ground	30 — RDDATA*
31 — Ground	32 — SIDESELECT*
33 — Ground	34 — DRVRDY*

J7 — DC POWER
(9-PIN VERTICAL HEADER)

1	— +5 VDC	2	— +5 VDC
3	— +5 VDC	4	— Ground
5	— Ground	6	— Ground
7	— Ground	8	— -12 VDC
9	— +12 VDC		

J8,J9,J10 — Expansion Interface Connectors
(Dual 31-Pin Card Edge)

A01	— NMI	B01	— Ground
A02	— D7	B02	— RESET
A03	— D6	B03	— +5 VDC
A04	— D5	B04	— IR2
A05	— D4	B05	— (-5 VDC)
A06	— D3	B06	— FCDMARQ*
A07	— D2	B07	— -12 VDC
A08	— D1	B08	— AUDIOIN
A09	— D1	B09	— +12 VDC
A10	— READY	B10	— Ground
A11	— AEN	B11	— MEMW*
A12	— A19	B12	— MEMR*
A13	— A18	B13	— IOW*
A14	— A17	B14	— IOR*
A15	— A16	B15	— (DACK3*)
A16	— A15	B16	— (DRQ3*)
A17	— A14	B17	— (DACK1*)
A18	— A13	B18	— (DRQ1*)
A19	— A12	B19	— REFRESH*
A20	— A11	B20	— CLK
A21	— A10	B21	— RFSHRQ
A22	— A09	B22	— BREQ*
A23	— A08	B23	— IR5
A24	— A07	B24	— IR4
A25	— A06	B25	— IR3
A26	— A05	B26	— (FDCDACK*)
A27	— A04	B27	— (DMATC)
A28	— A03	B28	— ALE
A29	— A02	B29	— +5 VDC
A30	— A01	B30	— OSC
A31	— A00	B31	— Ground

Note: Signals in parentheses on J8, J9, and J10 are shown for PC Compatible Reference only and are not used on the main logic board of the Tandy 1000.

J11— Parallel Interface
(34-Pin Card Edge)

1 — PPSTROBE*	2 — Ground
3 — PPDATA0	4 — Ground
5 — PPDATA1	6 — Ground
7 — PPDATA2	8 — Ground
9 — PPDATA3	10 — Ground
11 — PPDATA4	12 — Ground
13 — PPDATA5	14 — NC
15 — PPDATA6	16 — Ground
17 — PPDATA7	18 — Ground
19 — PPACK*	20 — Ground
21 — PPBUSY	22 — Ground
23 — PPPAEM	24 — Ground
25 — PPBUSY*	26 — NC
27 — Ground	28 — PPFAULT
29 — NC	30 — PPINIT*
31 — Ground	32 — PPAUTOFED*
33 — Ground	34 — NC

J12— Light Pen
(9-Pin Connector Male Rt. Angle D-Subminiature)

1 — +5 VDC	2 — Ground
3 — LPIN	4 — LPSW*
5 — NC	6 — NC
7 — NC	8 — NC
9 — NC	

J13— RGBI Video
(9-Pin Socket Rt. Angle D-Subminiature)

1 — Ground	2 — Ground
3 — Red	4 — Green
5 — Blue	6 — Intensity
7 — +12 VDC	8 — HSYNC
9 — VSYNC	

J14— Composite Output
(Dual Rt. Angle RCA-Type Phone Jack)

A — Video
B — Audio

5 / BUS INTERFACE SPECIFICATIONS

This specification is for the primary bus on the Tandy 1000 main logic board, which also is available to the option board connectors. The specification describes the signals in the following manner. See Figures 5 and 5.1.

- The following signal nomenclature is used in the schematic and literature. Signals designated with the suffix “*” are logically “true low” (normal inactive state is high); if they are not so designated, the signal is logically “true high.”
- Direction—input or output—is referenced to the CPU.
- Brief functional description of the signal.
- Description of the “drive” or “load” characteristics of the signal. This includes the specific source by IC type and reference designator, drive capability for “output” signals, and actual load for “input” signals. The drive/load is defined in “unit loads” and specified as “high/low.” This specification is for the main logic board only. Some signals have an alternate source, an external bus master such as the DMA.
- 1 Unit Load (UL) is defined as:

Io _h	= .04mA @ 2.4V
Io _l	= 1.6mA @ 0.5V

Signal Listing

A00 - A19	O	ADDRESS	SOURCE: U41, U42, U61 Drive - 65/15 UL Latch Strobe - ALE Output Enable - AEN Alternate external source
D0-D7	I/O	DATA	SOURCE: U62 Drive - 37/15 UL Direction Control - RD* (CPU read signal) Enable - DEN*
ALE	O	ADDRESS LATCH STROBE	SOURCE: U46
IOW*	O	I/O WRITE STROBE	Drive - 50/7.5 UL
IOR*	O	I/O READ STROBE	Output Enable - AEN
MEMW*	O	MEMORY WRITE STROBE	Pull-Up - 4.7K ohms
MEMR*	O	MEMORY READ STROBE	Alternate external source
CLK	O	CPU CLOCK	4.77MHz, 33% duty cycle
OSC	O	OSCILLATOR	SOURCE: U82 Drive - 75/7.5 UL
NMI	I	NON-MASKABLE INTERRUPT	14.32MHz, 50% duty cycle SOURCE: U82 Drive - 75/7.5 UL To System NMI Load: 1/1 UL, U117

READY	I	SYSTEM WAIT	SOURCE: OPEN-COLLECTOR OR 3-STATE BUFFERS Load: 1 UL and 1.0K ohm pull-up. 10/0.9 UL Set LOW by Peripherals (I/O or Memory) to extend READ or WRITE cycles.
RESET	O	SYSTEM RESET	Power On or Manual SOURCE: U82 Drive: 75/7.5 UL
BREQ*	I	BUS REQUEST	From external masters Load: 1 UL and 10K ohm pull-up. 10/0.9 UL
AEN	O	BUS GRANT	To external masters SOURCE: U82 Drive - 75/7.5 UL
IR2	I	INTERRUPT REQUEST#2	To system interrupt controller
IR3	I	INTERRUPT REQUEST#3	Load: 1 UL and 2.2K pull-down
IR4	I	INTERRUPT REQUEST#4	
AUDIO IN	I		From External Sound Source Load: 10k ohms.
AUDIO OUT	O		To External Source Drive: 1.25 Volts P-P into 10K

The following are not sourced by the CPU but are to be SOURCED (O) Output or LOADED (I) Input by an external DMA source:

RFSHRQ	I	REQUEST DMA CHANNEL#0	Dedicated input requests to DMA
DRQ1	I	REQUEST DMA CHANNEL#1	Load: 8237A-5/9517A
FDCDMARQ	I	REQUEST DMA CHANNEL#2	1 MOS load 40/160 UL
DRQ3	I	REQUEST DMA CHANNEL#3	
REFRESH*	O	ACKNOWLEDGE DRQ0*	Dedicated output
DACK1*	O	ACKNOWLEDGE DRQ1*	acknowledges from DMA.
FDCDACK*	O	ACKNOWLEDGE DRQ2*	Drive: 8237A-5/9517A
DACK3*	O	ACKNOWLEDGE DRQ3*	2/2 UL
DMATC	O	TERMINAL COUNT	Used by DMA Controller to indicate Terminal Count reached.
			Drive: 2/2 UL
+5VDC		+5VDC \pm 4% 3.0 Amps available on the bus.	
+12VDC		+12VDC \pm 5% 0.5 Amps available on the bus.	
-12VDC		-12VDC + 8.3% - 25% 0.06 Amps available on the bus.	
GROUND		Power Return for +5, +12, -12 VDC.	

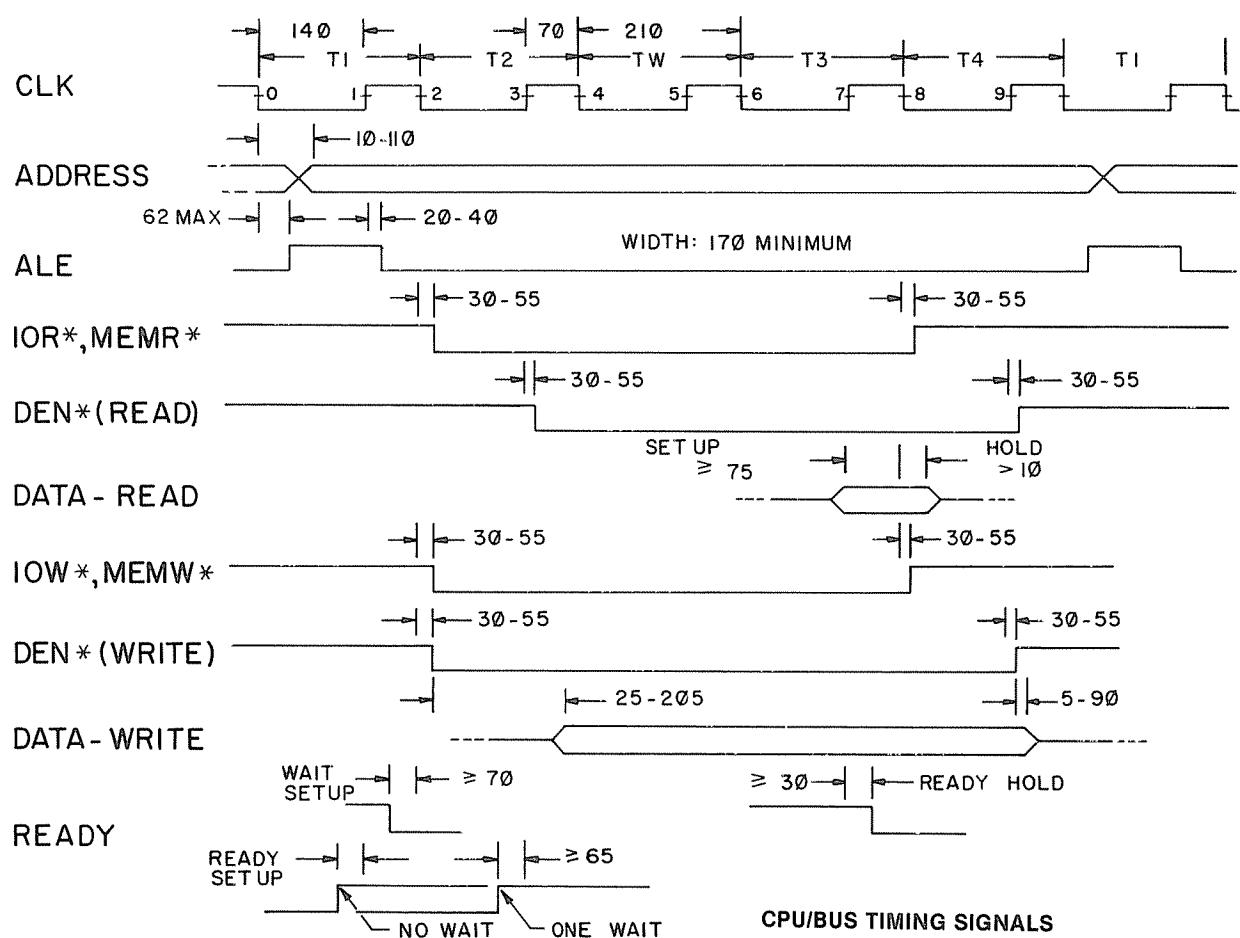


Figure 5
CPU/BUS Timing Signal

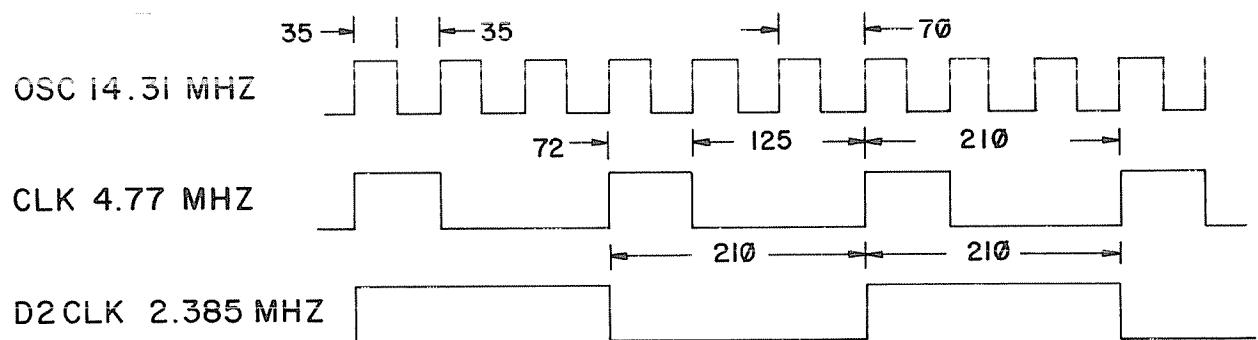


Figure 5.1
CPU/BUS Timing Signal

6 / THEORY OF OPERATION

Main Logic Board

The Block Diagram of the main logic board (Figure 6) shows the basic functional divisions.

CPU Function

The CPU function consists of the CPU (Intel 8088), the address, data interface, the CPU control signal generator, the bus control signal generator and the interrupt controller (Intel 8259A). It is located in the upper right hand corner of the board above the external bus connectors.

Non-CPU Function, Main Logic Board

The non-CPU functions can be divided into two main parts: memory and I/O. Memory consists of RAM and ROM. RAM or Video/System Memory serves as storage for both the video data and program data. ROM memory contains the BIOS and diagnostics. I/O consists of all the peripheral functions; keyboard, floppy disk controller, printer, joystick, light pen and sound.

Processor Address/Data Interface

The 8088 has three groups of Address/Data lines; AD0 - AD7, A8 - A15 and A16 - A19. AD0 - AD7 are multiplexed address and data lines. To separate and save the address that comes out first, the signals are applied to U61 (74LS373) and latched by ALE. Additionally, the signals are applied to data transceiver U62 (74LS245). U62 is enabled only during the data portion of the CPU cycle. (The exception is during an Interrupt Acknowledge cycle.) Direction of transmission is controlled by the RD* (READ) signal from the CPU. Address lines A8 - A15 are present during the entire CPU cycle and need only to be buffered. Address lines A16 - A19 are multiplexed with status signals S4 - S7 and need to be latched. The results are: A8 - A11, A16 - A19 are latched into U41 (74LS373) by ALE and A12 - A15 are buffered by half of U43 (74LS244). The outputs from these latches/buffers/transceivers are the BUS Signals A00 - A19, D0 - D7.

CPU Control Signal Generation

The 8088 CPU uses a 4.77 MHz clock with a special duty cycle (33% high, 67% low.) This clock is produced by the 8284 clock generator/driver U45. The 8284 receives a 14 MHz input clock and divides it by 3 to produce CPUCLK (4.77 MHz) and by 6 to produce D2CLK (2.385 MHz). In addition to being used by the control signal logic the clocks are buffered by U82 (74LS244) for the bus signals OSC (14 MHz), (4.77 MHz) and main logic signal D2CLK (2.385 MHz). (See the Bus Interface Specification)

The RESET signals (CPURESET, SYSRST*, RST*) originate at U45 (8284) which synchronizes the input RES*. RES* originates from C26 which is shorted to 0 volts by either the manual reset switch or by diode CR6 when the power is off.

The READY circuit synchronizes the system "ready" signals with the CPU clock and generates the CPU input CPUREADY. If a function needs one or more "wait" states added to its access, it must set the READY line low. From the main logic board, READY is set low by the sound IC for 32 extra "wait states" and the video/system memory sets READY low for typically one or two "wait" cycles. The READY circuit of the 8284 (U45) is operated in the non-asynchronous mode; i.e. two sequential edges of clock (a rising edge first) are required to set the CPUREADY signal true. Of the four inputs provided, two are used, RDY2 and AEN2. Inputs to RDY2 must be high and the input to AEN2 must be low to set CPUREADY high. Only one input is applied to AEN2: IOWAIT which is a positive pulse generating one "wait" state for every I/O cycle. The signal READY applied to the RDY2 input comes directly from the BUS and is the wired-or (logical OR) of any/all READY's from the subsystems which need "wait state(s)" inserted. READY is pulled-up by R34.

Oscillator Timing and Dynamic RAM Control

The main system timing starts with the 28.63636 MHz oscillator. This oscillator is a single package which produces a TTL output. From the oscillator, U39 divides the master frequency into 4 multiples. The timing diagram (Figure 6.1) shows this division. 14.31818 MHz is used to clock the video array chip, and also is used by the Intel 8284 to generate the CPU clock signal.

The first three outputs from the counter (U39) are used to derive 8 time states, (U38) and the last output is used to effectively double the number to 16. These 16 time states are shown at the bottom of Figure 6.1. These time states are then used as J-K inputs for F109 flip-flops, which generate the system timing signals RAS*, CAS* and MUX.

The timing diagram shows RAS* and CAS* as constantly occurring pulses which cycle every 279 ns. Only the RAS* and CAS* pulses for the video cycles are constant. During the CPU cycle, RAS* and CAS* pulse will occur only if the CPU is accessing memory. This function is controlled by U116 and ½ of U94. A CPU request for accesses is first latched by the first half of U116. As soon as the next CPU cycle time starts, the second half of U116 is clocked and the CPU access cycle starts. The CPU cycle lasts until the rising edge of RAS* in the video cycle.

The other signals generated by the system timing are STIS, DYMU, and CPULT. ST15 is a synchronization signal for the Video Array chip, and references time state 0 from U39. DYMUX occurs on the rising edge of MUX in the CPU cycle and latches the video data. The final signal, CPULT occurs only during a CPU access and is used to latch read data for the CPU.

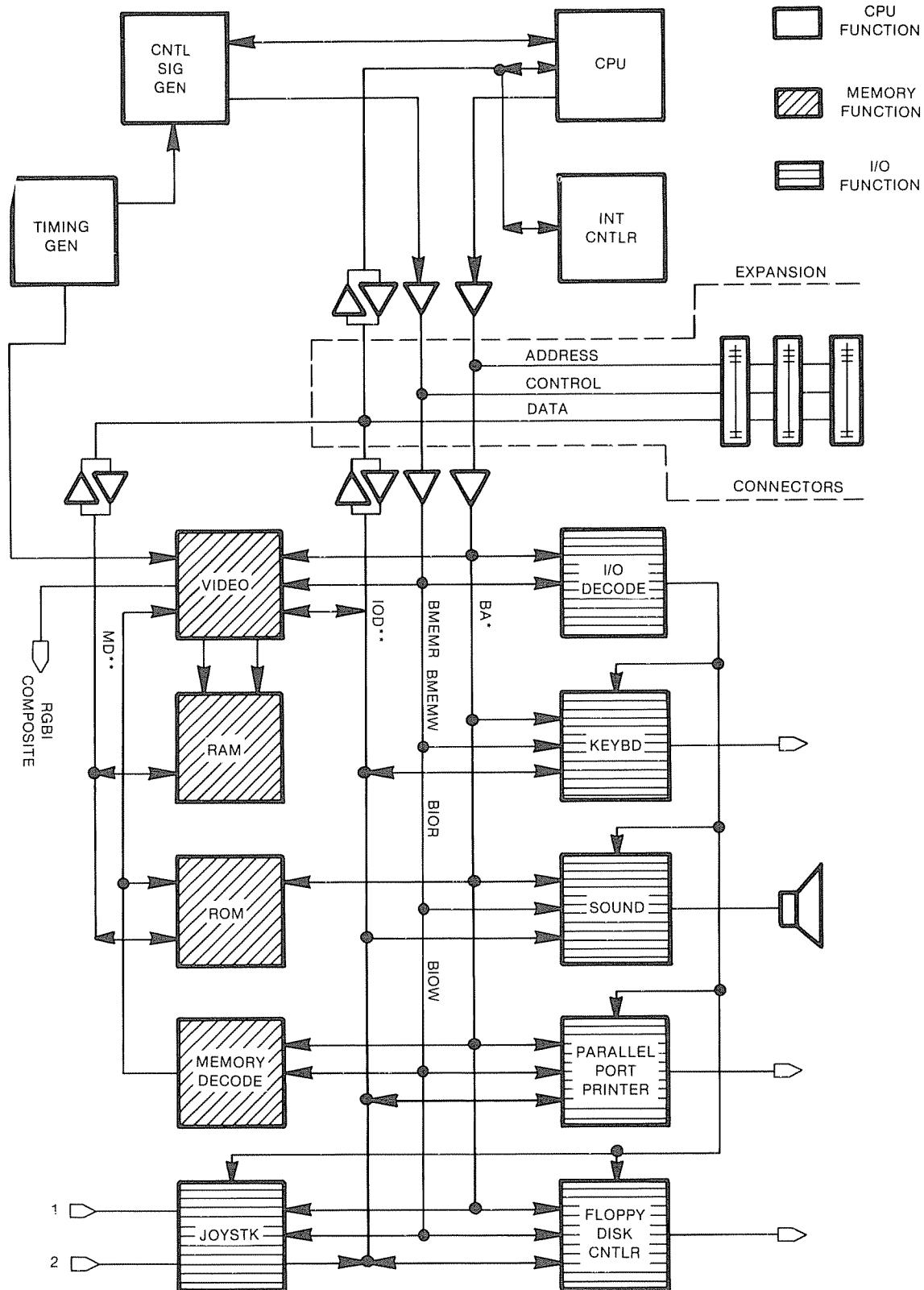


Figure 6
Main Logic Block Diagram

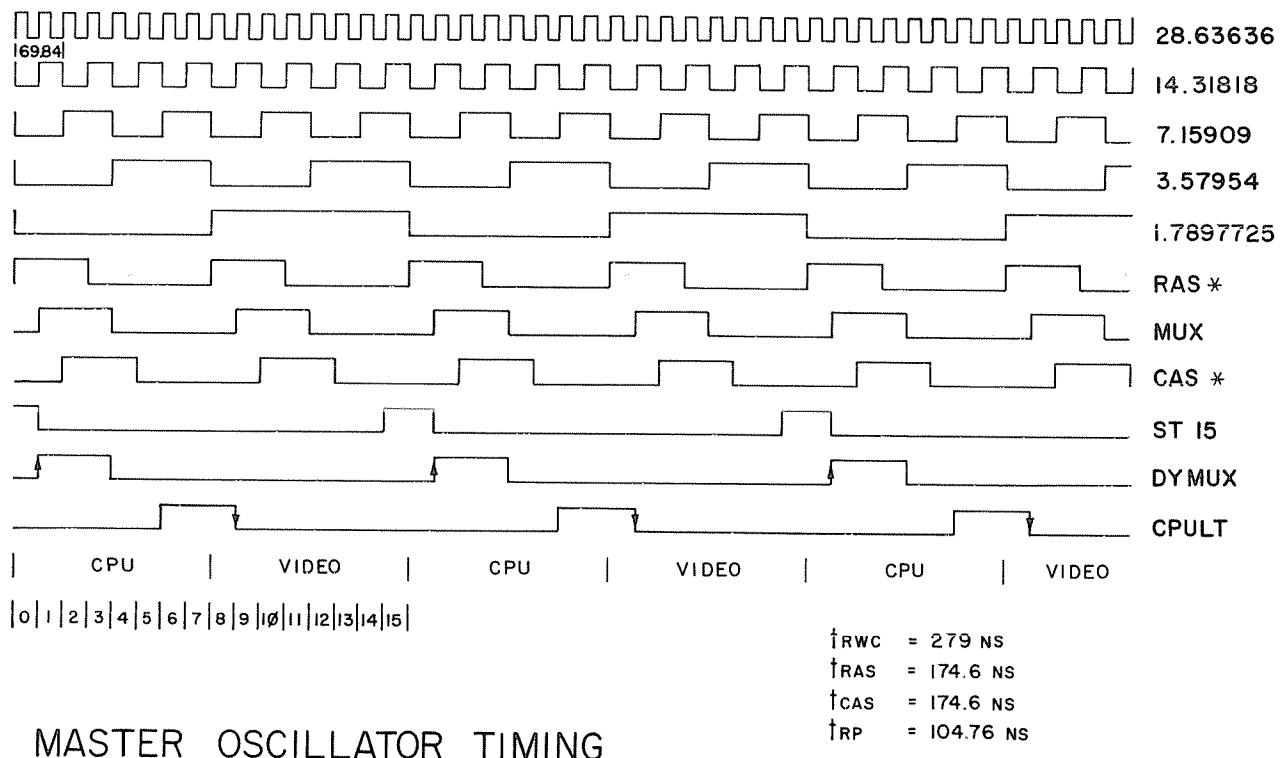


Figure 6.1
Master Oscillator Timing
(All Times in Nanoseconds)

IFL Equations

U53 Memory Address Decode

Code: 53G

Checksum: 50C9

Equations:

$$\begin{aligned}
 VSACC^* &= RFSH^* \cdot \overline{MEMR}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot \overline{MC2} \cdot \overline{MC1} \\
 &+ \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot \overline{MC2} \cdot MC1 \\
 &+ \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot MC2 \cdot \overline{MC1} \\
 &+ \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot MC2 \cdot MC1 \\
 &+ RFSH^* \cdot \overline{MEMR}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot MC3 \cdot \overline{MC2} \cdot \overline{MC1} \\
 &+ \overline{RFSH^* \cdot MEMW^*} \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot \overline{MC2} \cdot \overline{MC1} \\
 &+ \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot \overline{MC2} \cdot MC1 \\
 &+ \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot MC2 \cdot \overline{MC1} \\
 &+ \overline{RFSH^* \cdot MEMW^*} \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot MC3 \cdot \overline{MC2} \cdot \overline{MC1} \\
 &+ HGMEMAC
 \end{aligned}$$

$$\begin{aligned}
 HGMEMAC^* &= RFSH^* \cdot \overline{MEMR}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{16} \cdot 15 \\
 &+ RFSH^* \cdot \overline{MEMW}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{16} \cdot 15
 \end{aligned}$$

$$ROMSCO^* = RFSH^* \cdot \overline{MEMR}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{16} \cdot 15 \cdot 14 \cdot 13$$

$$ROMSC1^* = RFSH^* \cdot \overline{MEMR}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{16} \cdot 15 \cdot 14 \cdot \overline{13}$$

$$MEMSEL^* = VSACC^* + HGMEMAC^* + ROMCSO^* + ROMCS1^*$$

U80 Main I/O Address Code**Code: 80B****Checksum: 58F9****Inputs:****Addresses**

	15 · 14 · 13 · 12 · 11 · 10 · 9 · 8 · 7
IO0SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 0 · 0 · 0
IO1SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 0 · 0 · 1
IO4SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 1 · 0 · 0
IO6SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 1 · 1 · 0
IO7SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 1 · 1 · 1

Outputs:

INTCS*	= IO0SEL* · $\overline{6} \cdot 5 \cdot \overline{4} \cdot \overline{3}$
TMRCS*	= IO0SEL* · 6 · $\overline{5} \cdot \overline{4} \cdot \overline{3}$
PIOCS*	= IO0SEL* · 6 · 5 · $\overline{4} \cdot \overline{3}$
NMICS*	= IOSEL* · $\overline{6} \cdot 5 \cdot \overline{4} \cdot \overline{3}$
SNDCS*	= IO1SEL* · 6 · $\overline{5} \cdot \overline{4} \cdot \overline{3}$
JOYSTKCS*	= IO4SEL* · $\overline{6} \cdot \overline{5} \cdot \overline{4} \cdot \overline{3}$
PRINTCS*	= IO6SEL* · 6 · 5 · 4 · 3
FDCCS*	= IO7SEL* · 6 · 5 · 4 · $\overline{3}$
IOSEL^	= TMRCS^ + PIOCS^ + NMICS^ + SNDCS + PRINTCS^ + FDCCS^ + IO7SEL* · 6 · 5 · 4

U46 System Timing Synthesizer**Code: 46DC****Checksum: 3E69****Equations:**

$$\text{ALE} = \overline{\text{HLDA}} \cdot \text{CALE}$$

$$\begin{aligned}\text{DEN}^* &= \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \overline{\text{DT/R}} \cdot \text{C} \cdot \text{INTCS}^* \cdot \overline{\text{SS0}} (\text{IOR}) \cdot \\ &\quad (\text{during IOR}^*) \\ &+ \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \overline{\text{DT/R}} \cdot \text{C} \cdot \text{INTCS}^* \cdot \quad (\text{MEMR}) \cdot \\ &+ \overline{\text{HLDA}} \cdot \text{B} \cdot \text{DT/R} \cdot \cdot \text{INTCS}^* \cdot \overline{\text{SS0}} (\text{MEMW}) \cdot \\ &+ \overline{\text{HLDA}} \cdot \cdot \text{DT/R} \cdot \text{C} \cdot \text{INTCS}^* \cdot \overline{\text{SS0}} (\text{MEMW}) \cdot\end{aligned}$$

(during IOR^{*})

$$\text{IOR}^* = \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \text{B} \cdot \overline{\text{DT/R}} \cdot \overline{\text{SS0}}^*$$

$$\text{MEMR}^* = \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \text{B} \cdot \overline{\text{DT/R}} \cdot$$

$$\text{IOW}^* = \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \text{B} \cdot \text{DT/R} \cdot \overline{\text{SS0}}$$

$$\text{MEMW}^* = \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \text{B} \cdot \text{DT/R} \cdot \overline{\text{SS0}}$$

$$\text{IOWAIT} = \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \text{A} \cdot \overline{\text{DT/R}} \cdot \overline{\text{SS0}}$$

$$+ \overline{\text{HLDA}} \cdot \overline{\text{IO/M}} \cdot \text{A} \cdot \text{DTR}$$

U103 Video Address Decode**Code: 103C****Checksum: 44B0**

$$\begin{aligned}\text{GACS}^* &= \cdot \overline{\text{IOW}} \cdot \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot \overline{2} \cdot \overline{1} \cdot \overline{0} \cdot \text{MODE}^* \\ &+ \cdot \overline{\text{IOW}} \cdot \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot \overline{2} \cdot \overline{1} \cdot 0 \\ &+ \cdot \overline{\text{IOW}} \cdot \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot \overline{2} \cdot 1 \cdot \overline{0} \cdot \text{STATUS}^* \\ &+ \cdot \overline{\text{IOW}} \cdot \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot 2 \cdot 1 \cdot 0\end{aligned}$$

$$\text{STATUS}^* = \text{IO7SEL}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot \overline{2} \cdot \overline{1} \cdot 0$$

$$\text{MODE}^* = \cdot \text{IOW} \cdot \text{IO7SEL}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot \overline{2} \cdot \overline{1} \cdot \overline{0}$$

$$\text{LPCLR}^* = \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot \overline{2} \cdot 1 \cdot 0 \cdot \overline{\text{IOW}}$$

$$\text{LPSET}^* = \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot 2 \cdot \overline{1} \cdot \overline{0} \cdot \overline{\text{IOW}}$$

$$\text{PGCLK}^* = \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot 3 \cdot 2 \cdot 1 \cdot 0 \cdot \overline{\text{IOW}}$$

$$\text{6845CS}^* = \overline{\text{IO7SEL}}^* \cdot 6 \cdot \overline{5} \cdot 4 \cdot \overline{3} \cdot$$

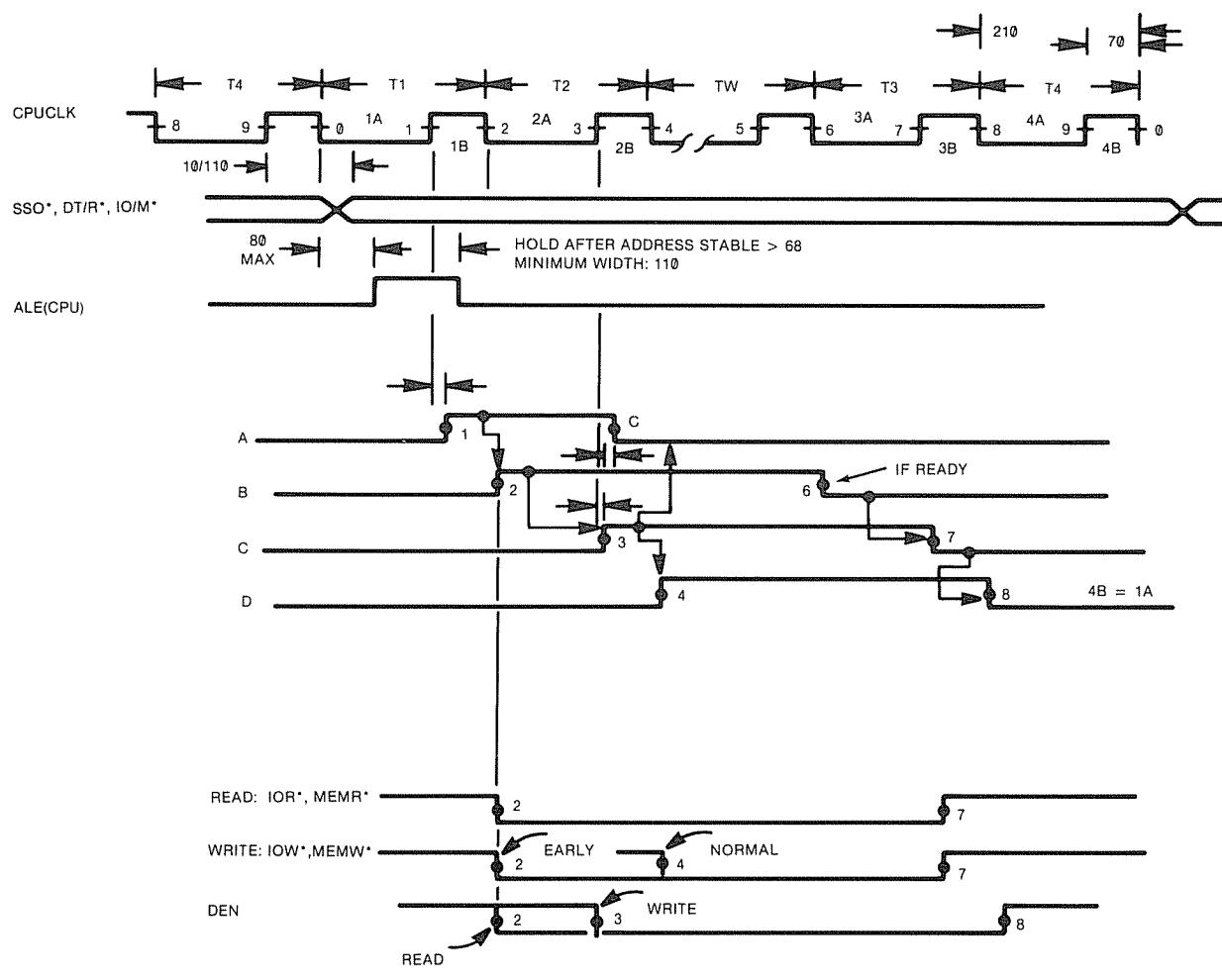
System Control Signal Generation

The System Control Signal Generator provides the timing strobes required by the system. These include IOW*, IOR*, MEMW*, MEMR*, ALE, DEN* and IO/M*. These signals are synthesized by U46 (IFL) from timing signals A,B,C,D, 8088 status signals SSO*, DT/R*, IO/M* plus HLDA and INTCS* (8259 chip select). Timing signals A, B, C, D come from flip-flops U23 and U47. The timing clock is CPUCLOCK. A CPU cycle is divided into five periods: T1, T2, T3, TWAIT, and T4. Each cycle has a clock rising edge and a clock falling edge. Thus T1+ denotes rising, and T1- denotes falling. Signal "A" is started by ALE true (T1+) and stopped by "C", (T2+). Signal "B" is started by "A" and (T1-) and stopped by CPUREADY, and "D". Signal "C" is started by "B", (T2+) and stopped by "BNOT", (T3+). Signal "D" is started by "C", (T2-) and stopped by "CNOT", (T3-). Characteristically, "A" is always one clock long while "B", "C" and "D" are variable in length depending on the number of inserted "wait" states. Thus any half-clock period between T1+ and T3- can be logically combined to create the output timing signals. See Figure 7.

All external devices, except the 8259A Interrupt Controller, are buffered by an LS244 that is controlled by the DEN* signal. Since the 8259A is not buffered, the DEN* signal must remain inactive during accesses to the 8259A.

Bus Specification

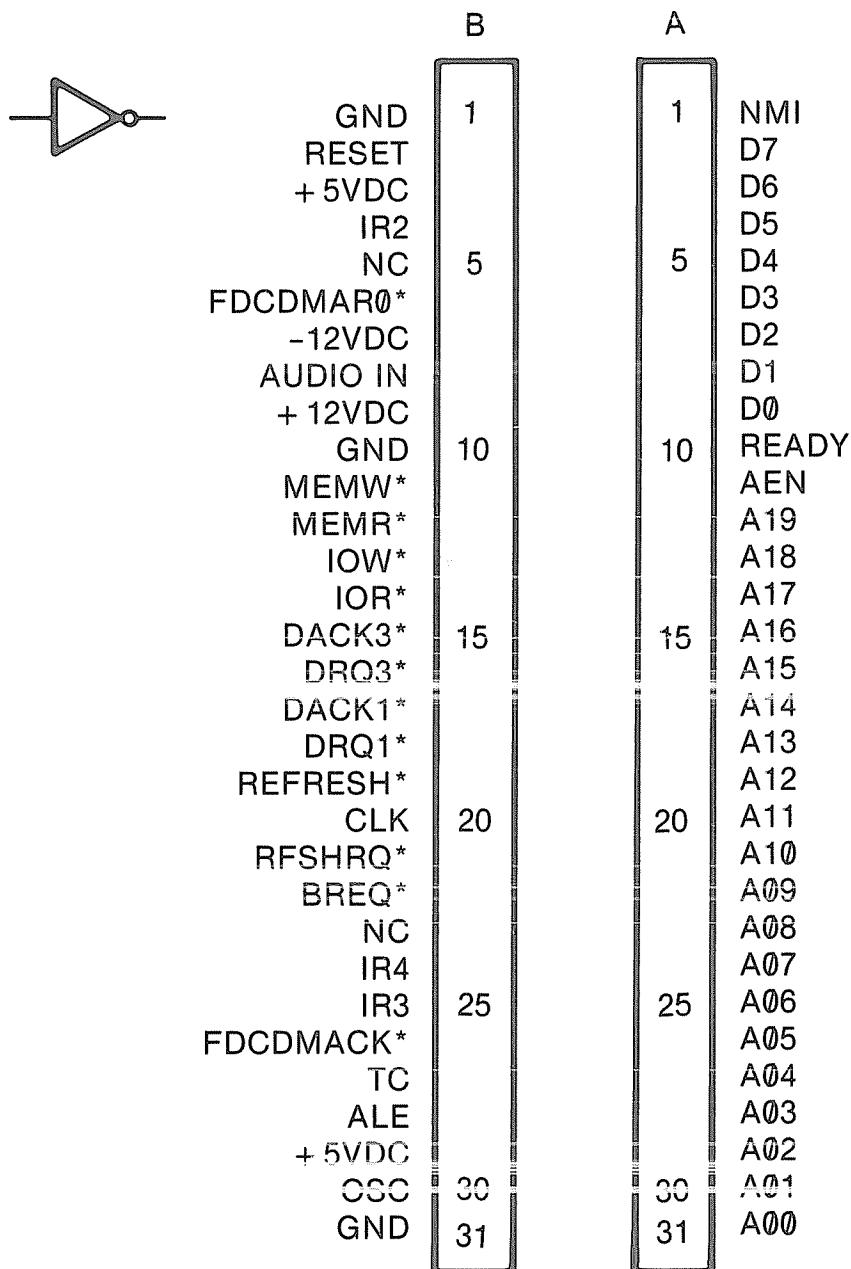
Specifications for the bus will include the expansion connector pin/signal assignments and the signal characteristics. Refer to the Expansion I/F Connector diagram. See Figure 8.



TIMING DIAGRAM

Figure 7
(All Times in Nanoseconds)

EXPANSION I/F CONNECTOR



The diagram illustrates the pinout for the Expansion I/F Connector, showing two vertical columns of pins labeled A and B. The pins are numbered sequentially from 1 at the top to 31 at the bottom. Column A (right) contains pins 1 through 10, 15, 20, 25, 30, and 31. Column B (left) contains pins 1 through 5, 10, 15, 20, 25, 30, and 31. The connector is represented by a triangular symbol with a circle at the bottom.

	B	A
GND	1	1
RESET		
+ 5VDC		
IR2	5	
NC		
FDCDMAR0*		
-12VDC		
AUDIO IN		
+ 12VDC		
GND	10	10
MEMW*		
MEMR*		
IOW*		
IOR*		
DACK3*	15	15
DRQ3*		
DACK1*		
DRQ1*		
REFRESH*		
CLK	20	20
RFSHRQ*		
BREQ*		
NC		
IR4		
IR3	25	25
FDCDMACK*		
TC		
ALE		
+ 5VDC		
CSC	30	30
GND	31	31

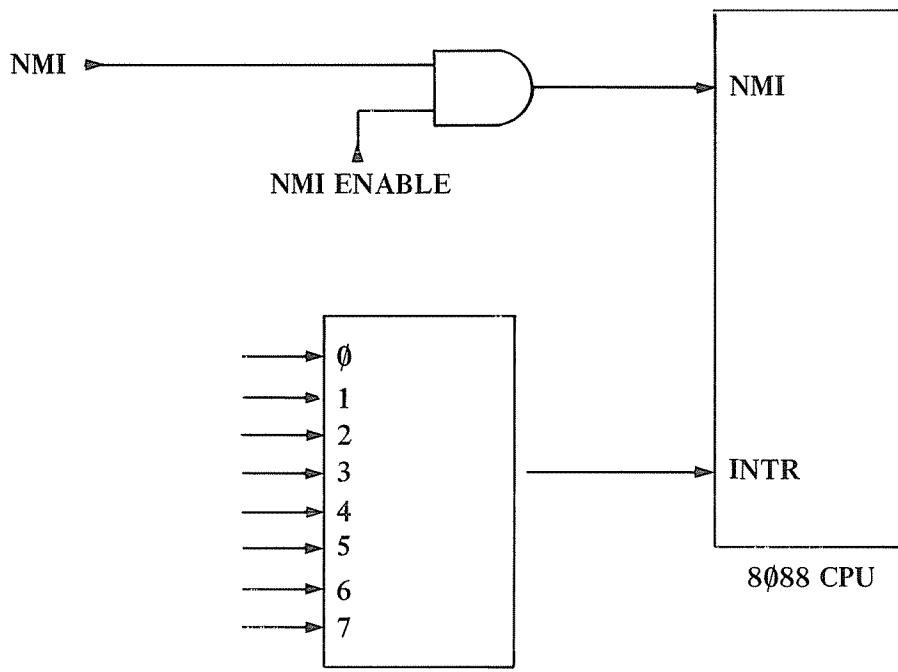
Figure 8

Interrupt Function

The 8088 supports two types of interrupts: maskable (by the CPU, INT) and non-maskable (NMI). See Figure 9. The 8259A Interrupt Controller is the source of the INT for the 8088. The 8259A has eight interrupt inputs controlled through software commands. It can mask (disable) and prioritize (arrange priority) to generate INT. These eight interrupts are:

#0	Timer Channel 0	Software Timer
#1	Keyboard	Keyboard Code Received
#2	Hard Disk Controller	Optional Function, Interrupt on Bus
#3	Modem	Optional Function, Interrupt on Bus
#4	RS-232	Optional Function, Interrupt on Bus
#5	Vertical Sync	Software Timer for Video
#6	Disk Controller, Floppy	Ready to Receive/Transmit Data
#7	Printer	Data Transmission Complete

The NMI interrupt is not maskable by the CPU but it can be enabled/disabled by hardware. The enable is at Port 00A0 Bit 7. The enable is cleared by RESET. There is no specific function assigned to NMI and it is available on the bus.

INTERRUPT STRUCTURE

8259A INTERRUPT CONTROLLER

INTERRUPT	FUNCTION
NMI	AVAILABLE ON BUS
Ø	8253 TIMER CH Ø
1	KEYBOARD
2	HARD DISK
3	SECONDARY COMM.
4	PRIMARY COMM.
5	VERTICAL SYNC.
6	FLOPPY DISK CONTROLLER
7	PARALLEL PORT

Figure 9

Bus Interface

The interface to the main bus is divided into three parts: address/control strobes, memory data and I/O data. The address/control strobe part (BA0 - BA19, BMEMR*, BMEMW*, BIOR*, BIOW*) is shared by both the I/O and the memory sections. Input buffers are U59, U60 and U42. One function of the address bus is the select logic for each of the functions. U80 decodes all the I/O chip selects except those for the Video/System Memory I/O ports which are decoded by U103. The memory selects are decoded by U53. The I/O data transceiver is U97 with its output enable decoded by U80. The memory transceiver is U14 and its output enable is decoded by U53. The direction control for both data transceivers are the "read" strobes; IOR* for U97 and MEMR- FOR U14.

Keyboard / Timer / Sound Circuits

The focal point for this circuit is the 8255 Programmable Peripheral Interface (PPI). It has three 8 bit parallel ports, A, B and C. Port A is configured as an input port and is used for keyboard data. Port B is configured as an output port and is used for control signals for the sound, keyboard and timer functions. Port C is split into 4 inputs, including the timer channel and #2 monitor and 4 outputs including the keyboard/multifunction interface signals. See Figure 10.

Keyboard Data

The computer receives data from the keyboard in an asynchronous serial format with one 8 bit word for each keystroke. This serial data is converted by the shift register, U91. This byte is then read by the CPU through the 8255 Port A. On receipt of a character an interrupt is set and the keyboard "BUSY" signal disables further transfers from the keyboard (1/2 of U104). To enable the keyboard again, the "keyboard clear" signal from 8255 Port B must be toggled. This signal when high clears the interrupt, the shift register and holds "BUSY" active (U78 pin 11.) Holding "BUSY" active prevents another character from being sent until the clear routine is complete. The serial data from the keyboard consists of a clock signal and a data signal. The clock consists of 8 consecutive positive pulses (signal normal state is logic low). The rising edge of each pulse is centered in the middle of each data period. The data signal consists of 8 data periods and a "end-of-character" bit. Normal state of the data signal is logic high which represents a logic 1. Thus the data signal will change only if the data bit is a 0. The ninth and last data bit is always a 0. In the absence of a ninth clock it will strobe a 1 into U104 and set the interrupt and busy signals. See the Keyboard Timing Chart in the Keyboard Chapter.

PROGRAMMABLE PERIPHERAL I/F 8255A-5 (PPI)

POR T ASSIGNMENTS

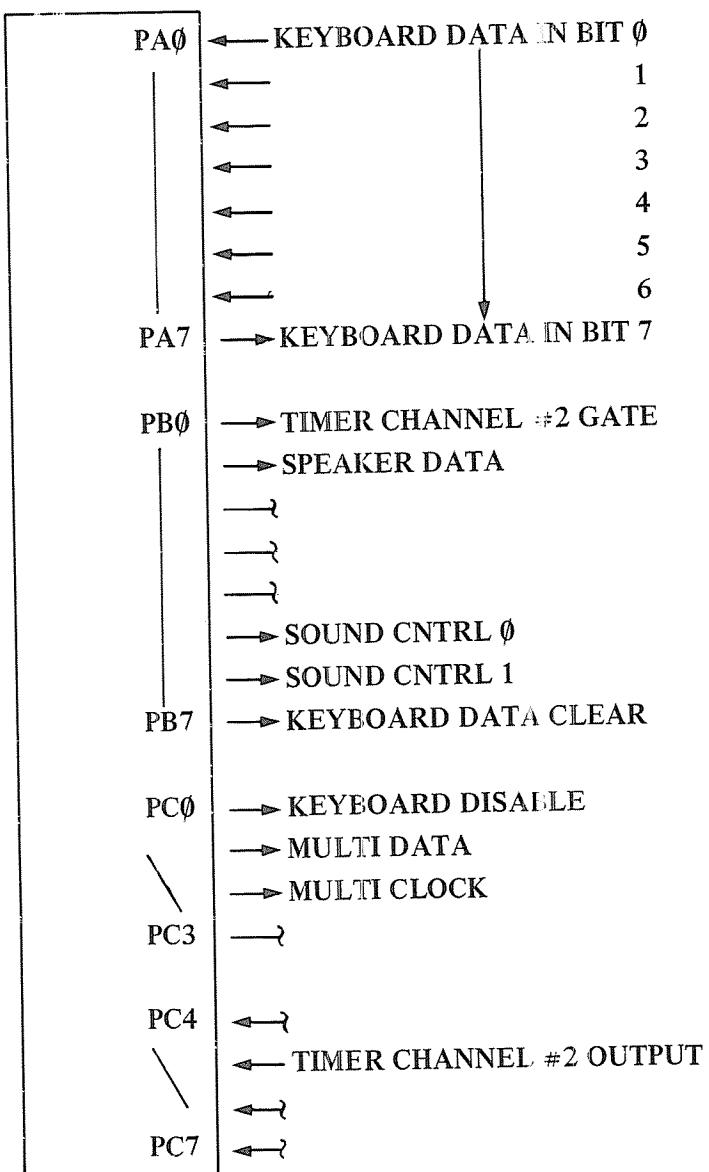


Figure 10

Timer Function

The Timer is an 8253 Timer/Counter consisting of three independent counters. The clock for all three counters is 1.1925 MHz. The gate for counter #0, #1 is permanently "on". The gate for counter #2 is controlled by a bit of the 8255 Port B. The output of counter #0 is dedicated to system interrupt #0 (8259 IR0) for software timing functions. The output of counter #1 is dedicated to the REFRESH function. When the optional DMA/Memory board is installed, DMA channel #0 is used for refreshing the RAM memory. Counter #1 sets RFSHRQ* (DRQ0) every 15 microseconds to initiate a single "dummy" memory read. The output of counter #2 is routed to the sound circuit and into the 8255 Port C for monitoring by the CPU. See Figure 11.

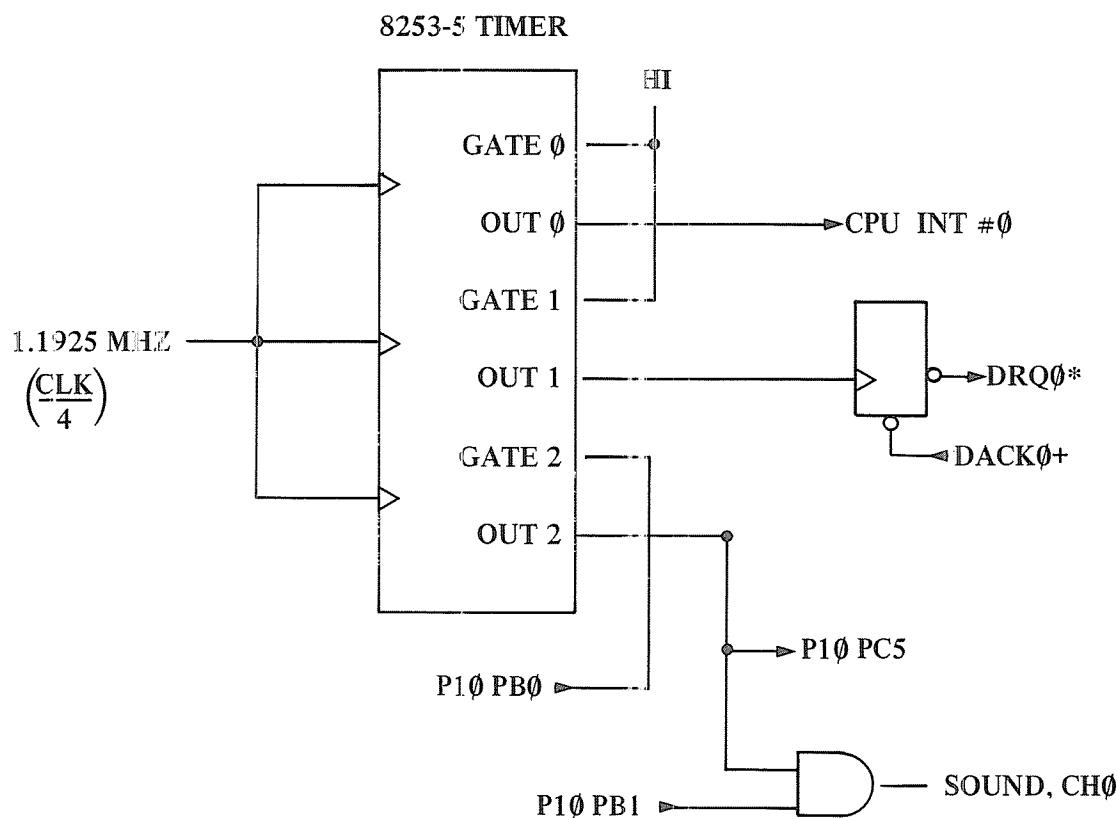
Sound Function

The sound function consists of an internal and an external sound circuit. The internal sound circuit is directly connected to the speaker via U118. The source of the sound frequencies is U96 Complex Sound Generator. Internally, U96 has four programmable sound generators. The frequency and output level of each is controlled by software. The four internal generators are summed with an external input into a single output. The external source is from the 8253 counter #2 (programmable frequency and fixed amplitude). In addition to being the only source for the unit speaker, it is one of three selectable sources for the external audio out signal. This signal is intended as an input into a external amplifier such as a stereo. The three sound frequency sources are:

1. Complex sound generator U96.
2. The 8253 counter at channel 2.
3. Any external source applied to bus interface pin B08, Audio In.

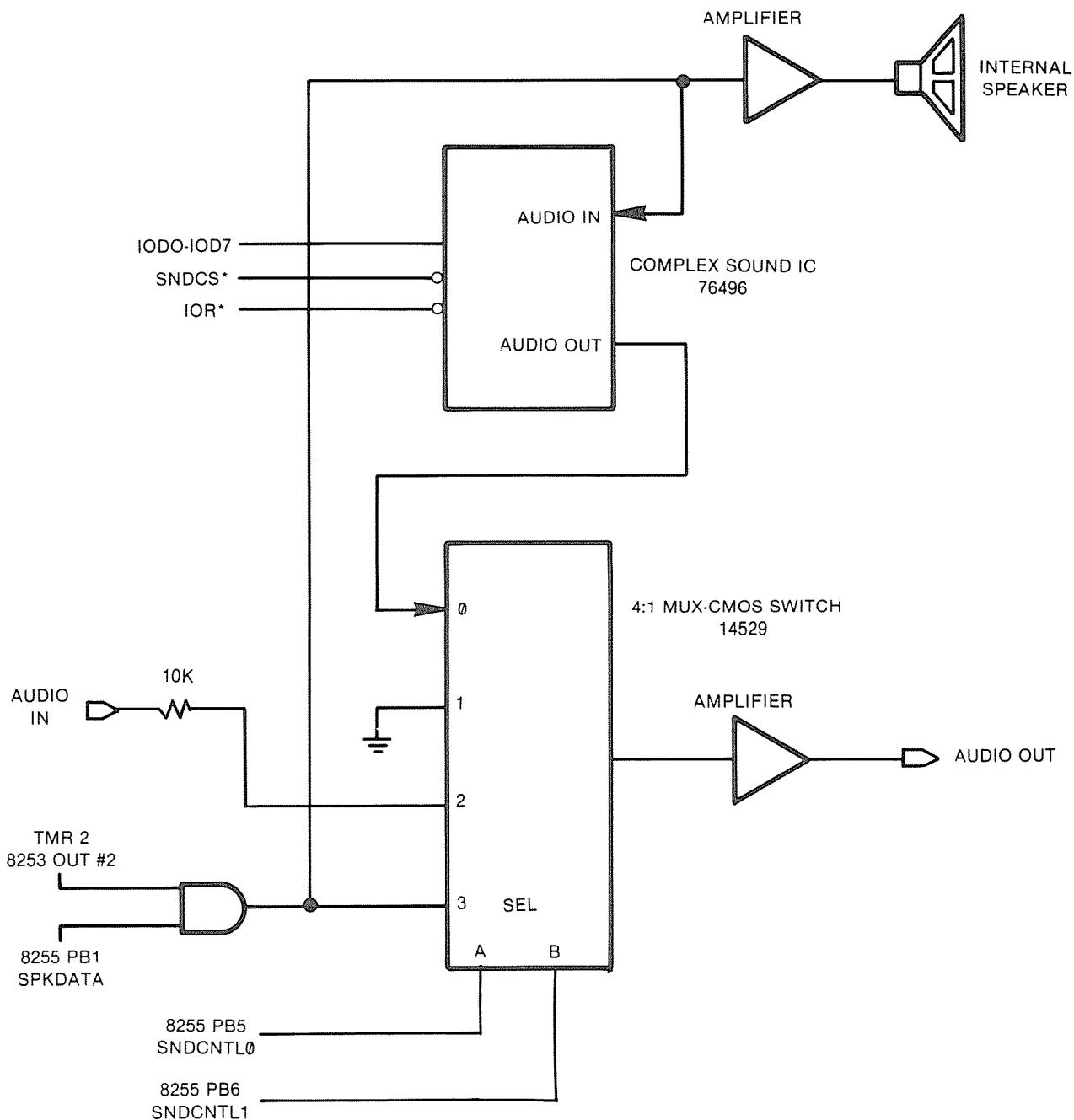
These are selected by an analog multiplexer U105. Selection signals are SNDCTL0, SNDCTL1 from the 8255. The output driver for Audio Out is U119 which is designed to drive a load impedance of 1000 ohms. See Figure 12.

SYSTEM TIMER 8253-5



CHANNEL 0: MODE 0, INTERRUPT ON T/C
1: MODE 0, NEGATIVE PULSE ON T/C
2: MODE 3, SQUARE WAVE OUTPUT

Figure 11



SOUND FUNCTIONAL BLOCK DIAGRAM

Figure 12

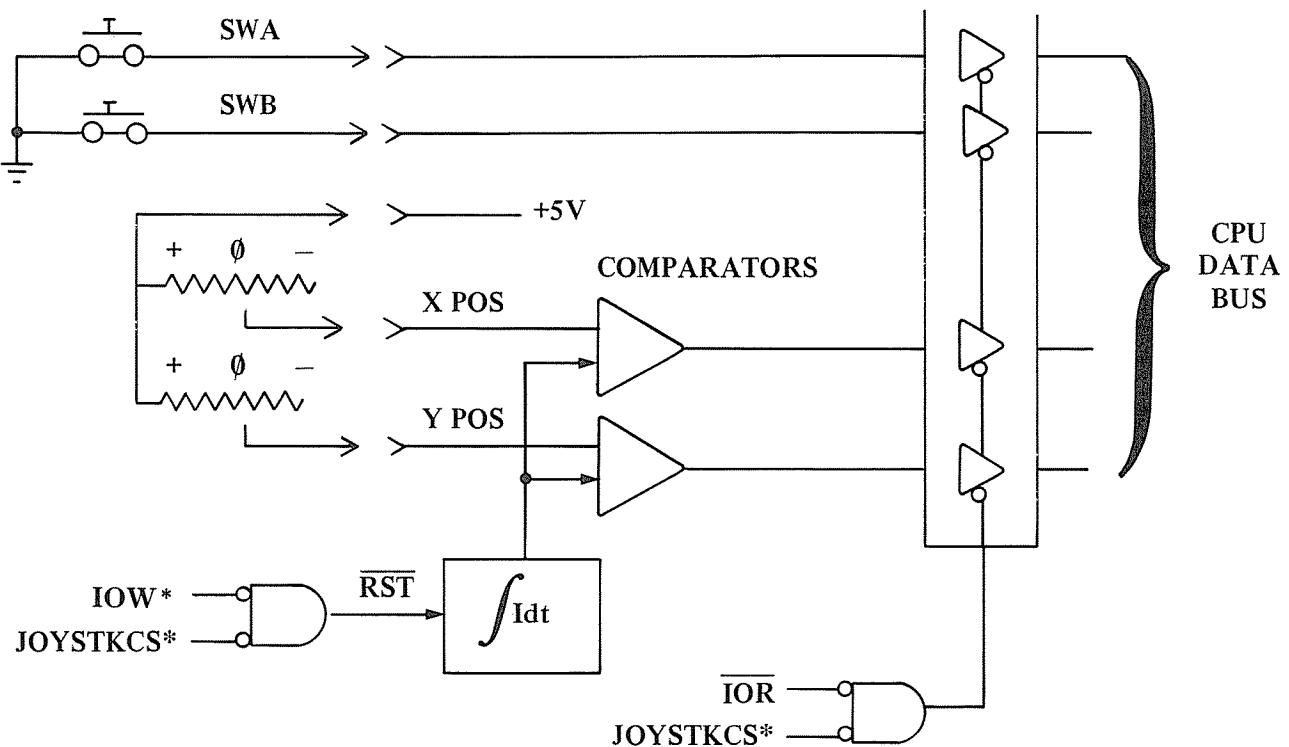
Joystick Interface

The joystick interface converts positional information from hand-held joysticks (1 or 2) into CPU data. Each joystick provides 1 or 2 push-buttons and X, Y position for a total of 4 bits each. You can use 2 joysticks. The joystick handle is connected to two potentiometers mounted perpendicular to each other; one for X position, one for Y position. Through the cable, the main logic board applies +5 VDC to one side and ground to the other of the pots. The pot wiper is the position signal: a voltage between 0 and +5 VDC. This signal is applied to one input of a comparator U119. The other comparator input is the reference signal (a ramp between 0.0 to +5.0 volts.) When the position signal is equal or less than the reference signal, the comparator output goes true. This comparator output is the X or Y position data bit. The ramp is reset to 0.0 VDC whenever a "write" is made at Port 200/201 Hex. The IOW* signal turns on Q2, which drains C6 to 0.0 volts. When Q2 is turned off, Q1, R3, R4, R9, and CR1 create a constant-current source that linearly charges C6 to +5.0 VDC in 1.12 milliseconds. The joystick information is "read" by the CPU at Port 200/201 Hex through U18. See Figure 13.

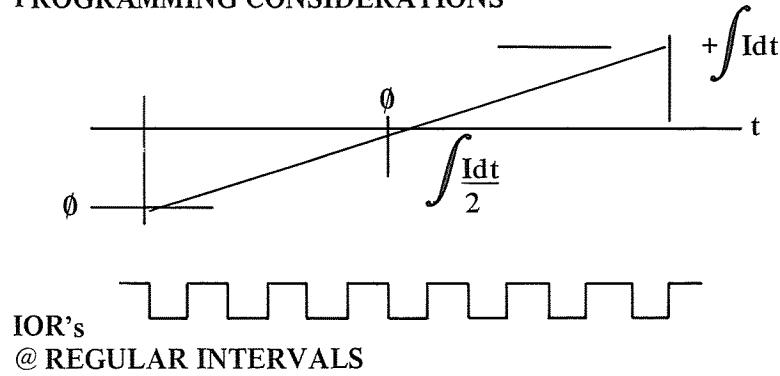
Printer Interface

The printer interface is totally contained in a custom Gate Array U108 and is shown in Figure 14. Functionally, the printer interface consists of an output data latch (write @ 378) and accompanying input data buffer. The latch and buffer reads back the output data (read @ 37A) with an accompanying input buffer for read-back (read @ 37A). The input buffer is for reading printer input signals (read @ 379), I/O address decoding, data transceiver, and interrupt logic. The interrupt is (logically) ACKNOWLEDGE* if interrupts are enabled (37A Bit 4).

JOYSTICK I/F

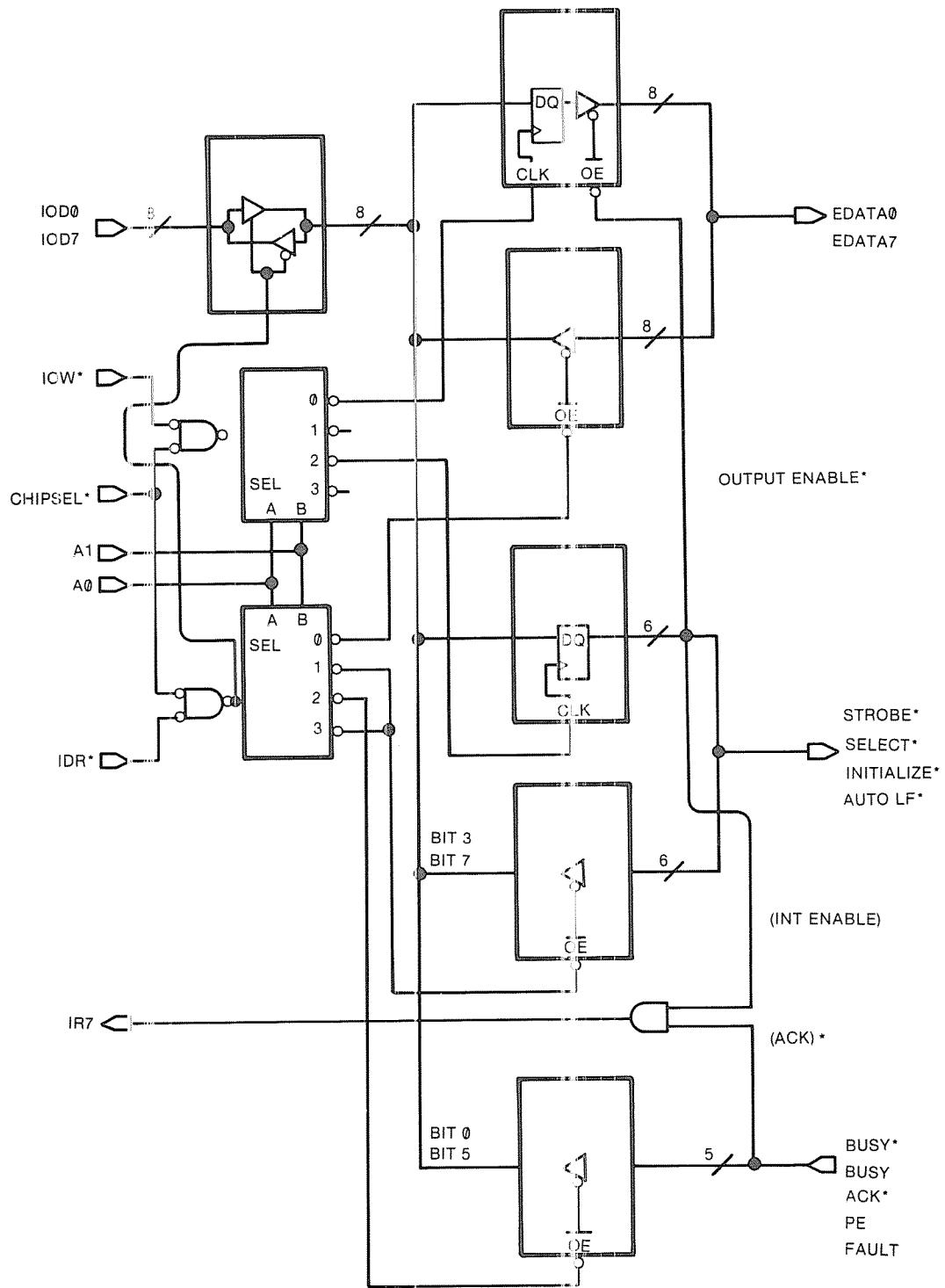


PROGRAMMING CONSIDERATIONS



ONCE TRIGGERED BY SOFTWARE THE
INTERGRATOR CIRCUIT PRODUCES A PULSE
THE DURATION OF WHICH IS DEPENDENT ON
JOYSK POSITION.

Figure 13



PRINTER SCHEMATIC

Figure 14

Floppy Disk Controller Interface

The Floppy Disk Controller interface consists of the 765 controller and support circuitry. The oscillator formed by U29, Y1 generates an 8.00 MHz clock that is divided down to 4.00 MHz and 2.00 MHz by U30. The 4.00 MHz signal is applied to the FDC for its internal processor clock (CLK pin 19) and to counter circuit U31 to generate the FDC write clock (WCK pin 21). U31 produces a pulse at count 15 that loads the next count of 8. Therefore, WCK is a 250 nanosecond pulse every 2.0 microseconds. The CPU interface consists of the chip select decode U98, U51 address A0, A1, function decode FDCCS*, and IOR*, IOW*. The function decode FDCDS* is separated into the lower four address range for the "DOR" register and into the upper four address range for the FDC; both are inhibited by AEN. The "DOR" latch U71 is for configuration control, drive select, reset, interrupt/DMA request enable, drive motor control, and software transfer terminal count. Latch U106 is used to delay the FDC DMA request (DRQ) as specified by the 765 specification. Counter U50 is used to add pre-compensation to the MFM coded write data (250 nanosecond pulse every 2.0 microseconds maximum). The 765 FDC signals "early" and "late" determine the number of 8 MHz clock periods (125 nanoseconds) the write data is delayed thru U69 - normal = 6, early = 4, late = 7. Data separator U69 converts "raw data" from the drive into read data (RDD) and read clock (RDW).

Introduction to the Video System Logic

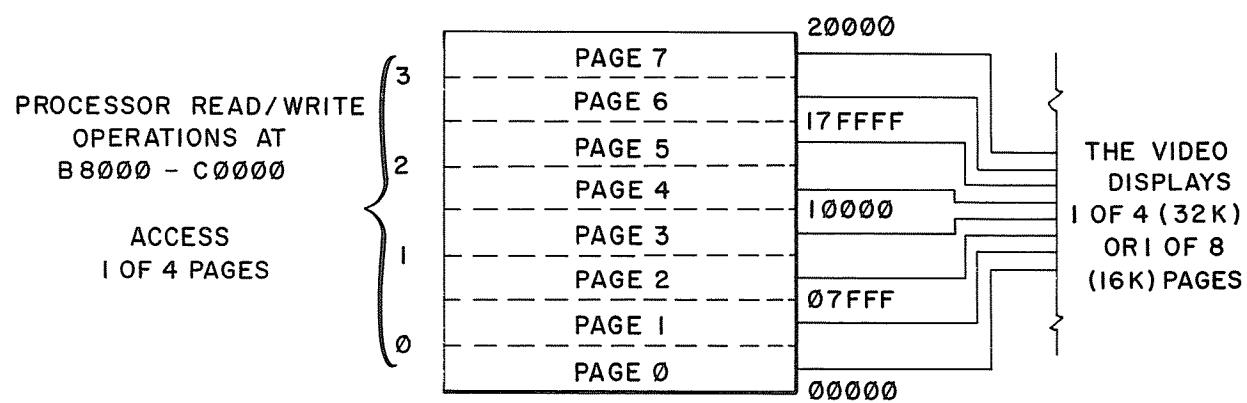
The Video System Logic is composed of three functional sections: Video Address Generation, Video Memory, and Video Data Processing.

The Video Address Generation logic is composed of the MC6845, one control register U99, and six multiplexers. The MC6845 generates the video addresses and video timing signals for all modes of operation. The control register is used for paging the 128K system memory. The MC6845 has a maximum address range of 32K. Since the Video/System RAM size is 128K, the RAM is divided into 4 pages of 32K each. Selection of the page is determined by the Page Register U99, by the Page Multiplexer U89, U90, and by associated gates. The CPU has the option of addressing the RAM at two different locations, one as 32K window starting at B8000 or as System RAM at an assigned 128K page between 00000 and A0000. The top two bits of the control register U99 are used to select different addressing modes for high resolution graphics. For programming ease, any of the graphics modes requiring only 16K of memory will be automatically selected by the addressing logic. Multiplexers U72 through U75 are used to select either the CPU or the video address and to switch between row and column addresses for the dynamic RAM chips.

The Video Memory is composed of two 8 bit rows of 64K dynamic RAMs (64K x 8 x 2) that is shared by the video and the CPU (8088). The video system sees the memory organized as 64K x 16 bits wide to allow a high video bit rate. See the RAM Timing Chart (page 43) for the RAM specifications. The CPU sees the memory as only 8 bits wide. During any read operation (either CPU or video), both banks of memory are accessed at the same time. The data is latched into U35 and U56 for the video or into U36 and U57 for the CPU. The video uses all 16 bits of memory; however, the CPU expects only 8 bits, and the extra bits are ignored. The CPU selects the 64K x 8 bank using address 00000; so the memory is organized as 128K x 8 to the CPU.

The RAM is located at an address determined by the memory configuration control port. In a 128K system that address is normally 00000 — 1FFFF. In addition this memory may be accessed at the 32K byte address from B8000 — BFFFF. A page register selects which of the 4 pages are available to the CPU. The CPU access is synchronized to the video so that no adverse effects are observed at any time.

The processor can address any location in memory while the video is using only a 16K or 32K page. This allows one video page to be displayed while another is being changed by the CPU. Therefore, the displayed page can be switched during vertical retrace. A video system memory map is shown on the next page.



VIDEO SYSTEM MEMORY MAP

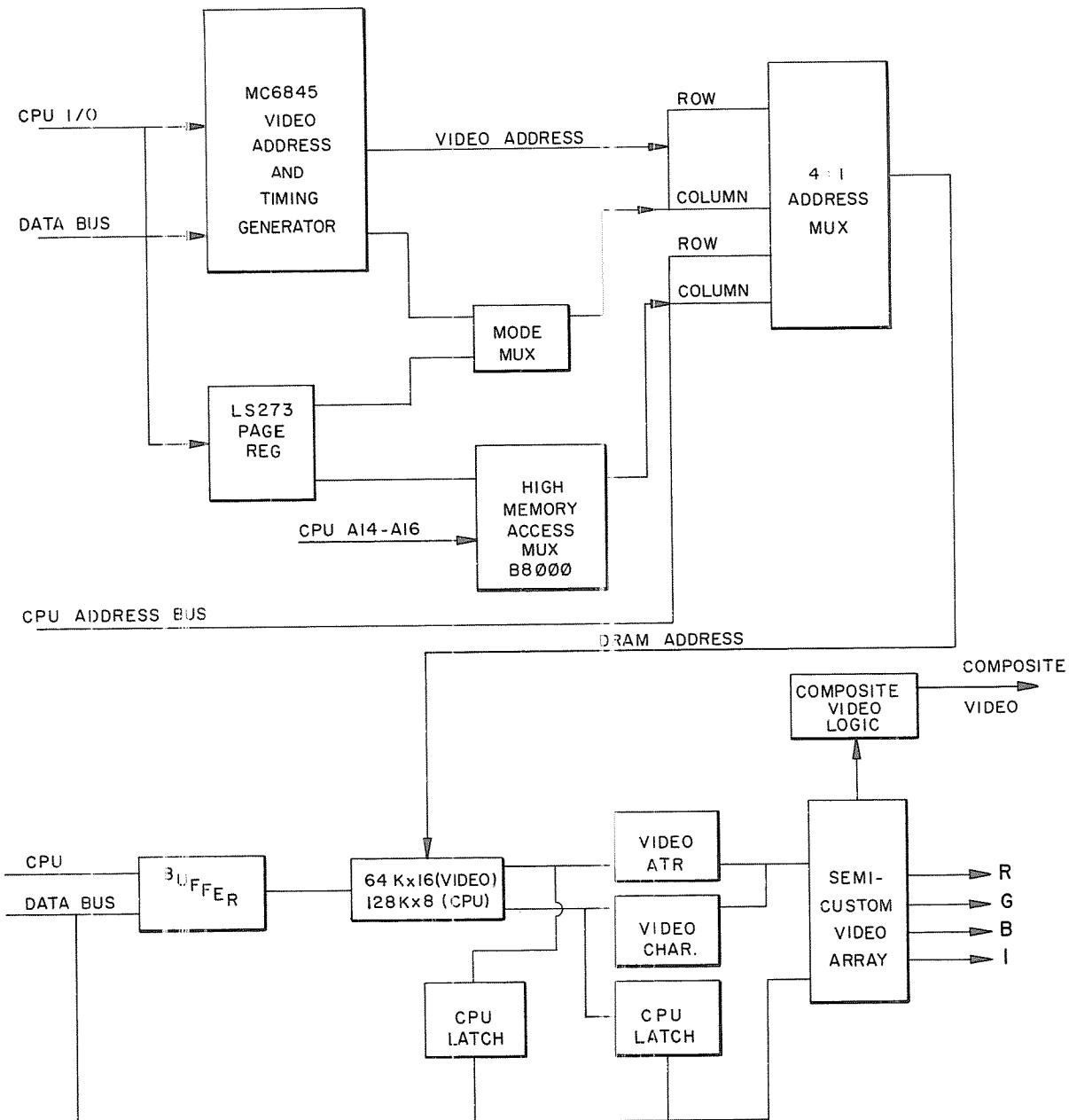
The third section of the video (Video Data Processing) is composed of only one 40-pin IC. However, a large amount of logic has been compressed into that single HCMOS custom IC. Figure 15 shows a block diagram of the logic. The multiplexed data input from the RAM is divided back into 16 bits of information. For the alphanumeric mode this is character byte and attribute byte data. In alphanumeric mode, the character data is used to address the character ROM. The character ROM output is loaded into a shift register controls the on/off selection of each video dot. The attribute byte defines foreground and background color. In graphics mode, the data bits are first rearranged depending on the mode, and then loaded into the shift register. The mode selection multiplexer selects alpha, 2 color, 4 color medium resolution, 4 color high resolution, or 16 color modes. The output of the mode selection multiplexer clocks the RGBI data before it goes to the palette RAM and then clocks it again after the palette. From this last register, the RGBI data passes through the border color mux and then through the output buffers as RGBI data. The RGB outputs are also used to generate the composite color signal.

The remaining logic of the Video Array consists of the timing logic, the control register logic and the timing delay logic. The timing logic provides the clocks and shift load signals for the latches and the shift registers. The control registers are loaded by the system software and provide the mode selection and color control bits. The timing delay logic synchronizes all the logic. See Figure 16 for the Video Array Block Diagram.

Main System Board RAM Timing Specification

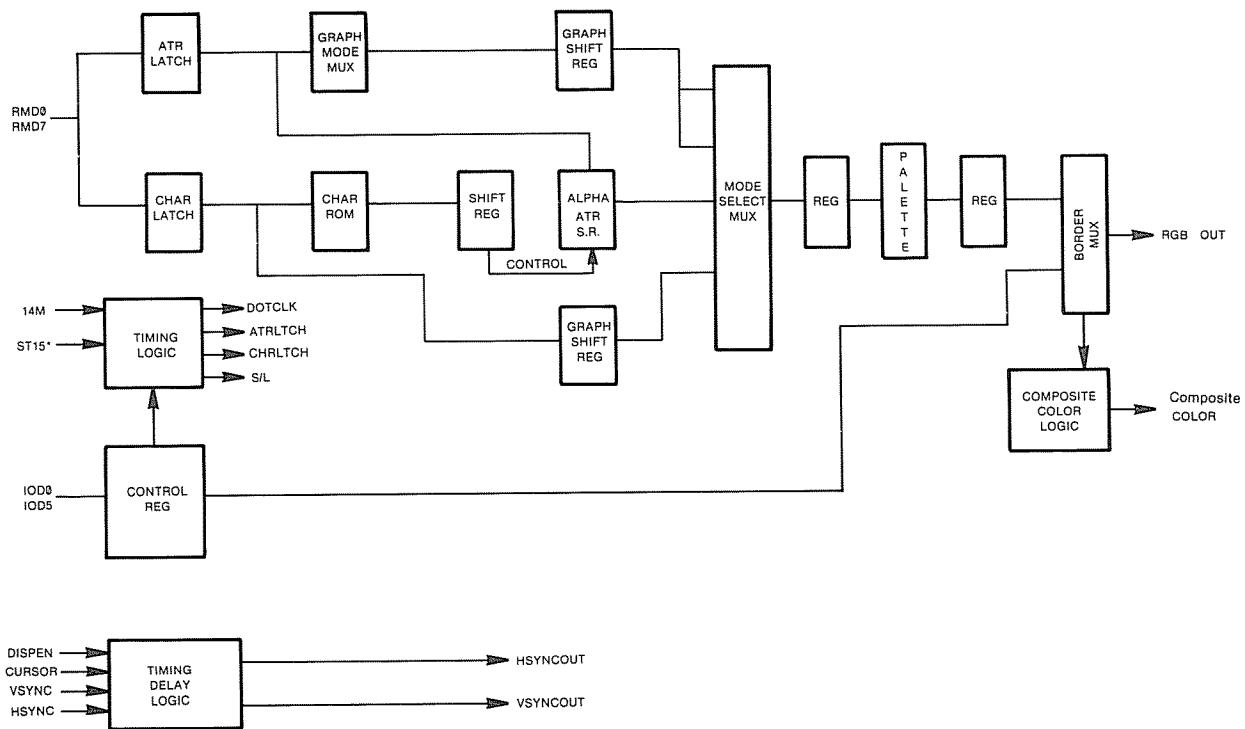
AC Operating Conditions and Characteristics

Parameter	Symbol	Min.	Max.	Units
Random Read or Write Cycle Time	tRC	279	—	ns
Read Write Cycle Time	tRWC	279	—	ns
Access Time from Row Address Strobe	tRAC	—	200	ns
Access Time from Column Address	tCAC	—	100	ns
Output Buffer and Turn-Off Delay	tOFF	0	30	ns
Row Address Strobe Precharge Time	tRP	100	—	ns
Row Address Strobe Pulse Width	tRAS1	170	—	ns
Column Address Strobe Pulse Width	tCAS	130	—	ns
Row Address Setup Time	tASR	0	—	ns
Row Address Hold Time	tRAH	20	—	ns
Column Address Setup Time	tASC	0	—	ns
Column Address Hold Time	tCAH	35	—	ns
Transition Time (Rise and Fall)	tT	—	50	ns
Read Command Setup Time	tRCS	0	—	ns
Read Command Hold Time	tRCH	0	—	ns
Read Command Hold Time Referenced to RAS	tRRH	0	—	ns
Write Command Hold Time	tWCH	35	—	ns
Write Command Hold Time Referenced to RAS	tWCR	95	—	ns
Write Command Pulse Width	tWP	35	—	ns
Write Command to Row Strobe Lead Time	tRWL	45	—	ns
Write Command to Column Strobe Lead Time	tCWL	45	—	ns
Data in Setup Time	tDS	0	—	ns
Data in Hold Time	tDH	35	—	ns
Data in Hold Time Referenced to RAS	tDHR	95	—	ns
Column to Row Strobe Precharge Time	tCRP	0	—	ns
RAS Hold Time	tRSH	85	—	ns
Refresh Period	tRFSH	—	2.0	ms
WRITE Command Setup Time	tWCS	0	—	ns
CAS to WRITE Delay	tCWD	45	—	ns
RAS to WRITE Delay	tRWD	120	—	ns
CAS Hold Time	tCSH	200	—	ns



VIDEO SYSTEM BLOCK DIAGRAM

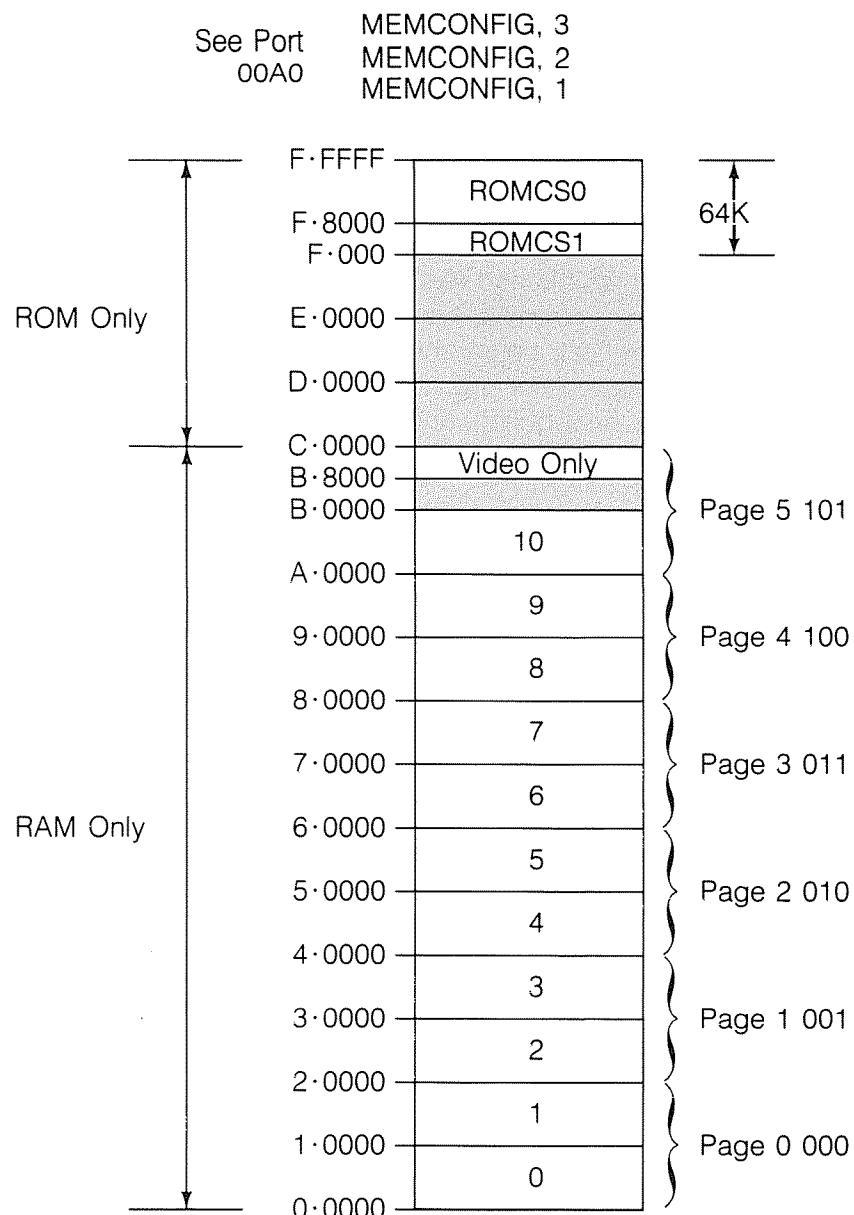
Figure 15



VIDEO ARRAY BLOCK DIAGRAM

Figure 16

Memory Map



Video System Modes

Display Modes

The video circuitry is designed to operate with three types of display devices: a standard TV using an optional RF modulator, a composite monitor and an RGBI color monitor. To support these different display types, both a composite video output and a 9-pin RGBI connector are provided.

The video display system is very flexible and can be programmed for a number of video modes. These modes use varying numbers of colors (2, 4, or 16). These 16 colors are defined by combinations of the RGBI as shown in the color chart below and can be used for foreground, background, and character blinking. If you are using a black and white monitor. (These colors will appear as shades of gray for use as reverse video, highlighting, and blinking.) In addition any 1 of the 16 colors or shades of gray can be used for the screen border.

Color	I	R	G	B
Black	0	0	0	0
Blue	0	0	0	1
Green	0	0	1	0
Cyan	0	0	1	1
Red	0	1	0	0
Magenta	0	1	0	1
Brown	0	1	1	0
Light Gray	0	1	1	1
Dark Gray	1	0	0	0
Light Blue	1	0	0	1
Light Green	1	0	1	0
Light Cyan	1	0	1	1
Pink	1	1	0	0
Light Magenta	1	1	0	1
Yellow	1	1	1	0
White	1	1	1	1

Available Colors Table

Operating Modes

The operating modes supported by the system software may be grouped into two categories: alphanumeric and graphic.

The alphanumeric mode has two basic types of operation: 80 character by 25 rows and 40 character by 25 rows. In both modes the characters are generated by a 256 character ROM. The character ROM is divided into the following groups:

- 96 Standard ASCII characters
- 48 Block Graphics characters
- 64 Foreign Language/Greek characters
- 16 Special Graphics characters
- 32 Word Processing/Scientific-Notation characters

In both modes all characters are 7 dots wide by 7 dots high and are placed in an 8 dot wide by 8 or 9 dot high matrix.

In both the 40 x 25 mode and the 80 x 25 mode, two bytes of data are used to define each character on the screen. The even address (0,2,4 etc.) is the character code and is used in addressing the character generator ROM. The odd address (1,3,5 etc.) is the attribute byte, that defines the foreground and background color of the character. The following chart shows how the attribute byte functions to control colors.

ATTRIBUTE BYTE								
BIT	7	6	5	4	3	2	1	0
3D9 Bit 5 = 0	Background				Foreground			
3D9 Bit 5 = 1	Blink	R	G	B	I	R	G	B
Blink = A 1 in bit 7 enables blinking of the foreground.								

Graphics Mode

The Video Color/Graphics System can be programmed for a wide variety of modes. The Tandy 1000 and its system ROM BIOS supports the following Graphics Modes:

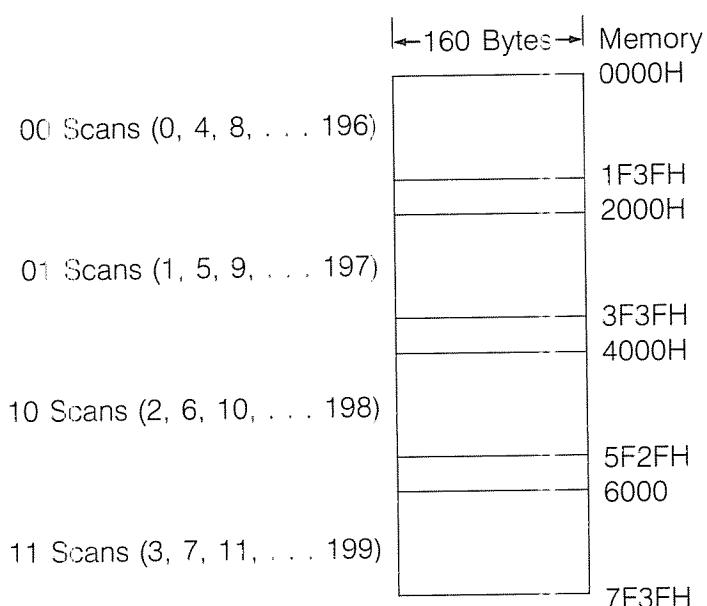
Mode	IMB PCjr	IBM PC
4-Color Medium-Resolution	X	X
16-Color Medium-Resolution	X	
16-Color Low-Resolution	X	
2-Color High-Resolution	X	X
4-Color High Resolution	X	

Low and medium resolution modes work on all types of display devices. The high-resolution mode may require a monitor for correct operation.

Graphics Memory Usage

Graphics memory uses either two or four banks of 8000 bytes. In either case pixel information for the display's upper-left corner is found at address 0000H. The 4-color high-resolution and 16-color medium-resolution graphics use four banks of 8000 bytes.

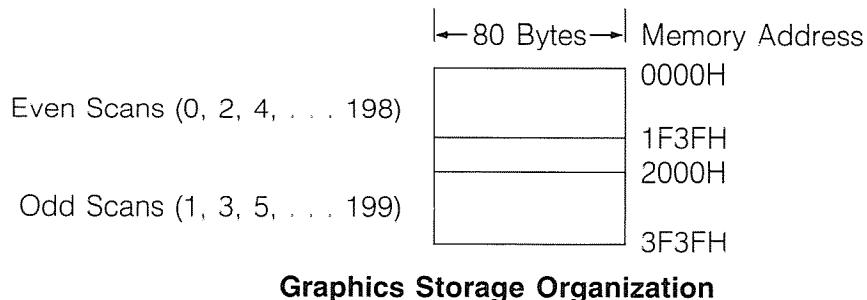
The following is a table of the graphics storage organization for four banks of 8000 bytes:



Graphics Storage Organization

The 2-color high-resolution graphics, the 4-color medium-resolution graphics, and the 16-color low-resolution graphics use only two banks of 8000 bytes.

The following is a table of the graphics storage organization for two banks of 8000 bytes:



High-resolution 2-Color Graphics

The high-resolution 2-color mode may require a high-resolution monitor for correct operation. This mode can display 2 of 16 possible colors. It contains 200 rows of 640 pixels, requires 16K bytes of read/write memory, and formats 8 pixels per byte. This mode is available in the IBM PC and IBM PCjr

- Byte 0 = eighth pixel
- Byte 1 = seventh pixel
- Byte 2 = sixth pixel
- Byte 3 = fifth pixel
- Byte 4 = fourth pixel
- Byte 5 = third pixel
- Byte 6 = second pixel
- Byte 7 = first pixel

High-Resolution 4-Color Graphics

The high-resolution 4-color mode may require a high-resolution monitor for correct operation. This mode can display 4 out of 16 colors. (Each pixel selects 1 of 4 colors.) It contains 200 rows of 640 pixels, requires 32K bytes of read/write memory and formats 8 pixels per two bytes (1 even-byte and 1 odd-byte). This mode is only supported on the IBM PCjr.

	Even Bytes	Odd Bytes
First Display Pixel	PA0 (7)	PA1 (7)
Second Display Pixel	PA0 (6)	PA1 (6)
Third Display Pixel	PA0 (5)	PA1 (5)
Fourth Display Pixel	PA0 (4)	PA1 (4)
Fifth Display Pixel	PA0 (4)	PA1 (3)
Sixth Display Pixel	PA0 (3)	PA1 (2)
Seventh Display Pixel	PA0 (1)	PA1 (2)
Eighth Display Pixel	PA0 (0)	PA1 (0)

Medium-Resolution 16-Color Graphics

The medium-resolution 16-color graphics mode works with all types of display devices. This mode specifies 1 of 16 colors for each pixel. It requires 32K bytes of read/write memory, contains 320 rows of 200 pixels, and formats each byte in the same manner as the low-resolution mode. This mode is available in the IBM PCjr only.

Second Pixel				First Pixel			
0	1	2	3	4	5	6	7
PA0	PA-	PA2	PA3	PA0	PA1	PA2	PA3

Low-Resolution 16-Color Graphics

The low-resolution mode works with all types of display devices. This mode contains 200 rows of 160 pixels, requires 16K bytes of read/write memory, specifies 16 colors for each pixel by the RGBI bits, and formats 2 pixels per byte. This mode is available in the IBM PCjr only.

Second Pixel				First Pixel			
0	1	2	3	4	5	6	7
PA0	PA1	PA2	PA3	PA0	PA1	PA2	PA3

Medium-Resolution 4-Color Graphics

The medium-resolution mode works with all types of display devices. This mode supports 4 of 16 possible colors. It requires 16K bytes of read/write memory, contains 320 rows of 200 pixels, selects 1 of 4 colors for each pixel, and formats 4 pixels per byte. This mode is available in the IBM PC and IBM PCjr.

Fourth Pixel		Third Pixel		Second Pixel		First Pixel	
0	1	2	3	4	5	6	7
PA0	PA1	PA0	PA1	PA0	PA1	PA0	PA1

System Logic Registers

Video Array Registers

The Video Array is addressed at I/O addresses 3D8, 3D9, 3DA, and 3DE. Address 3D8 and 3D9 are PC compatible control registers. Address 3DA is an address register for port selection inside the Video Array. Address 3DE is the data port. You can program all Video Array registers, except 3D8 and 3D9. Registers are programmed by first writing an address to 3DA and the data to 3DE. The following chart shows the address at each of these Video Array registers.

Register	Address Hex
Palette Mask	01
Border Color	02
Mode Control	03
Palette Registers	10 — 1F

Palette Mask Register

This 4-bit (write-only) register has a video array address of 01H. The following table lists each bit.

Bit	Palette Mask
0	0
1	1
2	2
3	3

This register allows any of the address lines into the palette where they are then forced to 0.

Border Color Register

This 4-bit (write-only) register can be addressed in the video array at 02H. The following table gives the register's bit functions.

Bit	Description
0	B (Blue) Border Color Select
1	G (Green) Border Color Select
2	R (Red) Border Color Select
3	I (Intensity) Border Color Select

Border Color Register

The screen-border color is defined by bits 0-3, that selects one of 16 colors. See the Colors Definition Table listed in this section.

Mode Control Register

This 5-bit (write-only) register is accessed at the video array address 03H. The following table gives the register's bit functions.

Bit	Description
0	Not used
1	Not used
2	Border Enable
3	4 Color High Res.
4	16 Color Mode

Mode Control Register

Bit 0 Not Used

Bit 1 Not Used

Bit 2 This bit enables the border color register. For PC compatibility this bit should be 0. For PCjr compatibility this bit should be 1.

Bit 3 For the 4 color 640 x 200 graphics mode, this bit should be set to 1 and for all other modes set to 0.

Bit 4 Set this bit to 1 for 16 color modes and to 0 for all other modes.

Palette Registers

The palette is a 16 x 4 high speed RAM that lets you redefine any color. To load the palette, write the hex address to the video array address register at 3DA. (The 16 palette registers are located at addresses 10 -1F.) Then the new palette color is written to 3DE. Only the 4 least significant bits are used as shown by the following table:

Bit	Description
0	Blue
1	Green
2	Red
3	Intensity

Palette Register Format

Bit 4 of the video array address register is used to select the palette. Once the palette is selected, hashing or noise will be observed on the display. To avoid this effect, the palette should be accessed during vertical or horizontal blanking, and the address register should be changed to less than 10 prior to returning to normal operation.

During the normal display operation, the RGBI information is used to address the palette as shown in the chart below. If a graphics mode (which uses fewer than 16 colors) is selected, the palette is addressed by the extra bits defined by the control registers at 3D8 and 3D9. Optionally, the extra bits may be masked off (PA3 and PA2 are set to 0 or PA3, PA2 and PA1 are set to 0) by using the palette mask register. When you use the mask register, only palette registers 0 and 1 will be used for 2 color modes. Only registers 0,1,2 and 3 will be used for 4 color modes.

Palette Address Bits	Palette Register															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PA0 (B)	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1
PA1 (G)	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
PA1 (R)	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
PA3 (I)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Video Memory Map and Registers

Video Memory Map

Address	Description
3D0	Not used
3D1	Not used
3D2	Not used
3D3	Not used
3D4	6845 Address Register
3D5	6845 Data Register
3D6	Not used
3D7	Not used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Video Array Address & Status
3DB	Clear Light Pen Latch
3DC	Set Light Pen Latch
3DD	Not used
3DE	Gate Array Data
3DF	CRT Processor Page Register

Operation of the video subsystem and mode selection is controlled by the registers listed in the above table. The video array registers at 3DA were explained earlier. The remaining control registers operate as follows:

6845 Address Register (3D4)

This 5-bit write-only register addresses 1 of the 18 internal data registers of the 6845 CRT controller. The selected register is then read or written through the 6845 data register.

6845 Data Register (3D5)

This port is used to access the internal data register previously selected through the 6845 address register.

PROGRAMMING TABLE FOR THE 6845 All Values in Hex (Decimal)

Register Address	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics
00 Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)
01 Horizontal Displayed	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)
02 Horizontal Sync Position	2D (45)	5A (90)	2D (45)	5A (90)	2C (44)	58 (88)	2C (44)	58 (88)
03 Horizontal Sync Width	0A (10)	0A (10)	0A (10)	0A (10)	08 (8)	10 (16)	08 (8)	10 (16)
04 Vertical Total	1C (28)	1C (28)	7F (127)	3F (63)	1F (31)	1F (31)	7F (127)	3F (63)
05 Vertical Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
06 Vertical Displayed	19 (25)	19 (25)	64 (100)	32 (50)	19 (25)	19 (25)	64 (100)	32 (50)
07 Vertical Sync Position	1A (26)	1A (26)	70 (112)	38 (56)	1C (28)	1C (28)	70 (112)	38 (56)
08 Interface Mode	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)
09 Max Scan Line Address	08 (8)	08 (8)	01 (1)	03 (3)	07 (7)	07 (7)	01 (1)	03 (3)
10 Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
11 Cursor End	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)
12 Start Address (High)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
13 Start Address (Low)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)

Monitor Mode**TV Mode**

Mode Register (3D8)

This mode register controls the basic operating characteristics of the video. It consists of a 6-bit write-only register, and each bit controls one aspect of the operation of the video subsystem.

Bit Description

- 0 High Resolution Dot Clock. This bit controls the operating speed of the video system. A "0" selects the lower speed for 40 character text or low resolution graphics modes. A "1" selects high speed for 80 character text or high resolution graphics modes.
- 1 Graphics Select. This bit selects alpha or graphics modes. A "0" selects the alpha mode. A "1" selects the graphics mode.
- 2 Black and White Select. This bit selects black and white or color mode for TV or composite monitors. A "1" will disable the color signal and give a black and white image. In RGB monitors, a different color palette is selected by this bit in 320 x 200 4 color graphics mode. This bit will have no other effect on RGB operation.
- 3 Video Enable. This bit enables or disables the video display. A "1" enables the video display.
- 4 640 Dot Graphics. This bit is used to select either of the two 640 x 200 graphics modes. A "1" selects 640 x 200.
- 5 Blink Enable. This control bit is used in the alpha mode only. A "1" selects blinking if the attribute bit is set (bit 7). A "0" selects 16 background colors. (With blinking selected only 8 background colors are available.)

Color Select Register (3D9)

This register is used to control several color features in the alpha modes and the 320 x 200 4 color mode.

Bit Description

- 0-3 Alpha Border. In either alpha mode, these bits are used to select the screen color. In the 320 x 200 4 color mode, these bits determine the background color if PA0 and PA1 are both 0. In the 640 x 200 2 color mode, they select the foreground color.
 - 0 Blue
 - 1 Green
 - 2 Red
 - 3 Intensity
- 4 Alpha Background/320 Graphics Foreground Intensity. When blink is enabled in the alpha mode, this bit is used to select the intensity. In the 320 x 200 4 color mode, the bit selects the intensity of the foreground.
- 5 320 x 200 4 Color Blue Control. This bit is used to control the blue output in 320 x 200 color graphics.

Status Register

The 4-bit "read only" register provides video and light pen status. It is addressed by a read operation at 3DA. (The video array address register is not used to select this port.) The following table gives the register's bit functions:

Bit	Status
0	Display Inactive
1	Light Pen Trigger Set
2	Light Pen Switch Made*
3	Vertical Retrace

Status Register

- Bit 0 When bit 0 is (0), the display is active. When (1), this indicates video is not displayed.
- Bit 1 When bit 1 is "high," this indicates that the light pen input has a positive-going edge, and has set the light pen trigger. When this trigger is "low," during a system power-on, it may be cleared by performing an I/O command to address 3DB. No specific data is required due to address-activated action.
- Bit 2 Bit 2 is the status of the light pen switch. When bit 2 is "low," the light pen switch is on. The switch is not latched or debounced.
- Bit 3 When bit 3 is "high," this indicates that the vertical retrace is active.

Light Pen Latch

Set 3DC

Reset 3DB

Any output to the port sets or resets the light pen latch (data byte has no effect). Before the 6845 can read the light pen again, the latch (3DB) must be cleared.

CRT/Processor Page Register

This 8-bit (write-only) register is addressed at 3DF. The descriptions below are of the register functions:

Bit	Description
0	CRT Page 0
1	CRT Page 1
2	CRT Page 2
3	Processor Page 0
4	Processor Page 1
5	Processor Page 2
6	Video Address Mode 0
7	Video Address Mode 1

CRT / Processor Page Register

CRT Page 0-2

Bits 0-2 select the 16K page used by the video. In 32K modes, bit 0 is ignored.

Processor Page 0-2

These processor page bits are combined with the CPU address to select the 32K segment of memory accessed at B8000. If an odd page number is selected (1,3,5, etc.) the window is reduced to 16K.

Video Address Mode 0-1

These bits are used in conjunction with the graphics control bit (bit 1 at 3D8) to select the video address supplied to the RAM. The following chart lists the values to be used for each video mode.

Mode Description	Video Address Mode	
	1 (Bit 7)	0 (Bit 6)
All Alpha Modes	0	0
Low-Resolution-Graphics Modes	0	1
High-Resolution-Graphics Modes	1	1
Unused, Reserved	1	0

CRT / Processor Page Register

General Memory Information

Mode Selection Summary

	40x25 Alpha B/W	40x25 Alpha Color	80x25 Alpha Color	160x200 16 Color Graphics	320x200 4 Color Graphics	320x200 4 Shades Of B/W	320x200 16 Color Graphics	640x200 2 Color Graphics	640x200 4 Color Graphics
3D8 Bit 0 HRESCK	0	0	1	0	0	0	1	0	1
3D8 Bit 1 GRPH	0	0	0	1	1	1	1	1	1
3K8 Bit 2 BW	1	0	0	0	0	1	0	0	0
3D8 Bit 4 HRESAD	0	0	1	0	0	0	0	1	1
3DA REG 03 Bit 3 4 Color	0	0	0	0	0	0	0	0	1
3DA Reg 03 Bit 4 16 Color	0	0	0	1	0	0	1	0	0

I/O Map

Address Block	Usage	Function
0000 — 001F	0000 — 000F	DMA Function
0020 — 003F	0020 — 0021	Interrupt Controller
0040 — 005F	0040 — 0043	Timer
0060 — 007F	0060 — 0063	PIO
0080 — 009F	0080 — 0083	DMA Page Register
00A0 — 00BF	00A0	NMI Mask Register
00C0 — 00DF	00C0 — 00C1	Sound Generator
00E0 — 01FF		Reserved
0200 — 020F	0200 — 0201	Joystick I/F
0210 — 031F		Reserved
0320 — 032F		Reserved Hard Disk
0330 — 036F		Not Assigned
0370 — 037F	0378 — 037B	Printer
0380 — 03CE		Not used
03D0 — 03DF	All	System Video
03E0 — 03EF		Reserved
03F0 — 03FF	03F2, F4, F5	Floppy Disk Controller
0400 — FFFF		Not Usable

System Configuration Port

I/O Address: 00A0

Data Bit		Function
D1	MEMCONFIG 1	Selects 1 Of 8 — 128K
D2	MEMCONFIG 2	Memory Pages Where
D3	MEMCONFIG 3	Video/System Ram Memory
		To Be Located. See
		Memory Map For Details.
		Register Located Main Logic.
D4		Reserved
D5		Reserved
D6		Reserved
D7	NMIEN	Enables NMI Input To
		CPU 0 = Mask 1 = Enable
		Register Located Main Logic.

ROM

System ROM

Size: 16K x 8 (128K)
 32K x 8 (256K) optional

Quantity: 1 or 2, socketed

Address Range — ROM: F0000 To FFFFF

Two 32K address segments are decoded in hardware.
 There will always be one system ROM located at the boot segment
 F8000 — FFFFF. The second system ROM will be limited to the
 second address segment F0000 — F7FFF.

No error detection capability.

RAM

RAM address range: 00000 to B8000

RAM memory used by the CPU must be continuous beginning at 00000.

Address selection granularity — 64K.

Video memory access at B8000/C0000.

Presence (quantity) of RAM in addition to video/system RAM determined by initialization routing.

Video system RAM memory address select defined by "MEMCONFIG" register at 00A0. On power-up or reset, address defaults to B8000.

No memory error detection capability.

Detailed Memory Map

Address¹	Description
0000	8237A-5 DMA Controller
0001	8237A-5 DMA Controller
0002	8237A-5 DMA Controller
0003	8237A-5 DMA Controller
0004	8237A-5 DMA Controller
0005	8237A-5 DMA Controller
0006	8237A-5 DMA Controller
0007	8237A-5 DMA Controller
0008	8237A-5 DMA Controller
0009	8237A-5 DMA Controller
000A	8237A-5 DMA Controller
000B	8237A-5 DMA Controller
000C	8237A-5 DMA Controller
000D	8237A-5 DMA Controller
000E	8237A-5 DMA Controller
000F	8237A-5 DMA Controller

Address²	Description
0020	8259A Interrupt Controller
0021	8259A Interrupt Controller
0022	8259A Interrupt Controller
0023	8259A Interrupt Controller
0024	8259A Interrupt Controller
0025	8259A Interrupt Controller
0026	8259A Interrupt Controller
0027	8259A Interrupt Controller
0028	Not used
0029	Not used
002A	Not used
002B	Not used
002C	Not used
002D	Not used
002E	Not used
002F	Not used

1. A4 - A15 are used to generate the chip select for the 8237A-5. A0, A1, A2, A3 are connected directly to the 8237A-5. The assigned addresses are 0000 - 000F. The DMA is optional.

2. A3 - A15(B) are used to generate the chip select for the 8259A. A0 is decoded directly by the 8259A. The assigned addresses are 0020-0021(B).

Address³	Description
0040	8253-5 Timer
0041	8253-5 Timer
0042	8253-5 Timer
0043	8253-5 Timer
0044	8253-5 Timer
0045	8253-5 Timer
0046	8253-5 Timer
0047	8253-5 Timer
0048	Not used
0049	Not used
004A	Not used
004B	Not used
004C	Not used
004D	Not used
004E	Not used
004F	Not used

Address⁴	Description
0060	8255A-5 PPI
0061	8255A-5 PPI
0062	8255A-5 PPI
0063	8255A-5 PPI
0064	8255A-5 PPI
0065	8255A-5 PPI
0066	8255A-5 PPI
0067	8255A-5 PPI
0068	Not used
0069	Not used
006A	Not used
006B	Not used
006C	Not used
006D	Not used
006E	Not used
006F	Not used

3. A3 - A15 are used to generate the chip select for the 8253-A. A0 is decoded directly by the 8253-A. The assigned addresses are 0040 - 0043.

4. A3 - A15 are used to generate the chip select for the 8255A-5. A1 and A0 are decoded directly by the 8255A-5. The assigned addresses are 0060 - 0063.

Detailed Memory Map—Continued

0060 — PORT A

Bit	Description
0	Keyboard Bit 0 — LSB
1	Keyboard Bit 1 —
2	Keyboard Bit 2 —
3	Keyboard Bit 3 —
4	Keyboard Bit 4 —
5	Keyboard Bit 5 —
6	Keyboard Bit 6 —
7	Keyboard Bit 7 — MSB

See Keyboard Specifications

0061 — PORT B — READ OR WRITE

Bit	Description
0	1 = 8253 Gate #2 Enabled
1	Speaker Data Out
2	Not used
3	Not used
4	Not Used
5	Sound Control 0
6	Sound Control 1
7	1 = Keyboard Clear

0062 — PORT C — READ/WRITE⁵

Bit	Description
0	(Out) Not Used
1	(Out) Multi-Data
2	(Out) Multi-Clock
3	(Out) Not Used
4	(In) Not Used
5	8253 Cut #
6	(In) Not Used
7	(In) Not Used

5. The hardware logic is configured so that Port C is split with an input at PC4 - PC7 and an output at PC0 - PC3.

Detailed Memory Map—Continued

Address⁶	Description
0080	DMA Page Reg. (Not Used)
0081	DMA Page Reg. (Ch 2)
0082	DMA Page Reg. (Ch 3)
0083	DMA Page Reg. (Ch 0, 1)
0084	Not used
0085	Not used
0086	Not used
0087	Not used
0088	Not used
0089	Not used
008A	Not used
008B	Not used
008C	Not used
008D	Not used
008E	Not used
008F	Not used

0081 — WRITE ONLY

Address	Description
Bit 0	DMA Ch 2 Address A16
Bit 1	DMA Ch 2 Address A17
Bit 2	DMA Ch 2 Address A18
Bit 3	DMA Ch 2 Address A19
Bit 4	Not used
Bit 5	Not used
Bit 6	Not used
Bit 7	Not used

0082 — WRITE ONLY

Address	Description
Bit 0	DMA Ch 3 Address A16
Bit 1	DMA Ch 3 Address A17
Bit 2	DMA Ch 3 Address A18
Bit 3	DMA Ch 3 Address A19
Bit 4	Not used
Bit 5	Not used
Bit 6	Not used
Bit 7	Not used

6. A3 - A15 are used to generate the chip select for the page register. The DMA is optional.

Detailed Memory Map—Continued

0083 — WRITE ONLY

Address	Description
Bit 0	DMA CH 0 — 1 Address A16
Bit 1	DMA CH 0 — 1 Address A17
Bit 2	DMA CH 0 — 1 Address A18
Bit 3	DMA CH 0 — 1 Address A19
Bit 4	Not used
Bit 5	Not used
Bit 6	Not used
Bit 7	Not used

Address⁷	Description
00A0	NMI Mask Register
00A1	NMI Mask Register
00A2	NMI Mask Register
00A3	NMI Mask Register
00A4	NMI Mask Register
00A5	NMI Mask Register
00A6	NMI Mask Register
00A7	NMI Mask Register
00A8	Not used
00A9	Not used
00AA	Not used
00AB	Not used
00AC	Not used
00AD	Not used
00AE	Not used
00AF	Not used

⁷ A0, A1, A2 = X.
X = don't care

Address⁸	Description
00C0	Sound SN76496
00C1	Sound SN76496
00C2	Sound SN76496
00C3	Sound SN76496
00C4	Sound SN76496
00C5	Sound SN76496
00C6	Sound SN76496
00C7	Sound SN76496
00C8	Not used
00C9	Not used
00CA	Not used
00CB	Not used
00CC	Not used
00CD	Not used
00CE	Not used
00CF	Not used

00A0, 00A1⁹

Bit	Description
0	Not Used
1	MEMCONFIG 1
2	MEMCONFIG 2
3	MEMCONFIG 3
4	X
5	X
6	X
7	1 = Enable NMI

8. The chip select is decoded for Write Only, and approximately 42 wait states are inserted.
 9. X = don't care.

Detailed Memory Map—Continued

Address¹⁰	Description
0200	Joystick
0201	Joystick
0202	Joystick
0203	Joystick
0204	Joystick
0205	Joystick
0206	Joystick
0207	Joystick
0208	Not used
0209	Not used
020A	Not used
020B	Not used
020C	Not used
020D	Not used
020E	Not used
000F	Not used

0201 — READ¹¹

Bit	Description
0	R — X Position
1	R — Y Position
2	L — X Position
3	L — Y Position
4	R Button #1
5	R Button #2
6	L Button #1
7	L Button #2

10. The assigned addresses are 0020 - 0021. A0, A1, and A2 = X.
11. A Write to 0200 restarts the integrator. Therefore, Write to 0201 before the port for joystick valves.

0378

Bit	Description
0	Data Bit 0 — LSB
1	Data Bit 1 —
2	Data Bit 2 —
3	Data Bit 3 —
4	Data Bit 4 —
5	Data Bit 5 —
6	Data Bit 6 —
7	Data Bit 7 — MSB

0379

Bit	Description
0	Not used
1	Not used
2	Not used
3	0 = Error
4	1 = Printer Selected
5	0 = End Of Form
6	0 = Acknowledge
7	0 = Busy

Address¹²

Address¹²	Description
0370	Not used
0371	Not used
0372	Not used
0373	Not used
0374	Not used
0375	Not used
0376	Not used
0377	Not used
0378	Printer — Data Latch
0379	Printer — Read Status
037A	Printer — Control Latch
037B	Printer — Not used
037C	Printer - Data Latch
037D	Printer - Read Status
037E	Printer - Control Latch
037F	Printer — Not used

12. A0 and A1 are decoded by printer logic. The assigned addresses are 0378 - 037F. A2 = X, and X = don't care.

Detailed Memory Map---Continued

037A (037E)

Bit	Description
0	0 = Strobe
1	0 = Auto FD XT
2	0 = Initialize
3	0 = Select Printer
4	1 = Enable Interrupt
5	0 = Enable Output Data
6	Not used
7	Not used

Address	Memory Map
3D0	Not used
3D1	Not used
3D2	Not used
3D3	Not used
3D4	6845 Address Register
3D5	6845 Data Register
3D6	Not used
3D7	Not used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Write Video Array Address & Read Status
3DB	Clear Light Pen Latch
3DC	Preset Light Pen Latch
3DD	Not used
3DE	Write Video Array Data
3DF	CRT Processor Page Register

**Memory Map
Video Array 3DA & 3DE**

Video Array¹³ Address (3DA)	Read (3DA)	Write (3DE)
00 Bit 0	Display Inactive	Not Used
00 Bit 1	Light Pen Set	Not Used
00 Bit 2	Light Switch Status	Not Used
00 Bit 3	Vertical Retrace	Not Used
00 Bit 4	Not Used	Not Used
01 Bit 0		Palette Mask 0
01 Bit 1		Palette Mask 1
01 Bit 2		Palette Mask 2
01 Bit 3		Palette Mask 3
02 Bit 0		Border Blue
02 Bit 1		Border Green
02 Bit 2		Border Red
02 Bit 3		Border Intensity
03 Bit 0		Not Used
03 Bit 1		Not Used
03 Bit 2		Border Enable
03 Bit 3		4 Color High Resolution
03 Bit 4		16 Color Mode
10 -- 1F Bit 0		Palette Blue
10 -- 1F Bit 1		Palette Green
10 -- 1F Bit 2		Palette Red
10 -- 1F Bit 3		Palette Intensity

13. A Read at 3DA retrieves the status of the Video Array. To write to a register within the Video Array, first write the register address at 3DA and then write the register data at 3DE.

Detailed Memory Map—Continued

MEMORY MAP

Address	Description
3D8 Bit 0	High Resolution Clock
3D8 Bit 1	Graphics Select
3D8 Bit 2	Black And White
3D8 Bit 3	Video Enable
3D8 Bit 4	640 Dot Graphics
3D8 Bit 5	Blink Enable
3D9 Bit 0	Background Blue
3D9 Bit 1	Background Green
3D9 Bit 2	Background Red
3D9 Bit 3	Background Intensity
3D9 Bit 4	Foreground Intensity
3D9 Bit 5	Color Select

MEMORY MAP (3DF)

Bit	Description
0	CRT Page 0
1	CRT Page 1
2	CRT Page 2
3	Processor Page 1
4	Processor Page 2
5	Processor Page 3
6	Video Address Mode 0
7	Video Address Mode 1

Address	Description
03F0	DOR Register
03F0	DOR Register
03F1	DOR Register
03F2	DOR Register
03F3	DOR Register (Write Only)
03F4	FDC — Status (Read Only)
03F5	FDC — Data (R/W)
03F6	FDC — Status (Read)
03F7	FDC — Data (R/W)
03F8	Not used
03F9	Not used
03FA	Not used
03FB	Not used
03FC	Not used
03FD	Not used
03FE	Not used
03FF	Not used

A1 = X

DOR A2 = 0

FDC A2 = 1

Detailed Memory Map—Continued

3F2 (WRITE ONLY)

Bit	Description
0	Drive Select A*
1	Drive Select B*
2	0 = FDC Reset
3	1 = Enable DMA Req/Interrupt
4	1 = Drive A Motor On
5	1 = Drive B Motor On
6	1 = FDC Terminal Count
7	Not Used

To Select Drive A: Bit 0 · Bit 1*

To Select Drive B: Bit 0 · Bit 1*

Troubleshooting The Main Logic Board

Troubleshooting a fault on the Main Logic Board requires a proficiency in digital logic and the use of sophisticated test equipment such as a logic analyzer. For those with this capability, the theory of operation, schematics and parts list are provided in this manual. To complete the information required, this trouble shooting guide describes the initialization and self-test diagnostics procedures contained in the on-board system ROM along with some hints based on the level of the user's experience.

During power-up or manual reset, the CPU begins operation with an "initialization/self-test" routine. When the 1000 passes this self-test, the operating system begins loading from the disk. The 8088 has a reset scheme that automatically starts with an instruction fetch at memory address FFFF0 hex which is located in the system ROM (U9). A large portion of the main logic must be operational for the CPU to "read" this information. At FFFF0 is a jump instruction to the "initialization" routine. The first instruction of this routine is a CLI (Clear Interrupt). Because the Interrupt Controller has not been programmed, any interrupts cause unpredictable behavior.

The next step is to initialize memory for the CPU to use as a scratch pad for analytic decisions. The system/video RAM is moved to begin at address A0000 hex. (A write to memory configuration port A0 also disables "non-maskable interrupts".) Then the video subsystem is programmed. Because the video subsystem continually refreshes the display, the RAM is continuously being accessed and therefore refreshed. The "character" RAM (even address) is filled with blanks (20h) and the "attribute" RAM (odd address) is filled with light gray color (07h). The display is then enabled and should reveal a "blank" screen and a cursor in the home position. To prevent the speaker from making unwanted noise the sound system is initialized. The Floppy Disk system reset "DOR" register is programmed to FDCRST—on, DRIVE #3—selected (Drives 0 and 1 deselected).

If the Video system is not functional at all, there is no way for the System to communicate with the operator via error messages. Usually at least a part of the system is functional, and you can reach some conclusions by observing the display. If the display is stable, the 6845 was programmed and the ROM can be read. Therefore the I/O and MEMORY bus are basically functional. The knowledge of what a correct display should appear like and observing, and analyzing the differences can aid in pinpointing a fault. Another indication can be the floppy drive light being on or off.

A 180h byte area of video/system RAM is tested to be used for "stack" and "data" by the CPU. The test consists of writing throughout the area in the following order all 0000's, 5555's, AAAA's and FFFF's from address BBE80 to BBFFF. (All video accesses are through the fixed video address window B8000—BFFFF). If there is a fault in writing/reading any of these data patterns, the following fault messages will be written on the screen:

```
''VID ADDR: BASE: BBE8 OFF: XXXXH''
''DATA FAULT: WRITTEN XXXX READ: XXXX''
```

When these messages appear the "offset" address should be referenced. If the offset address is at the top of the range being tested (BFFFE) this indicates that there is no available RAM in the system. The "data fault" message indicates the memory bit that is faulty. For bad bit(s) in the lower byte (even, character), displayed ASCII characters of the message or clear area may be wrong. For bad bit(s) in the upper byte (odd, attribute); the displayed message might have variations such as blinking, color change, and so on.

After establishing that a portion of the video/system memory is functional, you must determine the amount, if any, of available external memory. The external memory depends upon the DMA channel #0 for "refresh" and the DMA depends upon the Counter/Timer counter #1 for the "requests". Thus the 8253 Counter/Timer is tested. A rotating bit pattern is written/read from counter #2 with the output gate disabled. If it is faulty, the following message is displayed:

"FAULTY WRITE AND READ OF 8253 CHANNEL 2 REG"

If the test is passed counter #1 is programmed for a pulse at 15 microsecond intervals. Now the DMA controller is tested in a similar manner to verify its existence and proper operation. If it passes, channel #0 is programmed for "refresh" operation and enabled.

Next the external RAM memory size is determined. This is accomplished by reading a word of data at each 128K boundary complimenting the data, writing the data back, delaying a short time, and then reading it. When the data is wrong, assume no memory. The search is terminated. The add-on memory is address mapped to start at 00000 hex and be contiguous in 128K segments up to 512K total. When the amount of external RAM is determined, the video/system RAM is mapped to reside on top and be the uppermost 128K. At this point, the message:

"MEMORY SIZE = XXX K"

appears on the screen. If there is a possible fault, the displayed memory amount is different from the known amount. If only the base amount of 128K is accounted for, the most probable fault is an inoperative DMA refresh. Other amounts less than the full amount indicates a faulty memory.

Next, the keyboard system is initialized. First, the 8255 Programmable Parallel Interface is configured, and then the 8259 Interrupt Controller is tested by writing/reading to the "mask" register. If it fails, the message:

"FAULTY WRITE AND READ OF 8259 MASK REG"

is displayed. If it passes, the 8259 is programmed and put in polled mode, and the keyboard is flushed of all characters.

Finally, the entire RAM memory is tested because the next action is to boot the operating system from the floppy disk. The test is a modified address algorithm in which the data written is based upon the address and provides a unique byte in each location. Any errors are displayed as they are found. The display shows up to 15 lines, each time recording the data written versus the data read, base, and offset address at which the error occurred: The test makes 1 pass, and if any errors are found, stop. If there are no errors, the test proceeds.

Finally, with all the tests passed the system attempts to boot from a disk. Failure at this point indicates either a bad floppy controller subsystem or a faulty DMA subsystem. Alternate ROM-based tests are available for floppy disk testing.

7 / 54 WATT POWER SUPPLY THEORY OF OPERATION

Theory of Operation

AC Input Circuit

This circuit is composed of a fuse, an inrush current limiting circuit, a line filter, and a full wave bridge rectifier with capacitive filtering.

The fuse F1 is rated at 3.15 Amps. R1 limits the current charging C4 when the unit is first turned on.

The line filter is composed of components C1, C2, C3, and L1. The line filter restricts the amount of radio frequency noise that enters the AC line.

The Bridge Rectifier, D1, full wave rectifies the input AC. Capacitor C4 filters the rectified AC for a resultant DC voltage of about 170 Volts.

Switching Driver and Control Circuit

This circuit is a self-oscillating system, generally called an R.C.C., or Ringing Choke Converter. The R.C.C. circuit is not a constant frequency converter. When the input voltage is high and the load is light, the oscillating frequency will be highest.

When the circuit is energized, transistor Q1 is turned on by current through R2. When Q1 is turned on, current increases linearly through transformer T1, which induces a positive voltage in the bias winding, 3-2. The positive voltage induced in the bias winding regeneratively turns Q1 on harder. The current through the primary winding 5-4 increases linearly until the base drive of Q1 can no longer meet the condition of $I_b \times hfe \geq I_c$.

Where I_c = Q1 collector current or primary winding current.

I_b = Q1 Base current.

hfe = Q1 current gain.

The primary current then stops increasing, and Q1 is no longer biased on. During the time Q1 is off, energy is transferred to the secondary side through the then forward biased secondary diodes.

Short circuit protection is provided to prevent dangerous overcurrent conditions. The level of primary current is sensed at R8. If it should exceed a certain level, Q2 turns on and will short circuit the base of Q1. Q1 will turn it off and stop the current from exceeding a dangerous level. Over current protection is also provided internally by the IC voltage regulators (IC1 and IC2) that regulate the +12V and -12V outputs.

Components R5-R7, C6-C8, and D4,5 protect Q1 from high switching voltages.

5V Output Voltage Detecting Circuit

Output load current change is detected by sensing the output voltage at VR1. This signal is fed back through Opto-coupler PHC1 to Q2 which controls the base drive of Q1. The frequency at which Q1 switches and therefore the amount of energy that is transferred to the secondary side is varied according to the output load requirements.

Over Voltage Protection

If the output voltage should exceed 5.8V due to some fault condition, zener diode D10 turns on, energizing Photo-Thyristor PHC2. This turns on transistor Q2 which shorts out the base of Q1, turning it off and effectively shutting down the supply. Note that the input AC must be removed for a short interval before the power supply can restart.

Power Supply Operating Characteristics

	MIN	TYP	MAX	UNITS
Operating Voltage Range	100	120	135	VAC
Line Frequency	47	50/60	63	Hz
Output Voltages				
V01	4.85	5.05	5.25	Volts
V02	11.40	12.00	12.60	Volts
V03	-11.00	-12.00	-15.00	Volts
Output Loads				
I01	2.0	---	7.5	Amps
I02	0.2	---	1.25	Amps
I03	---	---	0.1	Amps
Over Current Protection Current Limit				
ICL1	---	---	15.0	Amps
ICL2	---	---	2.4	Amps
ICL3	---	---	1.0	Amps
Over Voltage Protection				
Crowbar	5.8	6.25	6.8	Volts
Output Noise				
V01	---	---	50	mV p-p
V02	---	---	100	mV p-p
V03	---	---	150	mV p-p
Efficiency	63	65	---	%
Hold Up Time:				
Full Load Nom Line	16	---	---	mSec
Insulation Resistance				
Input to Output	100	1000	---	M ohm
Input to Ground	100	1000	---	M ohm
Output to Ground	100	1000	---	M ohm
Isolation				
Input to GND and Output	1.7	---	---	KVDC

Troubleshooting the 54W Power Supply

1. Equipment needed for test setup:

- a. Isolation Transformer (minimum of 500 VA rating).

***** CAUTION *****

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peak. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

- b. 0-140V Variable Transformer (Variac) — Used for varying input voltage. We recommend using a minimum 10 amp, 1.4KVA rating.
- c. Voltmeter — Used for measuring DC voltages to 50 VDC and AC voltages to 200 VAC. We recommend 2 digital multimeters.
- d. Oscilloscope — Use a $\times 10$ and a $\times 100$ probe.

- e. Load Board with Connectors — See Table 1 for values of the loads required. The entries in the table for Load Board Values are the minimum power ratings for the load resistors used.

Note: Because of its design, this power supply must have a load present. Otherwise, damaging oscillations can result. Never test the power supply without a suitable load.

- f. Ohmmeter

2. Setup procedure:

Setup as shown in Figure 17. You should monitor the input and output voltages of the regulated bus, which is the +5V output, using the DVMs. Also monitor the +5V output with the oscilloscope, using 500mV/div sensitivity. You can also use the DVM monitoring the +5V output to check the other outputs. See the "No Output" section for test points within the power supply.

SET-UP PROCEDURE

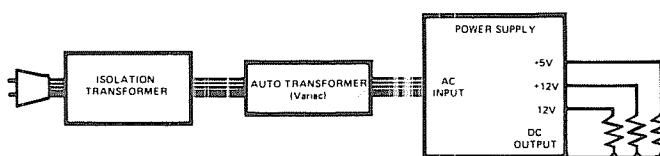


Figure 17

3. Visual inspection:

Check the power supply for any broken, burned, or obviously damaged components. Visually check the fuse. If there is a question, use the ohmmeter to check.

4. Startup:

Load the power supply with the minimum load as specified in Table 1. Bring up the power supply slowly with the variable transformer while monitoring the +5V output with the oscilloscope and DVM. The supply should start with approximately 40-60 VAC applied, and should regulate when you reach 100 VAC. If the output reaches +5 volts, do a performance test as shown in Table 2. If there is no output, refer to the "No Output" section.

LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	SAFE		SAFE	
			LOAD POWER	MAX LOAD	LOAD R	LOAD POWER
+ 5 V	2.0 A	2.5 ohm	30 W	7.5 A	0.67 ohm	50 W
+ 12 V	0.2 A	60 ohm	5 W	1.25 A	9.6 ohm	30 W
- 12 V	0	0	0	0.1 A	120 ohm	30 W

TABLE 1

5. Testing and adjustment:

After making repairs, apply maximum loading, and set the input voltage for 120 VAC. Observe the 5 Volt output, and adjust it for 5.05 Volts by varying VR1. Set up and note each of the following test conditions to be sure that the power supply is within the limits of the operating characteristics.

PERFORMANCE TEST

Test	Input	+ 5 Load	+ 12 Load	- 12 Load
1	105VAC	Max	Max	Max
2	135VAC	Max	Max	Max
3*	135VAC	Max	Max	Max
4	135VAC	Min	Min	Min
5	105VAC	Min	Min	Min

TABLE 2

*Vary the input voltage over the full range (105-135) while checking for any instability.

No Output

1. Check fuse:

If a fuse is blown, replace it but do not apply power until you find the cause of the failure.

2. Preliminary check on major primary components:

Check the bridge diode (D1), power transistor (Q1), and the catch diode (D4) for shorted junctions. If any of these components are shorted, replace them.

3. Preliminary check on major secondary components:

Using an ohmmeter on an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check over voltage protector:

Read the +5V output voltage using a DVM at the +5V output terminals while increasing input voltage from 0 volts. The output voltage appears at some input voltage and then returns to 0 volts. Check the diode D10, resistor R16, or photocoupler PHC2.

5. Check Q1 waveforms:

Read the waveform of Q1's collector with an oscilloscope using a $\times 100$ probe.

Figure 18 shows Q1's collector normal waveform.

Figure 19 shows Q1's base normal waveform.

Figures 20, 21, and 22 show waveforms of Q1's collector when secondary components are short-circuited as listed in Table 3. Check the listed parts according to the waveforms.

LIST OF SHORTED COMPONENTS

Collector Waveforms	Shorted Secondary Components
Figure - 18	C11, C12, C14, C16, C17, C18, C19, IC1-3, IC21-3, R-15
Figure - 19	D7, D8, T1 11-12, T1 7-8
Figure - 20, 21, 22	D9, T1 9, 10-13

TABLE 3

Q1 Collector Waveform
50V/div 5micro S/div
Input 100 VAC Load Minimum

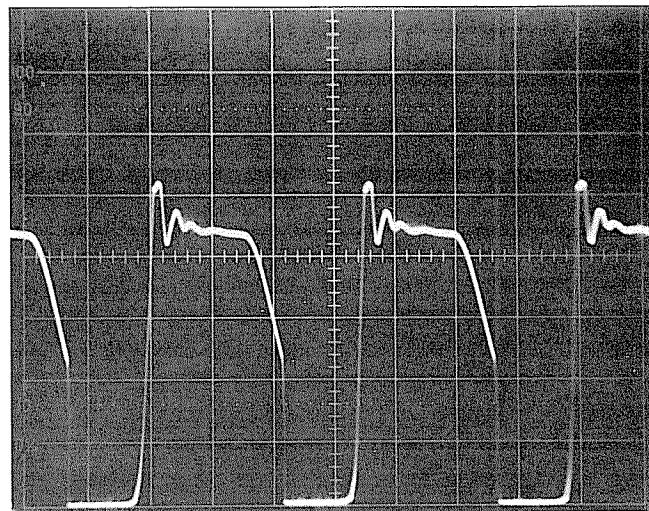


Figure 18

Q1 Base Waveform
1V/div 5micro S/div
Input 100 VAC Load Minimum

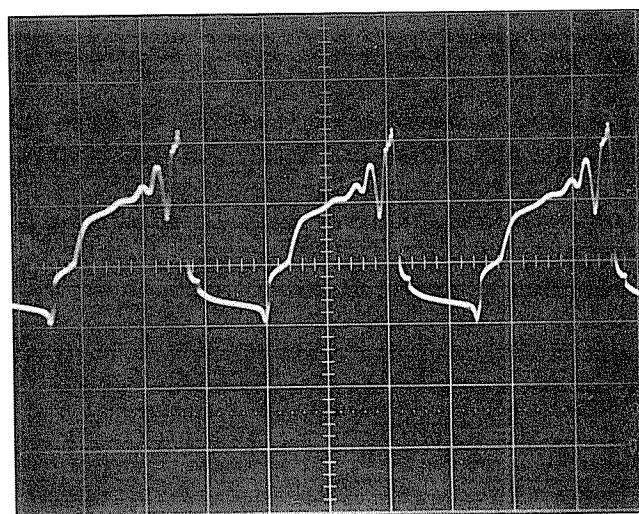


Figure 19

Q1 Collector Waveform
(Shorted Secondary Components)
50V/div 50micro S/div

Q1 Collector Waveform
(Shorted Secondary Components)
50V/div 50micro S/div

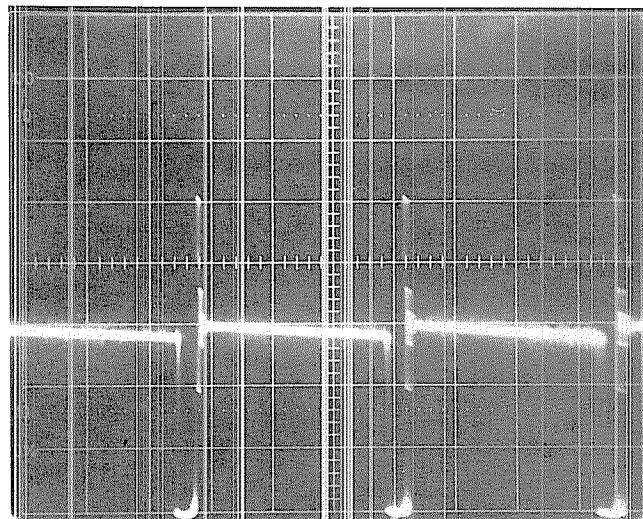


Figure 20

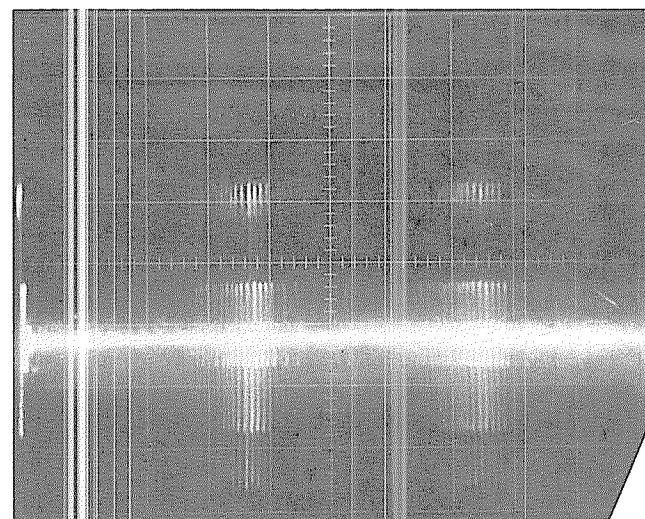


Figure 21

Q1 Collector Waveform
(Shorted Secondary Components)
550V/div 50micro/div

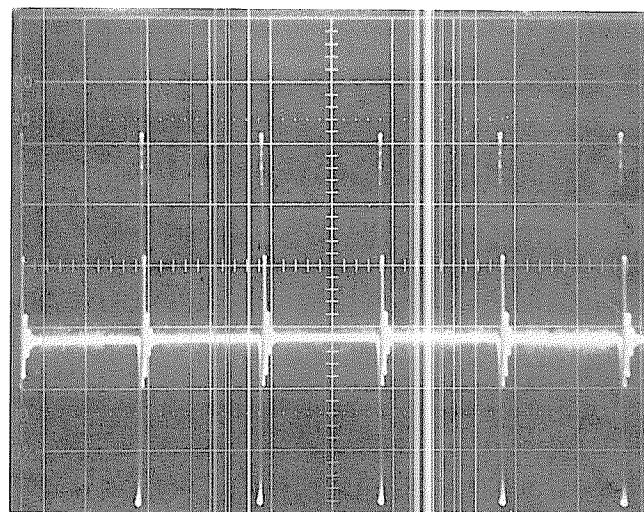
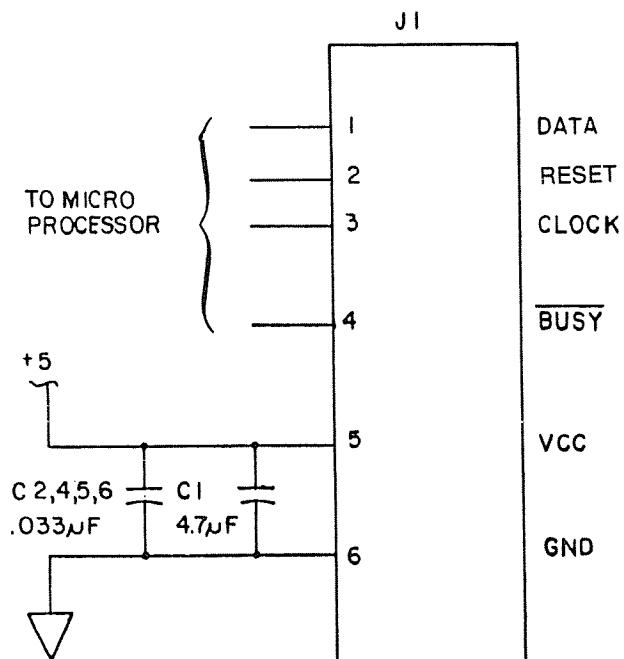


Figure 22

8 / KEYBOARD ASSEMBLY

The Tandy 1000 has a 90-key keyboard that includes 12 function keys, a numeric keypad, and special purpose keys for paging. The keyboard is connected to the Main Unit by a coiled cable and operated at a maximum distance of 4 feet from the main unit. Figure 23 shows the interconnecting cable connector to the keyboard assembly. The cable assembly can be disconnected from the keyboard assembly during repair.



Keyboard Assembly Connector
Figure 23

Keyboard Specifications

The keyboard is fully encoded with microprocessor control, and requires +5 VDC supplied from the Main Unit.

1. Key Type — all keys generate "make" and "break" codes. See the Key Code Chart. Break codes are formed by adding 80H to the make code. Keys 49 and 71 have alternate action that "makes" on one actuation of the key and "breaks" on succeeding actuation. No code is generated for these two keys when the key is released.
2. Number of Keys — 90
3. Repeat Strobe — there is a repeat strobe of 66 to 111 mSec when any key is depressed for more than 1 second, with the exception of SHIFT, CTRL, CAPS, ENTER, and NUMBER LOCK.

Key Code Chart

Key Number	Legend	Scan Code
1	F1	3B
2	F2	3C
3	F3	3D
4	F4	3E
5	F5	3F
6	F6	40
7	F7	41
8	F8	42
9	F9	43
10	F10	44
11	F11	59
12	F12	5A
13	INSERT +	55
14	DELETE -	53
15	BREAK	54
16	ESC	01
17	1 !	02
18	2 @	03
19	3 #	04
20	4 \$	05
21	5 %	06
22	6 ^	07
23	7 &	08
24	8 *	09
25	9 (0A
26	0)	0B
27	— —	0C
28	= +	0D
29	BACKSPACE	0E
30	ALT	38
31	PRINT	37
32	7 (backslash)	47
33	8 (Tilde)	48
34	9 PG UP	49
35	TAB	0F
36	Q	10
37	W	11
38	E	12
39	R	13
40	T	14
41	Y	15
42	U	16
43	I	17
45	P	19

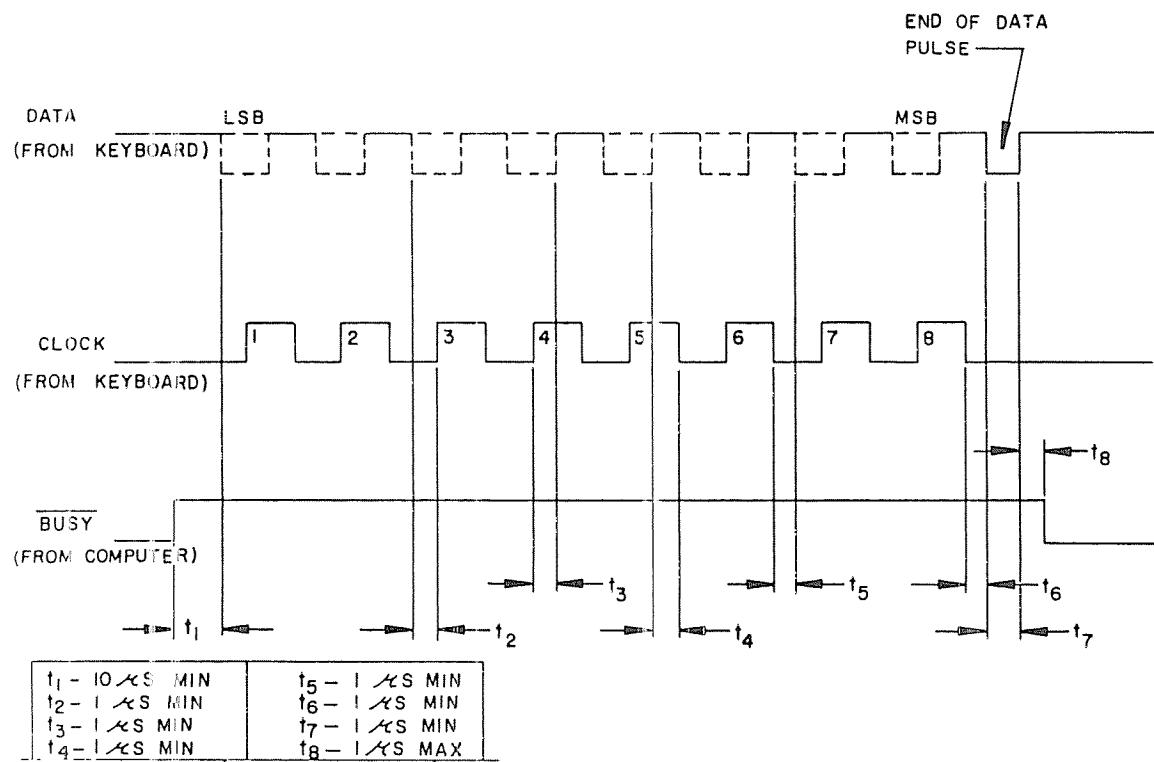
Key Number	Legend	Scan Code
46	{ [1A
47	}]	1B
48	HOLD	46
49	NUM LOCK	45
50	4 :	4B
51	5	4C
52	6	4D
53	CTRL	1D
54	A	1E
55	S	1F
56	D	20
57	F	21
58	G	22
59	H	23
60	J	24
61	K	25
62	L	26
63	;	27
64	,	28
65	ENTER	1C
66		29
67	HOME	58
68	1 END	4F
69	2 (Grave)	50
70	3 PG DN	51
71	CAPS	3A
72	SHIFT	2A
73	Z	2C
74	X	2D
75	C	2E
76	V	2F
77	B	30
78	N	31
79	M	32
80	, <	33
81	, ‡	34
82	/ ?	35
83	SHIFT	36
84		2B
85		4A
86		4E
87	0	52
88		56
89	ENTER	57

90 (Space Key)

91 thru 95 — reserved for International

Keyboard Timing

Figure 24 is the timing chart for the Tandy 1000 Keyboard Assembly.



Keyboard Assembly Timing Chart

Figure 24

Keyboard Layout

Shown below is the keyboard layout and number designation of the keys on the Tandy 1000 keyboard. They should be used with the Key Code Chart for determining data value transmitted by the keyboard.

F1	F2	F3	F4		F5	F6	F7	F8		F9	F10	F11	F12		INSERT	DELETE	BREAK
ESC	!	€	#	\$	%	^	&	*	()	-	=	BACK SPACE	ALT	PRINT	\	~
TAB	Q	W	E	R	T	Y	U	I	O	P	{	}		HOLD	NUM LOCK	1	5
CTRL	A	S	D	F	G	H	J	K	L	:	;;	ENTER			HOME	END	PG. UP
CAPS	SHIFT	Z	X	C	V	B	N	M	<	>	?	/	SHIFT	→	Ø	•	PG. DN

Keyboard Identification

Figure 25. Keyboard Identification

1	2	3	4		5	6	7	8		9	10	11	12		13	14	15	
16	17	18	19	20	21	22	23	24	25	26	27	28	29		30	31	32	
35	36	37	38	39	40	41	42	43	44	45	46	47		48	49	50	51	
53	54	55	56	57	58	59	60	61	62	63	64	65		66	67	68	69	
71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	
	91	92			90						93	94	95					89

NOTE: KEYS 91 THRU 95 NOT USED ON U.S. VERSION, USED ON
INTERNATIONAL VERSION ONLY

Key Number Identification

Figure 26. Key Number Identification

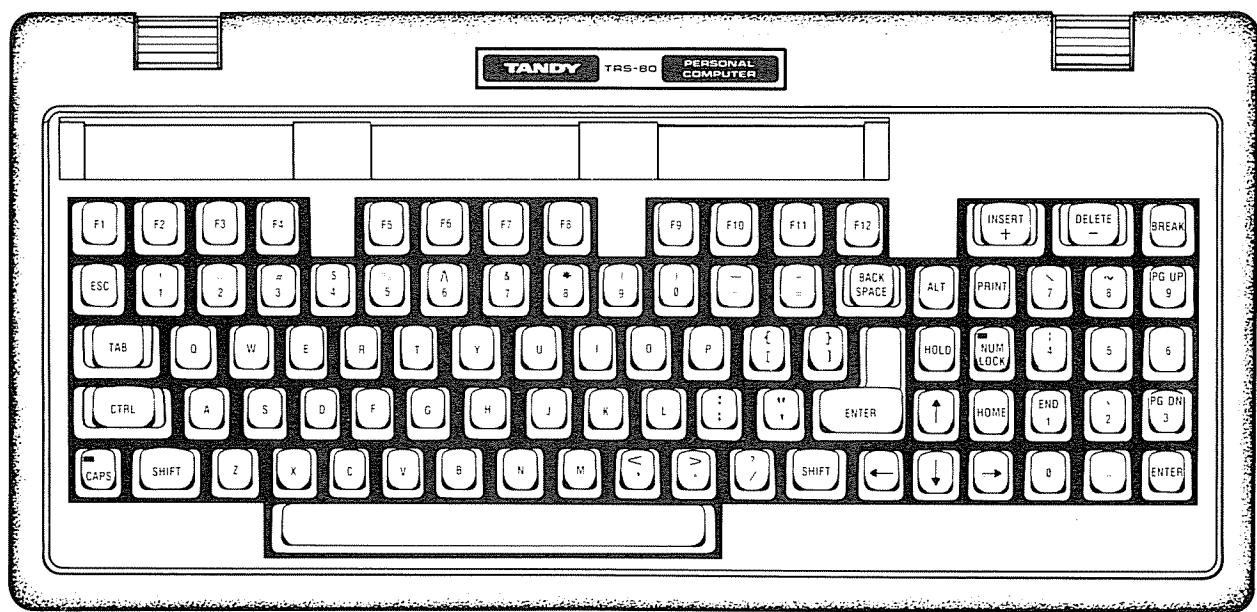


Figure 27
Tandy 1000 Keyboard

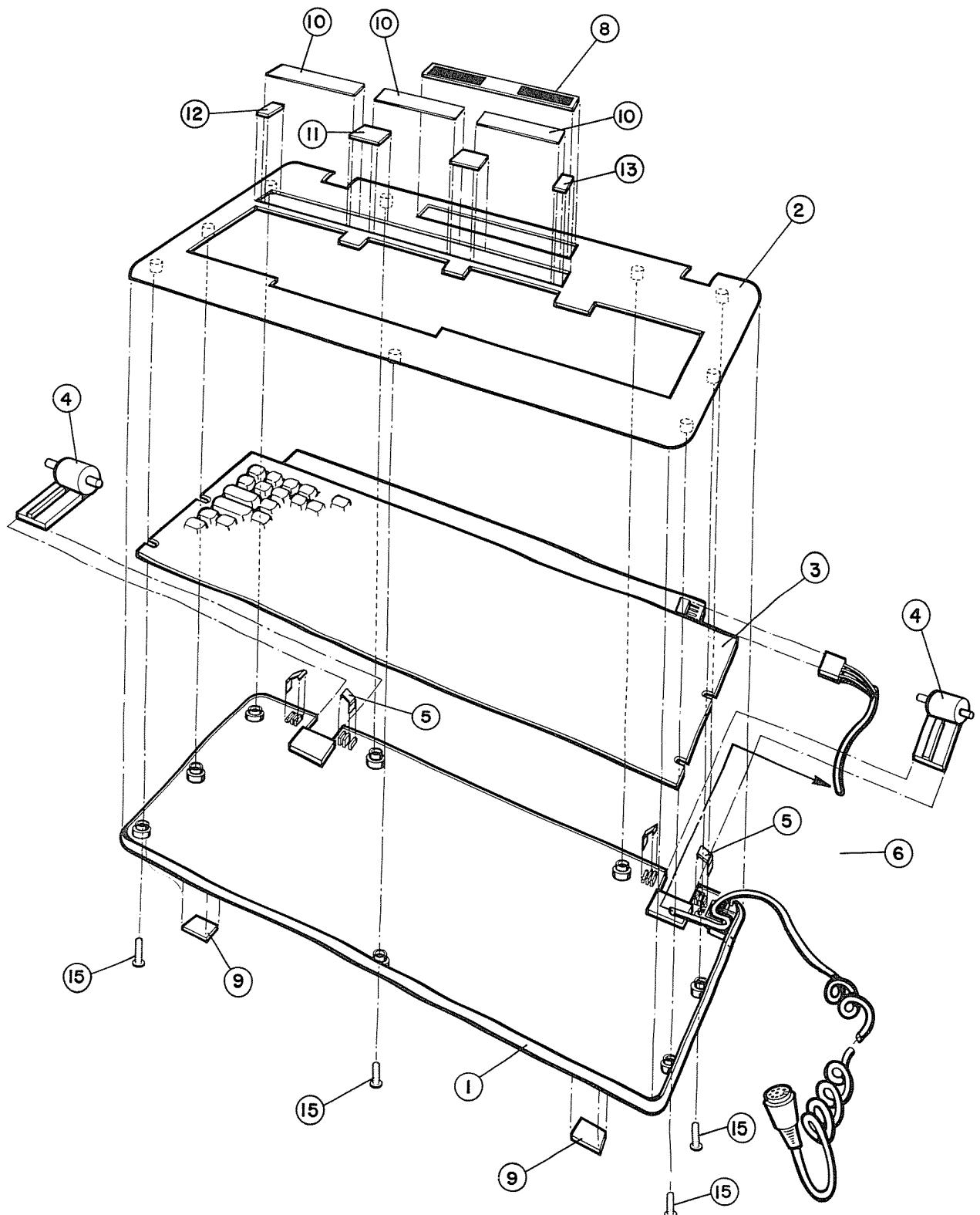
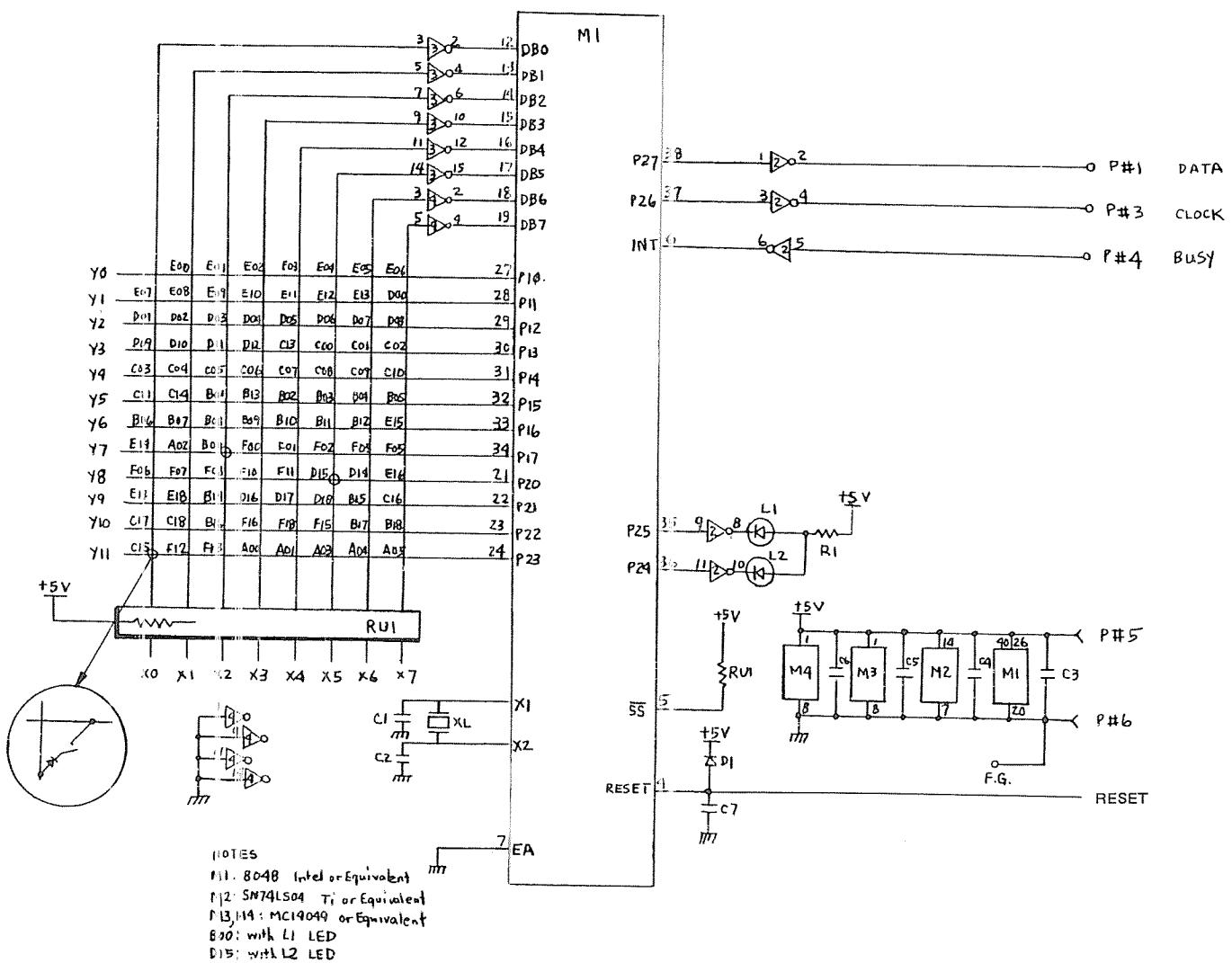


Figure 28
Keyboard Exploded View



Schematic of Keyboard Assembly

9 / PARTS LISTS

Tandy 1000 Main Logic Cat. No. 25-1000

Symbol	Qty.	Description	Part No.
—	1	Tandy 1000 PCB	8709556
R1*	1	Resistor 0 ohm 1/4 Watt 5%	8290000
R2*	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222
R3	1	Resistor 82K Ohms 1/4 Watt 5%	8207382
R4	1	Resistor 560 Ohms 1/4 Watt 5%	8207156
R5	1	Resistor 1 MEG Ohms 1/4 Watt 5%	8207510
R6-7	2	Resistor 10K Ohms 1/4 Watt 5%	8207310
R8	1	Resistor 1 MEG Ohms 1/4 Watt 5%	8207510
R9	1	Resistor 680K Ohms 1/4 Watt 5%	8207468
R10-11	2	Resistor 10K Ohms 1/4 Watt 5%	8207310
R12-13	2	Resistor 1 MEG Ohms 1/4 Watt 5%	8207510
R14	1	Resistor 10K Ohms 1/4 Watt 5%	8207310
R15		NOT USED	
R16	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222
R17	1	Resistor 33 Ohms 1/4 Watt 5%	8207033
R18	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222
R19	1	Resistor 33 Ohms 1/4 Watt 5%	8207033
R20	1	Resistor 4.7K Ohms 1/4 Watt 5%	8207247
R21	1	Resistor 10K Ohms 1/4 Watt 5%	8207310
R22		NOT USED	
R23	1	Resistor 10K Ohms 1/4 Watt 5%	8207310
R24	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222
R25	1	Resistor 910 Ohms 1/4 Watt 5%	8207191
R26-27	2	Resistor 4.7K Ohms 1/4 Watt 5%	8207247
R28	1	Resistor 33 Ohms 1/4 Watt 5%	8207033
R28A	1	Resistor 27 Ohms 1/4 Watt 5%	8207027
R29	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222
R29A	1	Resistor 470 Ohms 1/4 Watt 5%	8207147
R30-31		NOT USED	
R32	1	Resistor 10K Ohms 1/4 Watt 5%	8207310
R32A	1	Resistor 33 Ohms 1/4 Watt 5%	8207033
R33		NOT USED	
R34	1	Resistor 1K Ohms 1/4 Watt 5%	8207210
R35	1	Resistor 910 Ohms 1/4 Watt 5%	8207191
R36-37	2	Resistor 33 Ohms 1/4 Watt 5%	8207033
R38-39		NOT USED	
R40-45	6	Resistor 33 Ohms 1/4 Watt 5%	8207033
R46	1	Resistor 1K Ohms 1/4 Watt 5%	8207210
R46A	1	Resistor 47 Ohms 1/4 Watt 5%	8207047
R47	1	Resistor 1K Ohms 1/4 Watt 5%	8207210
R47A	1	Resistor 1K Ohms 1/4 Watt 5%	8207210
R48	1	Resistor 4.7K Ohms 1/4 Watt 5%	8207247
R49-51		NOT USED	
R52	1	Resistor 10K Ohms 1/4 Watt 5%	8207310
R53	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222

Main Logic Parts List continued

Symbol	Qty.	Description	Part No.
R54	1	Resistor 680 Ohms 1/4 Watt 5%	8207168
R55	1	Resistor 750 Ohms 1/4 Watt 5%	8207175
R56	1	Resistor 3.3K Ohms 1/4 Watt 5%	8207233
R57	1	Resistor 1.1K ohm 1/4 Watt 5%	8207211
R58	1	Resistor 750 Ohms 1/4 Watt 5%	8207175
R59	1	Resistor 160 Ohms 1/4 Watt 5%	8207116
R60	1	Resistor 22 Ohms 1/4 Watt 5%	8207022
R61	1	Resistor 360 Ohms 1/4 Watt 5%	8207136
R62	1	Resistor 75 Ohms 1/4 Watt 5%	8207075
R63	1	Resistor 2.7K Ohms 1/4 Watt 5%	8207227
R64	1	Resistor 100K Ohms 1/4 Watt 5%	8207410
R65	1	Resistor 680 Ohms 1/4 Watt 5%	8207168
R66	1	Resistor 10 Ohms 1/4 Watt 5%	8207010
R66A	1	Resistor 10K Ohms 1/4 Watt 5%	8207310
R67-69	3	Resistor 10K Ohms 1/4 Watt 5%	8207310
R70	1	Resistor 4.7K Ohms 1/4 Watt 5%	8207247
R71		Not used	
R72	1	Resistor 1K Ohms 1/4 Watt 5%	8207210
R73	1	Resistor 9.1K Ohms 1/4 Watt 5%	8207291
R74		Not used	
R75	1	Resistor 2.2K Ohms 1/4 Watt 5%	8207222
R75A	1	Resistor 470 Ohms 1/4 Watt 5%	8207147
R76	1	Resistor 4.7K Ohms 1/4 Watt 5%	8207247
R77-79		Not used	
R80-81	2	Resistor 100K Ohms 1/4 Watt 5%	8207410
R82	1	Resistor 4.7K Ohms 1/4 Watt 5%	8207247
R83-87		Not used	
R88	1	Resistor 10 Ohms 1/4 Watt 5%	8207010
RP1	1	Resistor Pak 10K Ohm 8-Pin SIP	8292310
RP2-3	2	Resistor Pak 1K Ohm 8-Pin SIP	8290210
RP4	1	Resistor Pak 10K Ohm 10-Pin SIP	8290010
RP5	1	Resistor Pak 33 Ohm 16-Pin SIP	8295044
RP6	1	Resistor Pak 33 Ohm 8-Pin SIP	8295033
RP7	1	Resistor Pak 4.7K Ohm 8-Pin SIP	8292246
RP8	1	Resistor Pak 2.2K Ohm 8-Pin SIP	8290039
C1	1	Capacitor .1 50V Mono Ax	8374104
C2-4		Not used	
C5	1	Capacitor .1 50V Mono Ax	8374104
C6	1	Capacitor .022 MFD 63V Film	8393224
C7-10		Not used	
C11-12	2	Capacitor .1 50V Mono Ax	8374104
C13	1	Capacitor 22 MFD 16V Elec Ax	8316221
C13	1	Capacitor 22 MFD 16V Elec Ax	8316221
C14-17	4	Capacitor .1 50V Mono Ax	8374104

Main Logic Parts List continued

Symbol	Qty.	Description	Part No.
C18-19	2	Capacitor 20 PFD 50V C. Disc	8300204
C20-21	2	Capacitor .1 50V Mono Ax	8374104
C22	1	Capacitor 20 PFD 50V C. Disc	8300204
C23		Not used	
C24	1	Capacitor 20 PFD 50V C. Disc	8300204
C25	1	Capacitor 180 PFD 50V C. Disc	8301184
C26	1	Capacitor 10 MFD 16V Elec Ax	8316101
C27	1	Capacitor 20 PFD 50V C. Disc	8300204
C28-39	11	Capacitor .1 50V Mono Ax	8374104
C40-43	4	Capacitor 68 PFD 50V C. Disc	8300684
C44-45	2	Capacitor .01 MFD 50V C. Disc	8303104
C46	1	Capacitor 20 PFD 50V C. Disc	8300204
C47-50	4	Capacitor .1 MFD 50V Mono Ax	8374104
C51	1	Capacitor 22 MFD 16V Elec Ax	8316221
C52-54	3	Capacitor .1 50V Mono Ax	8374104
C54A	1	Capacitor 470 PFD 50V C. Disc	8301474
C55-75	21	Capacitor .1 50V Mono Ax	8374104
C76	1	Capacitor .47 MFD 50V Mono Rad.	8384475
C77-81	5	Capacitor .1 50V Mono Ax	8374104
C82	1	Capacitor 22 MFD 16V Elec Ax	8316221
C83		Not used	
C84-85	2	Capacitor .1 50V Mono Ax	8374104
C85A	1	Capacitor 10 MFD 16V Elec Ax	8316101
C86-87	2	Capacitor .1 50V Mono Ax	8374104
C88	1	Capacitor .1 50V C. Disc	8304104
C89-91	3	Capacitor .1 50V Mono Ax	8374104
C92	1	Capacitor 20 PFD 50V C. Disc	8300204
C93	1	Capacitor .1 50V Mono Ax	8374104
C94	1	Capacitor 2200 PFD C. Disc	8302224
C95	1	Capacitor .1 50V Mono Ax	8374104
C96-97	2	Capacitor 20 PFD 50V C. Disc	8300204
C98	1	Capacitor .1 50V Mono Ax	8374104
C99	1	Capacitor 20 PFD 50V C. Disc	8300204
C100	2	Capacitor 2200 PFD C. Disc	8302224
C101	1	Capacitor 2.2 MFD 16V Elec Ax	8315221
C102	1	Capacitor .1 50V Mono Ax	8374104
C103	1	Capacitor 2.2 MFD 16V Elec Ax	8315221
C104	1	Capacitor 22 MFD 16V Elec Ax	8316221
C105		Not used	
C106	1	Capacitor .1 50 V Mono Ax	8374104
C107	1	Capacitor 10 MFD 16V Elec Ax	8316101
C108	1	Capacitor 10 MFD 16V Tant. Rad.	8336101
C109	1	Capacitor .1 50V C. Disc	8304104
C110-115	6	Capacitor 2200 PFD C. Disc	8302224
C116-117	2	Capacitor .1 50V Mono Ax	8374104
C118-121	4	Capacitor 470 PFD 50V C. Disc	8301470
C122-123	2	Capacitor .1 50V Mono Ax	8374104

Main Logic Parts List continued

Symbol	Qty.	Description	Part No.
C124	1	Capacitor 100 MFD 16V Tant. Rad.	8337100
C125	1	Capacitor 330 PFD 50V C. Disc	8301332
C126	1	Capacitor .1 50V C. Disc	8304104
C127		Not used	
C128	1	Capacitor .1 50V Mono Ax	8374104
C129-131		Not used	
C132	1	Capacitor .1 50V Mono Ax	8374104
U1	1	IC 74LS04 Hex Inverter	8020004
U2-5		Not used	
U6	1	IC 74S04 Hex Inverter	8015004
U7-8		Not used	
U9-10	2	IC 128K ROM	8040128
U9-10	2	Socket 28-Pin DIP	8509007
U11-12	2	IC 64K DRAM 150 ns	8041665
U11-12	2	Socket 16-Pin DIP	8509003
U13	1	IC 74LS244 Octal Buffer	8020244
U14	1	IC 74LS245 Transceiver	8020245
U14	1	Socket 20-Pin DIP	8509009
U15-16	2	IC 74F109 Flip Flop	8015109
U17	1	IC 74LS32 Quad 2-In OR	8020032
U18	1	IC 74LS244 Octal Buffer	8020244
U19	1	IC LM339 Quad Comparator	8050339
U20-21		Not used	
U22	1	IC 74LS08 Quad 2-In AND	8020008
U23	1	IC 74F109 Flip Flop	8015109
U24	1	IC 7407 Hex Buffer	8000007
U25-28	4	IC 64K DRAM 150 ns	8041665
U25-28	4	Socket 16-Pin DIP	8509003
U29	1	IC 74F04 Hex Inverter	8015004
U30	1	IC 74LS112 Flip Flop	8020112
U31	1	IC 74LS161A Counter	8020161
U32		Not used	
U33-34	2	IC 64K DRAM 150 ns	8041665
U33-34	2	Socket 16-Pin DIP	8509003
U35	1	IC 74LS374 Flip Flop	8020374
U36	1	IC 74LS373 Octal Latch	8020373
U37	1	IC 74F109 Flip Flop	8015109
U38	1	IC 74F138 Multiplexer	8015138
U39	1	IC 74F161 Counter	8015161
U40	1	IC 74LS04 Hex Inverter	8020004
U41	1	IC 74LS373 Octal Latch	8020373
U42-43	2	IC 74LS244 Octal Buffer	8020244
U44	1	IC 74F04 Hex Inverter	8015004
U45	1	IC 8284A Clock Generator	8040284
U45	1	Socket 18-Pin DIP	8509022
U46	1	IC 82S153 Programmable RFI	8075153

Main Logic Parts List continued

Symbol	Qty.	Description	Part No.
U46	1	Socket 20-Pin DIP	8509009
U47	1	IC 74F109 Flip Flop	8015109
U48-49	2	IC 64K DRAM 150 ns	8041665
U48-49	2	Socket 16-Pin DIP	8509003
U50	1	IC 74LS195A Shift Register	8020195
U51	1	IC 74LS32 Quad 2-In OR	8020032
U52	1	IC 8272 FDC	8040272
U52	1	Socket 40-Pin DIP	8509002
U53	1	IC 825153 Programmable RFI	8075153
U53	1	Socket 20-Pin DIP	8509009
U54-55	2	IC 64K DRAM 150 ns	8041665
U54-55	2	Socket 16-Pin DIP	8509003
U56	1	IC 74LS374 Flip Flop	8020374
U57	1	IC 74LS373 Octal Latch	8020373
U58	1	IC 74F04 Hex Inverter	8015004
U59-60	2	IC 74LS244 Octal Buffer	8020244
U61	1	IC 74LS373 Octal Latch	8020373
U62	1	IC 74LS245 Transceiver	8020245
U62	1	Socket 20-Pin DIP	8509009
U63	1	IC 8259A Interrupt Controller	8040259
U63	1	Socket 28-Pin DIP	8509007
U64	1	IC 8088 CPU	8048088
U64	1	Socket 40-Pin DIP	8509002
U65-68	4	IC 64K DRAM 150 ns	8041665
U65-68	4	Socket 16-Pin DIP	8509003
U69	1	IC FDC9216 Data Separator	8040216
U69	1	Socket 8-Pin DIP	8509011
U70	1	IC 74LS08 Quad 2-In NAND	8020008
U71	1	IC 74LS273 Octal Flip Flop	8020273
U72-75	4	IC 74ALS253 Multiplexer	8025253
U76	1	Custom Video Array	8079000
U76	1	Socket 40-Pin DIP	8509002
U77	1	IC 74LS86 Quad 2-In OR	8020086
U78	1	IC 74LS08 Quad 2-In AND	8020008
U79	1	IC 74LS138 Quad 1-In NAND	8020138
U80	1	IC 82S153 Programmable RFI	8075153
U80	1	Socket 20-Pin DIP	8509009
U81	1	IC 74S260 Dual 5-In NOR	8010260
U82	1	IC 74LS244 Octal Buffer	8020244
U83	1	IC 74LS38 Quad 2-In NAND	8020038
U84	1	IC 7416 Hex Inverter	8000016
U85	1	IC 74LS14 Hex Inverter	8020014
U86	1	IC 74LS02 2-In NOR	8020002
U87	1	IC 74LS32 Quad 2-In NOR	8020032
U88	1	IC MCM6845 CRT Controller	8040845
U88	1	Socket 40-Pin DIP	8509002
U89	1	IC 74LS157 Multiplexer	8020157

Main Logic Parts List continued

Symbol	Qty.	Description	Part No.
U90	1	IC 74LS153 Multiplexer	8020153
U91	1	IC 74LS164 Shift Register	8020164
U92	1	IC 74LS00 Quad 2-In NAND	8020000
U93	1	IC 74LS32 Quad 2-In OR	8020032
U94	1	IC 74LS74 Flip Flop	8020074
U95		Not used	
U96	1	IC SN76496 Tone Generator	8040496
U96	1	Socket 16-Pin DIP	8509003
U97	1	IC 74LS245 Transceiver	8020245
U97	1	Socket 20-Pin DIP	8509009
U98	1	IC 74LS32 Quad 2-In OR	8020032
U99	1	IC 74LS273 Octal Flip Flop	8020273
U100	1	IC 74LS174 Flip Flop	8020174
U101	1	IC 8255A-5 Program Interface	8040255
U101	1	Socket 40-Pin DIP	8509002
U102	1	IC 74LS05 Hex Inverter	8020005
U103	1	IC 82S153 Programmable RFI	8075153
U103	1	Socket 20-Pin DIP	8509009
U104	1	IC 74LS74 Flip Flop	8020074
U105	1	IC 14529 Dual 4-Channel Analog	8030529
U106	1	IC 74LS174 Flip Flop	8020174
U107	1	IC 74LS04 Hex Inverter	8020004
U108	1	Custom Gate Array	8041087
U108	1	Socket 40-Pin DIP	8509002
U109	1	IC 74LS04 Hex Inverter	8020004
U110	1	IC 74LS125A Quad Buffer	8020125
U111	1	IC 74LS04 Hex Inverter	8020004
U112	1	IC 74LS32 Quad 2-In OR	8020032
U113	1	IC 74LS244 Octal Buffer	8020244
U114	1	IC 8253-5 Timer	8040253
U114	1	Socket 24-Pin DIP	8509001
U115	1	IC 74LS112 Flip Flop	8020112
U116	1	IC 74LS74 Flip Flop	8020074
U117	1	IC 74LS08 Quad 2-In AND	8020008
U118	1	IC LM386 Audio Amp	8050386
U119	1	IC LM358 Op Amp	8050358

Main Logic Parts List continued

Symbol	Qty.	Description	Part No.
	1	Chassis-Main	8729314
	1	Support-Disk Drives	8729313
	1	Panel-Option Board	8729312
	1	Case Top	8719438
	1	Button Reset, Front	8719440
	1	Button Reset, Rear	8719441
	1	Cable Signal Floppy Disk	8709447
	1	Box, Diskette	8709447
	1	Cable AC In	8709447
	1	Cable Switch (AC Power To Switch - Line)	8709555
		Cable Switch (AC Power To Switch - Neutral)	8709554
	1	Fan	8790412
	1	Speaker	8490009
	1	Cable, Speaker	8490009

***Note:** R1 is used with ROM in Socket U9.
R2 is used with PROMs in Socket U9, 10.

Parts List:**54 Watt Power Supply****8790070**

Symbol	Description	Qty.	Part No.
—	54W Power Supply PCB	1	8790070
C1-2	Capacitor Film 0.1uF 250VAC + -20%	2	CC104MRGP
C3	Capacitor Ceramic 10000pF 400VAC +10/-0%	1	CC103PTCP
C4	Capacitor Electrolytic 47uF 200WV + -20%	1	CC476MPAP
C5	Capacitor Film 0.22uF 50WV + -10%	1	CC224KJYP
C6	Capacitor Ceramic 2200pF 400VAC + -20%	1	CC222MTCP
C7	Capacitor Ceramic 10000pf 1KV +80-20%	1	CC103ZXCP
C8	Capacitor Ceramic 1500pF 2KV + -10%	1	CC152KZCP
C9	Capacitor Film 0.047uF 50V + -10%	1	CC473KJYP
C10	Capacitor Film 0.01uF 50V + -10%	1	CC103KJYP
C11-12	Capacitor Electrolytic 10000uF 35WV 35WV + -20%	2	CC108MGAP
C13	Capacitor Electrolytic 1000uF 16WV + -20%	1	CC108MDAP
C14	Capacitor Electrolytic 470uF 35WV + -20%	1	CC477MGAP
C15	Capacitor Electrolytic 470uF 25WV + -20%	1	CC477MEAP
C16-18	Capacitor Electrolytic 4700uF 10WV + -20%	3	CC478MCAP
C19	Capacitor Electrolytic 2200uF 10WV or 16WV + -20%	1	CC228MDAP
C20	Capacitor Electrolytic 10WV 50WV + -20%	1	CC106MJAP
C21	Capacitor Ceramic 10000pf 1KV +80-20%	1	CC103ZXCP
SK1-2	Connector, 2 conductors Input/Fan	2	AJ-5951
SK3-1	Connector, 10 conductors Output	1	AJ-5952
SK3-2	Connector, 4 Conductors Output	1	AJ-5953
D1	Diode, Bridge 400V 4A	1	DX-2624
D2-3	Diode 200V 0.8A	2	DX-2701
D4-5	Diode 600V 1.0A	2	DX-1937
D6	Diode 500mW 200mA	1	DX-2702
D7	Diode 200V 5A	1	ADX-1375
D8	Diode 200V 0.8A	1	DX-2701
D9	Diode 40V 10A	1	DX-2703
D10	Diode 500mW 200mA	1	DX-2702
F1	Fuse, 125V 3.15A	1	AHF-1311
	Fuse Clip	2	AF-1268
HS1	Heatsink	1	0-D9-80466C
HS2	Heatsink	1	0-D9-80467B

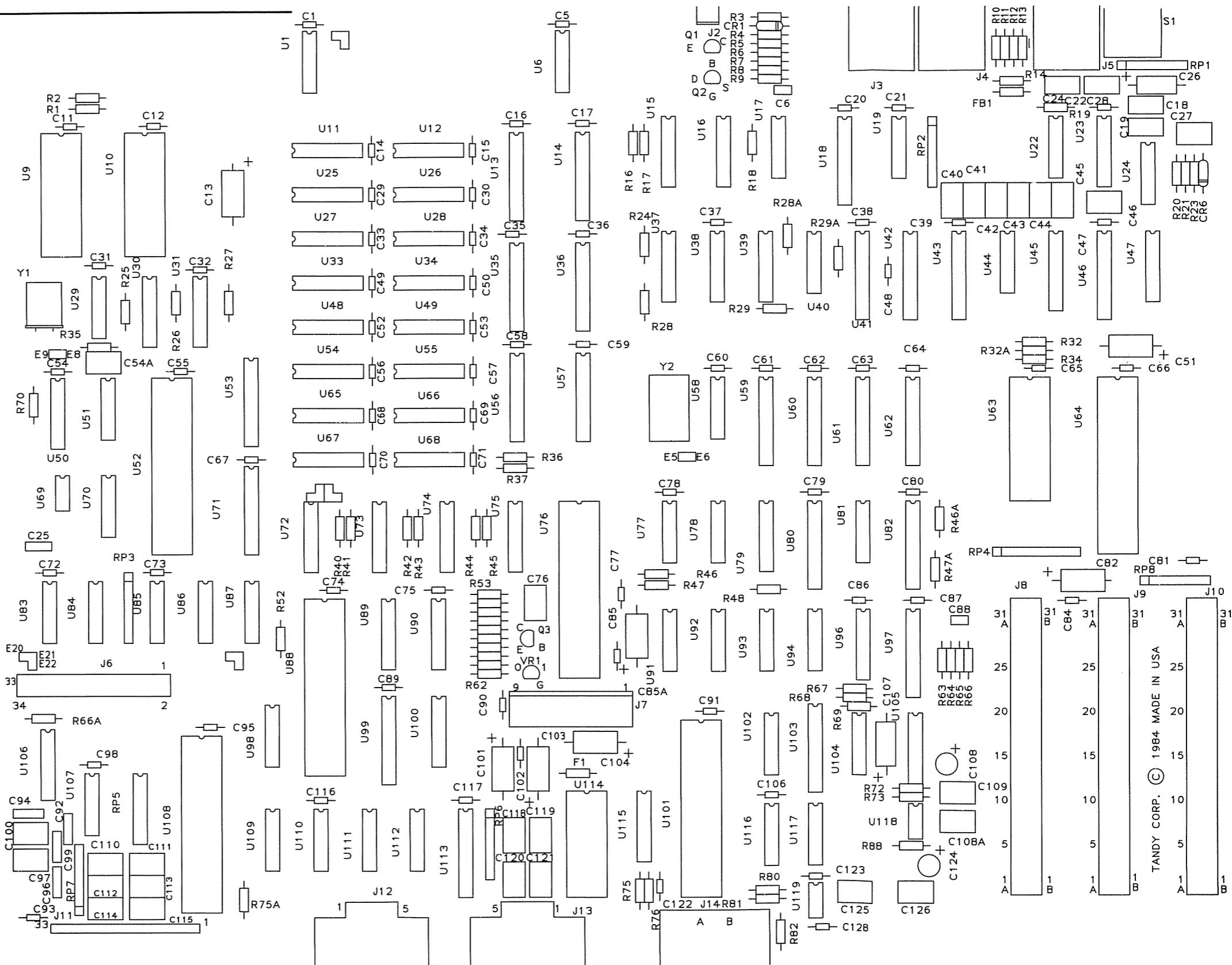
54 Watt Power Supply Parts List continued
879007

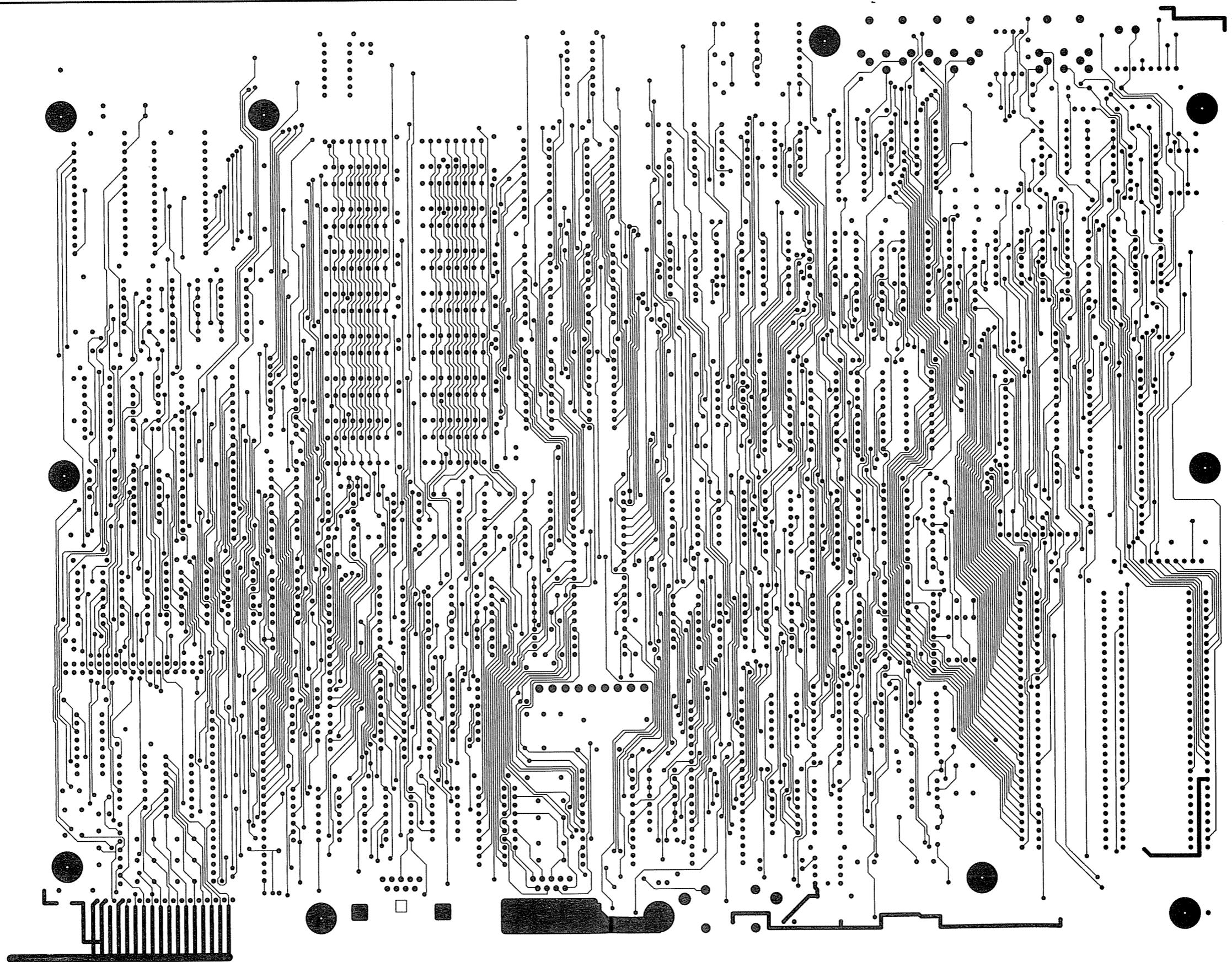
Symbol	Description	Qty.	Part No.
L1	Inductor 8mH	1	ACA-5522
L2	Inductor 4.3uH	1	ACA-5523
IC1	IC Circuit 30V 2A, Regulator	1	MX-6815
IC2	IC Circuit 35V 0.5A, Regulator	1	MX-4706
IC3	IC Circuit 37V 150mA, Regulator	1	MX-6816
PHC1	Photo Coupler 35V 50mA	1	ACS-0110
PHC2	Photo Coupler 400V 150mA	1	ASC-0111
R1	Resistor Wirewound 2 ohms 5W + - 10%	1	N0031FKH
R2	Resistor Carbon 100K ohms 1/2W + - 5%	1	N0371EFC
R3	Resistor Metal-oxide 27 2W + - 5% to 68 ohms	1	N0082EHD
R4-5	Resistor Metal-oxide 27K ohms 2W + - 5%	2	N0316EHD
R6-7	Resistor Metal-oxide 100 ohms 2W + - 5%	2	N0132EHD
R8	Resistor Metal-oxide 0.33 5W ohms + - 10%	1	N0522FKF
R9	Resistor Carbon 470 1/4W ohms + - 5%	1	N0169EEC
R10	Resistor Carbon 27K 1/4W ohms + - 5%	1	N0082EEC
R11	Resistor Carbon 100K ohms 1/2W + - 5%	1	N0371EFC
R12	Resistor Carbon 390 1/4W ohms + - 5%	1	N0162EEC
R13	Resistor Carbon 2.2K 1/4W ohms + - 5%	1	N0216EEC
R14	Resistor Carbon 1K 1/4W ohms + - 5%	1	N0196EEC
R15	Resistor Carbon 220 1/4W ohms + - 5%	1	N0149EEC
R16	Resistor Carbon 39 1/4W ohms + - 5%	1	N0092EEC
R17	Resistor Carbon 180 1/4W ohms + - 5%	1	N0144EEC
R18	Resistor Carbon 100 1/4W ohms + - 5%	1	N0132EEC
R19	Resistor Carbon 2.2K 1/4W ohms + - 5%	1	N0216EEC
R20	Resistor Carbon 2.2K 1/4 ohms + - 5%	1	N0216EEC
VR1	Variable Resistor 2K 0.5W ohms + - 20%	1	AP7444
T1	Transformer	1	ATA-1078
Q1	Transistor, NPN	1	2SC-2938
Q2	Transistor, NPN	1	2SD-1207

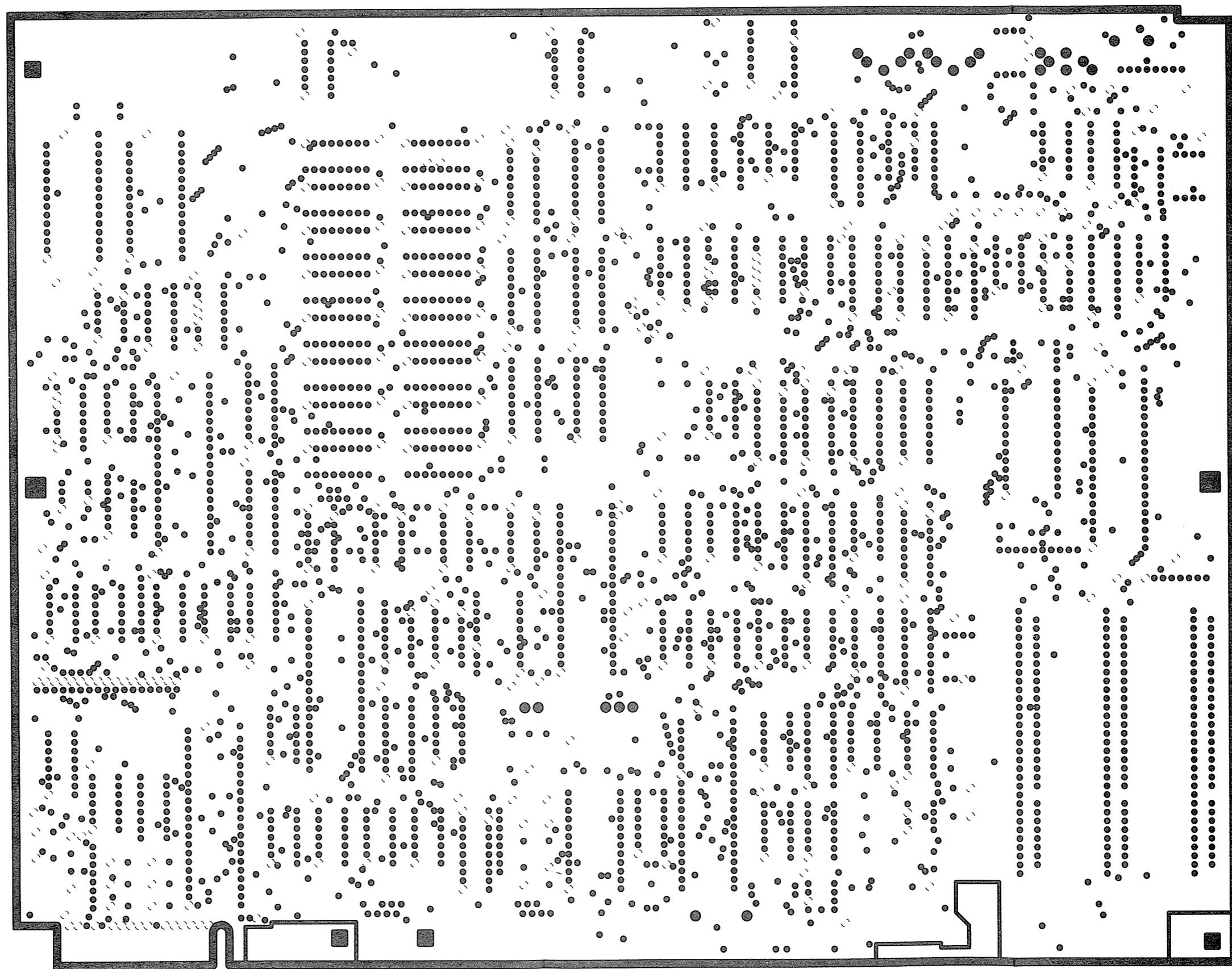
Parts List
Tandy 1000 Keyboard

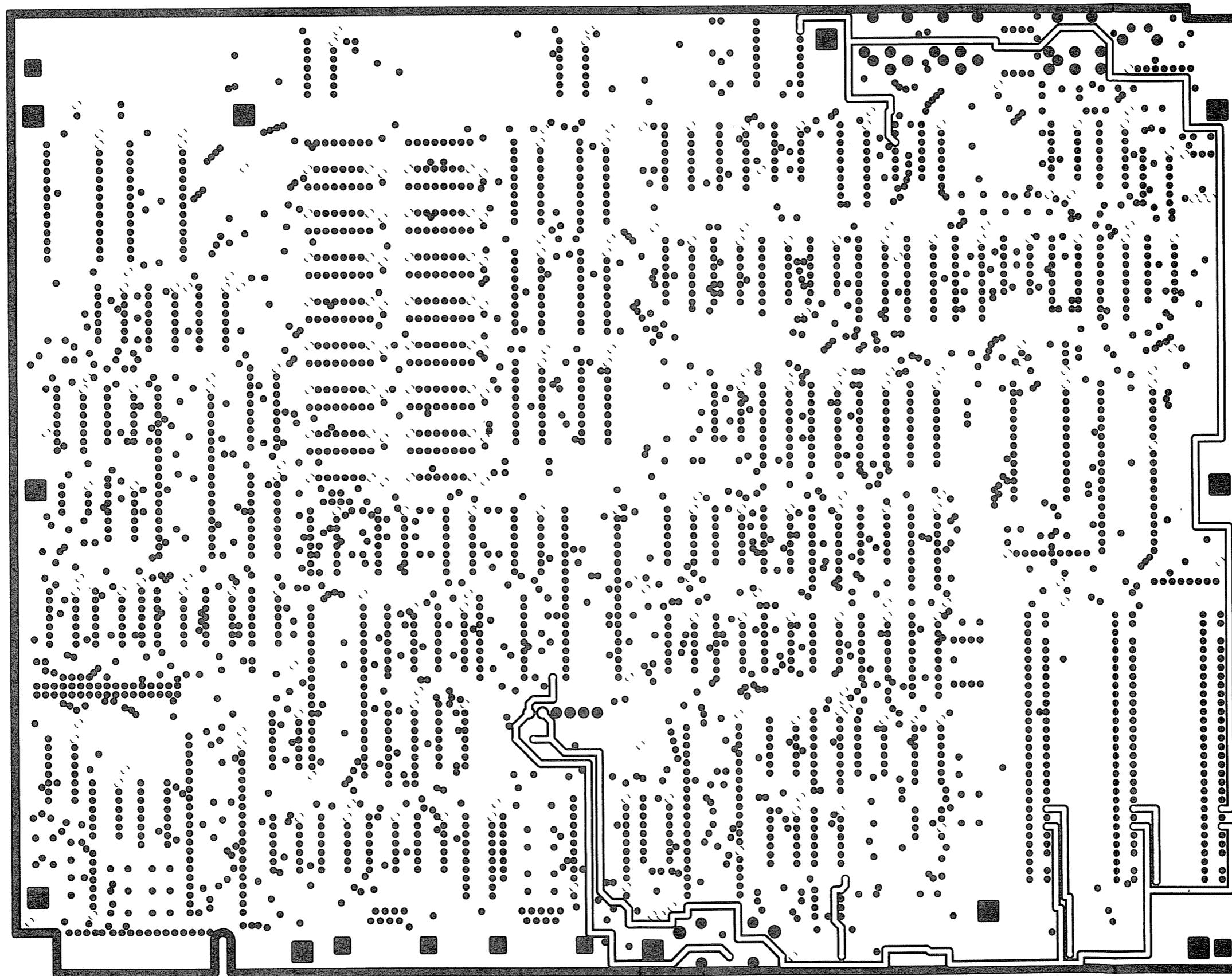
Item	Sym	Description	Part No.
1	1	Case, Keyboard Bottom	8719335
2	1	Case, Keyboard Top	8719334
3	1	Keyboard PCB Assembly	8080033
4	2	Support, Keyboard	8719336
5	4	Spring, Keyboard Support	8739014
6	1	Cable Assembly, Keyboard	8709567
8	1	Logo, Plastic	8719471
9	2	Pad, Keyboard Friction	8591004
10	3	ID Card, Function Key	87891012
12	1	Center Guide, ID Card	8719371
13	1	Right Guide, ID Card	8719372
14	4	Screw, #6 x 1/2" PPH PTF Zn	8569079
15	5	Screw, #6 x 7/16" PPH PTF Zn	8569229

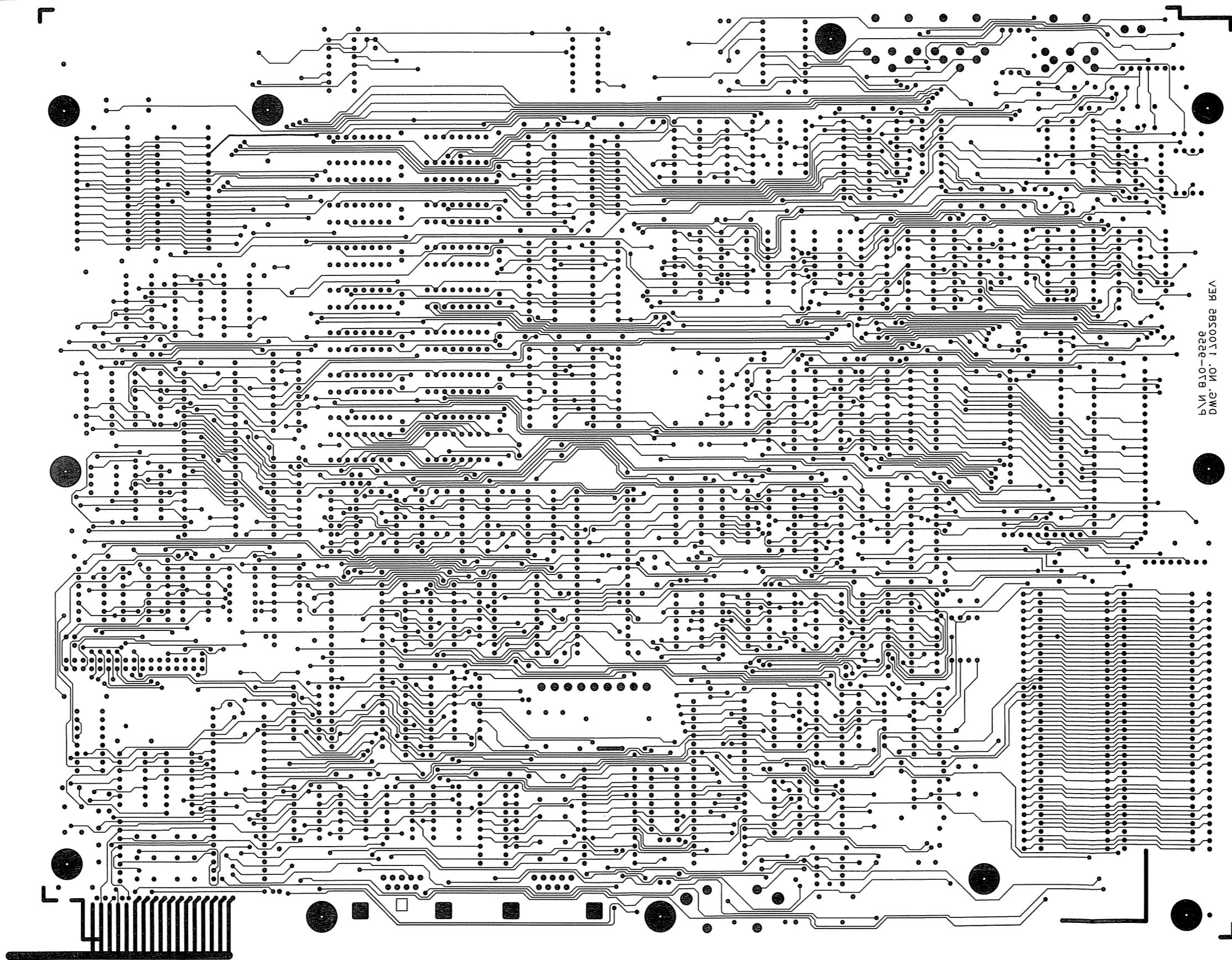
14.000 +/- .002 REF

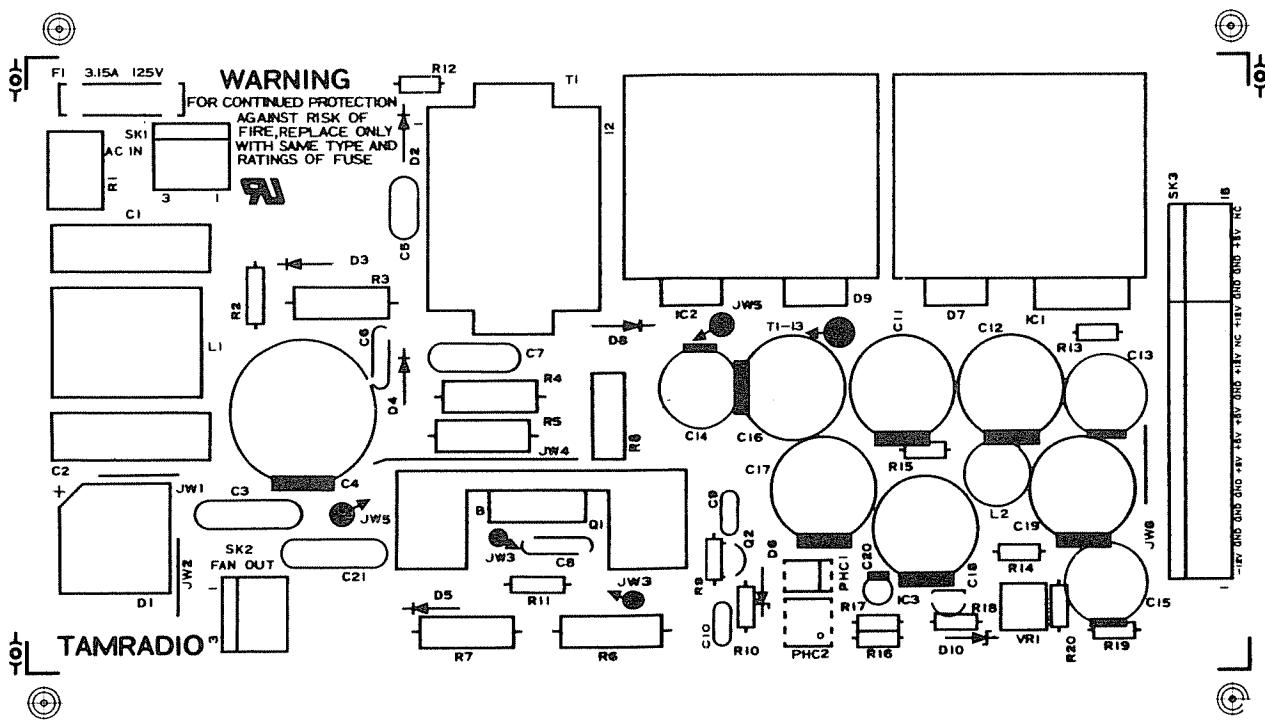
10 / COMPONENT LAYOUTS**Main Logic**



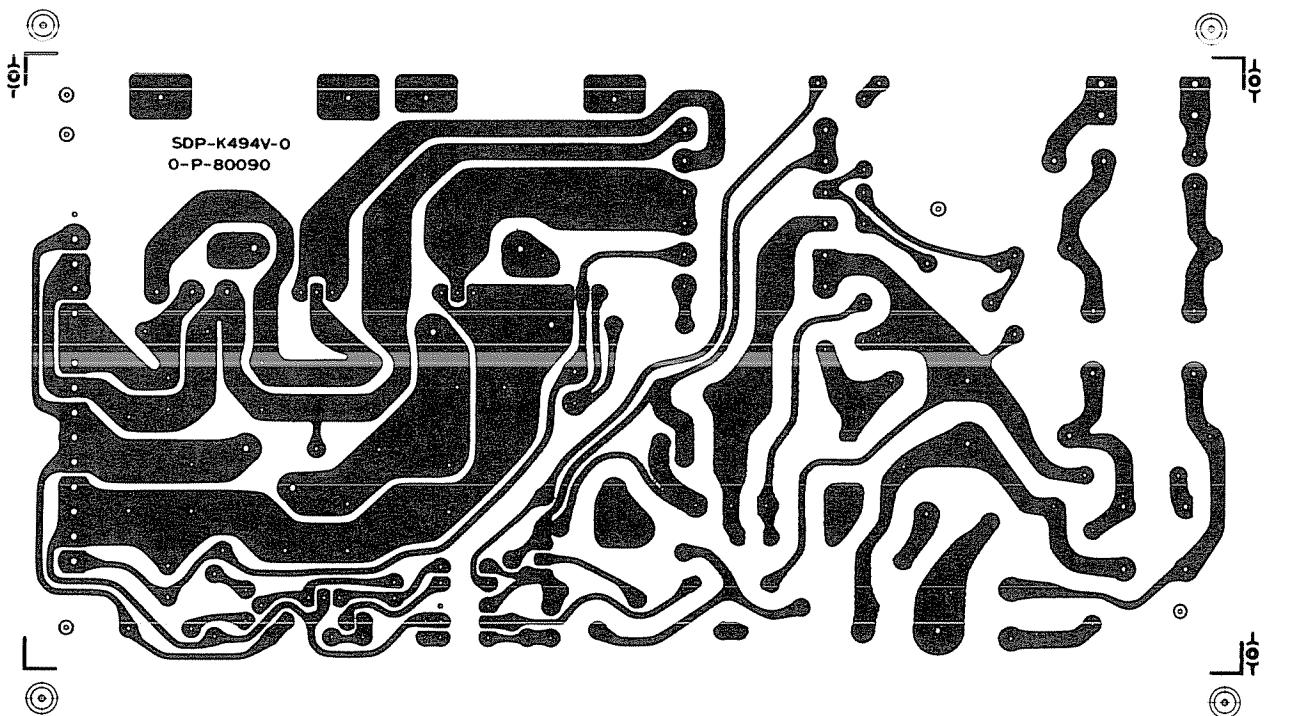






54 Watt Power Supply Component Layout

Silkscreen

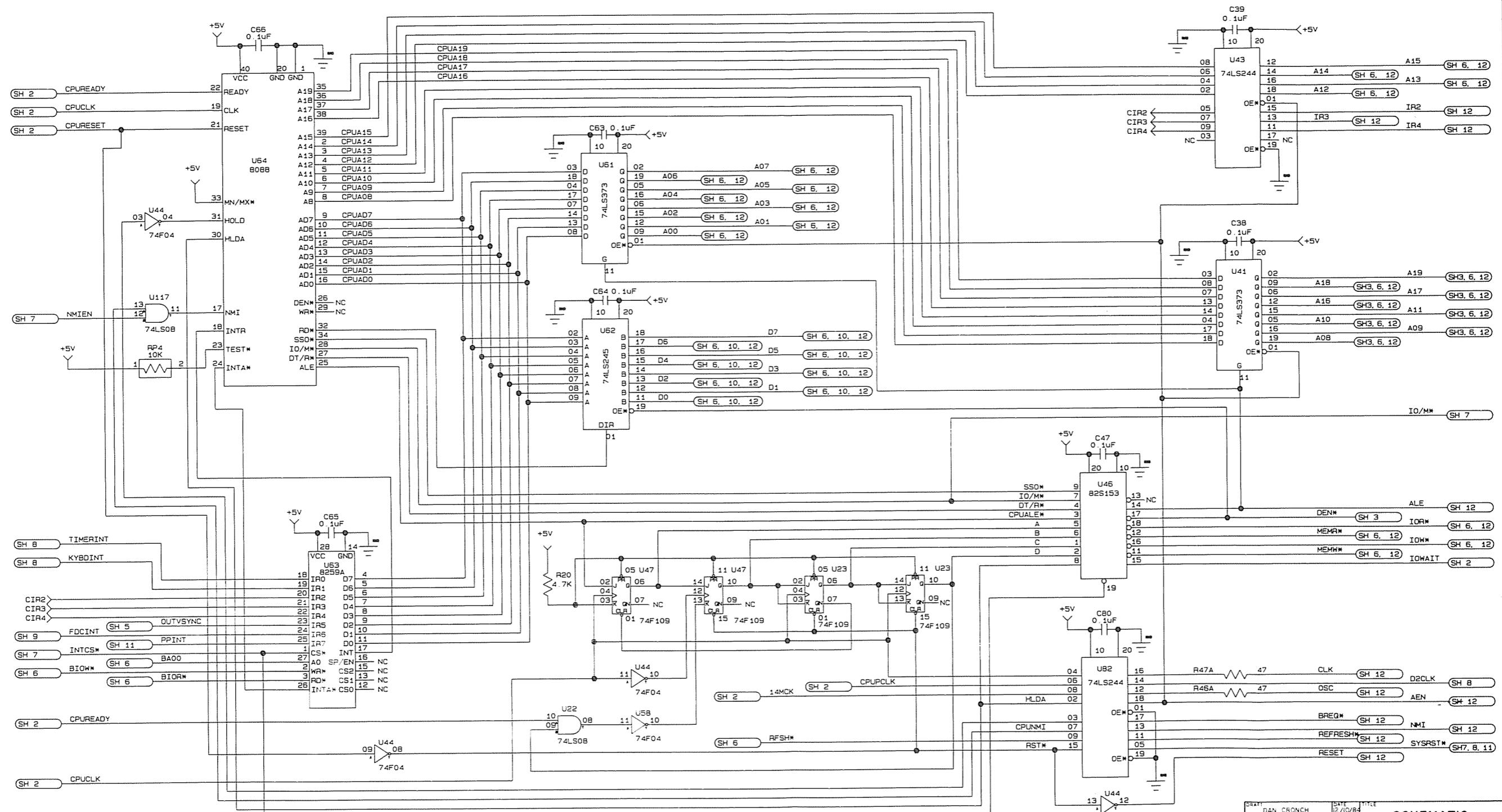


Solder Mask

11 / SCHEMATICS

Main Logic

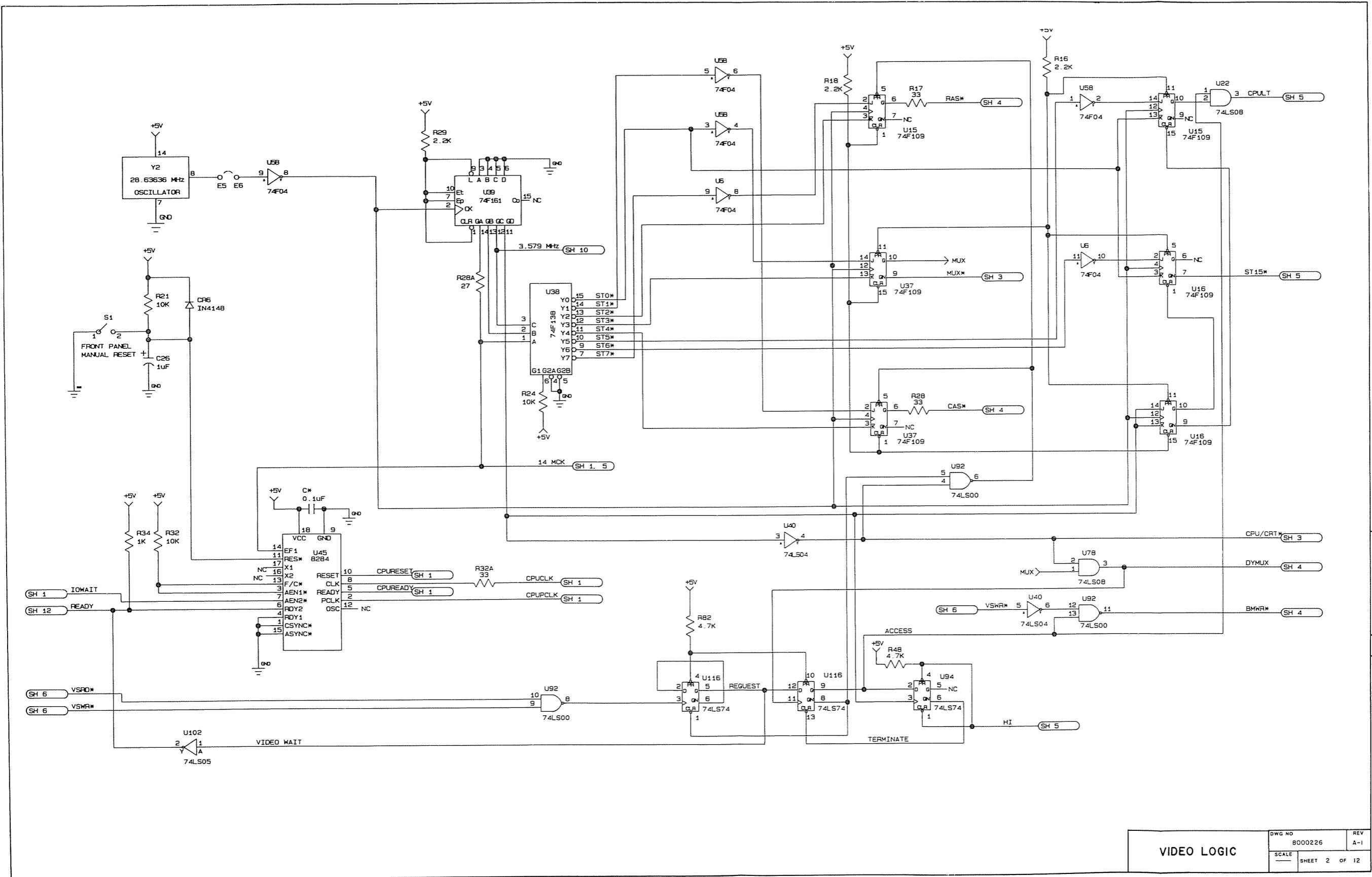
		REVISION		DATE	APPROVED
ZONE	LTR	DESCRIPTION			
	A	RELEASED FOR PRODUCTION	✓	11/9/84	
	A-1	PER TCO 11757	✓	12/10/84	✓
	A-2	PER TCO 12319, 12323 MANUALLY CHGD	✓	3/29/85	✓



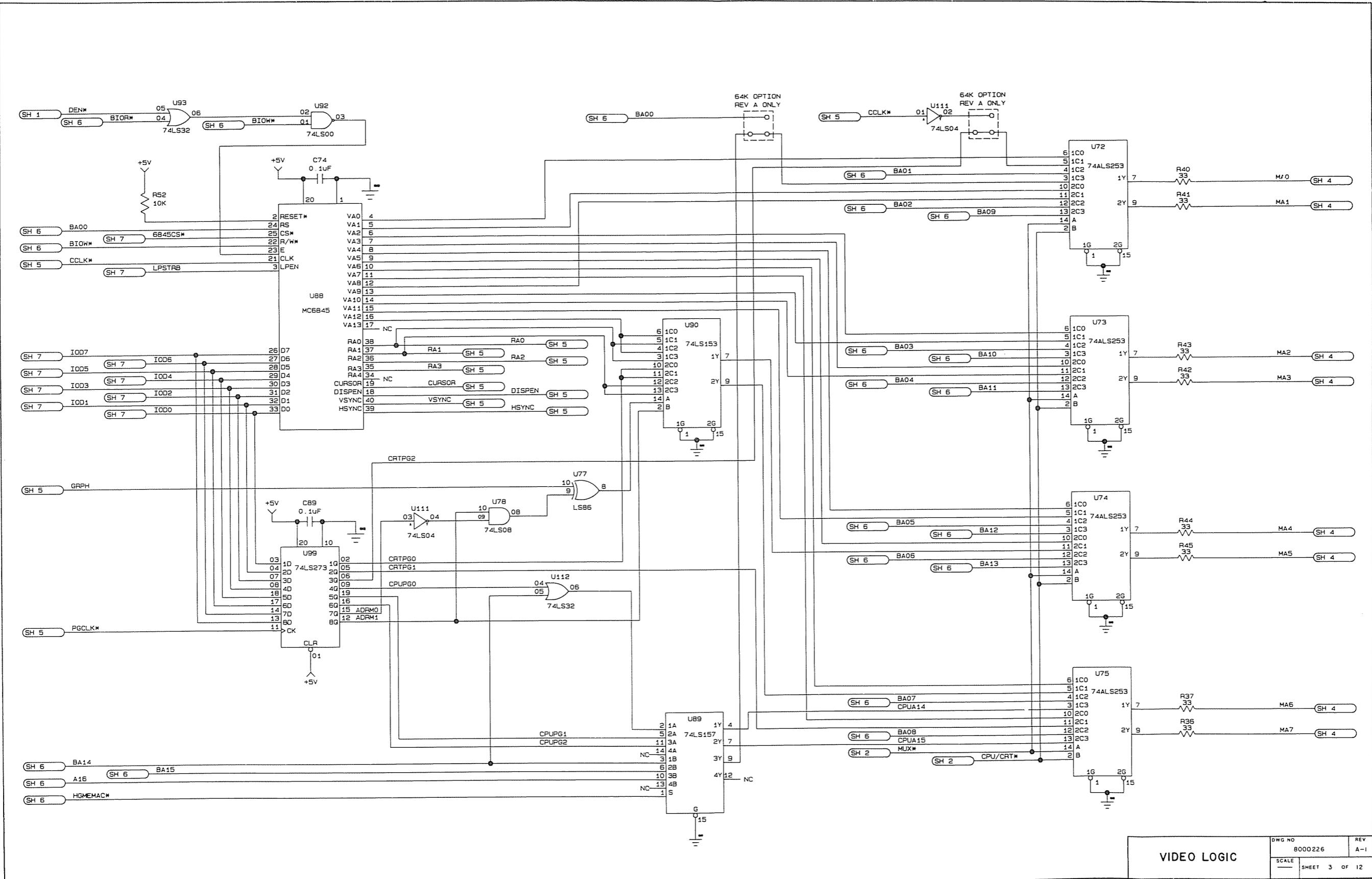
NOTE: THIS DWG IS
CAD GENERATED -
DO NOT REVISE MANUALLY

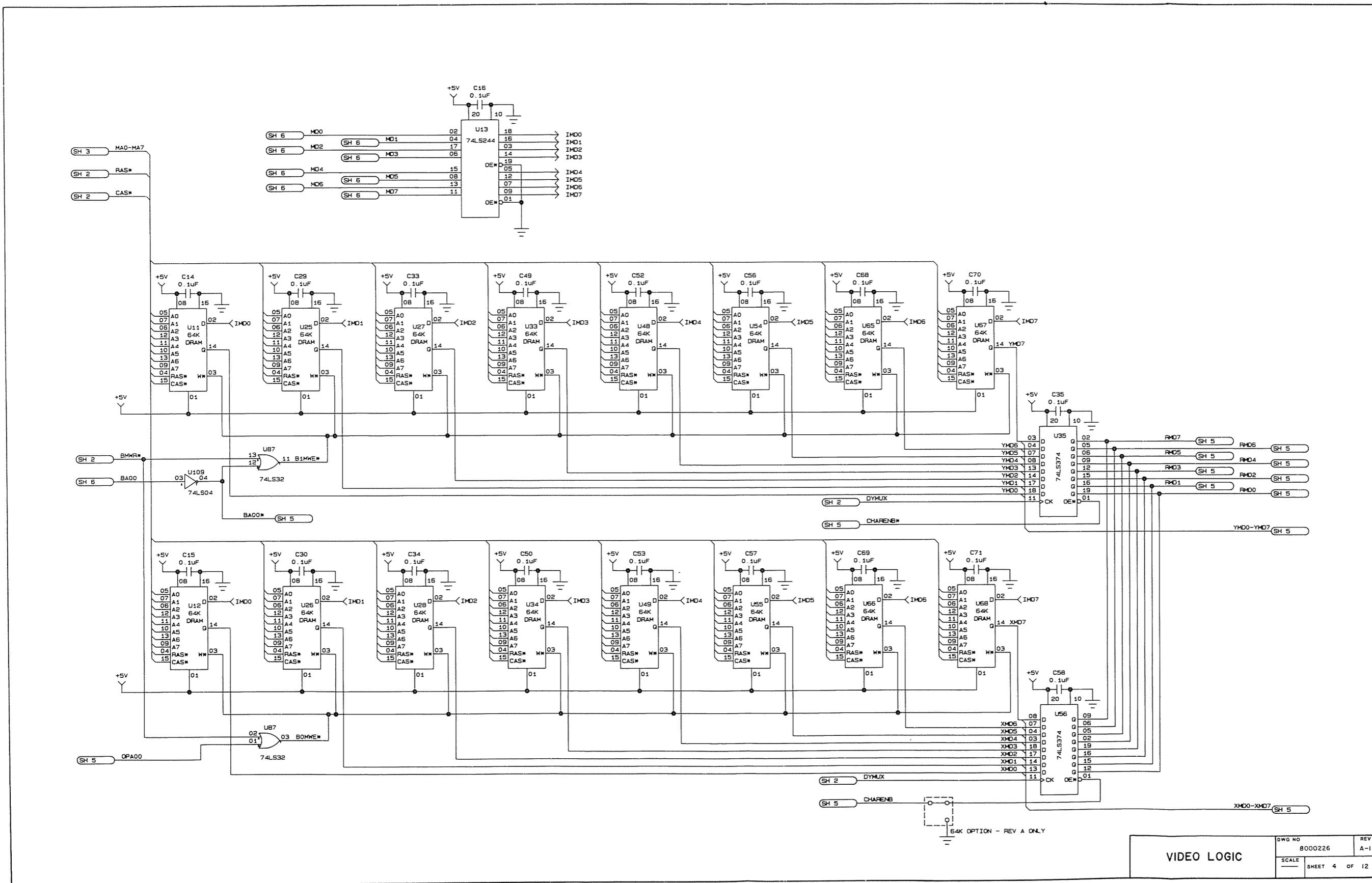
**SCHEMATIC—
MAIN LOGIC BOARD,
TANDY 1000
(CPU LOGIC)**

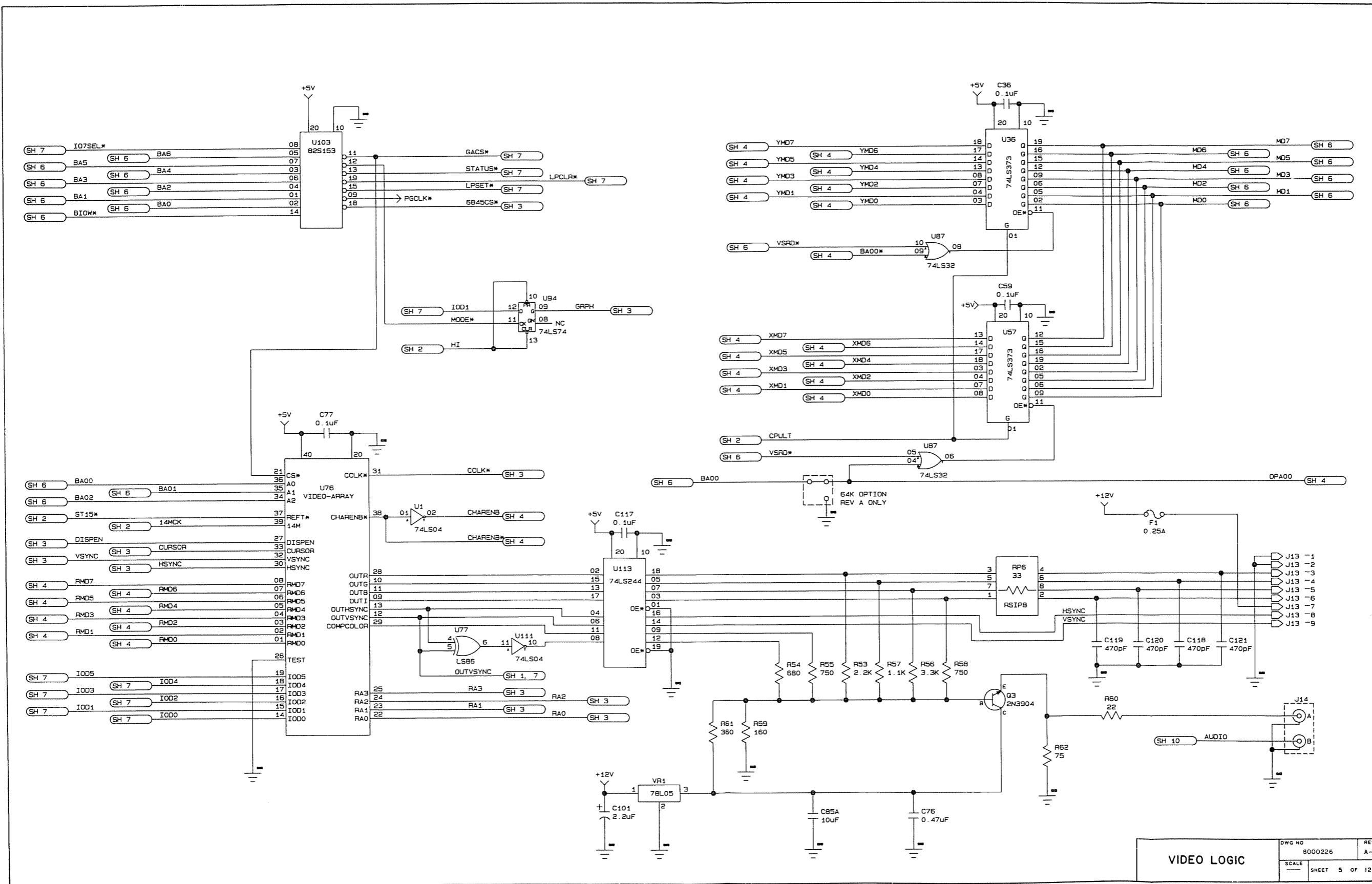
NO 8000226 SIZE D
SHEET 1 OF 12

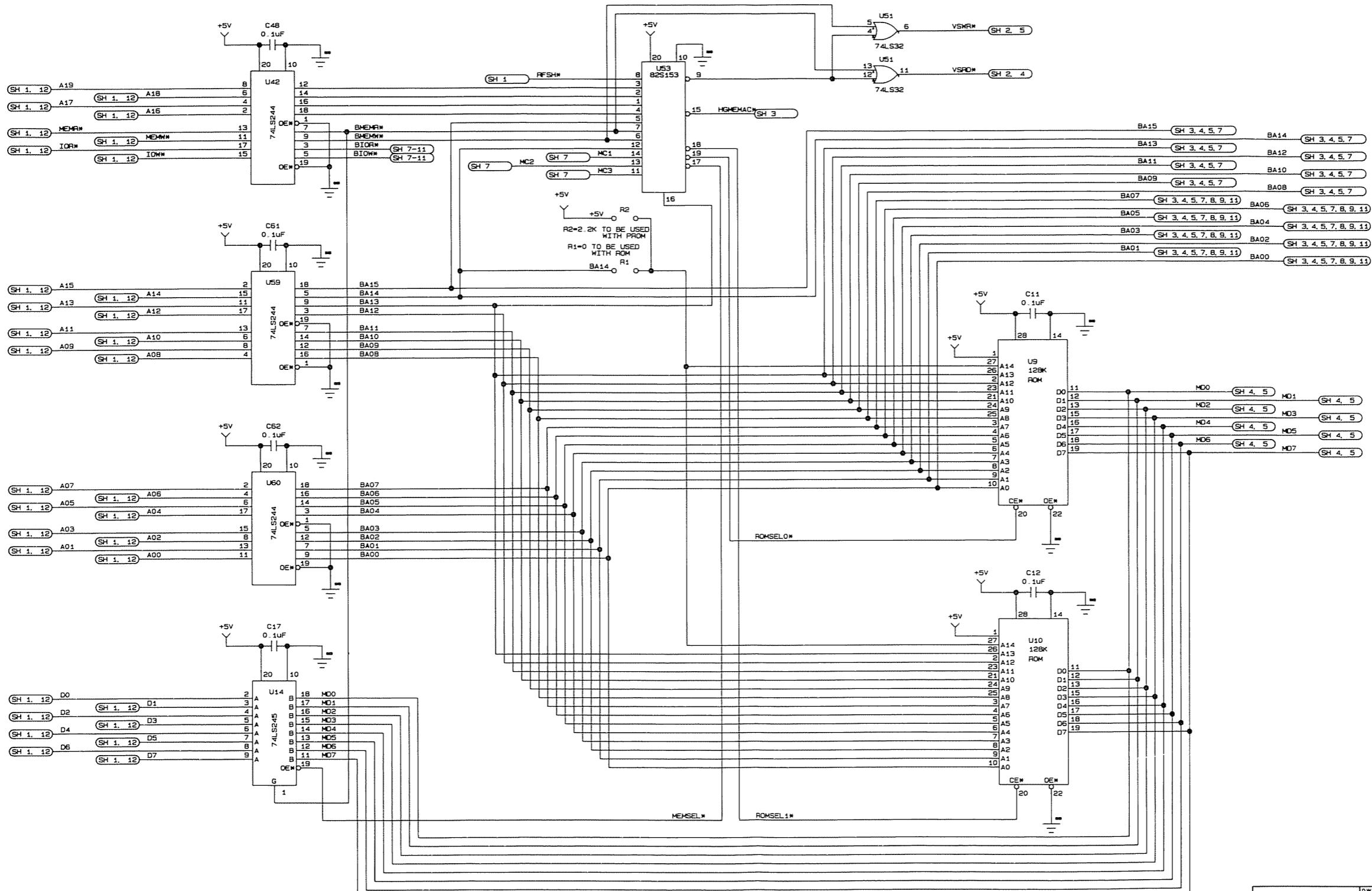


VIDEO LOGIC	DWG NO B000226	REV A-1
	SCALE	SHEET 2 OF 12



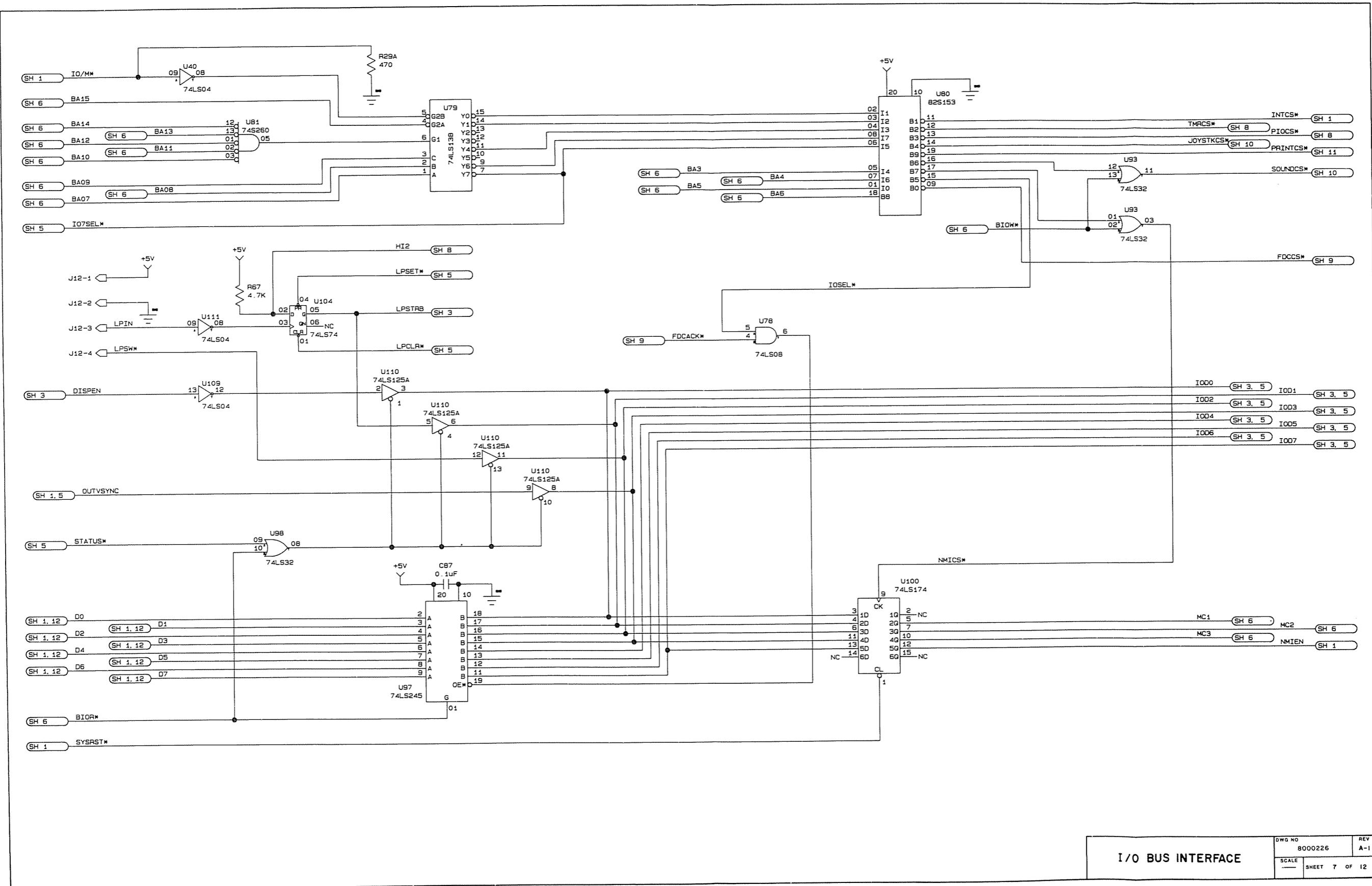






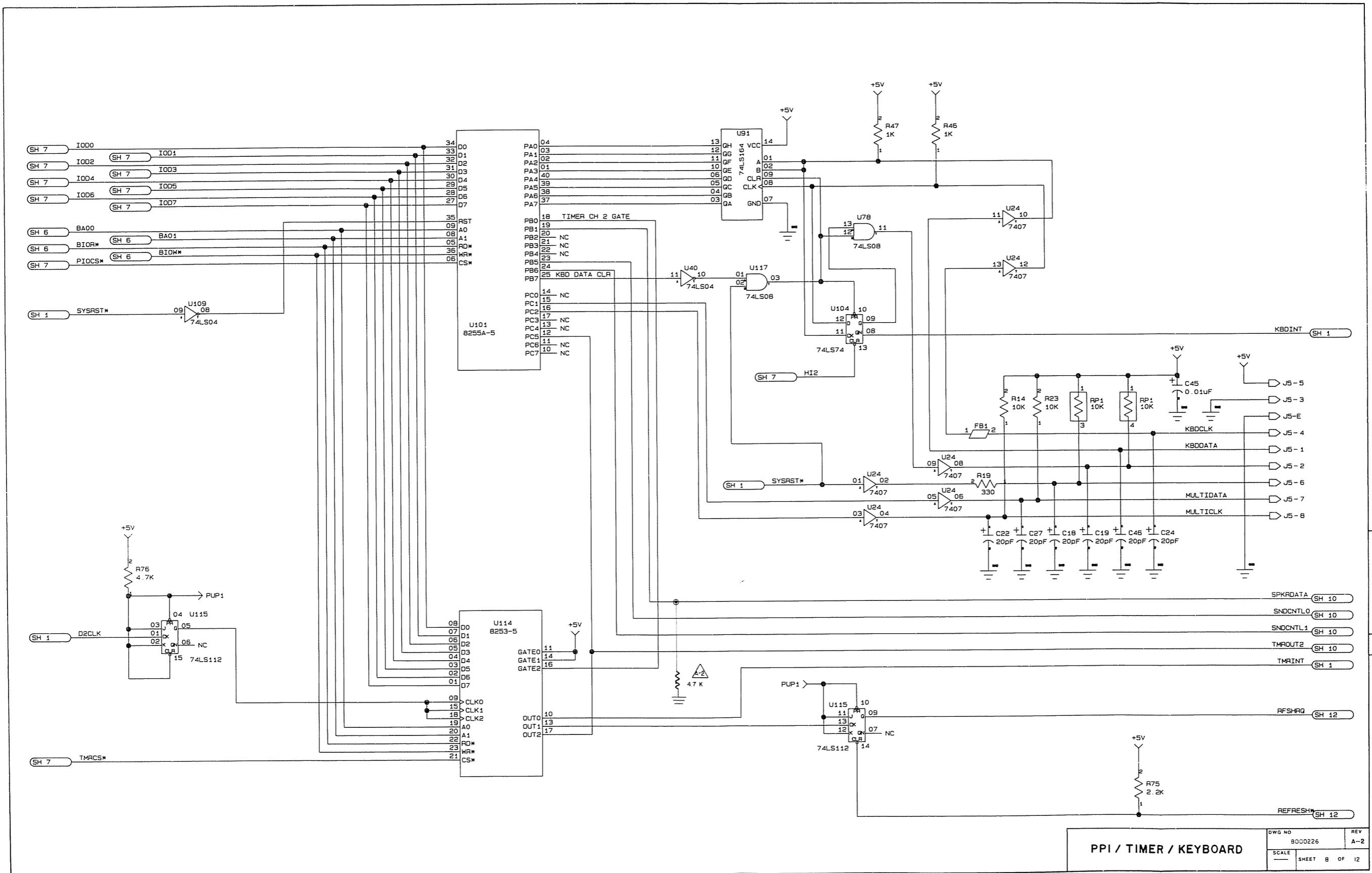
ROM

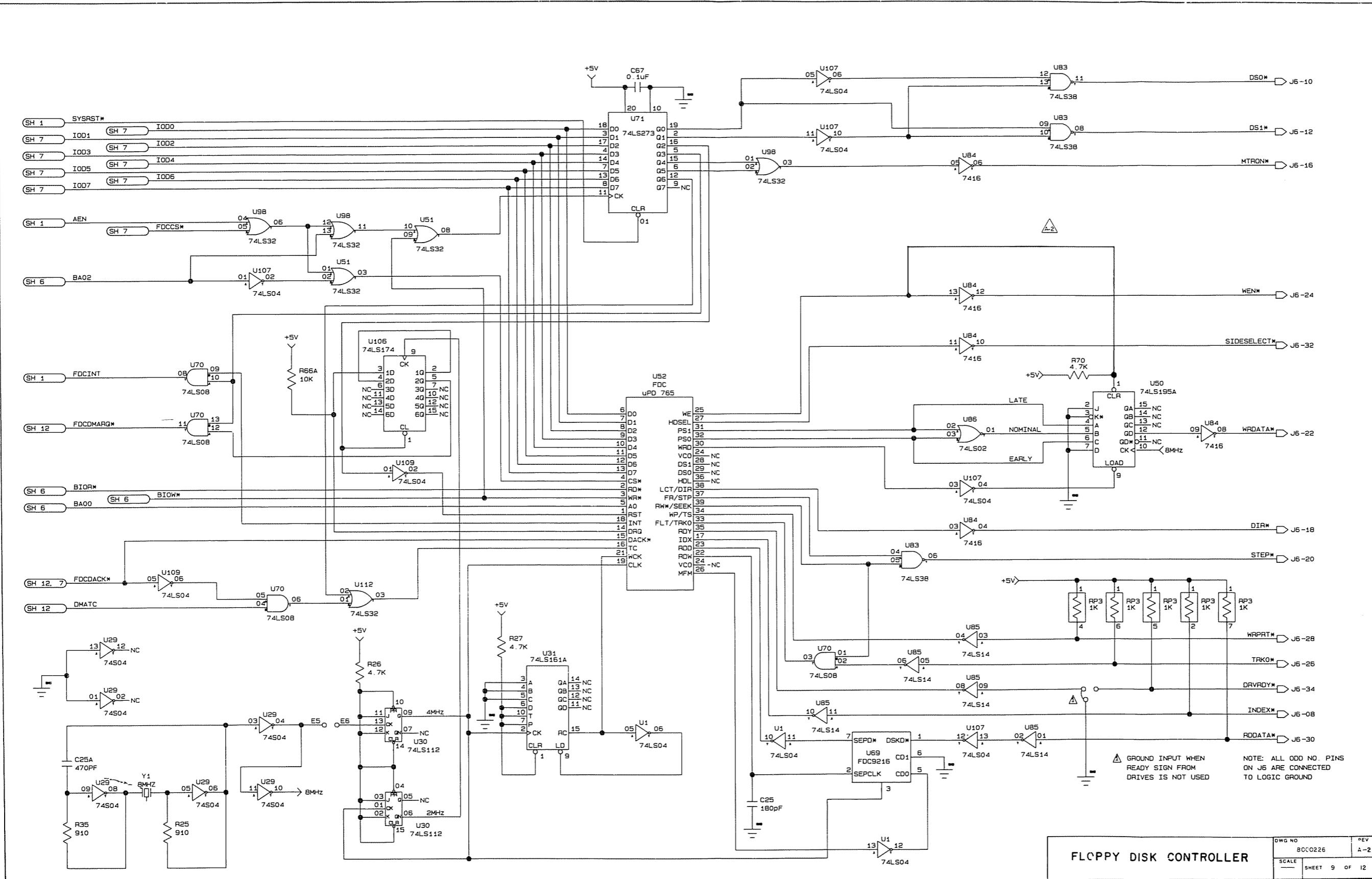
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8000226	A-1
SCALE	SHEET 6 OF 12

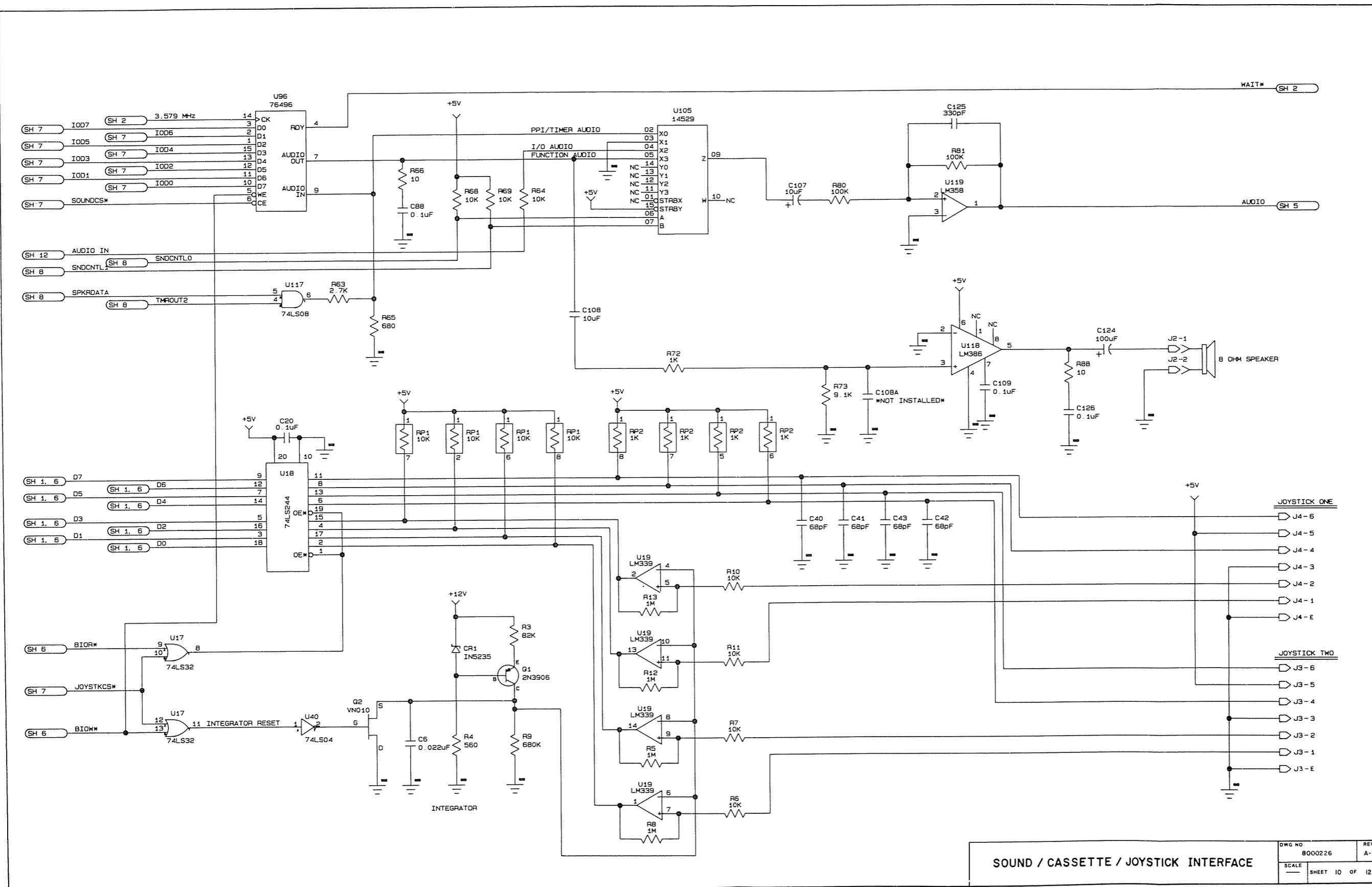


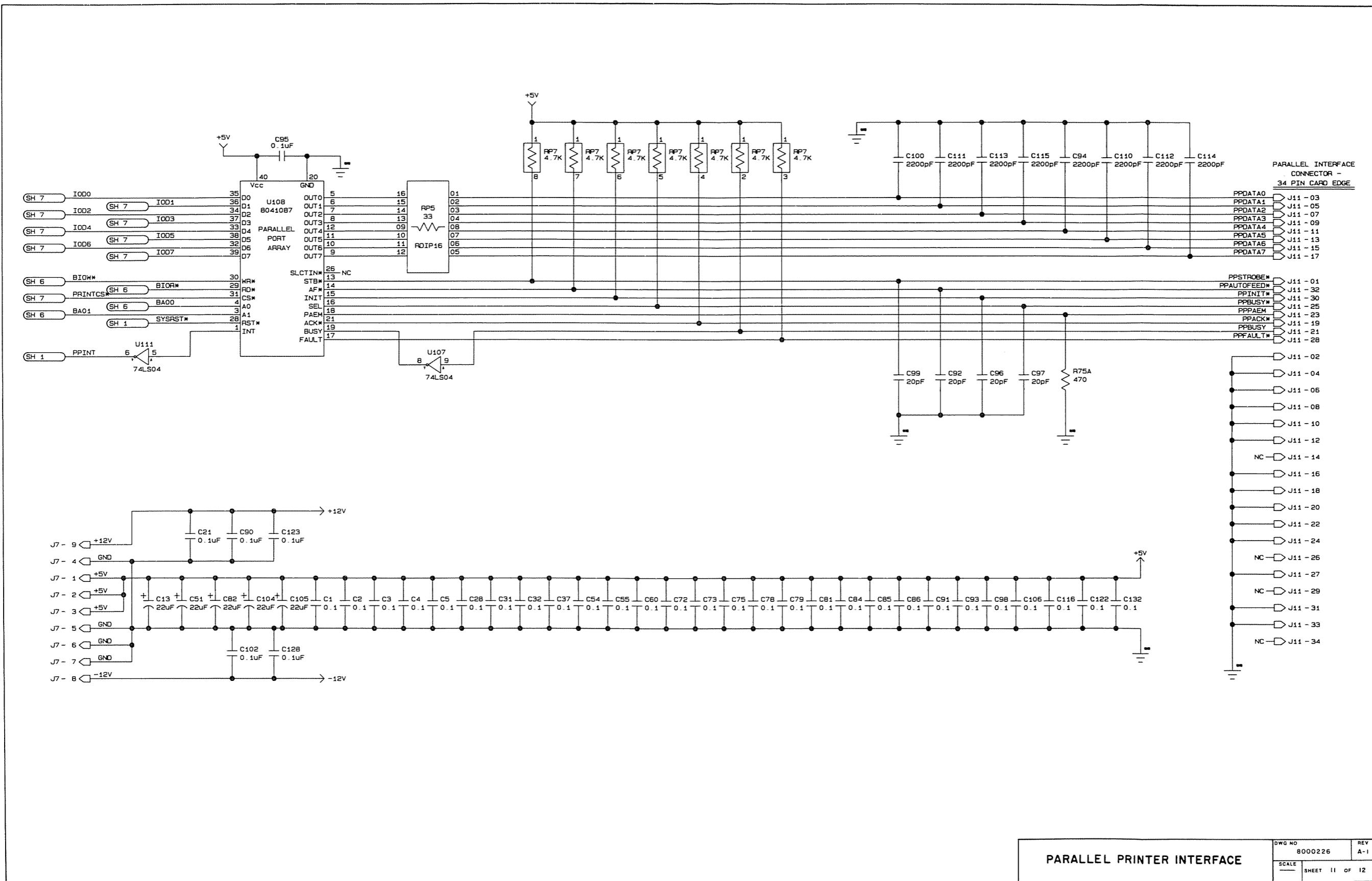
I/O BUS INTERFACE

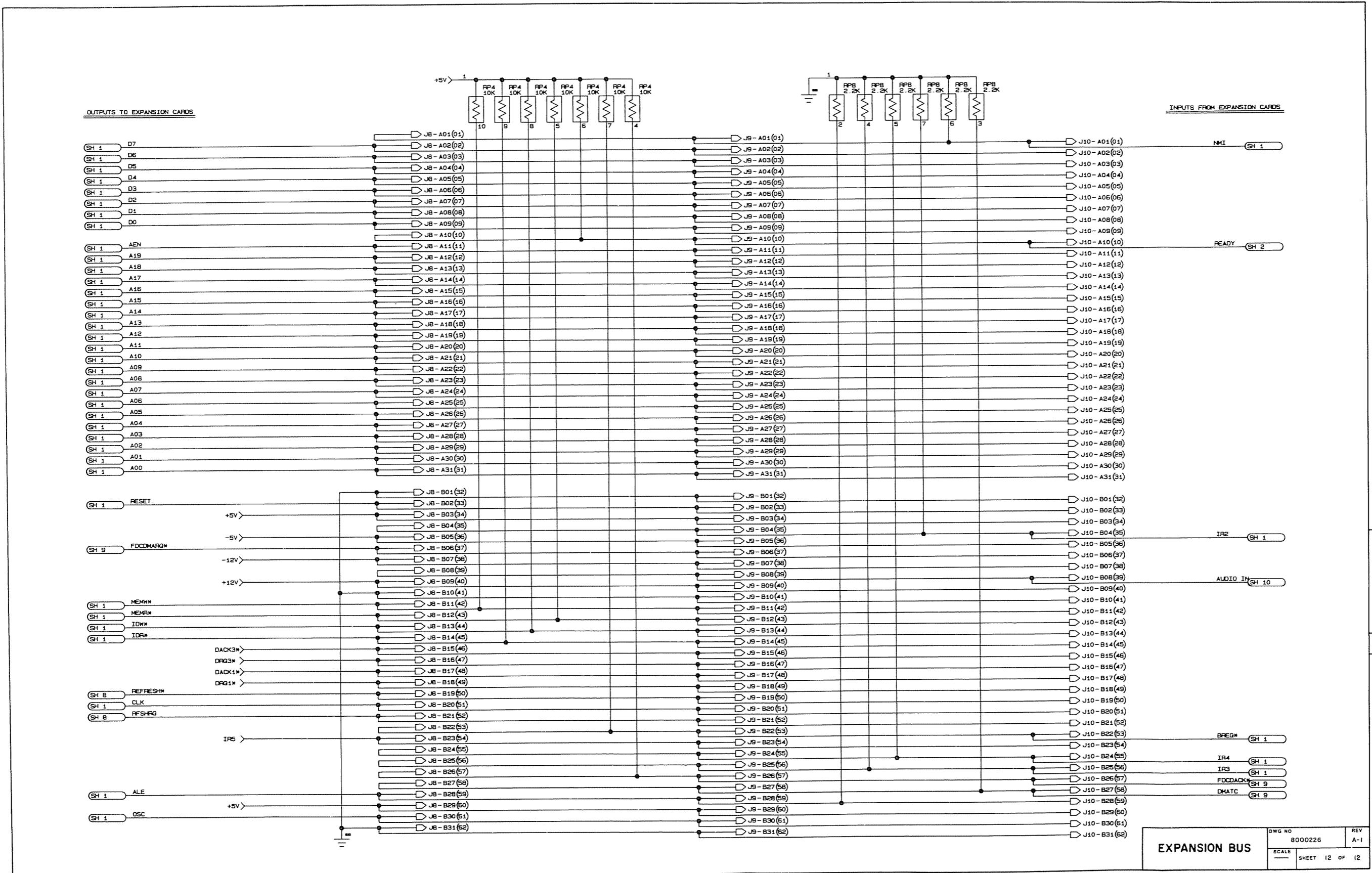
DWG NO	8000226	REV
SCALE	SHEET 7 OF 12	A-1

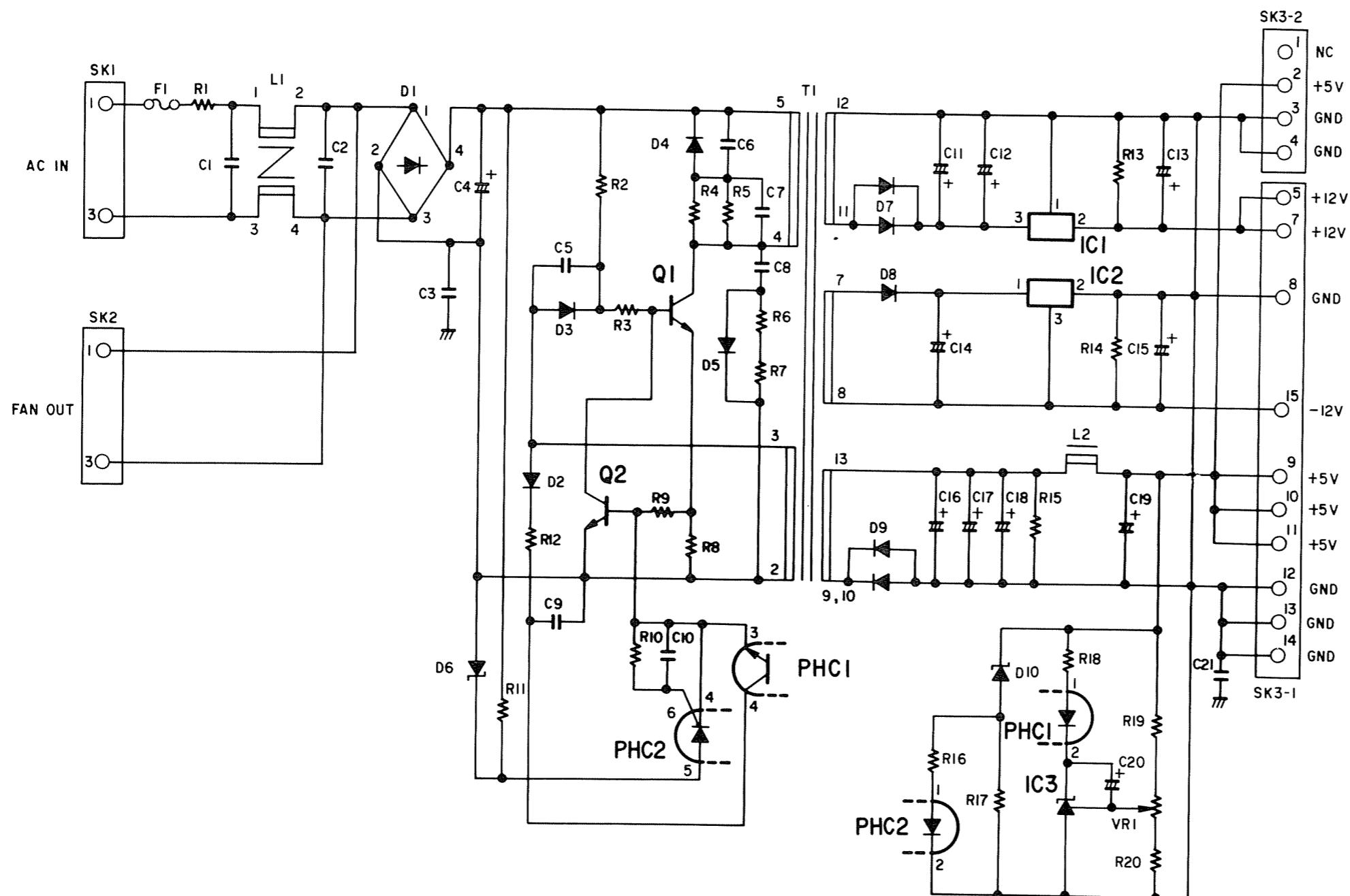




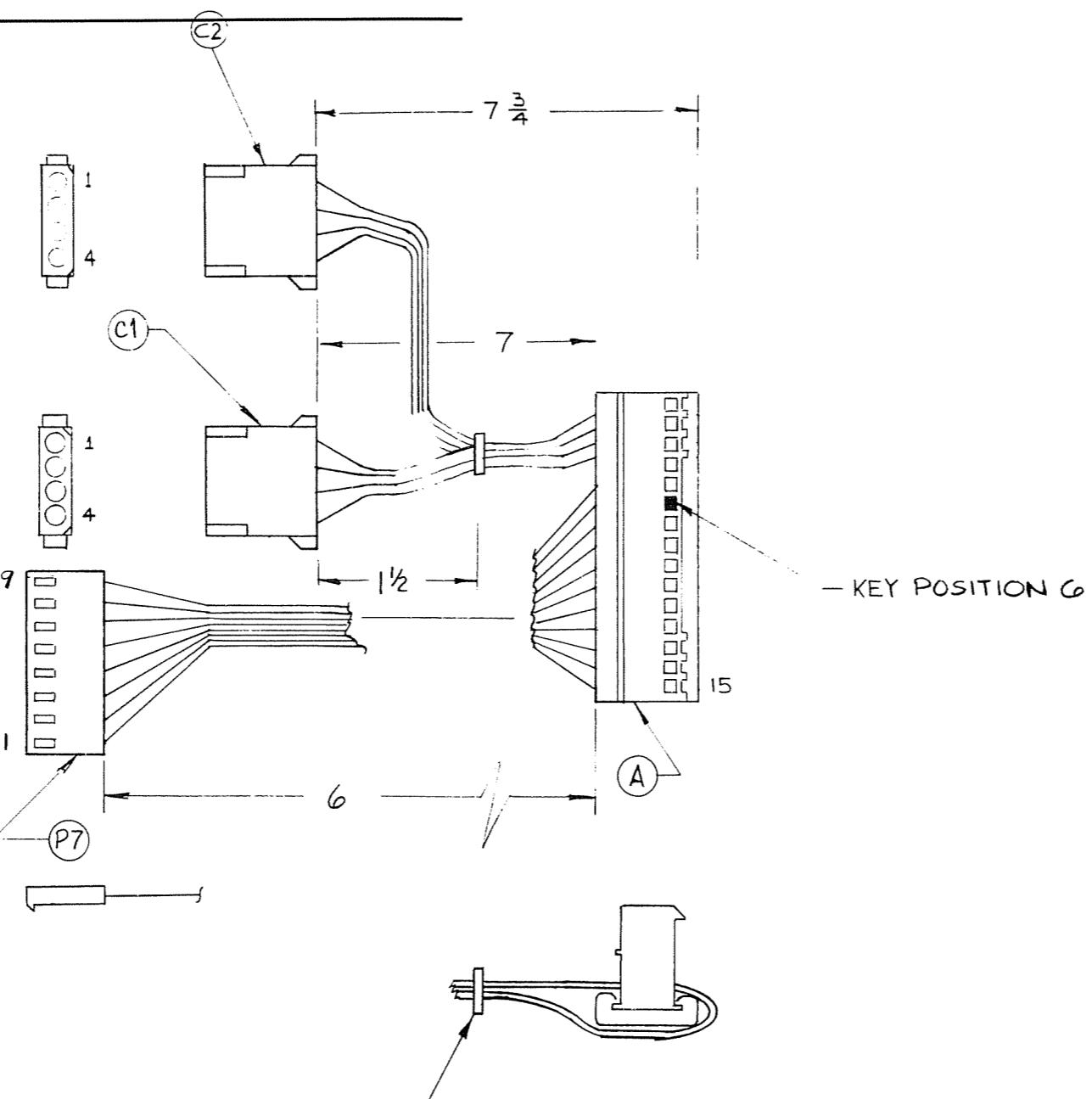






Power Supply

12 / CONNECTORS AND PIN DESIGNATIONS

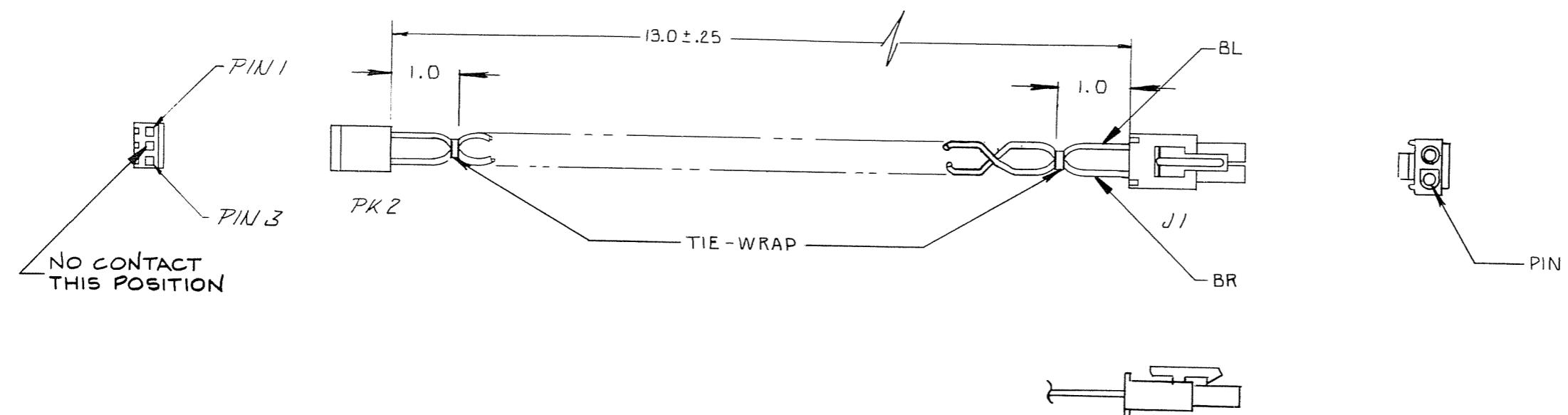


Cable, Assembly W1(6008131)

3 - OR EQUIVALENT

2 - TOLERANCE: $\pm \frac{1}{4}$

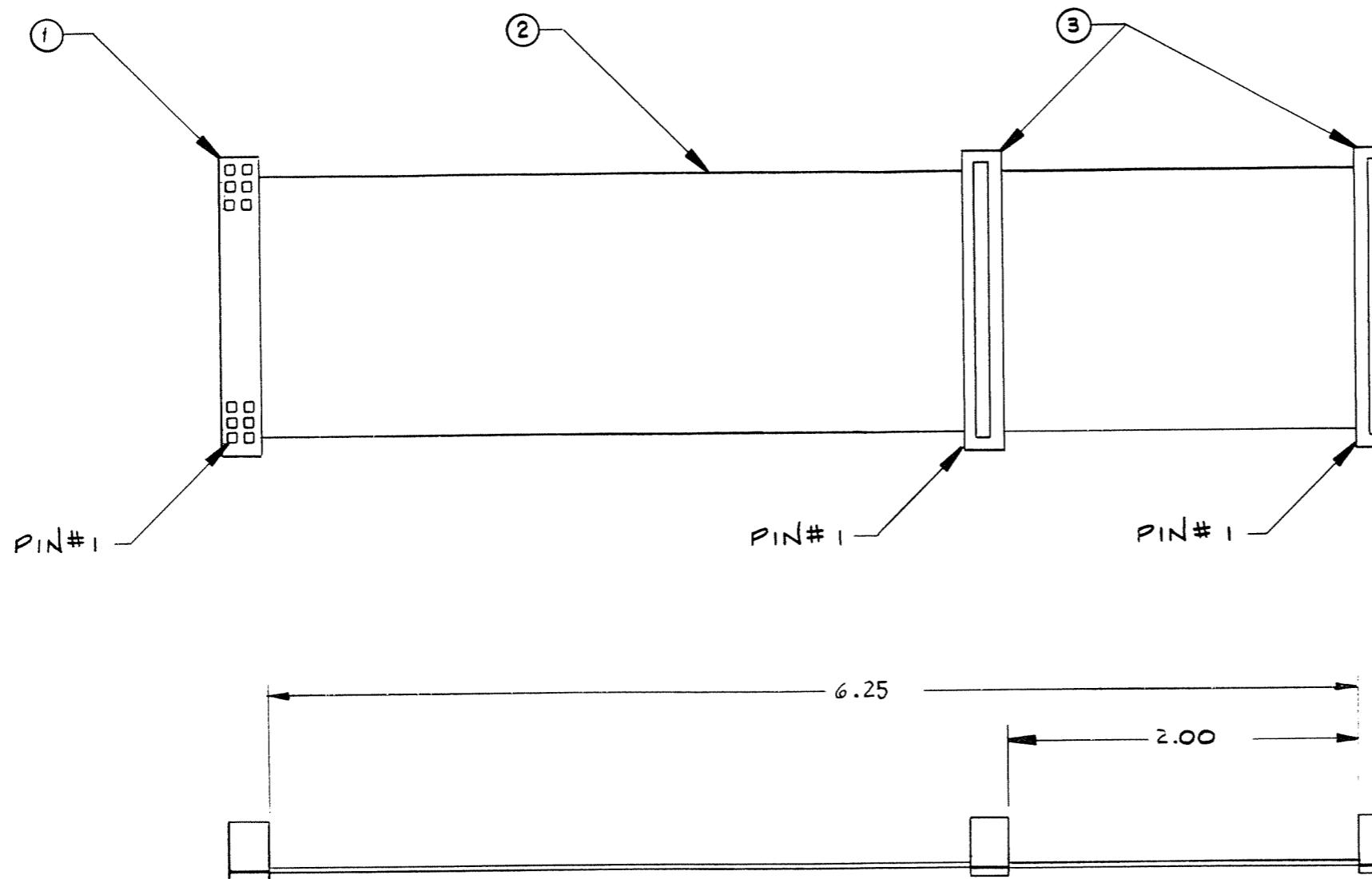
1 - TY-WRAPS AS REQUIRED



WIRE LIST					
FUNCTION	WIRE		CONNECTOR PIN#		
	AWG	COLOR	PK2	J1	
LINE	18	BRN	1	1	
NEUTRAL	18	BLU	3	2	

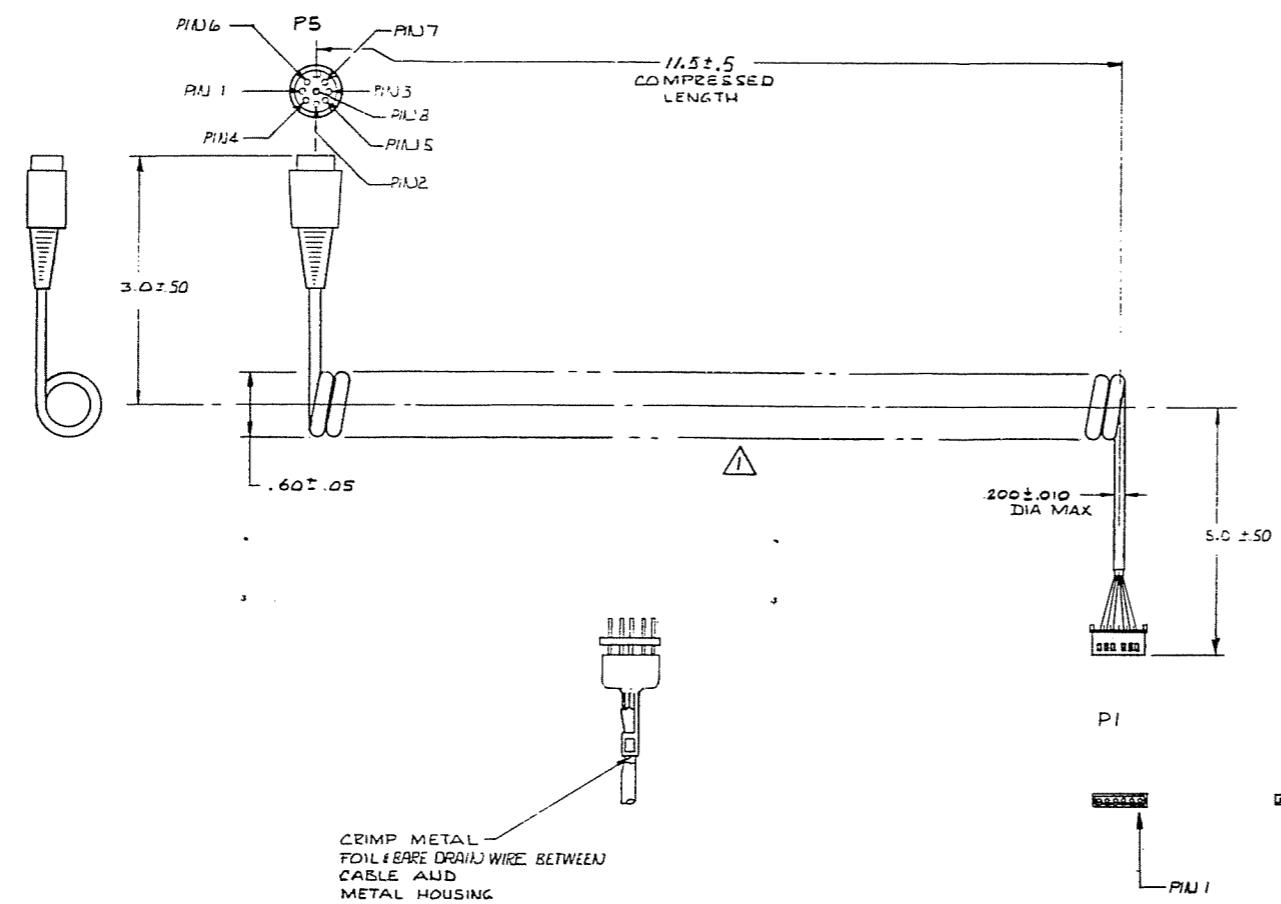
Cable, Assembly W2(6008141)

PARTS LIST				
DES	QTY	DESCRIPTION	MFG/PN	REMARKS
PK2	1	CONNECTOR 2 POS	MOLEX / 26-03-4030	
	2	CONTACTS	MOLEX / 08-50-0187	
J1	1	CONNECTOR 2 POS	MOLEX / 19-09-1029	OR EQUIVALENT
	2	CONTACTS	MOLEX 02-09-2101	OR EQUIVALENT
BR	AR	WIRE 18 AWG BROWN		80°C (LINE)
BL	AR	WIRE 18 AWG BLUE		80°C (NEUTRAL)



PARTS LIST				
ITEM	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
①	1	CONNECTOR - 34 POS. RECEPTACLE	MOLEX - 15-29-3343	
②	1	CABLE - RIBBON, 34 CONDUCTOR		.050 PITCH
③	2	CONNECTOR - 34 PIN EDGE CARD	3M-3463-0001/AMP 499930 - 3	

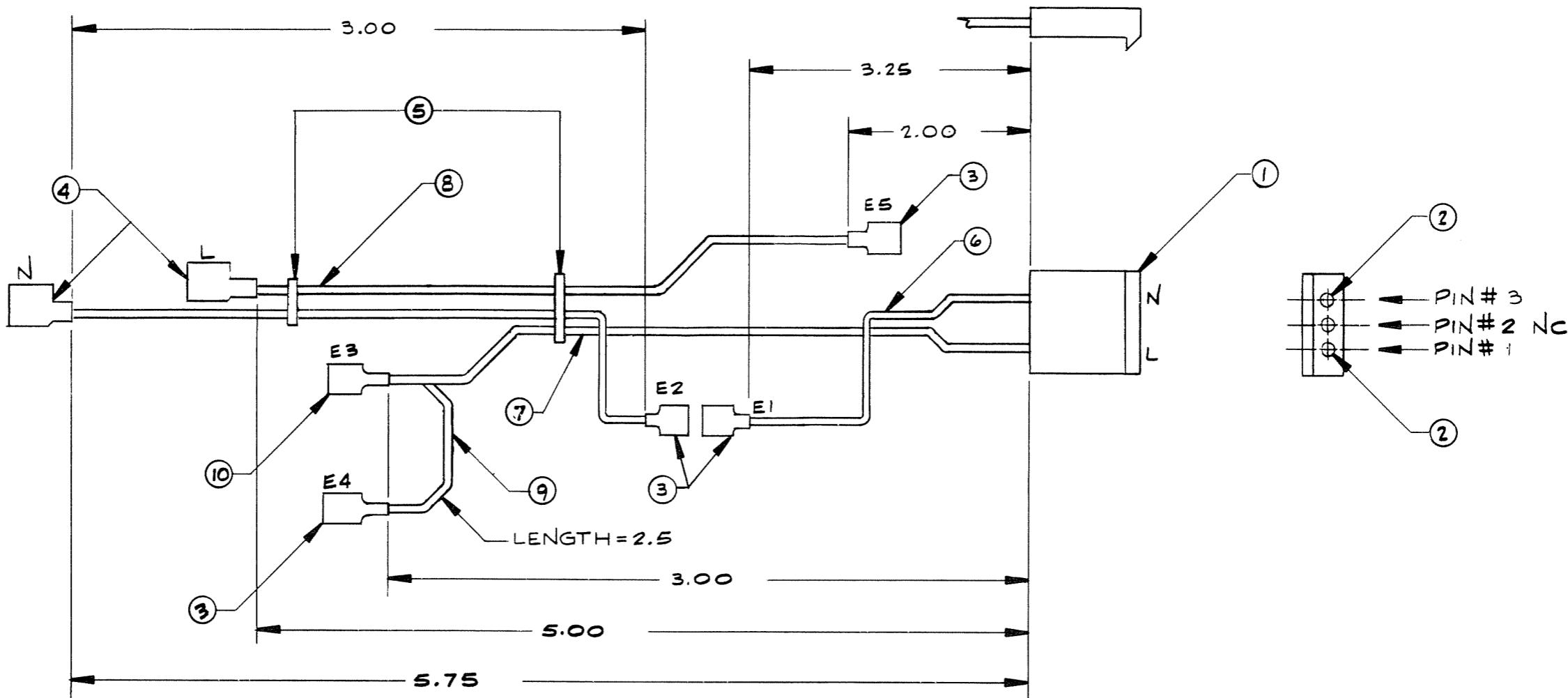
Cable, Signal W3(6008118)



PARTS' LIST			
DES	QTY	DESCRIPTION	MFG./PART NO.
P5	1	CONN 8 PIN DIN	HOSHIDEN TCP-028G-O-D40F
P1	1	GCKT HOUSING	MOLEX #50-37-5063
	6	CONTACT	MOLEX #08-10-1039

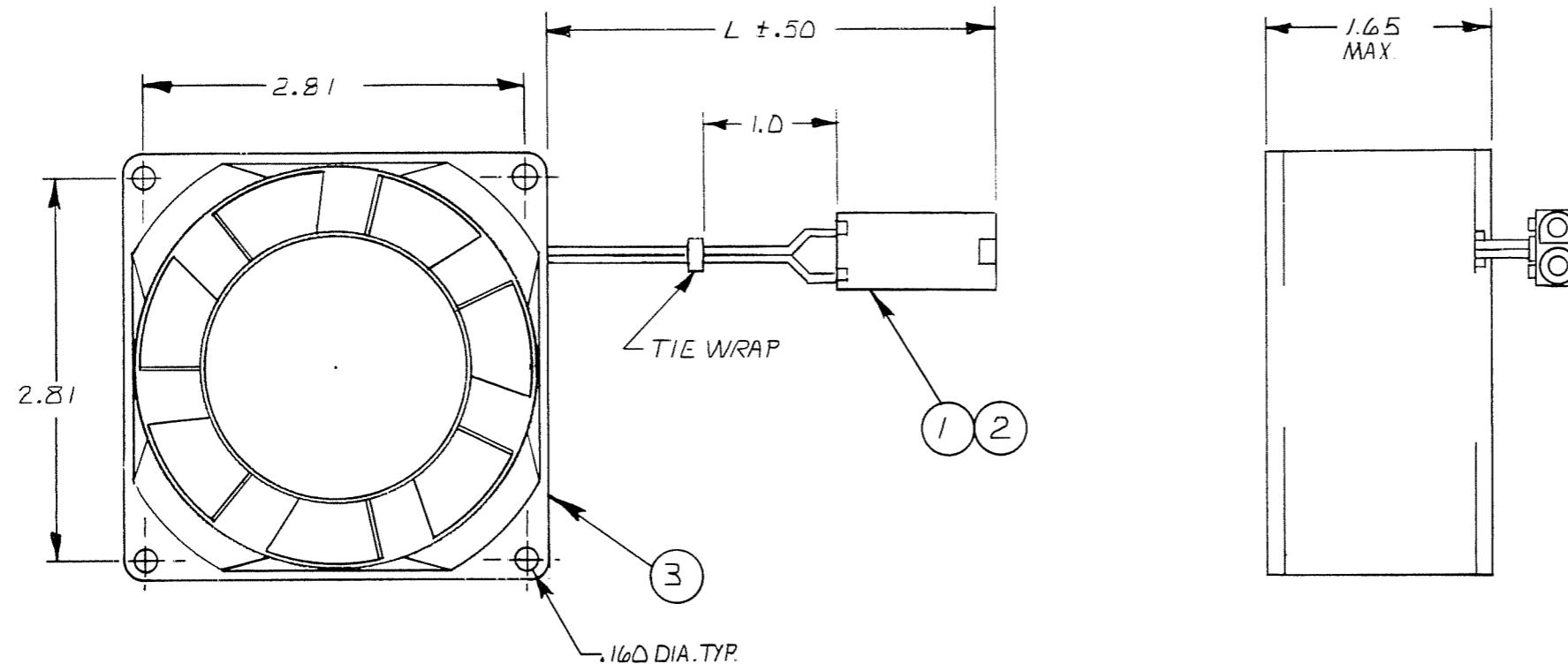
⚠ CABLE IS 6 CONDUCTOR SHIELDED;
EACH CONDUCTOR IS 26 AWG, 7 WIRE STRANDED;
FOIL SHIELD WITH DRAIN LUG; RE/
OUTER JACKET IS TANDY FAMU GRAY TPR.

NOTES (UNLESS OTHERWISE SPECIFIED):



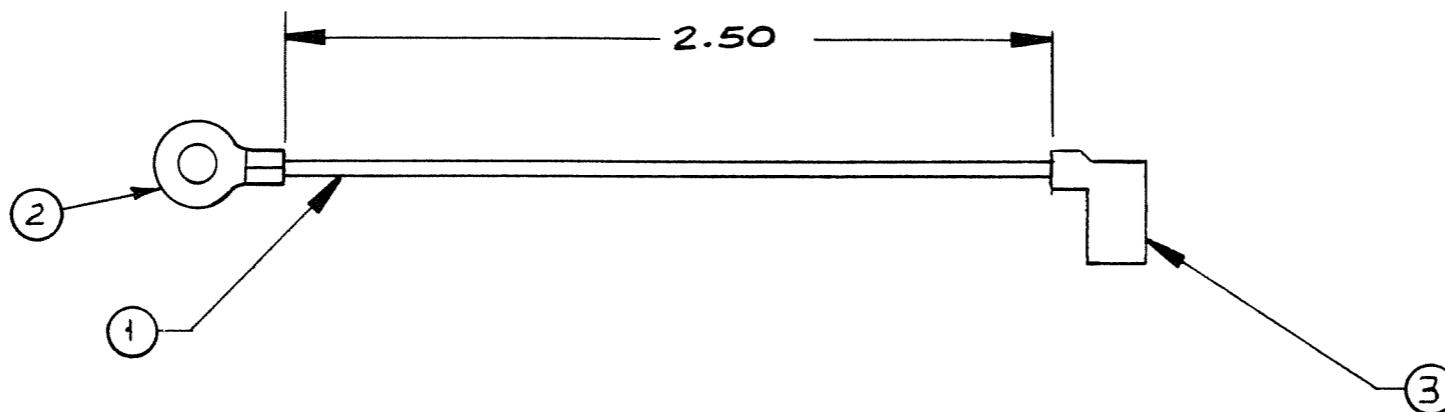
Cable, Assembly W6(6008121)

PARTS LIST				
LTR	QTY	DESCRIPTION	PART MFG NO	REMARKS
1	1	CONNECTOR - 3 PIN	MOLEX 26-03-4030 2	
2	2	CONTACT	MOLEX DB-5D-D187 2	
3	4	FASTON - (.25 X .032)	AMP# 2-520183-2 2	FULLY INSULATED
4	2	FASTON - RIGHT ANGLE (.25 X .032)	AMP # 2-520128-2 2	FULLY INSULATED
5	2	TY-WRAP		
6	1	WIRE - 18 AWG, BLUE		
7	1	WIRE - 18 AWG, BROWN		
8	1	WIRE - 18 AWG BROWN		
9	1	WIRE - 18 AWG BROWN		
10	1	FASTON (.25 X .032)	AMP# 3-350819-2 2	FULLY INSULATED



Cable, Assembly W7(2600009)

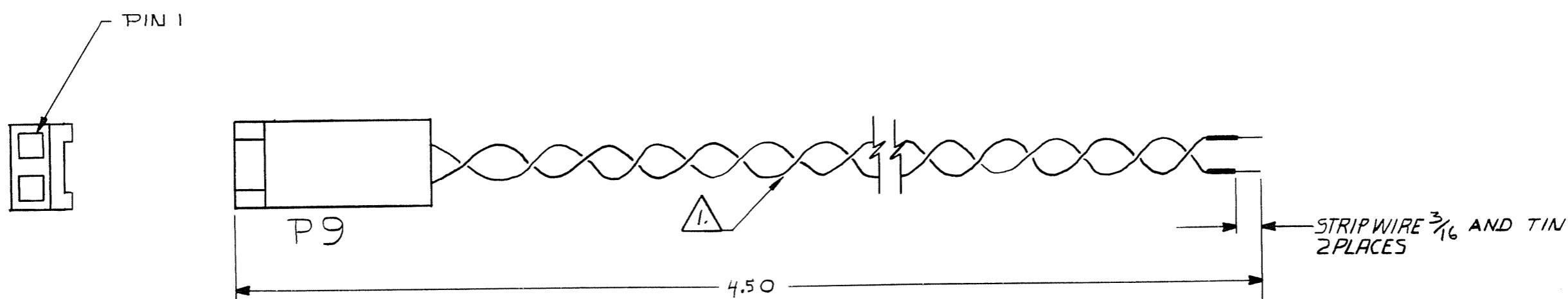
ITEM NO.	QTY.	DESCRIPTION	MFG / PART NO.	DIM. L	REMARKS
1	1	CONNECTOR-MALE	MOLEX/19-09-2029	—	
2	2	PINS	MOLEX/02-09-1102	—	
3	1	FAN	ROTRON/3U2E1	5.0	
			TORIN/31022-20	3.75	ALTERNATE
			NMB/EPO75-38-GZL1	5.50	ALTERNATE
			VEAUS/V52B4	3.75	ALTERNATE



PARTS LIST				
ITEM	QTY	DESCRIPTION	MFG PART NO.	REMARKS
(1)	1	WIRE - 18 AWG. GREEN W/YELLOW STRIPE		
(2)	1	RING TERMINAL	AMP # 350981-2 □	
3	1	FASTON (.25 X .032) RIGHT ANGLE	AMP # 2-520128-2 □	

△ OR EQUIVALENT
1. CABLE TOLERANCE ± .25

Cable, ground W8(6008125)



WIRE LIST			
FUNCTION	WIRE	CONNECTOR / PIN NO.	
	AWG	COLOR	P-9
SPKR OUT	24	GRY	1 TO SPEAKER + TERMINAL
GND	24	BLK	2 TO SPEAKER - TERMINAL

Cable, Assembly W15(6008070)

PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P9	1	CONN SOCKET 2 POS	MOLEX / 22-01-3027	
	2	CONTACT	MOLEX / 08-50-0113	

APPENDICES

The following sections contain reprints of manufacturer's documentation of components used in the Tandy 1000.

Tandy Corporation gratefully acknowledges permission by the following to reprint their copyrighted material in this manual.

A / Teac Corporation
3-7-3 Naka-Cho
Musashimo, Tokyo, Japan

TEAC FD-54B
MINI FLEXIBLE DISK DRIVE
SPECIFICATION

REV. C

TABLE OF CONTENTS

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1-1. APPLICATION

This SPECIFICATION provides a description for the TEAC FD-54B, double sided 48tpi mini flexible disk drive (hereinafter referred to as the FDD). Head load solenoid is not used in this FDD.

1-2. DISK

5.25 inch, soft or hard sectored flexible disks which comply with ISO, ANSI, or ECMA standard.

1-3. PHYSICAL SPECIFICATION

(1) Width: 146mm (5.75 in), Nom.

(2) Height: 41.3mm (1.63 in), Nom.

(3) Depth: 203mm (7.99 in), Nom.(excludes projections of interface connectors).

(4) Weight: Less than 1.5Kg (3.31 lbs)

(5) External view: See Fig.101

(6) Cooling: Natural air cooling

(7) Mounting: Mounting for the following directions are acceptable.

(a) Front loading, mounted vertically with front lever up.

(b) Front loading, mounted horizontally with indicator up. Do not mount horizontally with spindle motor up.

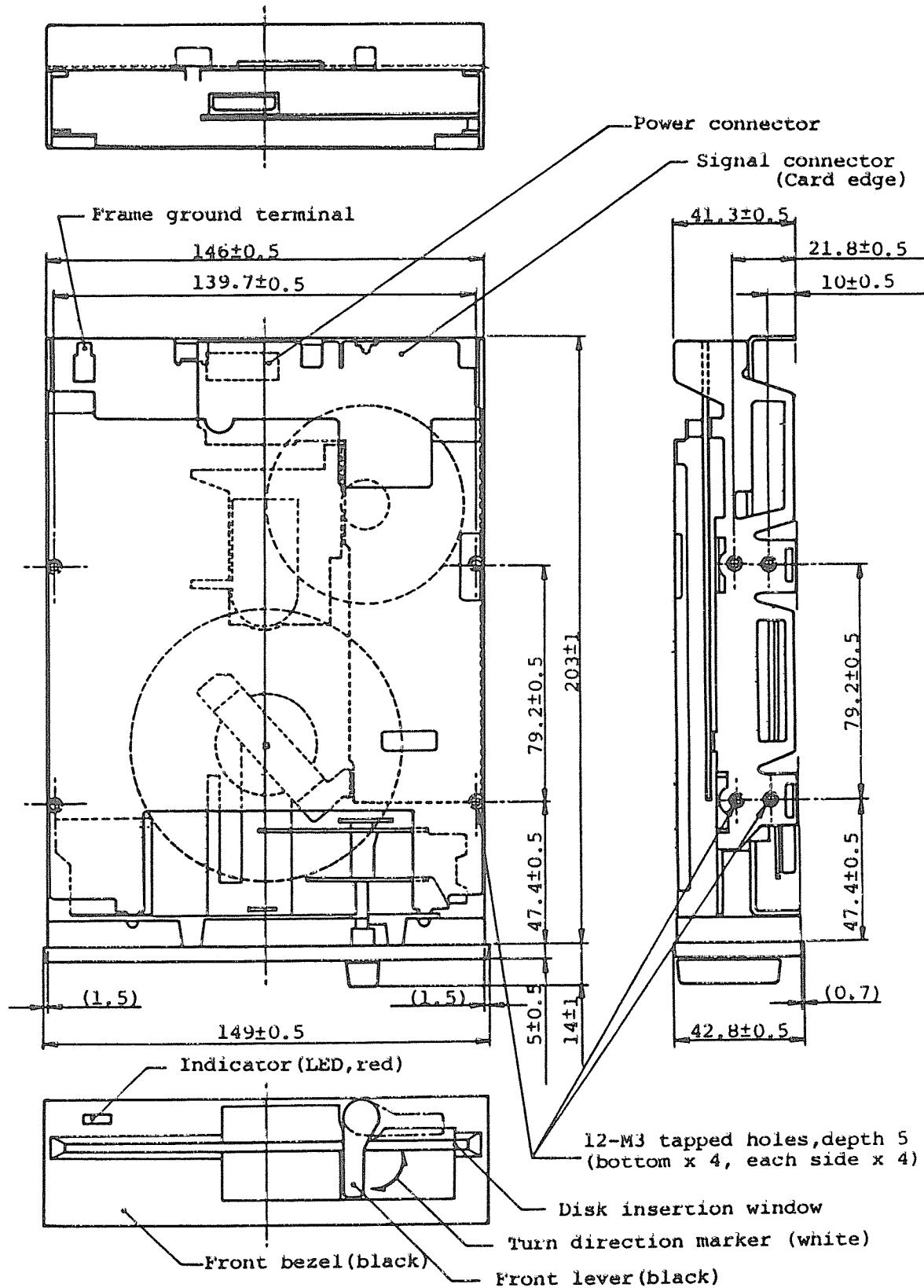
(c) Mounting angle in items (a) and (b) should be less than 30° with front bezel up.

Note: As to the most appropriate mounting condition and mounting for other directions than the above will be considered separately.

(8) Installation: With installation holes on the side frame or on the bottom frame of the FDD (see Fig.101)

(9) Material of frame: Sheet metal

(10) Material of front bezel : PPFOX (Xyron) or ABS
Standard color : Black



(Fig.101) External view

(Units:mm)

1-4. REQUIRED POWER

The following specifications are applicable at the power connector of the FDD.

(1) DC+12V

(a) Voltage tolerance

Read/write operation: Less than $\pm 5\%$

Others : Less than $\pm 10\%$

(b) Allowable ripple voltage: Less than 200mVp-p (including noise)

(c) Operating current consumption

Typical average: 0.25A

(using a disk of typical running torque)

Maximum average: Less than 0.6A

(using a disk of maximum running torque)

Peak: Less than 1.0A (400msec, Max. at spindle motor start)

(d) Waiting current consumption (spindle motor off)

Typical: 0.05A

Maximum: 0.08A

(2) DC+5V

(a) Voltage tolerance: $\pm 5\%$

(b) Allowable ripple voltage: Less than 100mVp-p (including noise)

(c) Operating current consumption

Typical average: 0.3A

Maximum average: Less than 0.36A

Peak: Less than 0.46A

(d) Waiting current consumption

Typical: 0.29A

Maximum: Less than 0.35A

(3) Power consumption

(a) Typical at operating: 4.5W

(b) Typical at waiting: 2.05W

(4) Power on sequence

Not specified. Since the FDD is equipped with power reset circuit, disk and data on the disk will not be damaged by power on or off.

1-5. ENVIRONMENTAL CONDITIONS

(1) Ambient temperature

- (a) Operating: $4^{\circ}\text{C} \sim 46^{\circ}\text{C}$ ($40^{\circ}\text{F} \sim 115^{\circ}\text{F}$)
- (b) Storage: $-22^{\circ}\text{C} \sim 60^{\circ}\text{C}$ ($-8^{\circ}\text{F} \sim 140^{\circ}\text{F}$)
- (c) Transportation: $-40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ ($-40^{\circ}\text{F} \sim 149^{\circ}\text{F}$)

(2) Temperature gradient

- (a) Operating: Less than 15°C (27°F) per hour
- (b) Transportation and storage: Less than 30°C (54°F) per hour

(3) Relative humidity

- (a) Operating: 20% ~ 80% (no condensation)
Maximum wet bulb temperature shall be 29°C (84°F)
- (b) Storage: 10% ~ 90% (no condensation)
Maximum wet bulb temperature shall be 40°C (104°F)
- (c) Transportation: 5% ~ 95% (no condensation)
Maximum wet bulb temperature shall be 45°C (113°F)

(4) Vibration

- (a) Operating: Less than 0.5G (less than 55Hz)
- (b) Transportation: Less than 1G (less than 100Hz)

(5) Shock

- (a) Operating: Less than 10G (less than 10msec)
- (b) Transportation: Less than 40G (less than 10msec)

(6) Altitude

(a) Operating: Less than 5,000m(16,500 feet)

(b) Transportation: Less than 12,000m (40,000 feet)

Note: The above requirements are applied for the FDD without shipping box..

When a long period is required for transportation such as by ship,
the storage environmental conditions shall be applied.

1-6. OPERATIONAL CHARACTERISTICS

(1) Data capacity

Recording method		FM	MFM
Data transfer rate (K bits/sec)		125	250
Tracks/disk		80	80
Innermost track bit density (bpi)		2,938 (side 1)	5,876 (side 1)
Innermost track flux density (frpi)		5,876 (side 1)	5,876 (side 1)
Data capacity	Unformatted	K bytes/track	3.125
		K bytes/disk	250
	Formatted (16 sectors /track)	K bytes/sector	0.128
		K bytes/track	2.048
		K bytes/disk	163.84
			6.25
			500
			0.256
			4.096
			327.68

(Table 101) Data capacity

(2) Disk rotation mechanism

- (a) Spindle motor: Direct DC brushless motor
- (b) Spindle motor speed: 300rpm
- (c) Motor servo method: Frequency servo by AC tachometer
- (d) Motor/spindle connection: Motor shaft direct
- (e) Disk speed: 300rpm
 - Long term speed variation (LSV): Less than $\pm 2\%$
 - Instantaneous speed variation (ISV): Less than $\pm 2\%$
- (f) Start time: Less than 400msec
- (g) Average latency: 100msec

(3) Index

- (a) Number of index: 1 per disk revolution
- (b) Detection method: LED and photo-transistor
- (c) Detection cycle: 200msec $\pm 2\%$

(d) Index/alignment dipole spacing: 0 ~ 400 μ sec, with specified test disk.

(4) Track construction

(a) Track density: 48tpi

(b) Number of cylinders: 40 cylinders

(c) Number of tracks: 40 tracks/surface, 80 tracks/disk

(d) Outermost track radius (track 00): Side 0 57.150mm (2.2500 in)

Side 1 55.033mm (2.1667 in)

(e) Innermost track radius (track 39): Side 0 36.513mm (1.4375 in)

Side 1 34.396mm (1.3542 in)

(f) Positioning accuracy: Less than $\pm 40\mu$ m, with specified test disk.

(Track 16, 23 ± 2 °C, 40 ~ 60%RH)

(5) Magnetec head

(a) Magnetic head: Gimball supported read/write head with tunnel erase,
2 sets

(b) Read/write head track width: 0.330mm (0.0130 in), Nom.

(c) Effective track width after tunnel erase:

0.300 \pm 0.025mm (0.0118 \pm 0.0010 in)

(d) Erase head track width: 0.170mm (0.0067 in), Nom.

(e) Read/write-erase gap spacing: 0.85 \pm 0.05mm (0.0335 \pm 0.0020 in)

(f) Read/write gap azimuth: 0° \pm 18°, with specified test disk.

(6) Track seek mechanism

(a) Head positioning mechanism: Band positioner

(b) Stepping motor: 4-phase, 200 steps per revolution

(c) Stepping motor drive: 2 steps per track

(d) Outermost and innermost stopper: Mechanical moving stopper of head
carriage

(e) Track 00 detection method: LED and photo-transistor

(f) Track to track time: Less than 6msec

(g) Settling time: Less than 15msec (excludes track to track time)

(7) Head load mechanism: Not used.

(When a disk is inserted and the door is closed,
the FDD becomes head load condition).

(8) File protect mechanism: Detection of write enable notch by LED and
photo transistor

(9) Window margin (shipping): More than 600nsec, with specified test disk.
MFM method, PLO separator, and 0 write pre-compensation.

1-7. RELIABILITY

- (1) MTBF: 8,000 power on hours or more (for typical usage)
- (2) MTTR: 30 minutes
- (3) Design component life: 5 years
- (4) Preventive maintenance: Not required (for typical usage)
- (5) Error rates
 - (a) Soft read error: 1 per 10^9 bits(up to 2 retries)
 - (b) Hard read error: 1 per 10^{12} bits
 - (c) Seek error: 1 per 10^6 seeks
- (6) Security standard: Complying with UL, CSA

1-8. SIGNAL INTERFACE

Four FDDs, Max. can be connected to one FDD controller by daisy chaining.

1-8-1. Electrical Characteristics

(1) Interface driver/receiver: See Fig.102.

(2) Electrical characteristics

The following specifications are applicable at the signal connector of the FDD.

(a) Input signal

LOW level (TRUE): 0V ~ 0.5V

DRIVE SELECT signal line: 12mA, Max. current

Other input signal lines: 6mA, Max. current

HIGH level (FALSE): 2.5V ~ 5.25V

(b) Output signal

LOW level (TRUE): 0V ~ 0.4V

Driver sink current capability: 12mA, Max.

(24mA, Max. for 0.5V LOW level)

HIGH level (FALSE): 5.25V, Max.

(depending on controller terminator)

(3) Terminator

(a) Resistance value:

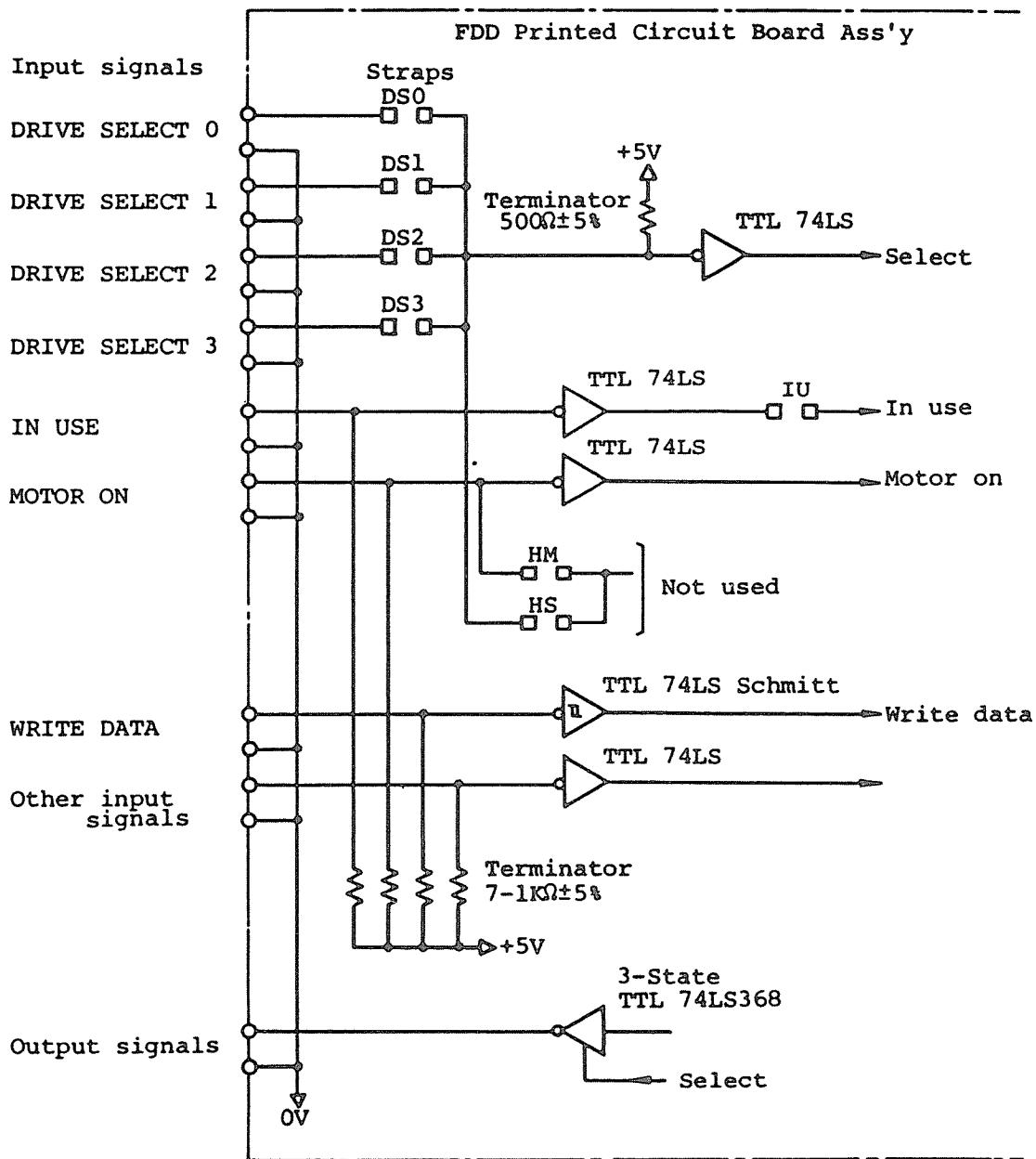
DRIVE SELECT signal line: $500\Omega \pm 5\%$

Other input signal lines: $1K\Omega \pm 5\%$

(b) All of the terminator resistors are mounted on the PCB with soldering joint. (Unremovable)

(c) Multiplex connection:

For the multiple connection of the FDDs by daisy chaining, multiple terminator resistors are connected to an input signal line in parallel except for the DRIVE SELECT signal lines.



(Fig.102) Signal interface circuit

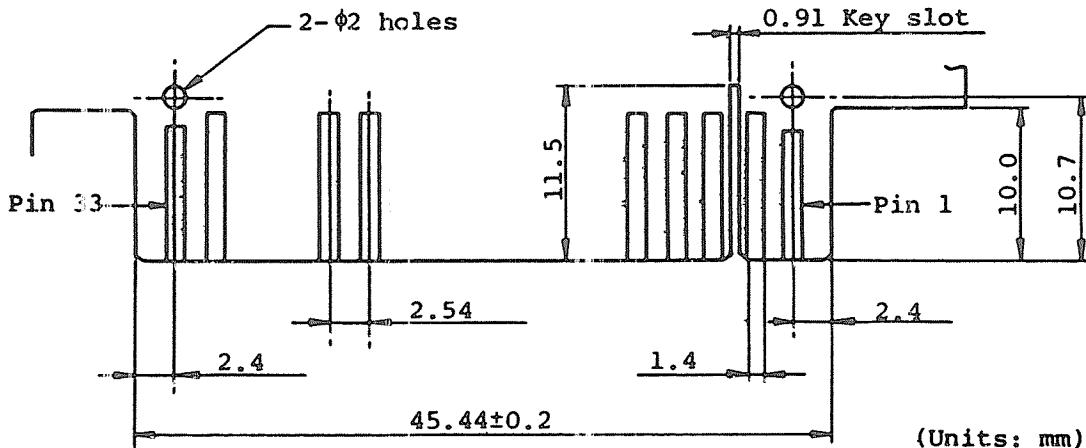
1-8-2. Signal Connector and Cable

(1) Signal connector

- (a) FDD side connector: Card edge (gold plated)
- (b) Pin numbers & pin pitch: 34 pins, 2.54mm (0.1 in) pitch
 - (17 pins on both sides, even number pins are bottom side of the FDD)
- (c) Polarizing key location: Between pins 4 and 6
- (d) Card edge dimensions: See Fig.103
- (e) Interface connections: See Table 102
- (f) Cable side matched connector: 3M, Scotchflex ribbon connector,
P/N 3463-0001
or AMP, thin leaf connector, P/N 583717-5
and connector P/N 1-583616-1
.or equivalent

(2) Maximum interface cable length: 1.5m, Max.

For the multiplex connection by daisy chaining, the total cable length shall be less than 1.5m.



- Notes:
- 1. PCB thickness: 1.6mm, Nom.
 - 2. The figure shows top view of the FDD.

(Fig.103) Card edge dimensions of signal connector

Signals	Directions	Terminal Nos.	
		Signals	0V
SPARE	INPUT	2	1
IN USE	INPUT	4	3
DRIVE SELECT 3	INPUT	6	5
INDEX/SECTOR	OUTPUT	8	7
DRIVE SELECT 0	INPUT	10	9
DRIVE SELECT 1	INPUT	12	11
DRIVE SELECT 2	INPUT	14	13
MOTOR ON	INPUT	16	15
DIRECTION SELECT	INPUT	18	17
STEP	INPUT	20	19
WRITE DATA	INPUT	22	21
WRITE GATE	INPUT	24	23
TRACK 00	OUTPUT	26	25
WRITE PROTECT	OUTPUT	28	27
READ DATA	OUTPUT	30	29
SIDE ONE SELECT	INPUT	32	31
READY	OUTPUT	34	33

Note: SPARE terminal is open condition.

(Table 102) Signal interface connections

1-8-3. Input/Output Signals

In the following, input signals are those transmitted to the FDD while output signals are those transmitted from the FDD.

LOW level of the signals is TRUE.

(1) DRIVE SELECT 0 ~ 3 input signals

- (a) Signals of four lines to select a specific FDD for operating in multiplex control by daisy chaining.
- (b) Only the DRIVE SELECT signal of the same number as of on-state strap among DSO ~ 3 straps is effective.
- (c) All the input and output signals except for the MOTOR ON and IN USE can be effective when this signal is effectively received.
- (d) The time required to make each input or output signal effective after the transmission of this signal is 0.5 μ sec, Max. including delay time through the interface cable.
- (e) When the DRIVE SELECT signal of the same number as of on-state strap among DSO ~ 3 straps becomes TRUE, the front bezel indicator turns on.

(2) MOTOR ON input signal

- (a) Level signal to rotate the spindle motor.
- (b) The spindle motor reaches to the rated rotational speed within 400msec after this signal becomes TRUE, and then data read or write operation can be executed.

(3) DIRECTION SELECT input signal

- (a) Level signal to define the moving direction of the head when the STEP line is pulsed.
- (b) Step-out (moving away from the center of the disk) is defined as HIGH level of this signal. Conversely, step-in (moving toward the center of the disk) is defined as LOW level of this signal.

(4) STEP input signal

- (a) Pulse signal to move the head. The pulse width shall be more than 0.8 μ sec and the head moves one track space per one pulse.
- (b) The access motion (head seek operation) is initiated at the trailing edge of the pulse and completes within 21msec after starting the access including the settling time. For the successive access motion in the same direction, the pulses shall be input with the interval of more than 6msec, while the pulses shall be input with the interval of more than 21msec for the access motion in a different direction.
- (c) This signal becomes ineffective when the WRITE PROTECT signal is FALSE and the WRITE GATE signal is TRUE.
Also this signal becomes ineffective when the TRACK 00 signal is TRUE and the DIRECTION SELECT signal is HIGH level (step-out).
- (d) This signal shall be input according to the timing in Fig.104.

(5) WRITE GATE input signal

- (a) Level signal to erase the written data and to enable the writing of new data.
- (b) This signal becomes ineffective when the WRITE PROTECT signal is TRUE.
- (c) This signal shall be made TRUE after satisfying all of the following three conditions.
 - i) More than 400msec after the start of the spindle motor.
Or the FDD is in ready state (refer to item (13)).
 - ii) More than 21msec after the effective receival of the final STEP pulse.
 - iii) More than 100 μ sec after the level change of the SIDE ONE SELECT signal.
- (d) None of the following operations shall be done for at least 1msec after this signal is changed to FALSE.
 - i) Stop the spindle motor.
 - ii) Make the DRIVE SELECT signal FALSE.
 - iii) Start the head access motion by the STEP pulse.

(6) WRITE DATA input signal

- (a) Pulse signal to designate the contents of the data to be written on the disk. The pulse width shall be 0.15 μ sec through 2.5 μ sec and the leading edge of the pulse is used.
- (b) This signal becomes ineffective when one of the following conditions is satisfied.
 - i) WRITE GATE signal is FALSE.
 - ii) WRITE PROTECT signal is TRUE.
- (c) This signal shall be input according to the timing in Fig.105.

(7) SIDE ONE SELECT input signal

- (a) Level signal to define which side of a two-sided disk is used for reading or writing.
- (b) When this signal is HIGH level, the magnetic head on the side 0 surface of the disk is selected, while the magnetic head on the side 1 surface is selected when this signal is LOW level.
- (c) The READ DATA signal on a selected surface becomes valid more than 100 μ sec after the change of this signal level.
- (d) Write operation (the WRITE GATE signal TRUE) on a selected surface shall be started more than 100 μ sec after the change of this signal level.
- (e) When the other side of the disk is selected after the completion of a write operation, the level of this signal shall be switched more than 1msec after making the WRITE GATE signal FALSE.

(8) IN USE input signal

This signal is effective only when the IU strap is on state (refer to Fig.102).

- (a) Level signal to indicate that all of the daisy chained FDDs are in use condition under the control of the host system.

(b) The front bezel indicator turns on when this signal becomes TRUE.

(9) TRACK 00 output signal

- (a) Level signal which indicates that the head is on track 00 (the outermost track).
- (b) This signal becomes valid more than 5.8msec after the effective receival of the STEP pulse.

(10) INDEX/SECTOR output signal

- (a) Pulse signal for the detection of the index hole or the sector holes.
- (b) This signal can be output in a correct timing more than 400msec after the start of the spindle motor.
- (c) When using a soft sectored disk, there will be one index pulse on this line per one revolution of the disk. When using a hard sectored disk, sector pulses and index pulse are output together.
- (d) Fig.106 shows the timing for this signal. Leading edge of the pulse shall be used as the reference.
- (e) If the output condition in item (1)-(c) is satisfied when no disk is inserted, this signal maintains TRUE.

(11) READ DATA output signal

- (a) Pulse signal for the read data from the disk composing clock bits and data bits together.
- (b) Fig.107 shows the timing for this signal. Leading edge of the pulse shall be used as the reference.
- (c) This signal becomes valid when all of the following four conditions are satisfied.
 - i) More than 400msec after the start of the spindle motor.
Or the FDD is in ready state (refer to item (13)).
 - ii) More than 21msec after the effective receival of the final STEP pulse.

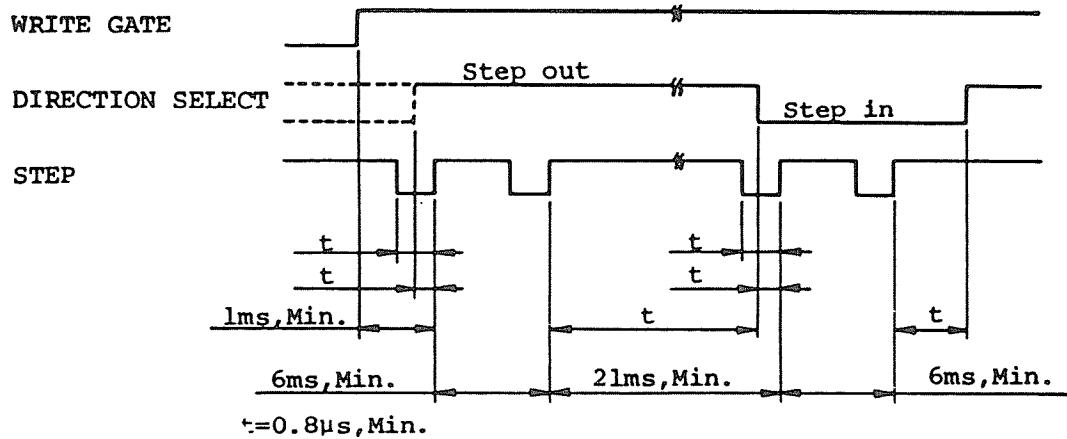
- iii) More than 1msec after the WRITE GATE signal becomes FALSE.
- iv) More than 100 μ sec after the level change of the SIDE ONE SELECT signal.

(12) WRITE PROTECT output signal

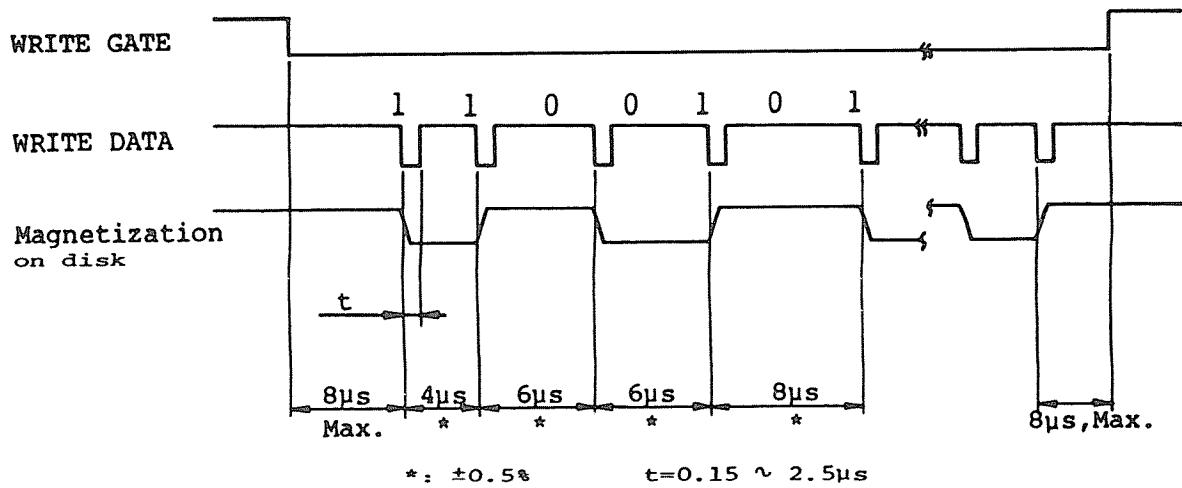
- (a) Level signal which indicates that the write enable notch of the disk is masked.
- (b) When this signal is TRUE, the data on the disk are protected from erasing and the writing of new data is inhibited.

(13) READY output signal

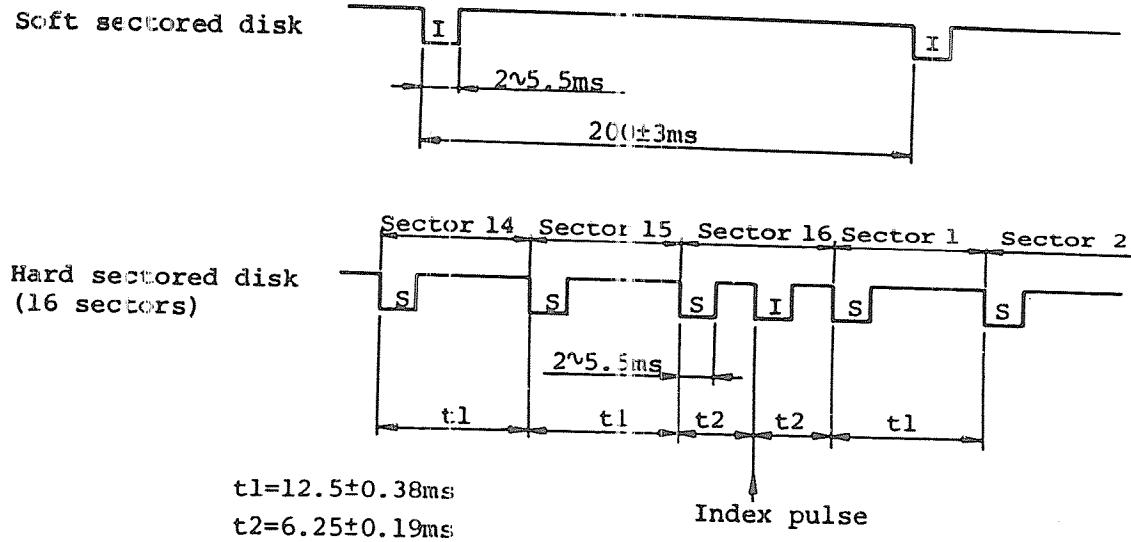
- (a) Level signal which indicates that the FDD is in ready state.
- (b) The FDD becomes ready state when all of the following four conditions are satisfied.
 - i) The FDD is powered on.
 - ii) Disk is installed.
 - iii) The disk rotates at more than 50% of the rated speed.
 - iv) Two INDEX pulses have been counted after item iii) is satisfied.
- (c) Required time for this signal to become TRUE after the start of the spindle motor is less than 800msec.
However, the spindle motor reaches to the rated rotational speed within 400msec after the start, and data read or write operation can be executed before the READY signal becomes TRUE.
- (d) If a hard sectored disk is used for the FDD, the above items (b)-iii), (b)-iv), and (c) cannot be applied. In such case, the ready state must be regarded as follows:
 - i) The FDD is powered on.
 - ii) Disk is installed.
 - iii) More than 400msec after the start of the spindle motor.



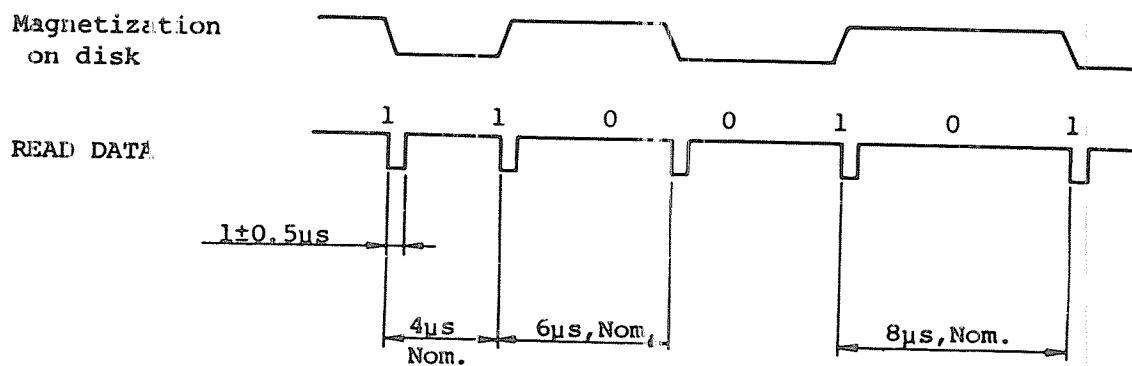
(Fig.104) STEP timing



(Fig.105) WRITE DATA timing (MFM method)



(Fig.106) INDEX/SECTOR timing



Note: The displacement of any bit position does not exceed $\pm 20\%$ from its nominal position.

(Fig.107) READ DATA timing (MFM method)

1-9. POWER INTERFACE

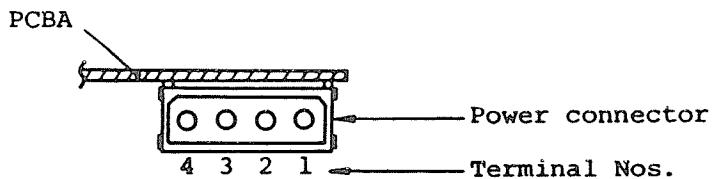
Refer to item 1-4 for power requirements.

(1) Power connector

- (a) FDD side connector: AMP, Mate-N-Lock connector, P/N 172349-1 or equivalent
- (b) Pin numbers: 4 pins
- (c) Protection method for mis-connection: Mechanical protection by the shape of the connector housing.
- (d) Pin location: See Fig.108
- (e) Power interface connections: See Table 103
- (f) Cable side matched connector: AMP, P/N 1-480424-0 and pins 60617-1, or 60619-1,
or equivalent

(2) Power cable

Any appropriate cables taking the maximum power consumption of the FDD and the power voltage at the connector into consideration will be acceptable.



(Fig.108) Power connector pin location (Rear view)

Voltage	Terminal Nos.
DC+12V	1
0V	2
0V	3
DC+5V	4

(Table 103) Power interface connections

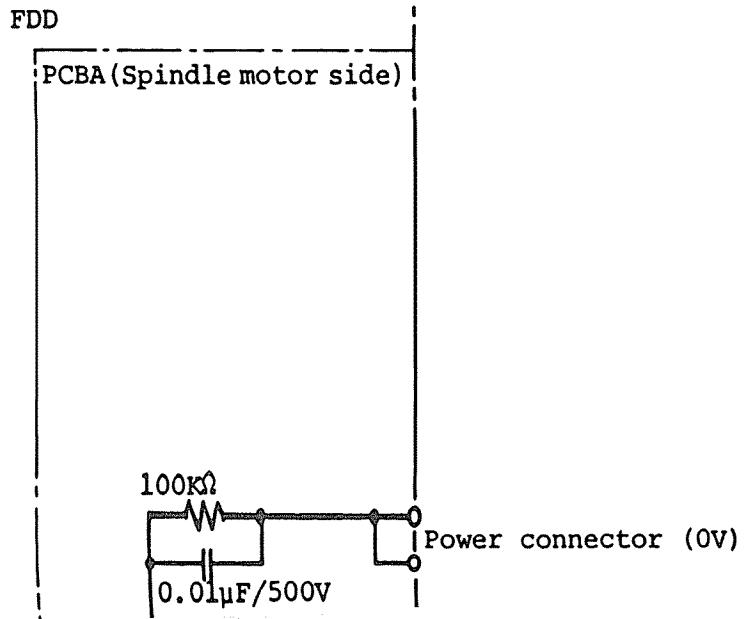
1-10. FRAME GROUNDING

(1) Frame grounding

- (a) Frame ground is AC coupled to DC 0V by $0.01\mu F//100K\Omega$.
- (b) Insulation resistance is more than $80K\Omega$ at less than DC 150V.

(2) Frame ground terminal (back side of the FDD)

- (a) FDD side terminal: AMP Faston 187 tab P/N 61761-2
or equivalent
- (b) Cable side matched terminal: AMP P/N 60972-2 or 60920-1
or equivalent



1-11. INDICATOR AND STRAPS

1-11-1. Indicator

LED Indicator on the front bezel turns on when either of the following conditions is satisfied.

- (a) When the DRIVE SELECT signal of the same number as of on-state strap among DS 0 ~ 3 straps becomes TRUE.
- (b) When the IU strap is on-state and the IN USE signal is TRUE.

1-11-2. Straps

All the straps are mounted on the FDD PCB (PCB to which the interface connector is connected). Insertion of a short bar onto the post pin of 0.64mm x 0.64mm (0.025 in) is defined as the on-state of the strap. Fig.110 shows the on-state of the straps at the shipment.

(1) DS 0 ~ 3 straps

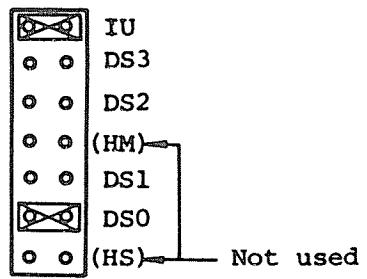
- (a) In the multiplex control by daisy chaining, these straps designate the address of the FDD.
- (b) By the combination with the DRIVE SELECT 0 ~ 3 signals (refer to Fig.102 and item 1-8-3 (1)), four addresses of 0 through 3 can be designated. Never designate more than 2 FDDs to a same address.

(2) IU strap

Strap to enable the IN USE signal. When this strap is off-state, the IN USE signal is ineffective.

(3) HS and HM straps

These straps are not used in this FDD. Set them to off-state.



Note: On-state straps at the shipment are DS0 and IU.

(Fig.110) Shipping straps

TEAC FD-54
MINI FLEXIBLE DISK DRIVE
MAINTENANCE MANUAL

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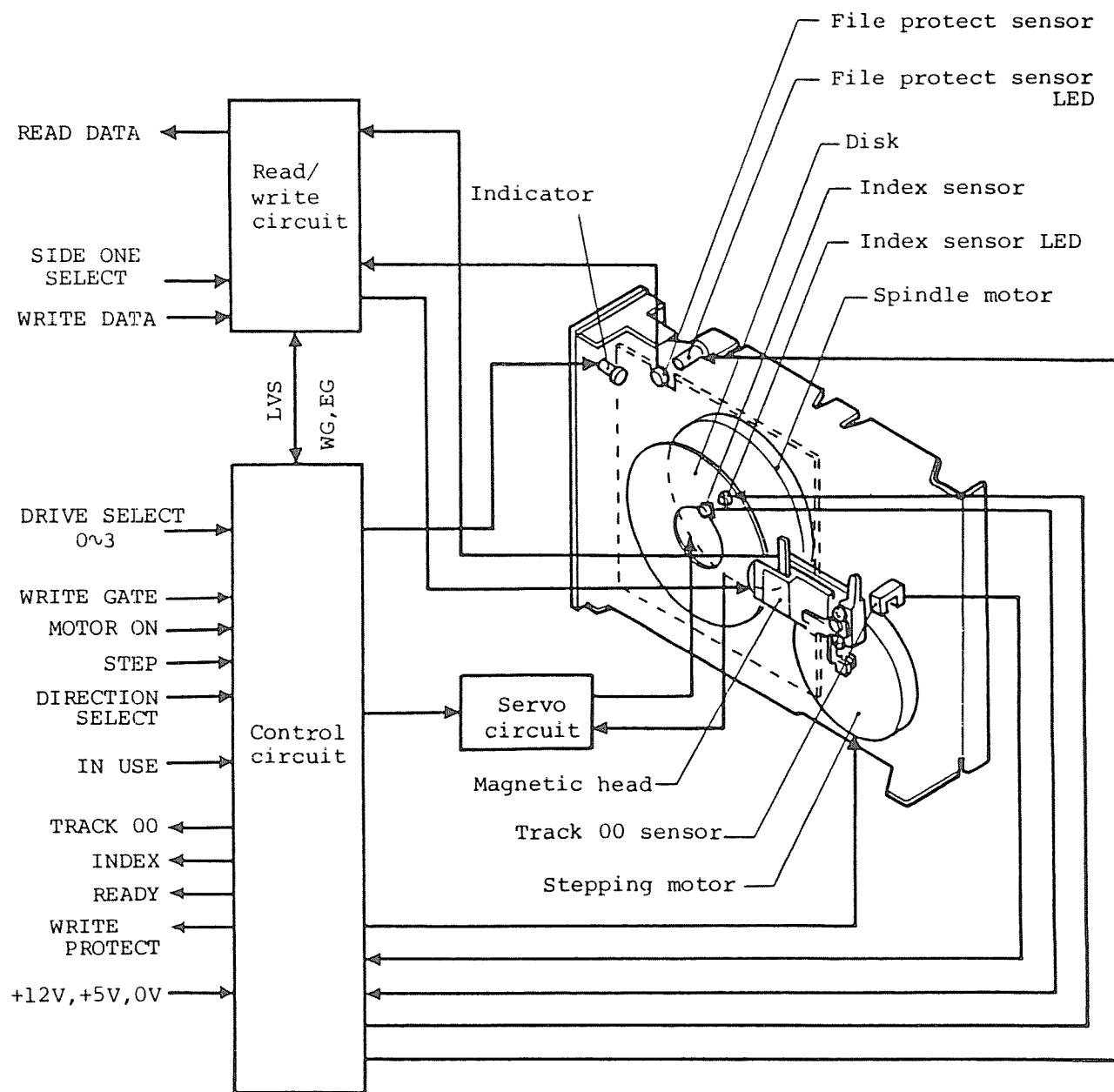
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SECTION 3

THEORY OF OPERATION

3-1. CONSTRUCTION AND FUNCTION

3-1-1. General Block Diagram



(Fig.301) General block diagram

3-1-2. Mechanical Section

Since the disk is a flexible recording media made of mylar film base and data interchangeability between disks and FDDs is required, the mechanical section of the FDD uses precision parts and it is also assembled with high precision. For this reason, only trained technicians can handle the internal mechanism. Never apply excessive impact nor drop the FDD down on the desk.

The mechanical section is constructed with frame (chassis), door mechanism, disk clamp mechanism, disk rotation mechanism, magnetic head and carriage, head seek mechanism, various detection mechanisms, etc.

(1) Frame (chassis)

The main structure for mounting the various mechanisms and printed circuit boards. The frame is made of sheet metal to maintain the stability of the FDD in strength, precision, durability, and expansion coefficient.

(2) Door mechanism and disk clamp mechanism

The door mechanism is constructed with clamp spring (plate spring), front lever, set arm, etc. The end of the clamp spring makes the disk clamp mechanism (collet Ass'y) move up and down.

When a disk is inserted and the front lever is closed, the tip of the collet is inserted in the central window of the disk and the window area is depressed to the spindle so that the center of the disk is clamped in the correct position along the outer circumference of the collet.

(3) Disk rotation mechanism

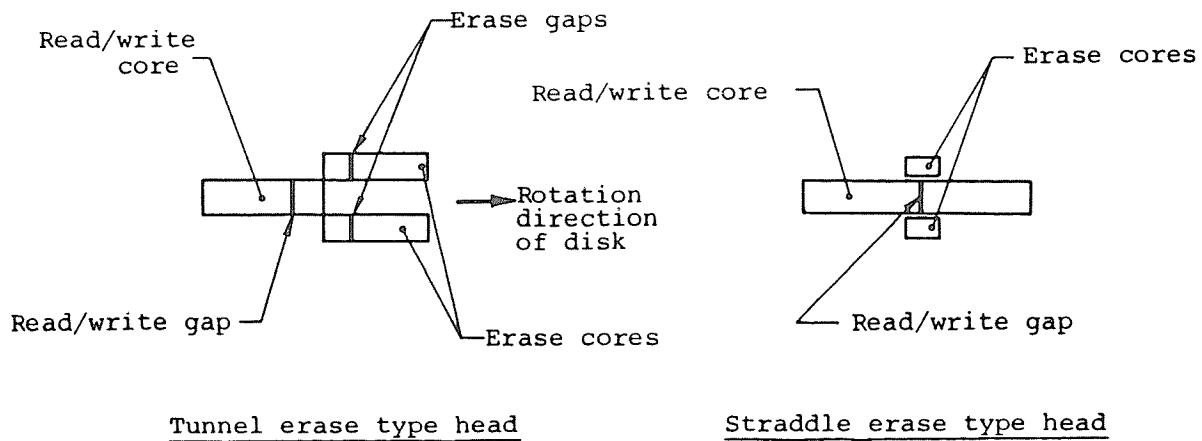
The disk rotation mechanism comprises DD motor Ass'y which includes spindle.

The DD motor is an outer-rotor type DC brushless motor which has the long life of 20,000 hours or more in continuous rotation.

The rotational speed is 300rpm and maintains stable rotational speed against load variations and environmental changes. This is achieved by a feedback signal from the internal AC tachometer.

The precisely combined collet and spindle are attached at the correct angle to maintain the center position correctly without damaging the center hole of the disk and so as to make the head be in contact with disk at the correct angle.

(4) Magnetic head and carriage



(Fig.302) External view of magnetic head core

For single sided FDDs, the external view of the magnetic head is button shaped and it is mounted on the carriage so that it is in contact with the SIDE 0 (the bottom side when the FDD is placed horizontally) head window area of the disk.

For double sided FDDs, both the SIDE 1 head and the SIDE 0 head are special flat type supported with the gimballed mechanisms. The two magnetic heads are mounted across the disk on one carriage.

In both types of head, the surface is designed for minimum disk wear and maximum read output. The head itself is a long life type for

improved head wear.

For the FD-54 drives, either of tunnel erase type head or straddle erase type head is used. The core of the tunnel erase type head is constructed with a read/write gap which is used for data write and data read operations and two erase gaps which are used to erase the edges of the recorded track immediately after the recording (tunnel erase). For the straddle erase type head, the core is constructed with a read/write gap and two erase cores for erasing the edges of the recorded track at the same time with the recording.

Even though the core construction of these two types of head are different, their functions in the FD-54 drives are the same and have complete interchangeability between the data recorded on the disks. The magnetic head and the carriage on which the head is mounted form the most important part of the FDD and is specially assembled with high precision.

(5) Head seek mechanism

The head seek mechanism consists mainly of stepper motor with a capstan (polly), steel belt (band), guide shafts, and carriage. The carriage is connected to the capstan of the stepping motor through the steel belt and is slided along the guide shafts. The flat type 4-phase stepping motor is adopted and it rotates 2 steps (3.6°) per one track space. The stepper motor is driven in a unique 1-2 phase driving method which brought a success in reducing the heat radiation and to obtain a high speed driving and positioning accuracy. The parallelism and the distance between the shafts and the center line of the disk, and shaft and disk themselves are precisely machined. Also the thermal expansion of the chassis, steel belt, carriage, etc. are taken into consideration in the process of design so that they are mutually offset with the expansion of the disk.

(6) Detection mechanisms

(a) File protect detection mechanism

This mechanism is constructed with an LED and a photo-transistor to detect the existence of the write enable notch of the disk jacket. When a disk with the notch covered is installed and the light pass for detection is disturbed, no write or erase current will be supplied to the read/write and erase heads and the recorded information on the disk is protected from an erroneous input of a write command. The LED is mounted on the PCBA DD motor servo and the photo-transistor on the front OPT Ass'y.

(b) Track 00 detection mechanism

This mechanism is constructed with a photo-interrupter for detecting the outermost track position (track 00) of the head and the track 00 stopper which is attached to the rear side of the head carriage. Inside tracks from the track 00 on the disk are used. Even if an erroneous step out command is input from the track 00 position, the command will be ignored by the internal circuit of the FDD. If the head moves out from the track 00 by some reason (such as impact during transportation), the head carriage strikes the track 00 stopper to protect the head from moving out of the returnable range at a next power on.

When step-in commands are input from the innermost track, the head seeks toward inward and stops with an appropriate space left against the head window edge of the disk. In order to recalibrate the track from this position (returning operation to the track 00), it is required to input the step-out commands with several additional steps to the maximum track number.

(c) Index detection mechanism

LED and photo-transistor for the detection of the index hole are

located at the index window area of the disk jacket.

The LED is mounted on the PCBA DD motor servo and the photo-transistor on the front OPT Ass'y. The index hole will be detected along the rotation of the disk.

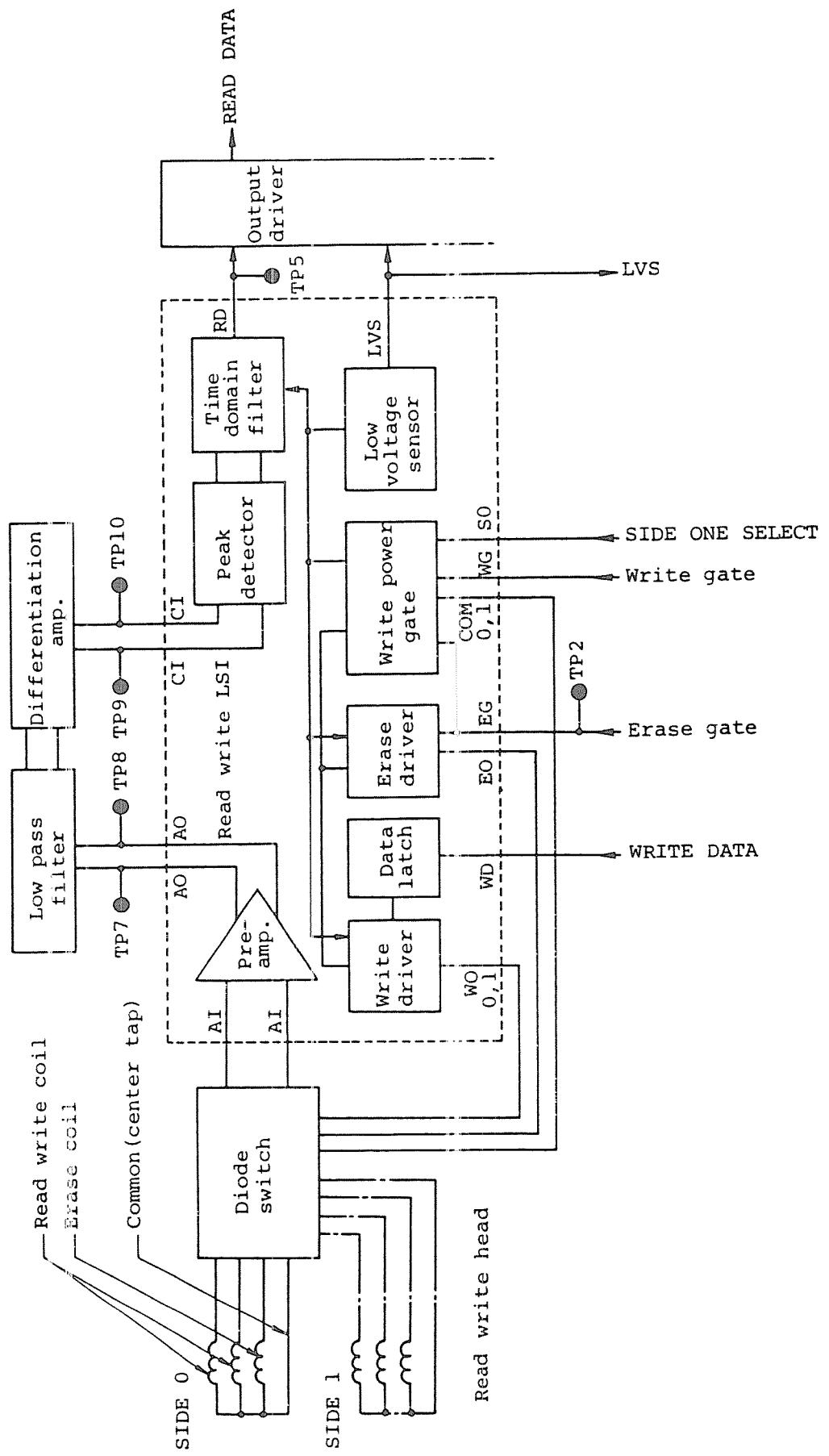
3-2. CIRCUIT DESCRIPTIONS

The electronics of the FDD is constructed with three sections which are read write circuit, control circuit, and servo circuit. Read write circuit and control circuit are mounted on the PCBA MFD control, and servo circuit is on the PCBA DD motor servo.

3-2-1. Read Write Circuit

The read write circuit is constructed with read circuit, write circuit, and low voltage sensor. They are mostly packed in a read write LSI (bipolar).

Fig.303 shows the block diagram.



(Fig. 303) Read write circuit block diagram

(1) Read circuit

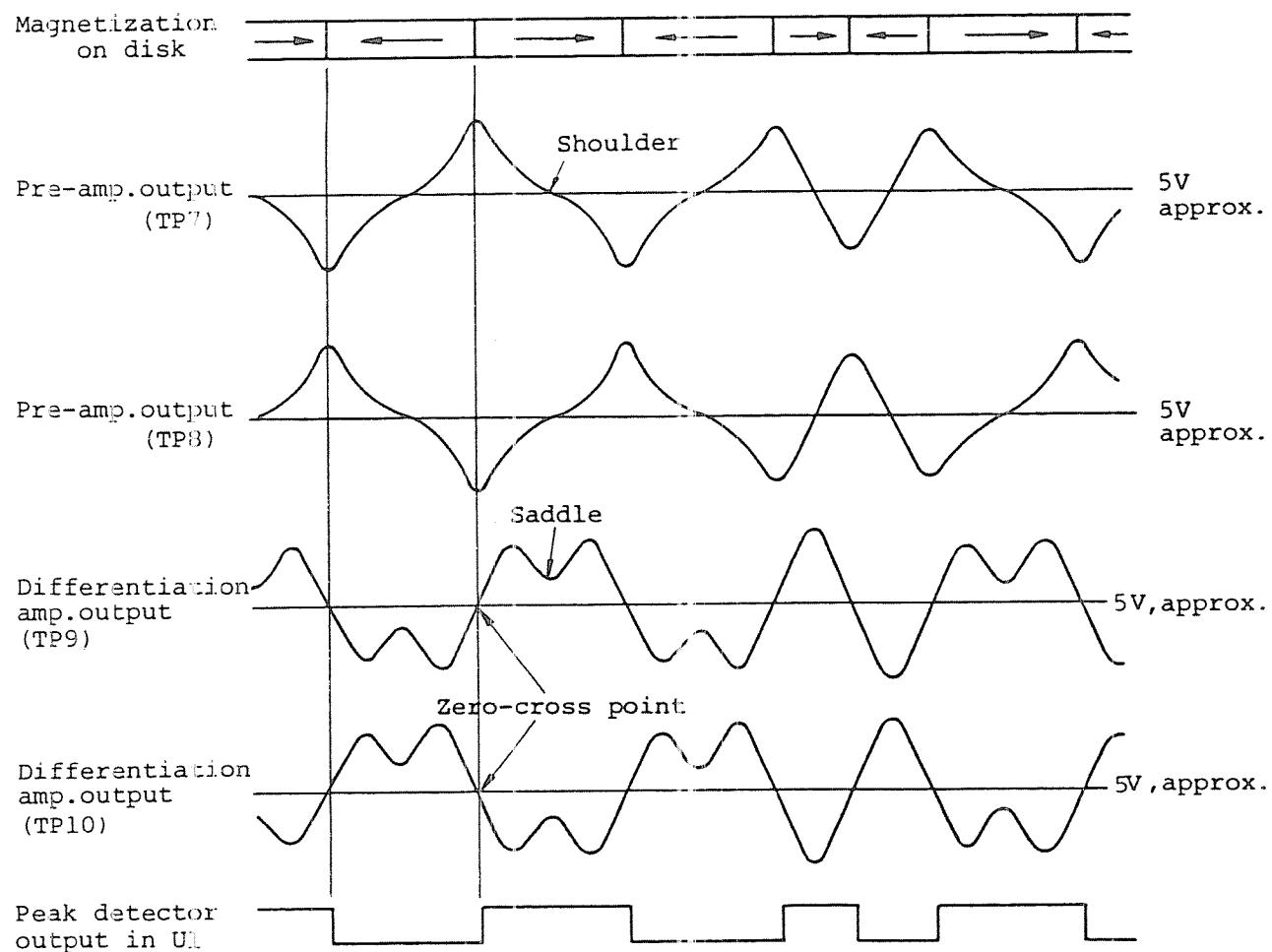
The read circuit consists of pre-amplifier, low pass filter, differentiation amplifier, peak detector, time domain filter and read gate (output driver).

In read operation, the minute voltage induced by the read/write head is amplified about 30dB by the pre-amplifier which is constructed with a video band differential amplifier. Undesirable high frequency noise is eliminated by the low pass filter (L1, L2, C30, etc.) and the read signal is supplied to the differentiation amplifier (Q3, Q4, L3, C35, etc.).

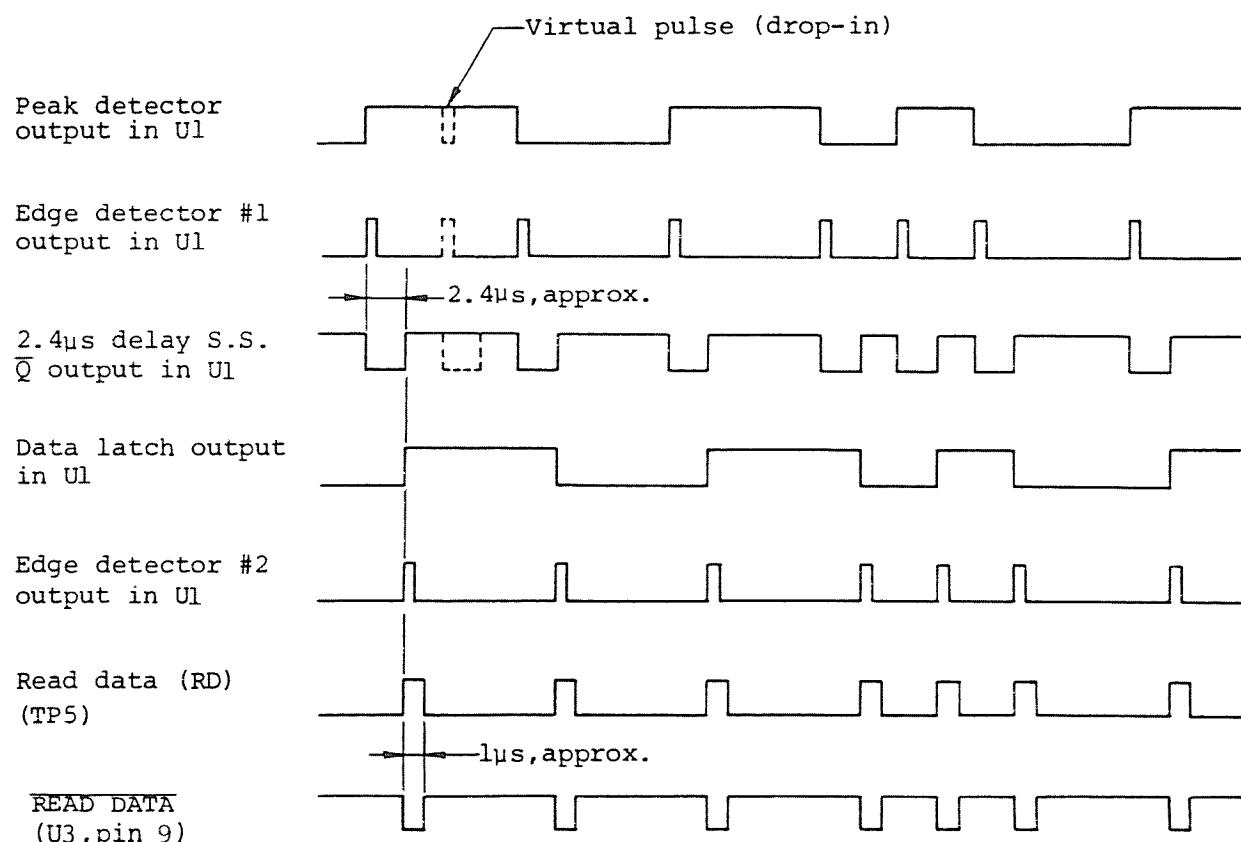
The differentiation amplifier phase-shifts the peak position of the reproduced waveform to the zero cross point, and at the same time, further amplifies the signal about 20dB with the most appropriate equalization. The peak detector which is constructed with a comparator converts the differentiated output into a square wave.

The time domain filter eliminates a virtual pulse caused by the saddle in the low frequency area (1F area, 62.5KHz, approx.) at outer tracks. The time domain filter is constructed with two edge detectors, 2.4 μ sec, delay single shot (LSI pin 7, RA5, C21), data latch, and 1 μ sec data single shot (LSI pins 8 and 9, RA5, C22).

Then the signal is output from the FDD through the read gate, U3 (pins 9, 10, 3-state output driver).



(Fig.304) Read amp. and peak detector waveforms



(Fig. 305) Time domain filter and read gate waveforms

(2) Write circuit

The write circuit consists of write power gate (with side selector), select gate, data latch, write driver, and erase driver.

The write power gate output (COM0 or COM1) becomes high voltage when the write gate signal or the erase gate signal is TRUE (HIGH level). These signals are generated by the write/erase gate in the control circuit when all of the following three conditions are satisfied.

- (a) The file protect sensor detects the notch of the disk jacket (write enable condition).
- (b) The WRITE GATE input signal is TRUE.
- (c) MX strap is on or the DRIVE SELECT signal is TRUE (LOW).

The write power gate output is supplied to the common terminal of the head through the diode switch. Table 301 shows the output voltage of the write power gate in various operations.

Conditions	Write power gate output voltage	
	COM 0 (for Side 0)	COM 1 (for Side 1)
Side 0 write operation	High	Low
Side 1 write operation	Low	High
Side 0 read operation	Middle	Low
Side 1 read operation	Low	Middle

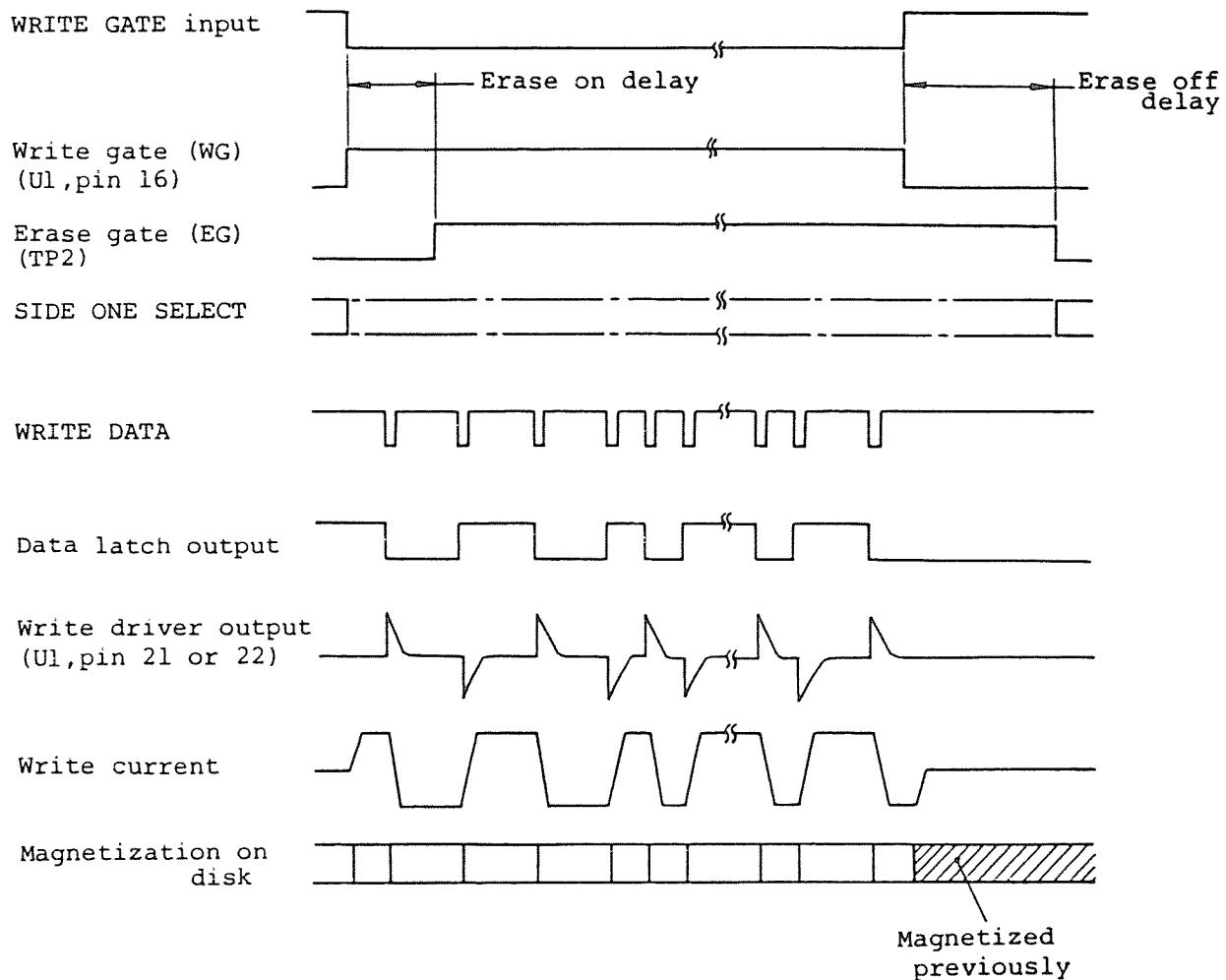
High: 10.5V, approx. Middle: 4V, approx. Low: 0V, approx.

(Table 301) Write power gate output voltage

For the tunnel erase head, the erase gate signal is delayed appropriately against the write gate signal. Since the erase gap is about 0.85mm behind the read/write gap, it is necessary for the erase driver to delay the write gate signal so that the written data is completely trimmed by the erase head (tunnel erase).

For the straddle erase head, the write gate and the erase gate signals have the same timing. The tunnel erase or the straddle erase produces a guard band between the tracks preventing deterioration of the S/N ratio resulting from a off-track (positioning error). It also ensures disk interchangeability.

The WRITE DATA input pulse is latched by the data latch. And appropriate write current is supplied to the read/write head by turning on and off the two write drivers alternately. When the write driver is active, no read data pulse is generated by the read circuit.

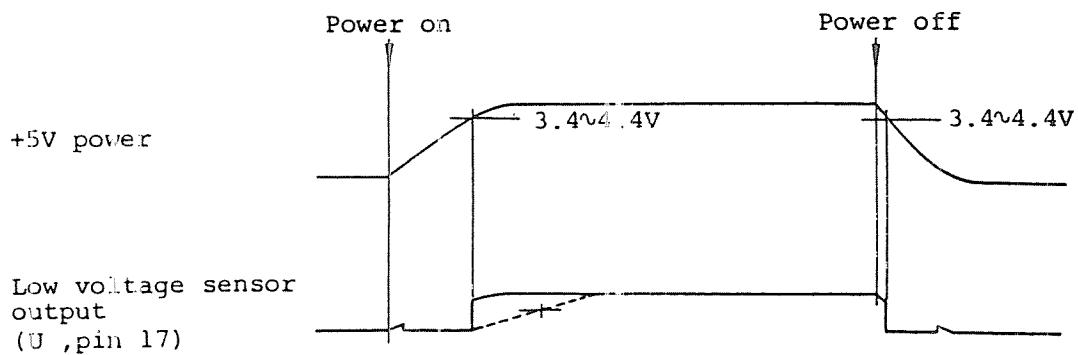


Note: Solid line of the Erase gate (EG) signal shows the tunnel erase type and dotted line shows the straddle erase type. Erase on delay and Erase off delay are applied only for the tunnel erase type.

(Fig.306) Write circuit waveforms

(3) Low voltage sensor

The low voltage sensor is equipped to protect the FDD from erroneous operation due to the internal circuit construction of the FDD during unstable condition of the supplied voltage such as at power on or off. The output of this sensor is supplied to almost all the functional blocks of the read write circuit, and control circuit to protect the write driver and erase driver from erroneous operation under the unstable condition of the DC power voltage.



Note: Dotted line shows the LVS input pin 34 of U2, control LSI.

(Fig.307) Low voltage sensor waveforms

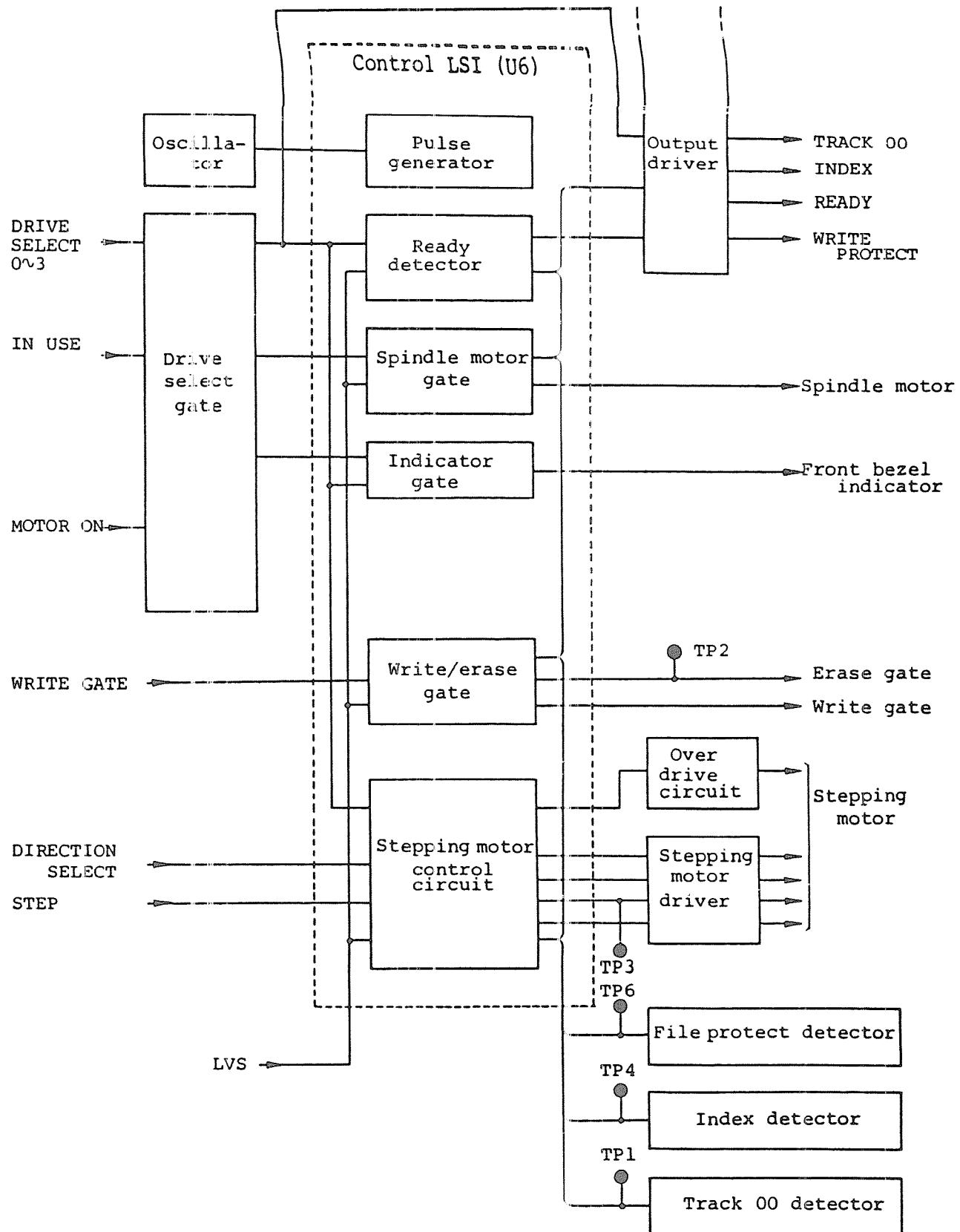
3-2-2. Control Circuit

The control circuit consists of gates, detectors, and the stepping motor control circuit. The gates are drive select gate to determine the drive select condition, spindle motor gate to determine the rotational condition of the spindle motor, write/erase gate to control the actual write operation, etc. The detectors are index/sector detector, track 00 detector, file protect detector, and ready detector. The former three detectors (photo-transistors) are mounted on the front OPT Ass'y and the transport frame. And the other circuits are mounted on the PCBA MFD control (mostly packed in a control LSI (CMOS)). Fig.308 shows the block diagram.

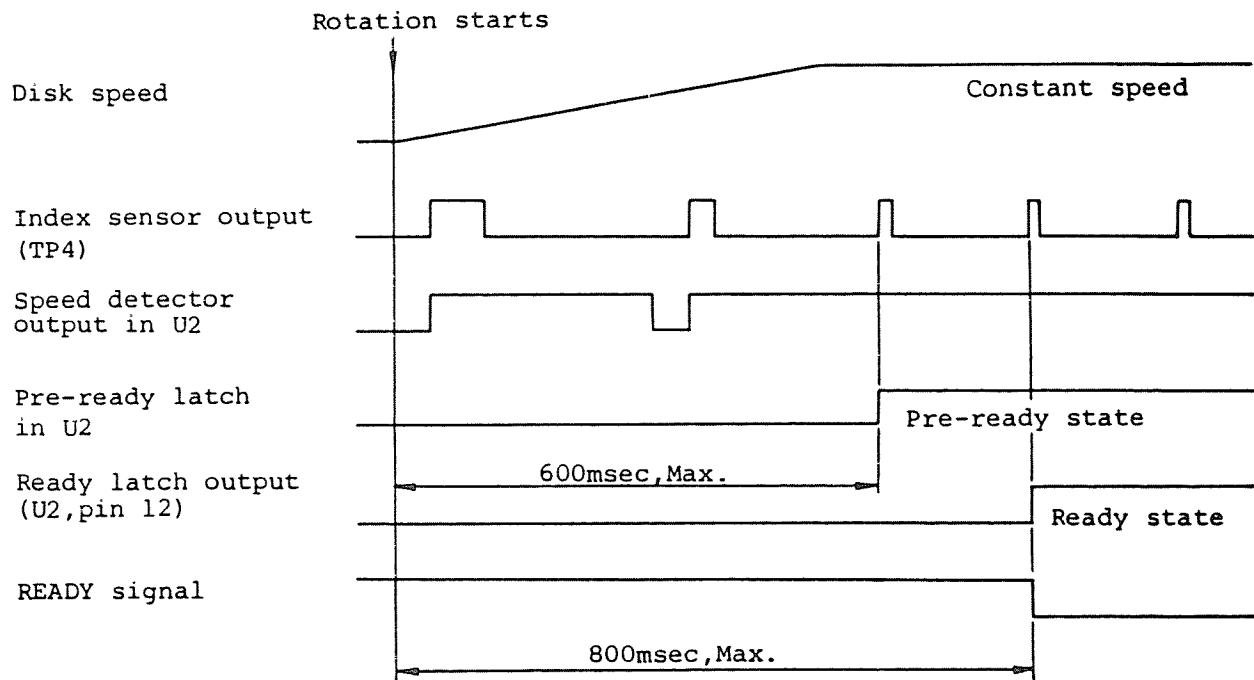
Drive select gate classifies the external input signals into several functions and transmits them into the control LSI. The selection of straps (short bars) determines the select condition of the drive, spindle motor operating conditions, and turn-on condition of the front bezel indicator. Refer to items 1-11 of the Specification as to the detailed function of each strap.

The write/erase gate judges the FDD whether it can execute write operation or not and issues write gate and erase gate signals for the write circuit. For the FDD with tunnel erase head, a specified delay time is established in the erase gate signal by an internal counter (refer to Fig.306).

The ready detector consists of speed detector and ready latch. The output of the speed detector which is constructed with a re-triggerable counter becomes always TRUE (HIGH) when the rotational speed of an installed disk (soft sectored) is more than 50%, approx. of the rated speed. The ready latch detects the second index pulse after the speed detector detects the 50% of the rated speed, then the READY condition is informed to the host system through the output driver, U7 (pin 13 ~ 14).



(Fig.308) Control circuit block diagram



(Fig.309) Ready detector waveforms

Stepping motor control circuit is constructed with direction latch, internal step pulse generator, shift register, phase drive selector, overdrive timer, etc.

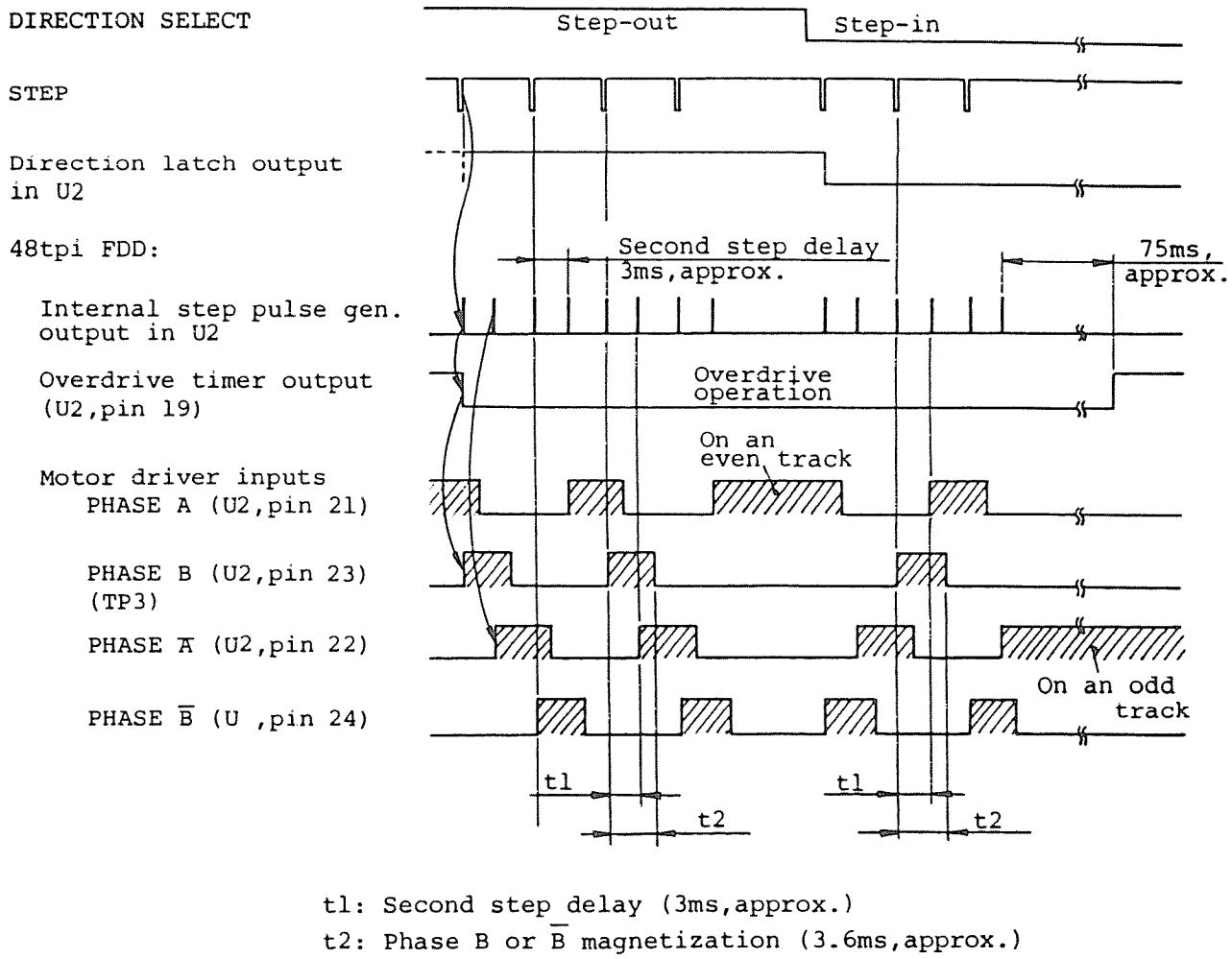
Direction latch is a circuit to sample and hold the head seek direction designated by the DIRECTION SELECT signal at every input of the STEP pulses.

The internal step pulse generator is constructed with a counter and a pulse generator. The counter is triggered at the trailing edge of the STEP input pulse, and the second internal step pulse is generated with a delay of 3msec, approx. from each STEP input pulse by the pulse generator. It makes the stepping motor rotate for 2 steps (3.6°) in response to one STEP input pulse.

Outputs of the direction latch and the internal step pulse generator are input to the shift register and phase drive selector, and they are converted to the appropriate timing signals for uni-polar 1-2 phase drive of the 4-phase stepping motor. These phase drive signals are supplied to the stepping motor driver, U5 (output pins 12 ~ 15). In order to improve the torque margin in the seek operation, partially 2-phase drive period is provided by the phase drive selector only in the initial stage when the drive phase is changed.

When the head stops on an even track, phase A is magnetized, while phase \bar{A} is magnetized when the head stops on an odd track. The phase B and \bar{B} are magnetized only during the seek operation.

The output from the internal step pulse generator is also supplied to the over-drive timer constructed with a re-triggerable counter. During the active period of this timer (75msec, approx.), +12V power is supplied to the stepping motor coils through the over-drive circuit (Q1) to produce enough torque required for the head seek and the settling operations. After the completion of the settling, only +5V power is supplied to the stepping motor through the diode, CR1, which minimize the power loss by supplying only the required torque for the holding of the stop position. By the above consideration, heat radiation from the motor is depressed to the minimum level and the stepping motor power consumption of 0.33W, approx. at the stop condition is achieved.



(Fig.310) Stepping motor control circuit waveforms

3-2-3. Servo Circuit

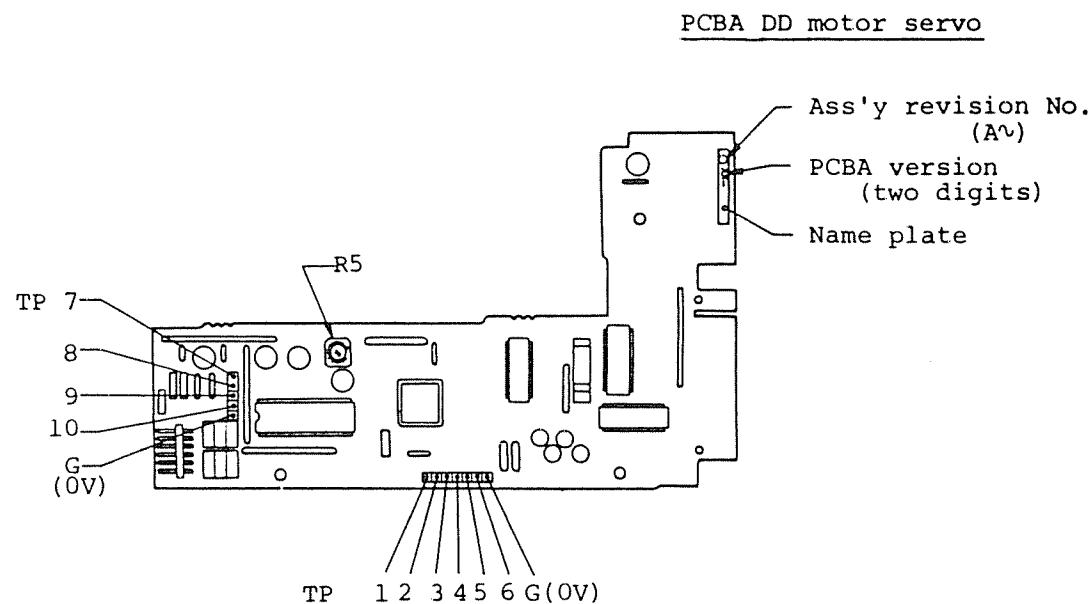
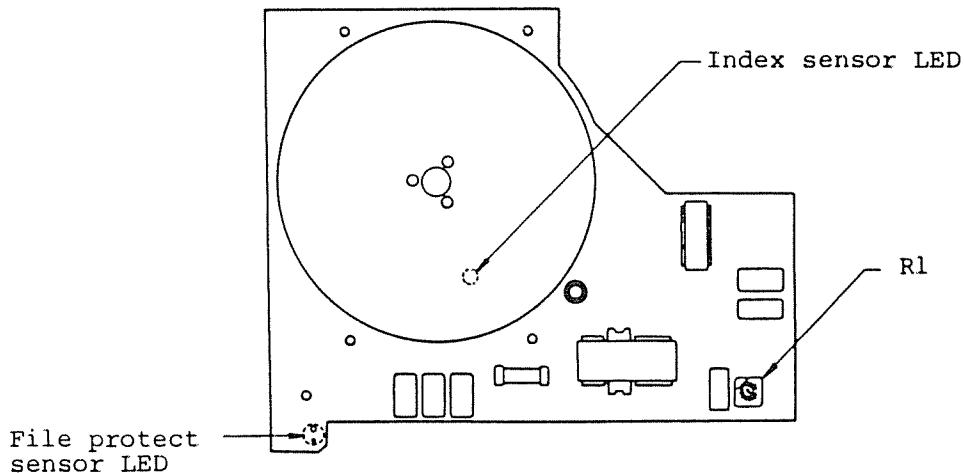
The servo circuit aims to maintain the rotational speed of the spindle motor at 300rpm, and the circuit is mounted on the PCBA assembled with the spindle motor.

Start and stop of the spindle motor (DD motor Ass'y) is controlled by the MOTOR ON signal supplied through the spindle motor gate in the control circuit.

The spindle motor is a long life DC brushless motor having 3-phase coils. The coils are driven by the exclusive drive IC. Energization and magnetized direction of the coils are controlled by the signal from the hall elements mounted on the PCBA around the rotor so that they are changed corresponding to the designated rotational direction. The rotational speed is maintained stably and precisely. The feedback signal from the AC tacho-meter in the rotor is converted into the drive voltage (F-V conversion) by servo IC, and supplied to the driver IC through the phase compensation circuit.

3-3. FUNCTION OF TEST POINTS AND VARIABLE RESISTORS

Fig.311 shows the mounting positions of the test points and variable resistors.



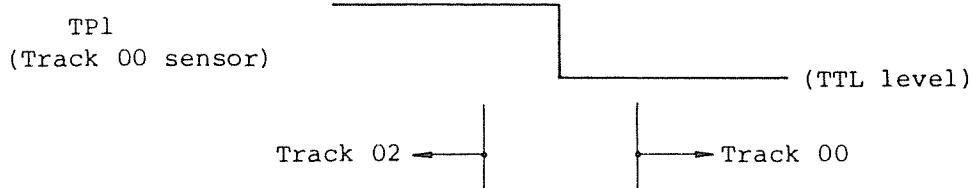
(Fig.311) Location of test points and variable resistors

3-3-1. Function of Test Points

Twelve test points (two for ground) are equipped on the PCBA MFD control for the check and adjustment of the FDD.

(1) TP1 (Track 00 sensor)

Test point to observe the output of the track 00 detection phototransistor (shumitt inverter included). As well as TRACK 00 output signal, TP1 becomes LOW level when the head is on track 00 or around track 00 position.

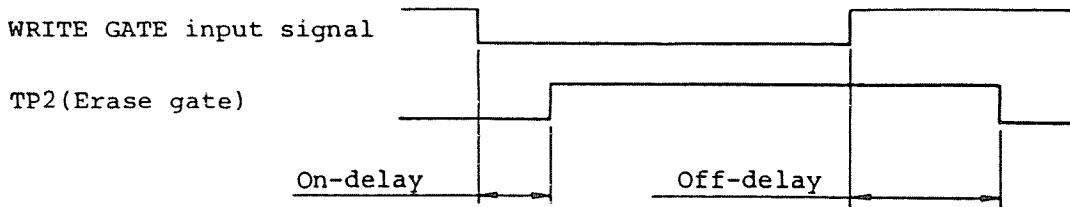


(Fig.312) Typical waveform of TP1

Note: The TRACK 00 output signal goes TRUE (LOW level) only when the phase A coil of the stepper motor is energized and the direction latch is set to the step-out direction (refer to Fig.310). Therefore, the level change timing of the TRACK 00 signal is not consistent with that of the TP1 signal.

(2) TP2 (Erase gate)

Test point to observe the output of the erase gate. When TP2 is HIGH level, erase current flows through the erase head. This TP is used for the check and adjustment of the required delay time of the erase gate signal against the WRITE GATE input signal when the tunnel erase head is used.



(Fig.313) Typical waveform of TP2(for tunnel erase head)

Delay	Straddle erase head	Tunnel erase head
On-delay	0μs	200 ~ 320μs
Off-delay	0μs	860 ~ 950μs

(Table 302) Erase gate delay

(3) TP3 (Phase B)

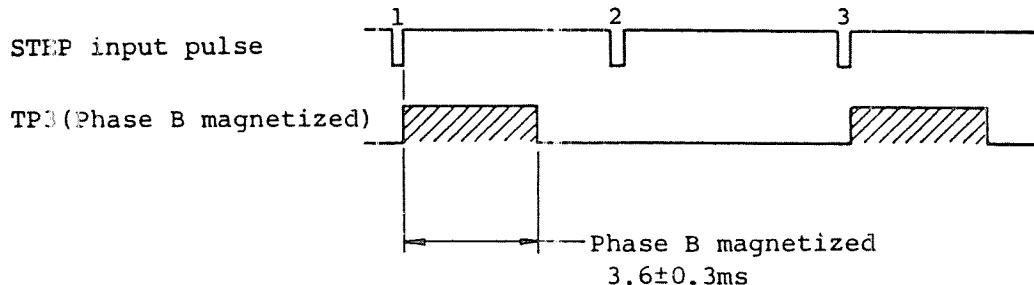
Test point to observe the phase B magnetized period of the stepping motor.

The stepping motor rotates for 2-steps in response to one STEP input pulse. Therefore, TP3 becomes HIGH level for a specified period when a step-out command from an even track or when a step-in command from an odd track is executed. Refer to Fig.310.

(4) TP4 (Index)

Test point to observe the output of the index detection photo-transistor (shumitt inverter included).

The signal level at this TP is opposite to that of INDEX output signal. When the index hole or sector hole (hard sectored disk) is detected, HIGH going pulse is observed at TP4. The photo-transistor is mounted on the front OPT Ass'y and the LED is mounted on the back side of the

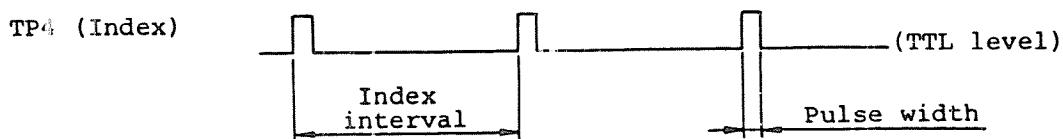


(Fig.314) Typical waveform of TP3

PCBA DD motor servo.

The test point is used for the following purposes.

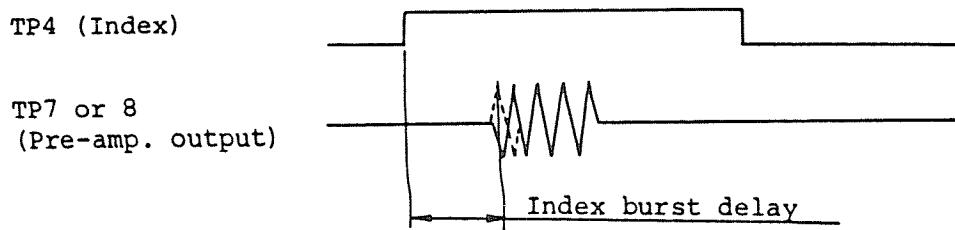
- (a) Confirmation and adjustment of the disk rotational speed. Speed is adjusted by the variable resistor R1 on the PCBA DD motor servo.
- (b) Confirmation and adjustment of the index burst timing. Burst timing is adjusted by the index sensor installation screw in the front OPT Assembly



(Fig.315) Typical waveform of TP4 (Speed observation)

Items	Timing
Index interval	200±4ms
Pulse width	2 ~ 5.5ms
Burst delay	200±200μs

(Table 303) Index timing

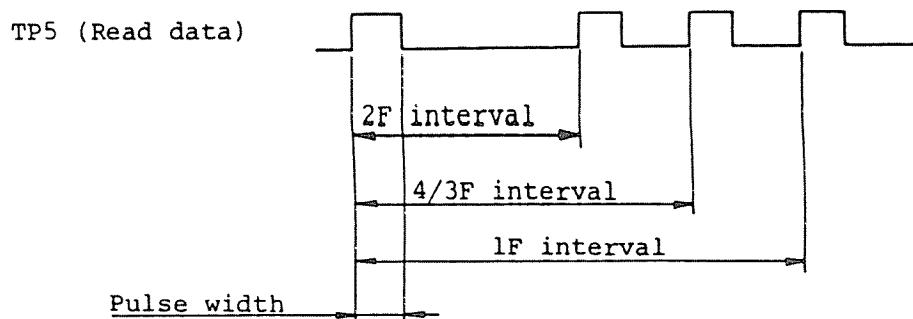


(Fig.316) Typical waveform of TP4 (Burst timing observation)

(5) TP5 (Read data)

Test point to observe the read data pulse.

The signal level at this TP is opposite to that of the READ DATA output signal.



(Fig.317) Typical waveform of TP5

Fig.317 shows the waveform at TP5 in normal data read operation.

In the FM method, 2F and 1F intervals are observed, while 2F, 4/3F, and 1F intervals are observed in the MFM method.

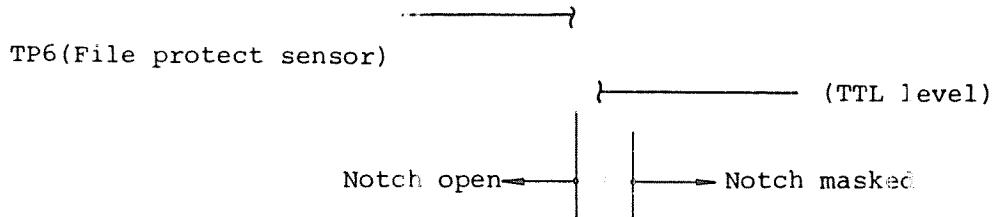
Items	Timing
2F interval	4 μ s, Nom.
4/3F interval	6 μ s, Nom.
1F interval	8 μ s, Nom.
Pulse width	1±0.5 μ s

(Table 304) Read data pulse timing

(6) TP6 (File protect sensor)

Test point to observe the output of the file protect detection photo-transistor (shumitt inverter included).

As well as the WRITE PROTECT output signal, TP6 becomes LOW level when a disk with the masked write protect notch (write operation cannot be done) is installed.



(Fig.318) Typical waveform of TP6

(7) TP7, TP8 (Pre-amplifier)

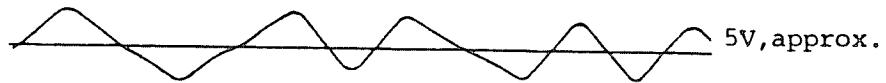
Test point to observe the read pre-amplifier output signals.

The pre-amplifier has two outputs of the order of several dozen to several hundred mVp-p, and they differ in phase by 180° (opposite phase). Both outputs are observed at TP7 and TP8 respectively.

For an accurate observation of the read waveforms, use two channels of an oscilloscope with one channel set to Invert mode and Add mode of both channels. Use G (0V) test point for the oscilloscope ground.

TP7 and TP8 are used for checking various characteristics of the read/write head and also for the check and adjustment of the head seek mechanism such as track alignment.

TP7,TP8
(Pre-amp.)



(Fig.319) Typical waveform of TP7 and TP8

(8) TP9, TP10 (Differentiation amplifier)

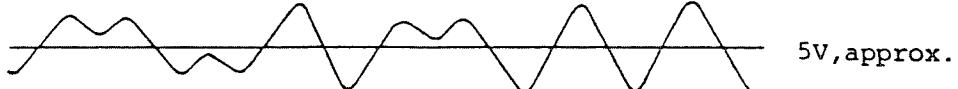
Test points to observe the differentiation amplifier output signals. Like the pre-amplifier, the differentiation amplifier also has two outputs of the order of several hundred mVp-p to several Vp-p which differ in phase by 180°. Both outputs are observed at TP9 and TP10 respectively.

For an accurate observation of the waveforms, use two channels of the oscilloscope with one channel set to Invert mode and Add mode of both channels.

Use G (0V) test point for the oscilloscope ground.

TP9 and TP10 are used for checking the total operation of the read/write head and the read amplifier and for the check and adjustment of the head seek mechanism such as track alignment.

TP9,TP10
(Differentiation
amp.)



(Fig.320) Typical waveform of TP9 and TP10

(9) TP G (0V) -- PCBA MFD control, PCBA read write amp.

TP G is equipped respectively for two test point blocks (TP1 ~ 6 and TP7 ~ 10). They are used as the ground terminals for measurement equipment. Be sure to use a small size clip to obtain a probe ground of the equipment.

3-3-2. Function of Variable Resistors

On the PCBA MFD control and the PCBA DD motor servo, maximum two variable resistors are mounted.

The PCBA MFD control of some PCBA versions and some revision numbers has not the variable resistor R5. Also some types of DD motor Ass'y have not the variable resistor R1 on the PCBA DD motor servo.

However, there is interchangeability in function and performance between these PCBAs with the variable resistor and without the variable resistor as far as they have the same parts number (8 digits) and the same version number (2 digits).

The variable resistors are correctly adjusted before the shipment of the FDD and fundamentally they shall not be readjusted except for by a trained technicians.

(1) R1 on PCBA DD motor servo (Disk rotational speed adjustment)

Variable resistor for adjusting the rotational speed of the disk.

It is adjusted so that the index pulse interval at TP4 or at the INDEX output signal is $200\text{msec} \pm 4\text{msec}$ (see Fig.315).

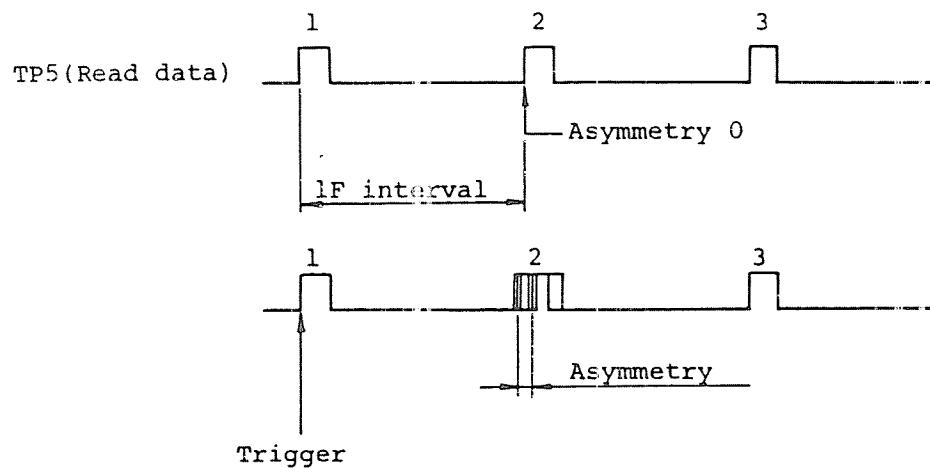
For the DD motor Ass'y without the variable resistor R1, the rotation speed of the motor is fixed by the ceramic oscillator in the servo circuit and no adjustment is required.

(2) R5 on PCBA MFD control (Read data asymmetry adjustment)

Variable resistor for adjusting the asymmetry of the read data pulse. Some PCBAs have this variable resistor and others have fixed resistor instead of it.

For a PCBA with the variable resistor, R5, write 1F data and observe the pulse intervals at TP5 or at the READ DATA output signal during read operation. Then adjust the variable resistor so that the read data asymmetry in Fig.321 takes the minimum value. For a double sided FDD, repeat this operation alternately for side 0 and side 1 heads to

obtain the minimum asymmetry for both sides.



(Fig.321) Read data asymmetry

SECTION 4

MAINTENANCE

4-1. GENERAL

4-1-1. Periodic Maintenance

The FDD is designed to be free from periodic maintenance such as replacement of parts, grease-up, etc. when it is operated at a normal operation duty.

However, cleaning of the magnetic head using a cleaning disk is recommended since it is effective to improve the reliability of the data. If some of the parts in the FDD are operated at a specially heavy duty condition, or if the FDD is operated over 5 years, it is recommended to replace the wear parts according to Table 403.

Periodic maintenance items	Recommended cycle	Required time	Referred items
Cleaning of magnetic head	Refer to 4-3-1 and 4-3-2	5 min.	4-3-1
Replacement of wear parts	Refer to 4-1-3 and 4-5.		

(Table 401) Periodic maintenance items

4-1-2. Check and Adjustment

Table 402 shows all of the check and adjustment items.

Following items do not require periodic maintenance. Check and adjustment should be done when required during replacement of the maintenance parts or during trouble shooting referring to items 4-2 and 4-3.

The numbered procedure in Table 402 shows a typical procedure of the general check and adjustment all over the FDD.

Steps	Check and adjustment items	Required time	Referred items
1	Adjustment of collet shaft plate	5 minutes	4-4-1
2	Adjustment of front lever position	5 minutes	4-4-2
3	Check and adjustment of disk pad lever (bail) (double sided only)	5 minutes	4-4-3
4	Check of file protect sensor	5 minutes	4-4-4
5	Check and adjustment of disk rotation speed	5 minutes	4-4-5
6	Check and adjustment of head touch	5 minutes	4-4-6
7	Check and adjustment of asymmetry	5 minutes	4-4-7
8	Check of read level	5 minutes	4-4-8
9	Check of resolution	5 minutes	4-4-9
10	Check and adjustment of track alignment	10 minutes	4-4-10
11	Check and adjustment of track 00 sensor	5 minutes	4-4-11
12	Check and adjustment of track 00 stopper	5 minutes	4-4-12
13	Check and adjustment of index burst timing	5 minutes	4-4-13

(Table 402) Check and adjustment items

4-1-3. Maintenance Parts Replacement

It is recommended to replace the wear parts periodically if the FDD is operated at a specially heavy duty condition or if it is operated over five years. Periodic replacement is not required for the parts if the FDD is operated at a normal operation duty.

Table 403 shows all of the maintenance parts. Replace the wear parts according to the recommended replacement cycle. Periodic replacement is not required for parts without a recommended replacement cycle.

The replacement of the parts should be done according to each referred item in Table 403.

Notes for Table 403:

- (1) Since the parts number versions of PCBA MFD control (C) vary depending on some factors such as signal interface condition, be sure to confirm the version by checking the name plate on the actual printed circuit board.
- (2) The head carriage Ass'y are used always in pair with two guide shafts. The head carriage Ass'y represented by listed parts number in Table 403 includes these guide shafts which parts number is different from that of a head carriage Ass'y itself without these guide shafts.
- (3) The listed parts numbers of the front bezel Ass'y and front lever Ass'y are those of standard color (black). For designating other color, use the corresponding parts number.
- (4) Periodic replacement is not required for parts without a recommended replacement cycle. Replace the parts when required such as during repair.
- (5) If two recommended cycles are listed, the cycle which the parts reach first should have priority.

- (6) The required time for replacement includes the time for basic check and adjustment after the replacement.
- (7) Order the maintenance parts using the parts number.

(Table 403-1) FD-54A (single sided, 48tpi) Maintenance parts list

Maintenance parts			Replacement		
Parts name	Description	Parts No.	Replacement cycle	Required time	Referred items
Head carriage Ass'y (C) (For spare parts)	Note (2)	17966930-00	7,000 head load & motor on hrs. or 5x10 ⁶ seeks	45 min.	4-5-1
Stepping motor Ass'y (C)		14733730-00	5x10 ⁶ seeks	30 min.	4-5-2
Steel belt (C)		16792300-00	Replace with stepping motor Assy	-	4-5-2
DD motor Ass'y (C) (Spindle motor)		14733780-00	20,000 motor on hrs.	20 min.	4-5-3
Collet Ass'y (C)		17966923-00	3x10 ⁵ clamsp	15 min.	4-5-4
PCBA T00 sensor		15532004-00	-	10 min.	4-5-5
PCBA MFD control (C)		15532006-XX	-	30 min.	4-5-6
Note (1)					
Front OPT Ass'y (C)		15090730-00	-	15 min.	4-5-7
Front bezel Ass'y	Note (3)	17966807-00	-	10 min.	4-5-9
Front lever Ass'y (C)	Note (3)	17966924-00	-	5 min.	4-5-10
Pad (Head pad)		16786634-01	2,500 head load & motor on hrs.	10 min.	4-5-8
Clamp cam Ass'y (C)		17966929-00	1.5x10 ⁵ clamps	10 min.	
Eject Ass'y (C)	Option	17966926-00	1.5x10 ⁵ clamsp	10 min.	

(Table 403-2) FD-54B (Double sided, 48tpi) Maintenance parts list

Maintenance parts			Replacement		
Parts name	Description	Parts No.	Replacement cycle	Required time	Referred items
Head carriage Ass'y (C) (For spare parts)	Note (2)	17966928-00	7,000 head load & motor on hrs. or 5×10^6 seeks	45 min.	4-5-1
Stepping motor Ass'y (C)		14733730-00	5×10^6 seeks	30 min.	4-5-2
Steel belt		16792300-00	Replace with stepping motor Ass'y	-	4-5-2
DD motor Ass'y (C) (Spindle motor)		14733780-00	20,000 motor on hrs.	20 min.	4-5-3
Collet Ass'y (C)		17966923-00	3×10^5 clamps	15 min.	4-5-4
PCBA T00 sensor		15532004-00	-	10 min.	4-5-5
PCBA MFD control (C)		15532006-XX Note (1)	-	30 min.	4-5-6
Front OPT Ass'y		15090730-00	-	15 min.	4-5-7
Front bezel Ass'y	Note (3)	17966807-00	-	10 min.	4-5-9
Front lever Ass'y (C)	Note (3)	17966924-00	-	5 min.	4-5-10
CSS Ass'y		17966927-00	3×10 clampsp	10 min.	4-5-11
Clamp cam Ass'y (C)		17966929-00	1.5×10^5 clamps	10 min.	
Eject Ass'y (C)	Option	17966926-00	1.5×10^5 clamps	10 min.	

4-1-4. Maintenance Jigs and Tools

The following are the jigs and tools required for adequate maintenance of the FDD.

(1) Equipment

(A) When Simulator KA (off-line exerciser for FD-54, abbreviated to SKA) is used:

(a) SKA

The following accessories are necessary for operating the SKA (the accessories are supplied with the SKA).

- i) SKA/FDD interface cable (-00 type)
- ii) Check cable #1 (for observation of control signals)
- iii) Check cable #2 (for observation of read amp. output signals)
- iv) SKA/FDD power cable

(b) Oscilloscope (two channels)

(c) DC power supply (+12V, 1.2A and +5V, 2A) or SKA power supply.

The following accessory is required for the power supply (The accessory is supplied with the SKA power supply).

- i) Power cable (4P)

(d) Thermometer and hygrometer

(B) When SKA is not used:

- (a) FDD controller and DC power supply (user's system)
- (b) Oscilloscope (two channels)
- (c) Frequency counter

- (d) Digital volt meter
- (e) DC clip-on ammeter
- (f) Thermometer and hygrometer

(2) Tools

- (a) Cross-point screwdrivers, M2.6 and M3
- (b) Common screwdrivers, small size and medium size
- (c) Hexagon wrench key, 1.5mm
- (d) A pair of tweezers
- (e) Round nose pliers
- (f) Cutting pliers
- (g) Solder and soldering iron
- (h) Hexagon screwdriver, M3

(3) Special jigs

- (a) MAX media jig (Jig D, P/N 17890746-01)

(4) Disks

- (a) Work disk (commercially available disk)
- (b) Cleaning disk (commercially available cleaning disk)
 - i) Single sided type
 - ii) Double sided type
- (c) Level disk (P/N 14900015-00)
- (d) Alignment disk
 - i) Single sided, 48tpi type (P/N 14900016-20)
 - ii) Double sided, 48tpi type (P/N 14900016-21)

(5) Other articles used during maintenance

- (a) Absolute alcohol (Ethanol)
- (b) Cotton swab or gauze
- (c) Locking paint (3 Bond, 1401B)
- (d) Binding agent (Sumitomo Chemical, Cyano-bond SF, Red)
- (e) Screws and washers (Refer to item 5-2-2)
- (f) Lubricant (Kantoh Kasei, 946P)

Note: Be sure to use well calibrated equipment and disks.

4-2. PRECAUTIONS

4-2-1. Torque Applied to Screws and Locking Paint

The following torque should be applied to screws, unless otherwise specified.

Size of screws	Torque
M2	2kg.cm
M2.6	4.5kg.cm
M3	6kg.cm
M3 set screw	4.5kg.cm

(Table 404) Torque applied to screws

For tightening or loosening M3 set screws for adjustment and parts replacement, the following procedure should be followed.

- (1) For adjustment, remove out the set screw and also remove the locking paint which had applied to the screw itself and around it.
- (2) Apply fresh locking paint to the first three threads of the set screw with some narrow object such as a pair of tweezers.
- (3) Adjust or tighten the set screw with the specified torque.

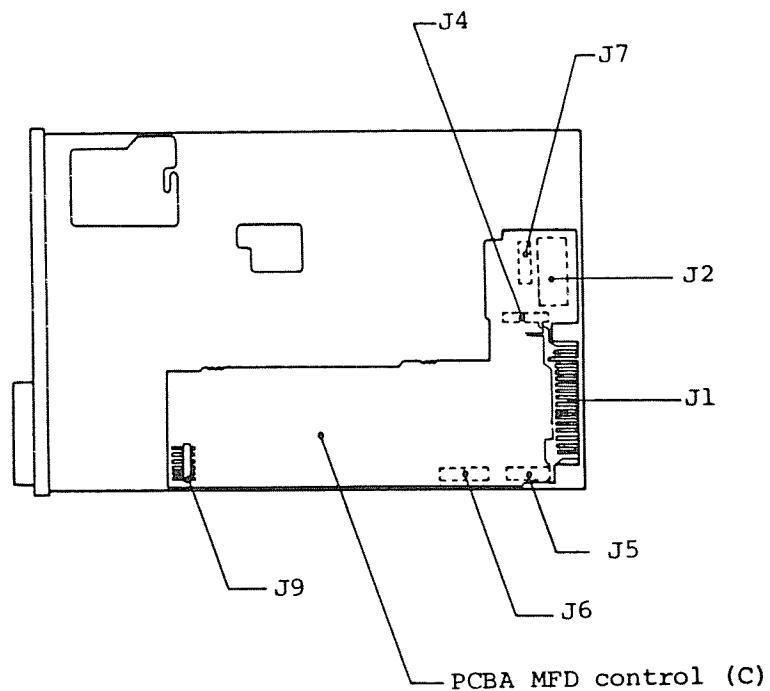
For other screws than set screws, apply a drop of locking paint to the designated points after tightening them.

4-2-2. Handling of Connectors

(1) Types of connectors

The following connectors are used for the FDD.

- (a) J1: Interface connector
- (b) J2: Power connector
- (c) J4: Track 00 connector
- (d) J5: Front OPT connector
- (e) J6: Stepping motor connector
- (f) J7: Spindle motor (DD motor Ass'y) connector
- (g) J9: Head connector



(Fig.401) Types of connectors

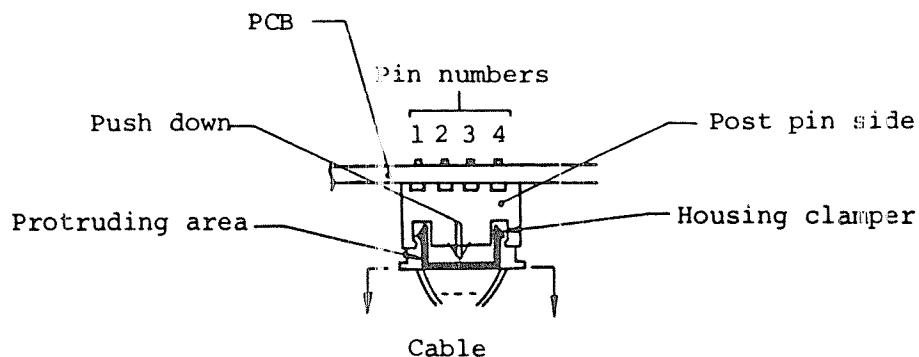
(2) Connection and disconnection of the connectors

Be sure to turn the power off before connecting and disconnecting the connectors. Connection or disconnection should be done straightly and correctly without applying excessive force to the cables and the post pins.

(3) Precautions for handling the white connectors (J4, J5, J6, J7)

(a) Disconnection of the connector

As shown in Fig.402, carefully push down the edges of the protruding area of the connector little by little with the finger nails or with a screwdriver.



(Fig.402) Disconnection of white connector

(b) Connection of the connector

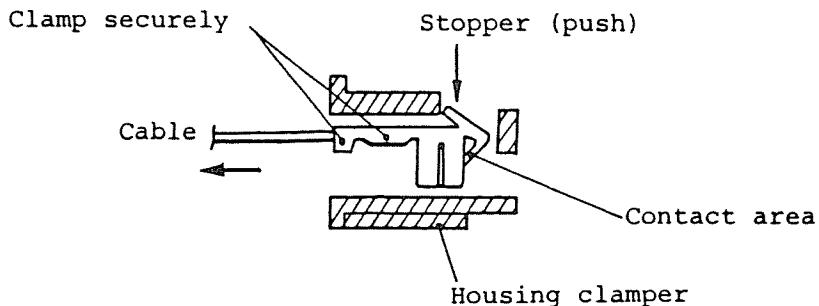
Push the connector into the post pin under the PCBA matching the housing clamper to the groove.

(c) Removal of the pin (for reference)

Refer to Fig.403.

Depressing the stopper of the pin lightly with a narrow object such

as a pair of tweezers, pull the cable in the direction indicated by the arrow.



(Fig.403) Sectional view of white connectors

(d) Insertion of the pin (for reference)

Before insertion, check the following three points.

- i) Confirm that the sheath and the core of the cable are securely clamped.
- ii) Confirm that the stopper is lifted as in Fig.403 and it inhibits accidental removal.
- iii) No tarnish or contamination should be on the contact area of the pin or the PCB side post pin. If there is, remove it.

Contact failure may happen if any of these three points is not satisfied.

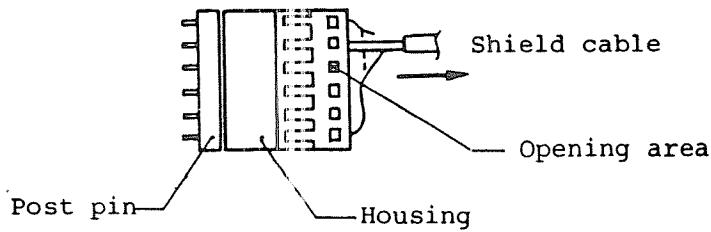
When you insert the pin, it should be so inserted that the stopper faces the opening side of the housing.

After the insertion, check the connection by pulling the cable lightly.

(4) Precautions for handling the black connector (J9)

(a) Disconnection of the connector

Pull out J9 connector straightly by inserting the narrow points of



(Fig.404) Disconnection of J9

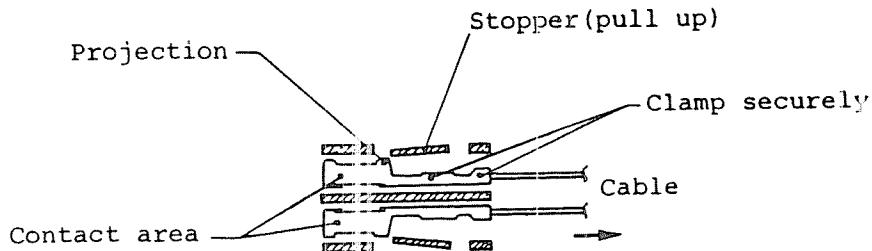
the tweezers into the opening area at the back side of the housing as shown in Fig.404. Be careful not to pull the fine wires.

(b) Connection of the connector

Make the polarizing key position of the housing correspond with the lack of the post pin, and push the housing carefully with the fingers.

(c) Removal of the pin

Lifting up the stopper of the housing with a narrow object such as cutter knife, pull the cable with a pair of tweezers in the direction indicated by the arrow. Refer to Fig.405.



(Fig.405) Sectional view of black connector

(d) Insertion of the pin

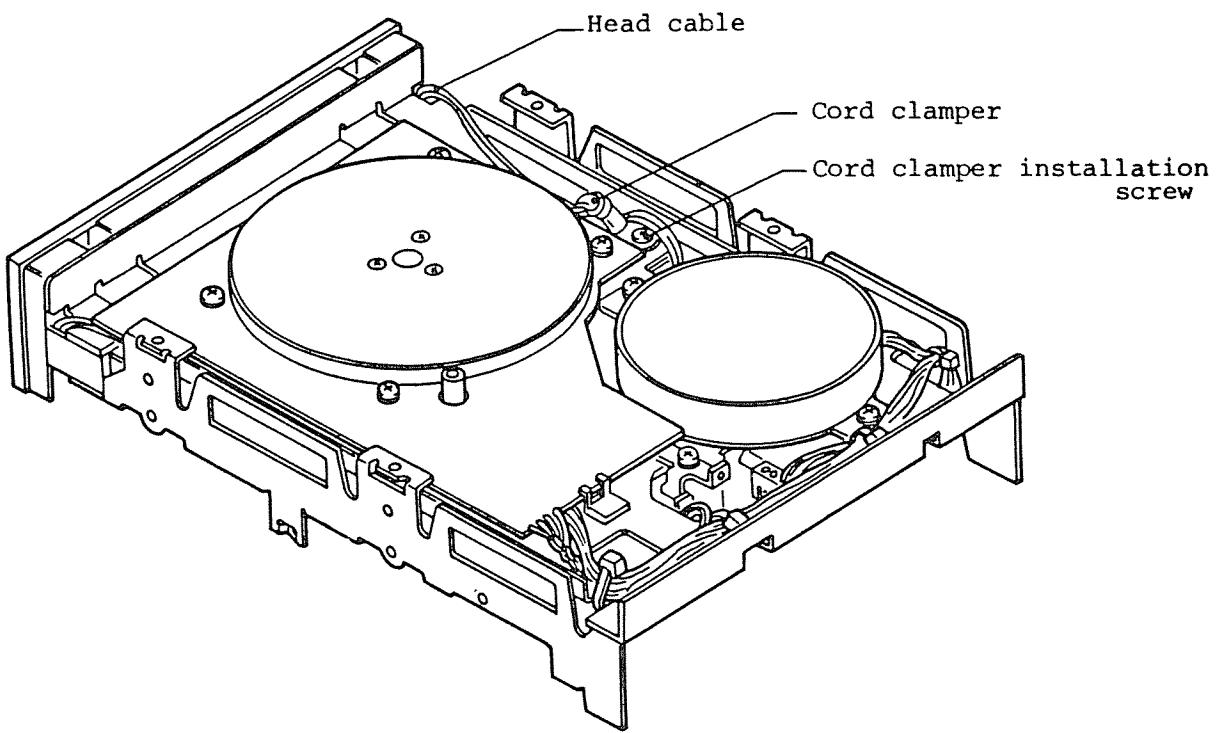
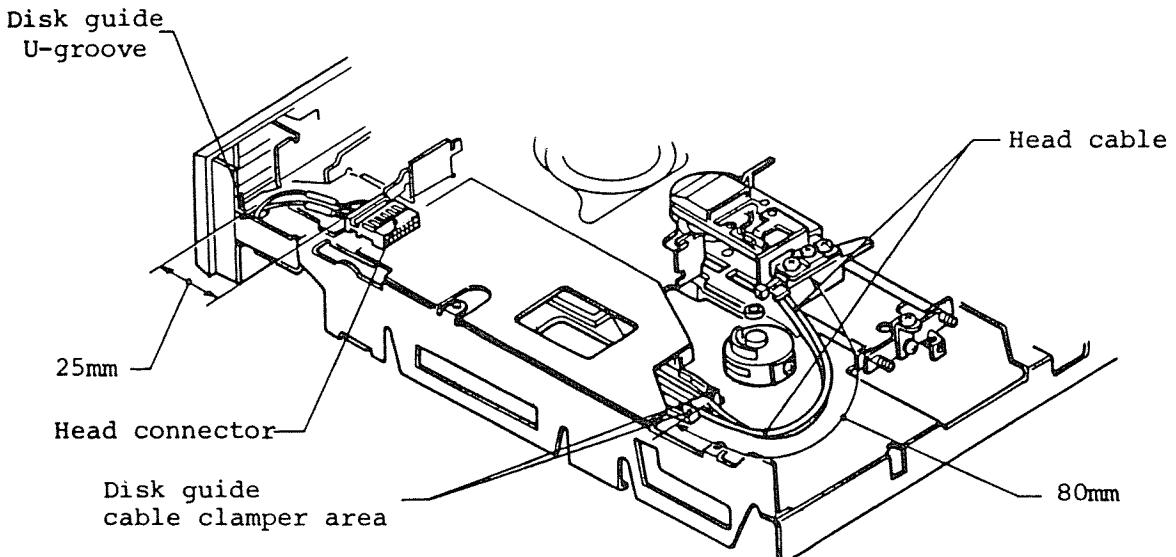
Before insertion, check the pins according to item (3)-(d), i) through iii).

When you insert the pin, it should be so inserted that the projection side faces the stopper of the housing. After the insertion, pull the cable with a pair of tweezers softly in order to confirm whether it is securely connected.

4-2-3. Head Cable Treatment

Head cable should be arranged correctly by the clamps with appropriate margin in length so that the head carriage can move on the guide shafts smoothly.

- (1) Clamp the head cable with cable clamper area of the disk guide so that the cable has appropriate looseness when the head carriage is set to track 00 (rear end of the moving area). The appropriate length of the head cable from the head carriage output to the cable clamper is approximately 80mm (see Fig.406).
Also confirm that the head cable do not touch the tail end of the steel belt.
- (2) Thread the head cable through the hole of the disk guide and arrange it under the chassis to hold with a cord clamper. There should be no excessive looseness of the cable between the cable clamper and the cord clamper which may cause undesirable contact of the cable to the disk when inserted. The cable length between the cable clamper and the cord clamper is 65mm, approx.
- (3) Remove the front bezel according to item 4-5-9. Thread the head cable along the U-groove of the disk guide and pull it up on the chassis to connect it to the head connector, J9. The cable length between the U-groove of the disk guide and the head connector is 25mm, approx. (see Fig.406).
If the head cable is too long, turn the cable around the cord clamper under the chassis.



Note: The figure uses the double sided FDD. The same cable arrangement is applied to the single sided FDD.

(Fig.406) Head cable arrangement

4-2-4. Initial Setting of SKA

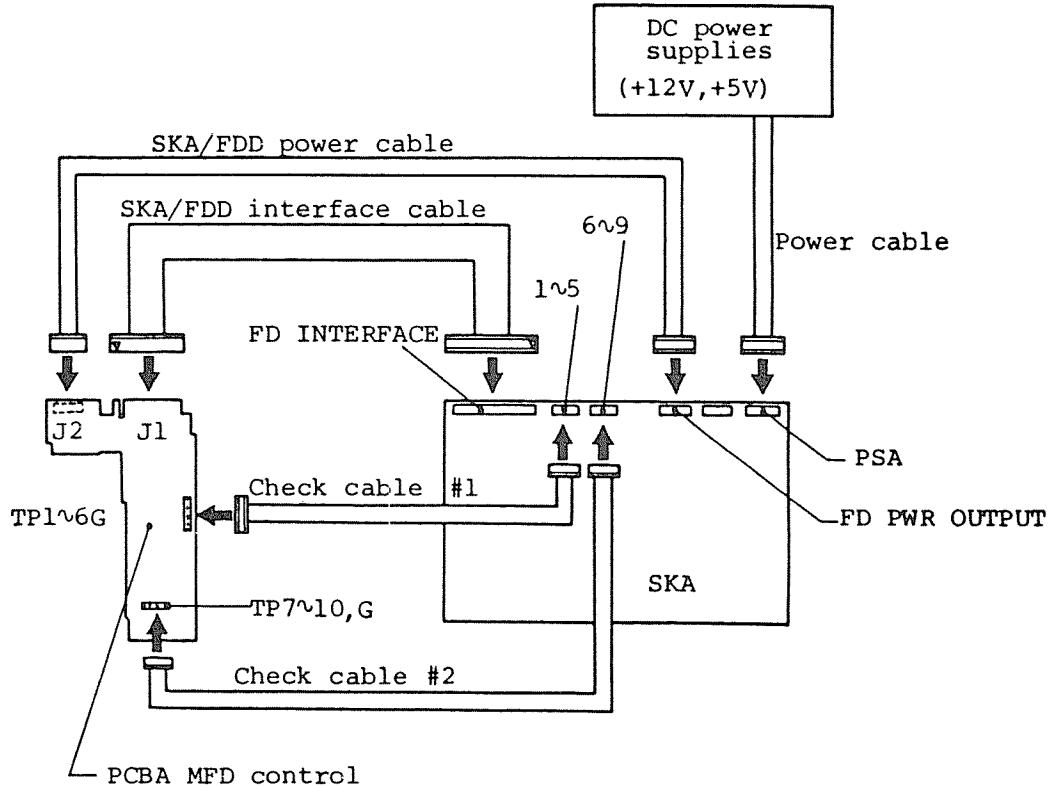
Following initial setting is required for operating the SKA.

Note: Use matched SKA for the FD-54 series. The SKA for the FD-54 has 430Ω terminator at the interface receiver which is different from that conventionally used 150Ω terminator for the FD-55 series. As to the other performance, SKA for the FD-54 and for the FD-55 are the same.

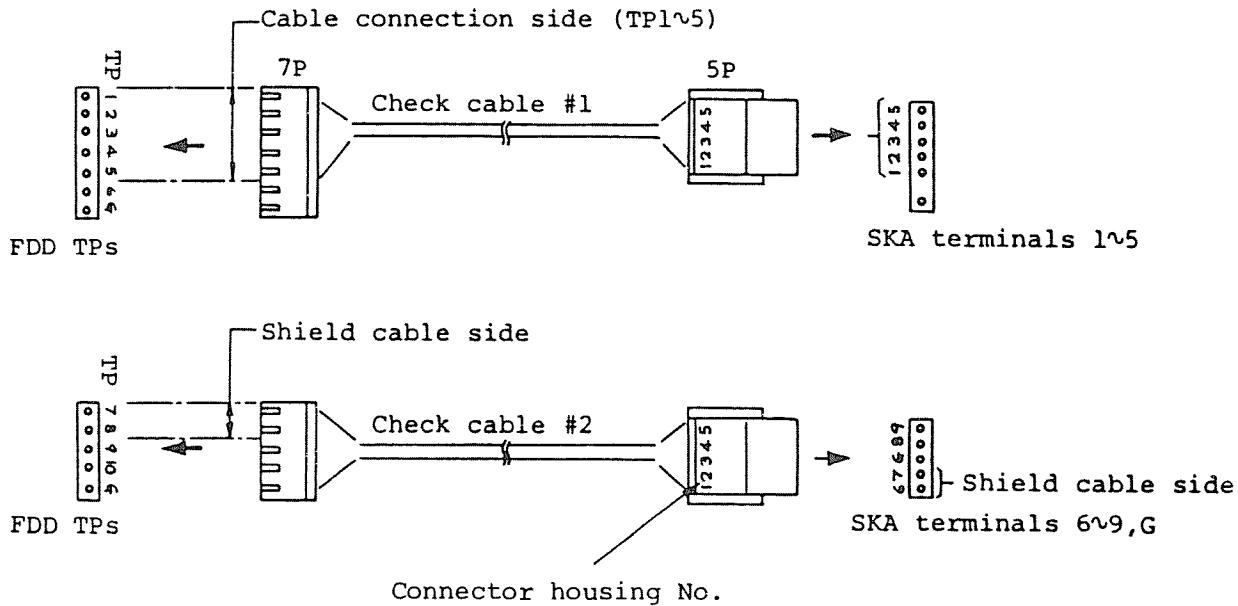
The SKA for the FD-54 series can also be used in the FD-55 series.

4-2-4-1. Cable connection and setting of power supply voltage

- (1) Set the output voltage of DC power supply to +12V and +5V, approx.
- (2) Turn the DC power off and connect the power cable to the PSA (SKA PWR) connector of the SKA.
- (3) Set the FD PWR switch of the SKA to the OFF position.
- (4) Connect the FD PWR OUTPUT of the SKA and the FDD with the SKA/FDD power cable.
- (5) Connect the SKA/FDD interface cable. Pay attention to the identification mark of the connector (▽) so that it locates at the pin 1 and 2 side.
- (6) Connect the check cable #1 (Flat cable, 7P connector at the FDD side and 5P connector at the SKA side) between the terminals 1 ~ 5 of the SKA and TP1 ~ TP6, G of the FDD. For the SKA side, be sure to match the pin numbers of the connector housing and the terminal numbers of the connector. For the FDD, cable connection side pins should be connected to the TP1 ~ 5 side.
- (7) Connect the check cable #2 (shield cable is used partially, 5P connectors



(Fig.407) Connection of SKA cable



(Fig.408) Connection of check cable

at both ends) between the terminals 6 ~ 9, G of the SKA and TP7 ~ TP10, G of the FDD. Be sure to match the pin numbers of the connector housing and the terminal numbers of the SKA as in Fig.408.

The shield cable side is TP7, 8, and terminals 6, 7 of the SKA.

(8) Turn the DC power on. Set the FD PWR switch of the SKA to the PSA side.

(9) Key in "CB". (+5V VOLTAGE)

(10) Adjust the DC power voltage so that the DATA indicator of the SKA
□□□ (V) indicates the value within the range of $5.00 \pm 0.1V$.

(11) Key in "F". (STOP)

(12) Key in "CC". (+12V VOLTAGE)

(13) Adjust the DC power voltage so that the DATA indicator of the SKA
□□□ (V) indicates the value within the range of $12.00 \pm 0.24V$.

(14) Key in "F". (STOP)

Note: The above items (1), (2), (9) ~ (14) may be omitted for replacement of the FDD or a temporary FDD power off. Remain DC power on and control the FDD power by the SKA PWR switch.

4-2-4-2. Setting of the maximum track number

Before the check and the adjustment of the FDD, set the maximum track number according to the following instructions.

Usually the maximum track number is set to 79 at the initial setting, change it to 39.

The setting will be maintained until the main DC power (for SKA) is turned off, or until the RESET switch of the SKA is depressed. Since the FD PWR switch is independent of this setting, it is convenient to maintain the main DC power on for the successive operations.

- (1) Key in "CF" (SET TMAX)
- (2) The maximum track number set at that time is indicated with the latter two digits of the DATA indicator (track).

Note: If there is no change in the maximum track number in item (2), depress "F" key.

- (3) Key in the maximum track number (39) of the FDD in two digits of decimal notation.

e.g. MAXIMUM TRACK NUMBER 39 (40 cylinders): CF 39

4-2-4-3. Setting of step rate and settling time

Generally, the step rate and the settling time of the FDD is the same as the initial value of the SKA (step rate: 6msec, settling time: 15msec) and no initial setting is required.

For the confirmation or the change of the initial setting, execute according to the following procedure. Once the setting is done, it will be maintained until the main DC power (for SKA) is turned off, or until the RESET switch of the SKA is depressed.

(1) Key in "DB". (SET STEP RATE)

(2) Step rate set at that time is indicated by 0.1msec scale on the DATA indicator  (ms).

e.g. DATA indicator  indicates 6.0msec.

(3) Key in a new step rate down to one decimal place (unit: msec).

Note: If there is no change in step rate in item (2), omit item (3) and forward to item (4).

(4) Key in "F". (STOP -- Setting of the step rate completes.)

(5) Settling time at that time is indicated by 0.1msec scale on the DATA indicator  (ms).

e.g. DATA indicator  indicates 15.0msec.

(6) Key in new settling time down to one decimal place (unit: msec).

Note: If there is no change in settling time in item (5), omit item (6) and depress "F" key to complete the operation.

(7) Depress "F" key. (STOP -- Setting of the settling time completes.)

e.g. STEP RATE 6msec, SETTLING TIME 15msec : DB 30 F 150 F

4-2-4-4. Level disk calibration

Setting of the following calibration value is required for accurate measurement before the check of the read level or the resolution. Use a level disk with a calibration value (100% center) written on the label. The setting will be maintained until the main DC power (for SKA) is turned off or until the FESET switch of the SKA is depressed. If the calibration value is the same as the initial value (100%) of the SKA, the initial setting of the following is not required.

(1) Innermost track read level

- (a) Key in "D0". (CALIBRATION READ LEVEL)
- (b) Calibration value set at that time is indicated in the latter three digits of the DATA indicator (%) .
- (c) Key in a new calibration value written on the level disk label (three digits, Max.)
- (d) Key in "F". (STOP)

Note: If there is no calibration change in item (b), omit item (c) and depress "F" key.

(2) Innermost track resolution

- (a) Key in "D1". (CALIBRATION RESOLUTION)
- (b) Calibration value set at that time is indicated in the latter three digits of the DATA indicator (%) .
- (c) Key in a new calibration value written on the level disk label (three digits, Max.)

(d) Key in "F". (STOP)

Note: If there is no calibration change in item (b), omit item (c) and depress "F" key.

e.g. READ LEVEL 103%, RESOLUTION 96%: DO 103 F, D1 96 F

4-2-4-5. Alignment disk calibration

Setting of the following calibration value is required for accurate measurement before the check and adjustment of the track alignment. Use a correctly calibrated (0% center) alignment disk with a calibration value written on the label. The setting will be maintained until the main DC power (for SKA) is turned off or until the RESET switch of the SKA is depressed.

If the calibration value is the same as the initial value (0%) of the SKA, the initial setting of the following is not required.

(1) SIDE 0 alignment

(a) Key in "E0". (CALIBRATION SIDE 0 ALIGNMENT)

(b) The calibration value set at the time is indicated in the latter two digits of the DATA indicator (%) , and the polarity is indicated in the initial digit. If a "0" is indicated, the polarity is positive. Polarity indication: plus + , minus -

(c) Key in a polarity and a new calibration value (two digits, Max.) written on the alignment disk label.

Designation of polarity: Depress "B" key only for minus designation.
(No designation is required for plus).

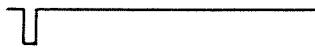
(d) Key in "F". (STOP)

(2) Side 1 alignment (Double sided only)

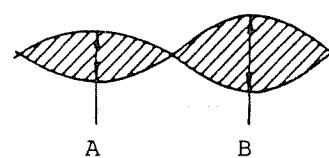
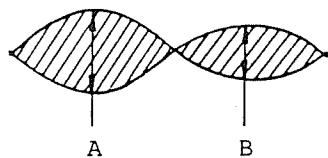
(a) Key in "E1". (CALIBRATION SIDE 1 ALIGNMENT)

(b) The same as in item (1)-(b) ~ (d).

INDEX output signal



Lobe pattern
(TP9,10)



Notes: 1. The lobe pattern ratio is calibrated in the SKA according to the following expression.

$$\text{Lobe pattern ratio} = \frac{A-B}{\text{Larger one of A \& B}} \times 100 - \text{Calibration value ('after calibration')}$$

2. If the calculated value with the above expression is positive, the polarity is plus, while the polarity is minus when the value is negative.

(Fig.409) Calibration of alignment lobe pattern

(3) Index burst timing

(a) Key in "E5". (CALIBRATION INDEX TIMING)

(b) The calibration value set at that time is indicated in the latter three digits of the DATA indicator (μs), and the polarity is indicated in the initial digit. (Refer to item (1)-(b)).
If a "0" is indicated, the polarity is positive.

(c) Key in a polarity and a new calibration value (three digits, Max.) written on the alignment disk label. Refer to item (1)-(c) for the polarity designation.

(d) Key in "F". (STOP)

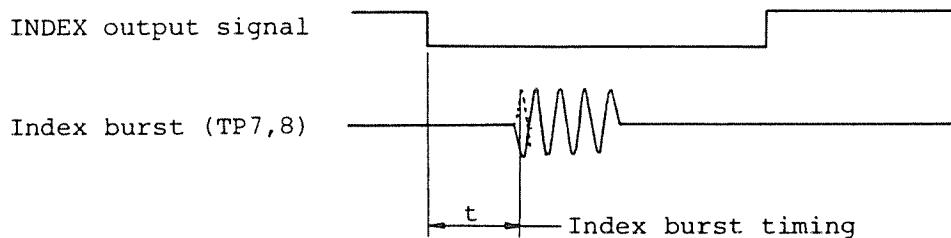
Note: If there is no change in the calibration value in item (b), omit

item (c) and depress "F" key.

e.g. Double sided FDD, SIDE 0 ALIGNMENT +3%, SIDE 1 ALIGNMENT -5%,

INDEX TIMING -25 μ s:

E0 3 F, E1 B 5 F, E5 B 25 F



Notes: 1. The index timing is calibrated in the SKA according to the following expression.

$$\text{Calibrated timing} = t - \text{calibration value } (\mu\text{s})$$

2. If the calculated value with the above expression is positive, the polarity is plus, while the polarity is minus when the value is negative.

(Fig. 410) Calibration of index burst timing

4-2-4-6. Humidity setting

For the check and adjustment of the track alignment using an alignment disk, set the environmental relative humidity to the SKA in order to improve the precision of measurement.

This setting is important when the relative humidity is considerably different from 50%.

The initial setting of the following is not required if the relative humidity is the same as the initial value (50%) of the SKA.

(1) Key in "E2". (CALIBRATION RH ALIGNMENT)

(2) The relative humidity set at that time is indicated in the latter two digits of the DATA indicator (%) .

(3) Input the relative humidity percentage in the measurement environment (two digits, Max.).

e.g. RELATIVE HUMIDITY 58%: E2 58

4-2-4-7. Setting of SKA gain

For this FDD, the SKA gain should be maintained at the initial state (H GAIN indicator is off). If the H GAIN indicator turns on by an erroneous key-in, turn it off by keying in "DD".

4-2-5. Others

(1) Total error test

In the check and adjustment in item 4-4, read/write error test is not included. After the adjustment or the replacement of the maintenance parts, it is recommended to perform a data error test by connecting the FDD to the user's system or the TEAC simulator KB. The window margin test is the most recommended item.

(2) Setting of FDD straps

It is required to confirm before the operation that the straps (short bars) on the PCBA MFD control are at the appropriate position for the system to be used in the check and adjustment.

When the SKA is used, depress a key which number is the same as the on-state short bar among DS0 ~ 3 straps of the FDD and confirm that the indicator is on before various key operations.

If the IU short bar is on, you can turn on the front bezel indicator by "A" (IN USE) key of the SKA.

- Notes:
1. For simplifying the explanation, following shows only the case when the DS0 short bar is on.
 2. If the strap position of the FDD is changed from the initial setting at the system installation, be sure to change it back to the initial position after the maintenance operations.

(3) Connection of the probe ground

Connect the probe ground of the equipment as follows:

(a) For the observation at the test points (TP) 7 ~ 10:

Connect the probe ground to the G test point (OV) on the PCBA MFD control.

(b) For the observation at the other test point:

Connect the probe ground to the G test point (0V) on the PCBA MFD control. Or GND (0V) terminal of the system power supply unit, or the SKA GND terminal may be used.

(c) For the observation of the SKA test point:

Connect the probe ground to the SKA GND terminal.

Note: When you use the SKA, almost all checks including the read amp. output at TP7 ~ TP10 of the FDD will be done automatically through the check cables #1 and #2 and interface cable. Also these signals can be observed by an oscilloscope using the test points on the SKA.

(4) Maintenance environment

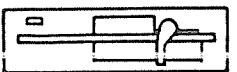
Maintenance of the FDD should be done on a clean bench at room temperature and humidity. It is recommended to execute the check and adjustment of the track alignment after leaving the FDD for at least 2 hours at room temperature and humidity. The magnetic head, disk, steel belt, etc. might suffer from dust and dirt if the maintenance is not undertaken in a clean environment.

(5) Orientation of the FDD

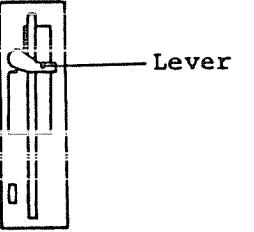
Position the FDD as shown in Fig.411 unless otherwise specified. Horizontal and vertical orientations with lever side up should be used.

(6) Head load

The FD-54 series have no head load solenoid. They are always in head load condition as far as a disk is inserted and the front lever is closed.



Horizontal setting



Vertical setting

(Fig.411) General orientation of the FDD during maintenance

(7) Work disk

When you use the SKA, use a soft sectored disk.

4-3. PREVENTIVE MAINTENANCE

4-3-1. Cleaning of Magnetic Head by Cleaning Disk

When you use the FDD in dusty environment, it is recommended to clean the magnetic head surface periodically (e.g. once a month) with a commercially available cleaning disk. Especially for a double sided FDD, it is difficult to clean the head surface, be sure to use the cleaning disk.

For typical usage under typical environmental condition, the cleaning is recommended when data errors often occur.

(A) Equipment

- (1) Cleaning disk
- (2) SKA or user's system

(B) Cleaning procedure

(1) General method

- (a) Start the spindle motor and install an appropriate cleaning disk.

Notes: 1. Do not use a damaged cleaning disk on the surface.
2. For a single sided FDD, be sure to install a single sided cleaning disk. The cleaning surface of the disk should be in contact with the head surface.

When the FDD is placed horizontally, the magnetic head is located down and it faces the back side of the disk.

If a double sided cleaning disk is installed in a single sided FDD, it may damage the head pad.

3. For a double sided FDD, a double sided cleaning disk should be used. Side 0 (lower side) and side 1 (upper side) heads are cleaned simultaneously.

(b) Clean the head at a suitable track position for 10 ~ 30 seconds, approx. In order to avoid the concentration on a specific track, it is a good way to make the head move between track 00 and the innermost track during cleaning.

Note: The most appropriate cleaning time is different for each type of cleaning disk used.

Excessively long cleaning time is not effective but has possibility to accelerate the head wear.

(c) Remove the cleaning disk.

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Execute drive select by key "0". (DS0 indicator turns on).

(d) Key in "C0" and confirm that the TRACK indication of the SKA becomes "00". (RECALIBRATE)

(e) Install an appropriate cleaning disk. See item (1)-(a), "Notes".

(f) Key in "C6". (SEEK TEST)

(g) After 10 ~ 30 seconds, depress "F" key.

(h) Eject the cleaning disk.

4-3-2. Direct Cleaning (Single sided FDD only)

This cleaning method is applied only to a single sided FDD.

If this method is applied to a double sided FDD, gimballed mechanism of the head might be damaged.

If visible dirt is on the head surface when the head pad arm is lifted up manually during maintenance, perform direct cleaning as follows:

(A) Equipment

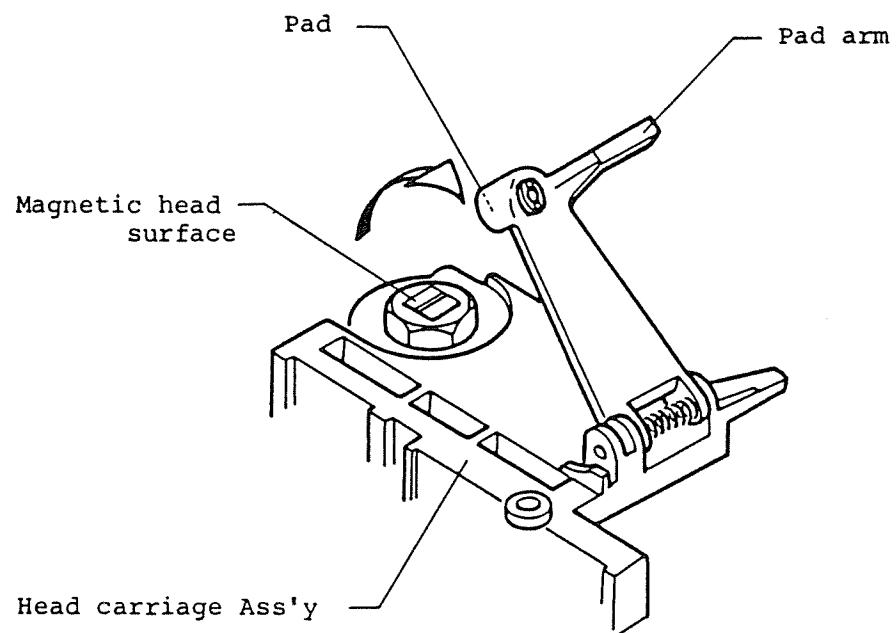
- (1) Absolute alcohol (Ethanol)
- (2) Cotton swab or gauze

(B) Cleaning procedure

- (1) Lightly dampen a cotton swab or a gauze with alcohol.
- (2) Lift up the pad arm (see Fig.412) and clean the head surface carefully with the cotton swab or the gauze.

Note: Do not touch the pad surface.

- (3) Wipe the head surface with clean dry cloth after the evaporation of the alcohol.
- (4) After confirming that the dirt is cleaned off and no fluff is left on the head surface, let the pad arm down carefully.



(Fig.412) Direct cleaning of magnetic head (Single sided only)

4-4. CHECK AND ADJUSTMENT

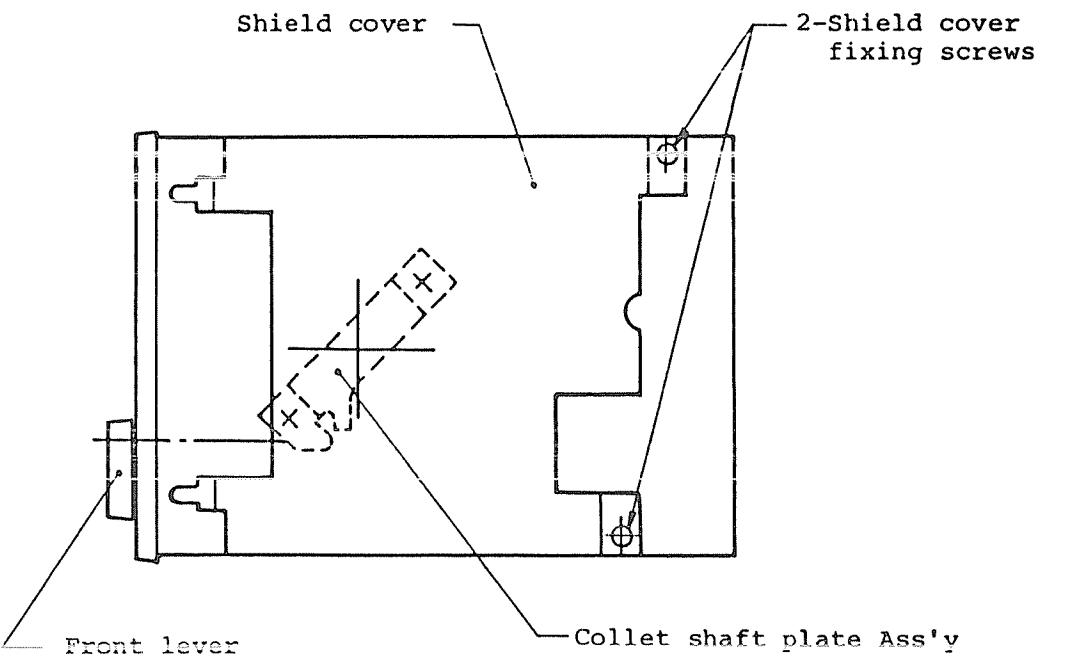
4-4-1. Adjustment of Collet Shaft Plate

(A) Equipment

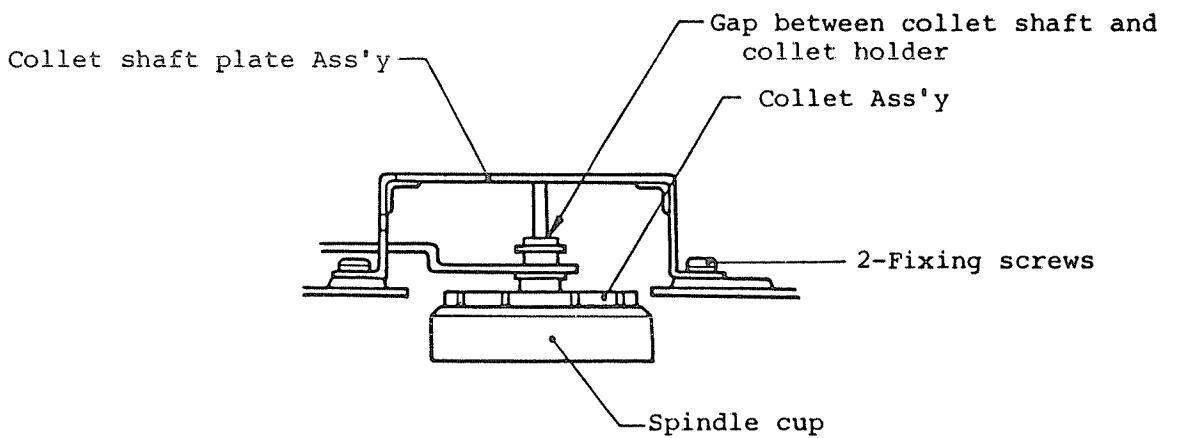
- (1) Cross point screwdriver, M3
- (2) Locking paint

(B) Adjustment procedure

- (1) Remove two fixing screws of the shield cover (see Fig.413) and remove it.
- (2) Loosen two fixing screws of the collet shaft plate Ass'y so that the collet shaft plate can be moved manually without getting out of place.
- (3) Clamp the collet by turning the front lever.
- (4) In this condition, adjust the collet shaft plate and tighten two fixing screws with the specified torque so that the visual distance of the gap between the collet shaft and the hole of the collet holder becomes even (see Fig.414).
- (5) Up and down the collet by turning the front lever and confirm that it does so smoothly without being caught by the spindle cup.
- (6) Apply a drop of locking paint of the fixing screws.
- (7) Install the shield cover in the reverse order of item (1).



(Fig.414) Location of collet shaft plate



(Fig.413) Gap of collet shaft plate

4-4-2. Adjustment of Front Lever Position

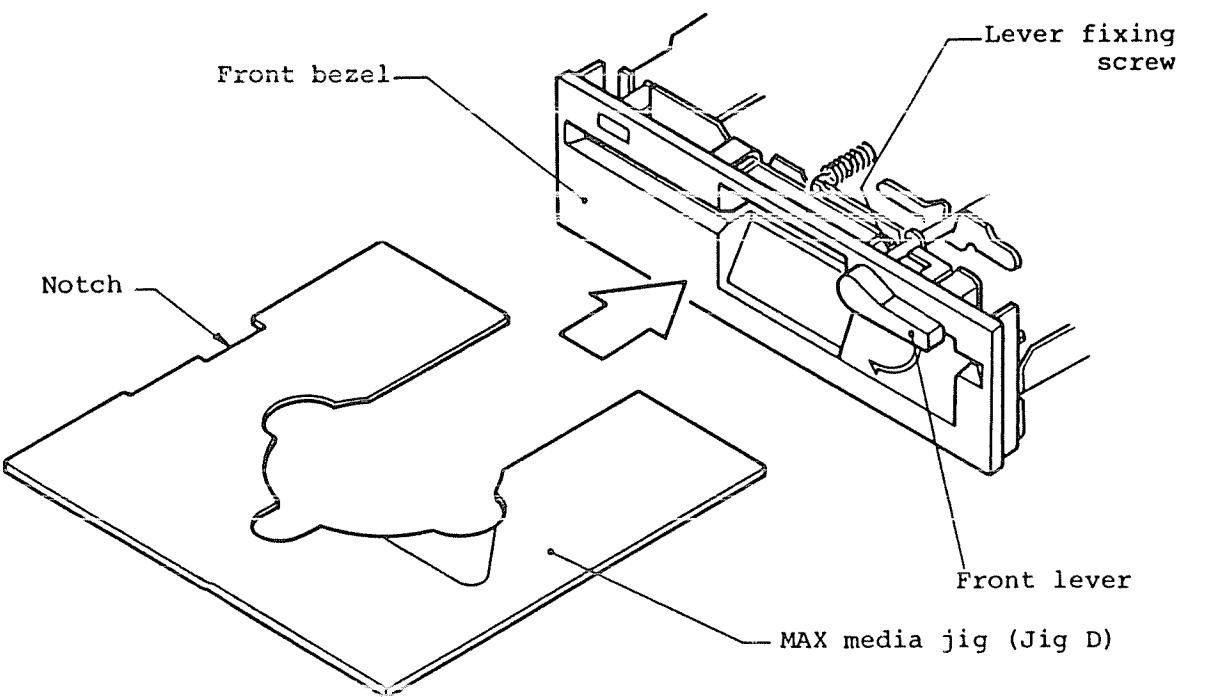
(A) Equipment

- (1) Hexagon wrench key, 1.5mm
- (2) MAX media jig (Jig D)

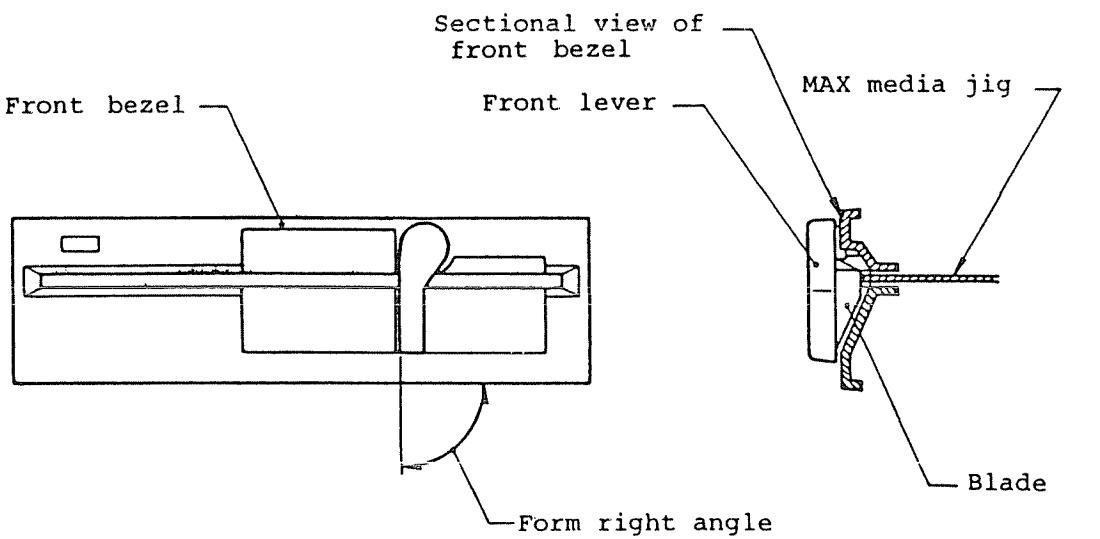
(B) Adjustment procedure

- (1) Turn the front lever to close position and loosen a lever fixing set screw to pull out the lever for 0.5mm, approx.
- (2) Tighten the set screw.
- (3) Turn the front lever to open position and insert the MAX media jig as shown in Fig.415 (the notch side to be left).
- (4) Turn the front lever to close position and loosen the set screw again. Then push the lever against the MAX media jig.
Confirm that the pin of the lever shaft goes into the slot of the front lever.
- (5) Position the handle of the front lever forms right angle against the longitudinal side of the front bezel. And tighten the set screw with the specified torque. (See Fig.416).
- (6) Close the front lever and confirm that the blade of the lever does not nip the MAX media jig.
- (7) Open the front lever and remove the jig.

Note: Refer to item 4-2-1 as to handling of the set screws.



(Fig.415) Adjustment of front lever



(Fig.416) Front lever position

4-4-3. Check and Adjustment of Disk Pad Lever (Bail)

This item applies only to the double sided FDDs.

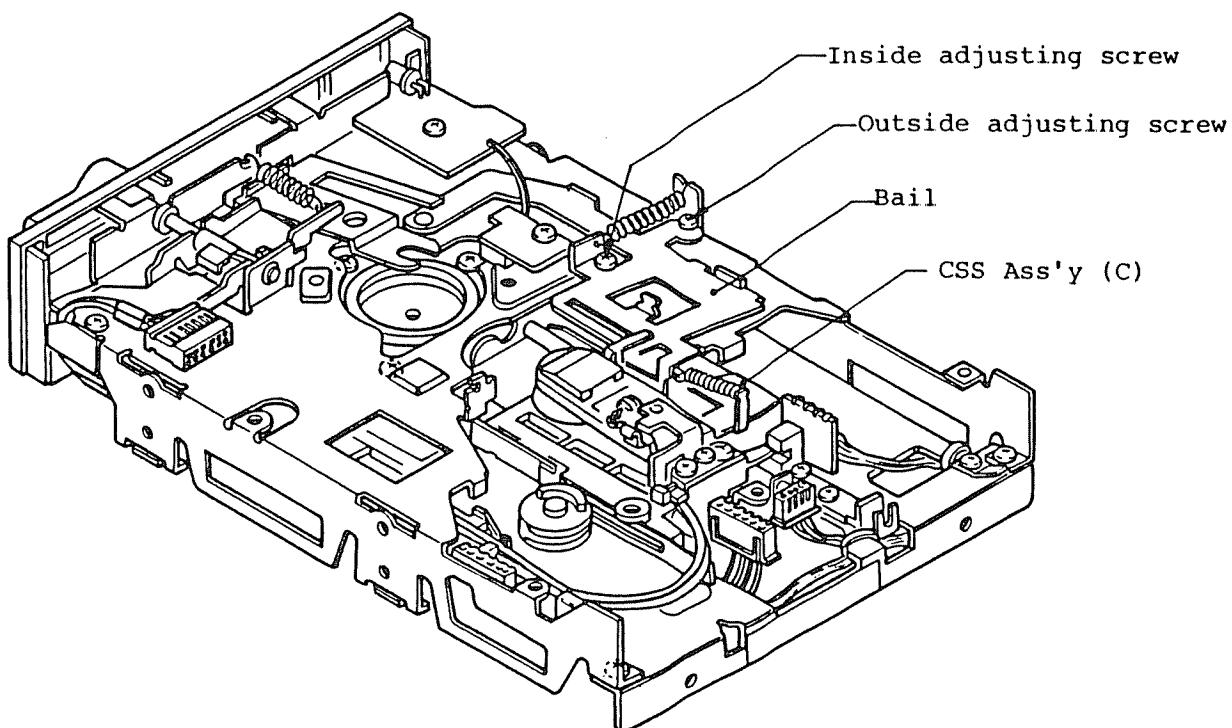
(A) Equipment

- (1) Cross point screwdriver, M2.6
- (2) Binding agent

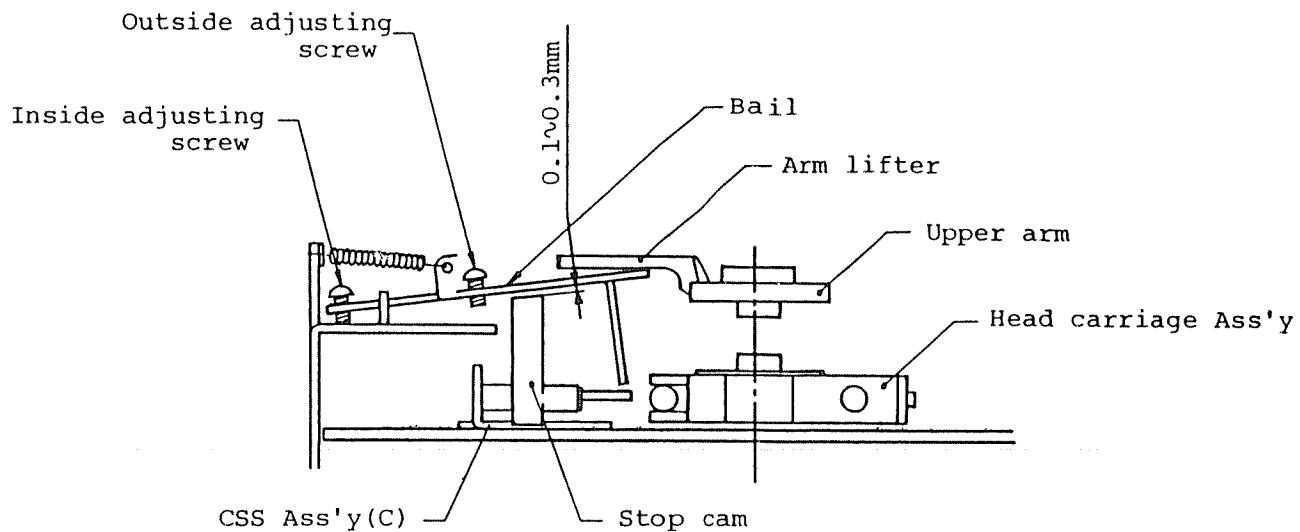
(B) Check and adjustment procedure

- (1) Open the front lever to be able to insert the disk.
- (2) Confirm a little gap (0.1 ~ 0.3mm, approx.) is spaced between the bail and the top of the stop cam of the CSS Ass'y (C). (See Fig.418).
- (3) If the item (2) is not satisfied, turn the outside adjusting screw (see Fig.417) of the bail so that the bail and the top of the stop cam are separated with 0.2mm, approx.
- (4) In the process of inserting a disk slowly, confirm that the disk jacket does not touch the side 0 nor the side 1 head and goes into the FDD smoothly with appropriate space margin.
- (5) Open and close the front lever two or three times to confirm the clampings of the disk are done smoothly.
- (6) In the process of ejecting the disk slowly, confirm that the side 0 and side 1 heads do not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface) and that the disk can be drawn out smoothly with appropriate space margin.

- (7) Insert the disk again and close the front lever.
- (8) Confirm that a little gap ($0 \sim 0.5\text{mm}$, approx.) is spaced between the stop cam and the disk jacket without activating the stop cam of the CSS Ass'y when the disk jacket is depressed lightly with a finger from the front bezel side.
- (9) If the item (8) is not satisfied, turn the inside adjusting screw (see Fig. 417) of the bail so that the gap between the disk jacket and the stop cam becomes $0.1 \sim 0.2\text{mm}$, approx.
- (10) Apply binding agent to the two adjusting screw to fix it to the bail.
- (11) Open the front lever to draw out the disk.



(Fig.417) Adjustment of bail



Note: The figure is viewed from the front bezel side.

(Fig.418) Gap of bail and stop cam

4-4-4. Check of File Protect Sensor

(A) Equipment

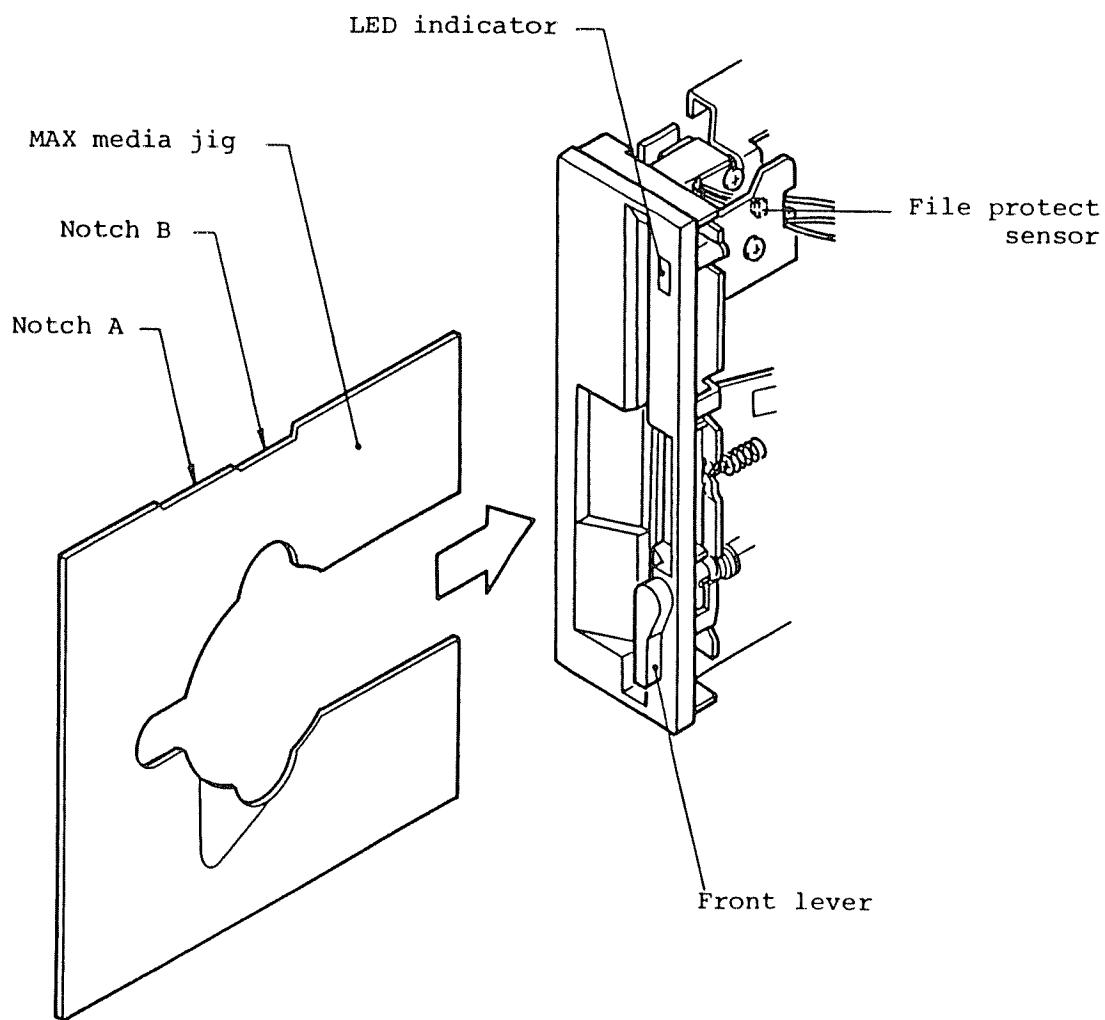
- (1) MAX media jig (Jig D)
- (2) Digital voltmeter (or oscilloscope)
- (3) SKA or user's system

(B) Check procedure

(1) General method

- (a) Place the FDD on the work bench with the LED indicator up and the front lever down. (See Fig.421).
- (b) Connect a digital voltmeter or an oscilloscope (DC range, 1V/div) to TP6 (File protect sensor) on the PCBA MFD control.
- (c) Install the MAX media jig as in Fig.421 and set it so that the notch A area is located on the light pass from the file protect sensor.
- (d) Adjust the orientation of the FDD so that it is not exposed with strong light outside.
- (e) Confirm that the voltage measured at TP6 when power is supplied to the FDD is within the following range.
Notch A position TP6 voltage: 0.5V, Max.
- (f) Pull out the jig a little so that the notch B area is located on the light pass.
- (g) Confirm that the voltage measured at TP6 when power is supplied to the FDD is within the following range.

Notch B position TP6 voltage: 3V, Min.



(Fig.421) Check of file protect sensor

(2) SKA method

- (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Execute the general method described in item (1)-(a) through (e). WRROT indicator of the SKA turns on when drive selection is executed by key "0". (DSO indicator turns on).
- (c) Execute the general method described in item (1)-(f) and -(g). WRROT indicator of the SKA turns off.

4-4-5. Check and Adjustment of Disk Rotation Speed

This item is only applied to the FDD which has a DD motor Ass'y with the variable resistor R1 for adjusting the rotational speed of the disk on the PCBA DD motor servo. Refer to Fig.311 as to the mounting position of the variable resistor R1.

For the DD motor Ass'y without the variable resistor, the rotation speed is fixed by the ceramic oscillator in the servo circuit and no adjustment is required.

(A) Equipment

- (1) Common screwdriver, small size
- (2) SKA or user's system
- (3) Frequency counter (not required when the SKA is used)
- (4) Work disk (soft sectored)

(B) Check and adjustment procedure

(1) General method

- (a) Connect the frequency counter to TP4 (Index) of the PCBA MFD control or to the INDEX interface signal line.
- (b) Start the spindle motor and install a work disk.
- (c) Set the head to track 00.
- (d) Confirm that the pulse interval at TP4 is within the following range.
TP4 pulse interval: $200 \pm 3\text{msec}$
- (e) If the value in item (d) is out of the specified range, adjust the variable resistor R1 on the PCBA DD motor servo to obtain the median value in the specified range in item (d).

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

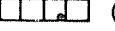
(c) Insert a soft sectored work disk.

(d) Execute drive select by key "0". (DS 0 indicator turns on).

(e) Key in "C0" and confirm that TRACK indication becomes "00".

(RECALIBRATE)

(f) Key in "C3". (INDEX PERIOD)

(g) Confirm that the DATA indicator  (ms) indicates a value within the following range.

INDEX interval: $200.0 \pm 3.0 \text{ msec}$

(h) If the value in item (g) is out of the specified range, adjust the variable resistor R1 on the PCBA DD motor servo to obtain the median value in the specified range in item (g).

4-4-6. Check and Adjustment of Head Touch

Note: The adjustment applies to a single sided FDD only.

(A) Equipment

- (1) Work disk
- (2) Common screwdriver, small size
- (3) SKA or user's system
- (4) Oscilloscope (not required when the SKA is used)
- (5) DC clip on ammeter (not required when the SKA is used)
- (6) Locking paint

(B) Adjustment procedure

(1) General method

- (a) Connect an oscilloscope to TP9 or TP10 (Differentiation amp.) on the PCBA MFD control.
Oscilloscope range: AC mode, 0.2V

- (b) Start the spindle motor and install a work disk.

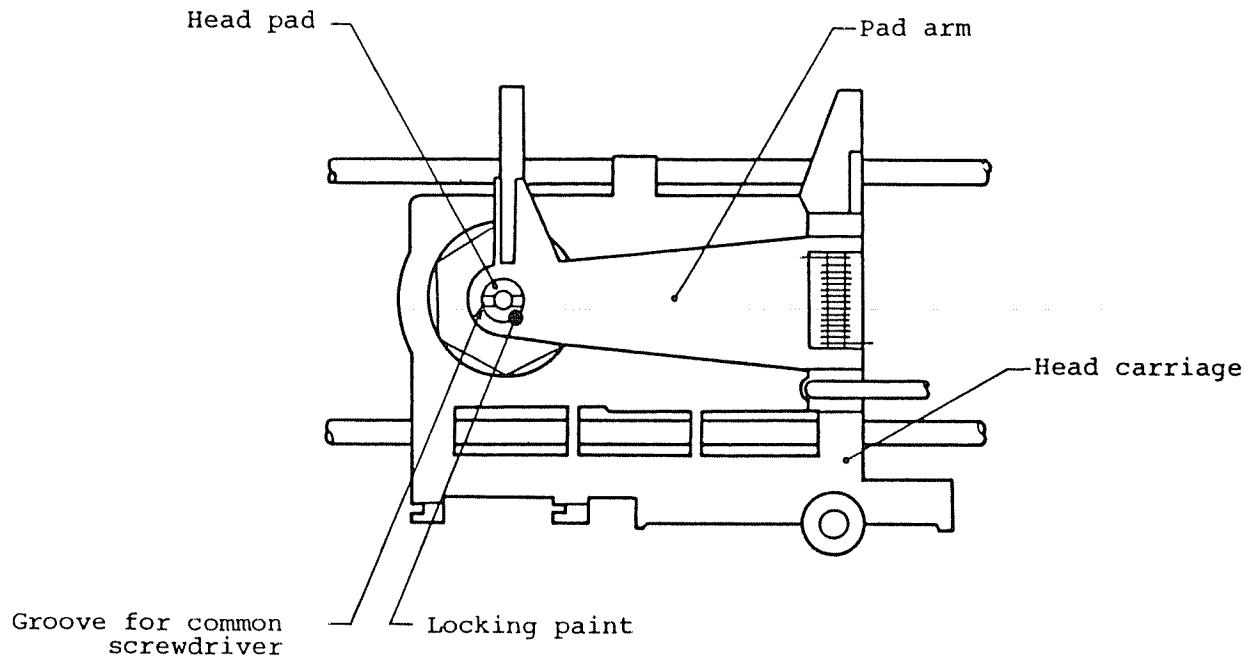
- (c) Set the head to the innermost track.

- (d) Repeat the cycle of one write rotation and one read rotation.

Write data should be the fixed pattern of 2F (250KHz of WRITE DATA frequency).

- (e) Write down the average read level measured during the read operation of item (d).

- (f) Execute item (d) and (e) with a slight depression (very slight depression easy to release: 10 ~ 20g) by a finger on the top of the upper head (double sided) or of the pad arm (single sided), and measure the average read level as in item (e).
- (g) Confirm that the read level measured in item (e) is greater than 80% of that in item (f).
- (h) For a double sided FDD, execute items (d) through (g) respectively for the side 0 and the side 1 heads.
- (i) After making the head move to track 00, execute items (d) through (h).
- (j) Head touch adjustment for a single sided FDD:
- i) At the innermost track, turn the groove on the upper side of the head pad by 30° steps, approx. with a common screwdriver (see Fig.420). At each turning of the groove, execute write and read operations in item (d).
Be sure to take apart the common screwdriver from the head pad during write or read operation.
Note: Be careful not to push the head pad strongly with the common screwdriver. Also do not touch the pad surface to which a disk will be in contact.
- ii) After turning the pad position around 360°, set the position again to the position where the highest read level was obtained. Then execute items (d) through (g) at the innermost track.
- iii) Continue the operation until the items (g) and (i) are sufficiently satisfied. Following causes are assumed for the insufficient result in item (g) or (i) after fine adjustment of the pad position.



(Fig.420) Adjustment of head pad position (single sided FDD)

① Inferior head pad:

Replace the pad according to item 4-5-8.

② Inferior disk:

Disk and/or jacket is deformed or damaged. Replace the work disk with a new one.

③ Inferior head:

Replace the head carriage Ass'y according to item 4-5-1.

- iv) Remove the work disk and apply a drop of locking paint around the rotating area of the head pad. Be careful not to smear the groove for common screwdriver with the locking paint.

(k) Possible causes for the insufficient head touch in a double sided FDD:

Following causes are assumed for the insufficient result in items (g) through (i) on a double sided FDD.

i) Inferior disk:

Disk and/or jacket is deformed or damaged. Replace the work disk with a new one.

ii) Inferior head flexure:

Because of the failed performance of the bail or the CSS Ass'y in item 4-4-3, the flexure on which the head piece is located may be deformed. Remove the disk. Then open and close the front lever slowly to observe the gap between the side 0 and the side 1 heads from the front bezel. If the two head surfaces are not in parallel each other, it is considered to be the deformation.

Replace the head carriage Ass'y according to item 4-5-1.

(2) SKA method

- (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Start the spindle motor by key "5". (MON indicator turns on). Install a work disk and execute drive select by key "0". (DS0 indicator turns on).
- (c) Key in "C0" and confirm that the TRACK indicator becomes "00".
(RECALIBRATE)
- (d) Key in "C1" (SEEK TMAX)
- (e) Key in "D3". (WRITE/READ LEVEL PRE 2F)
- (f) Write 2F and read operations are repeated.
The DATA indicator  (mV) indicates the average read level of TP7 and TP8 (Pre-amp.) after each cycle of operation (one rotation of write and one rotation of read) is finished.
- (g) Observe the DATA indicator  (mV) with a slight depression (very slight depression easy to release: 10 ~ 20g) by a finger on the top of the upper head (double sided) or of the pad arm (single sided).
- (h) Confirm that the read level measured in item (f) is more than 80% of that in item (g).
- (i) For a double sided FDD, depress "F" key to stop and then depress "4" key to execute items (e) through (h) for the side 0 and the side 1 heads respectively. The side is changed alternately by a depression of "4" key. If side 1 is selected, SIDE 1 indicator of the SKA turns on.

(j) Key in "C0" (RECALIBRATE) and execute items (e) through (i) in the similar way.

(k) Head touch adjustment for a single sided FDD:
Refer to item (j) of "General method".

(L) Possible causes for the inferior head touch in a double sided FDD:
Refer to item (k) of "General method".

4-4-7. Check and Adjustment of Asymmetry

(A) Equipment

- (1) Work disk
- (2) SKA or user's system
- (3) Oscilloscope

(B) Check and adjustment procedure

(1) General method

(a) Connect an oscilloscope to TP5 (Read data) on the PCBA MFD control
or to the READ DATA interface line.
Oscilloscope range : DC mode, 2V, 1 μ sec

(b) Start the spindle motor and install a work disk.

(c) Set the head to the innermost track.

(d) Execute 1F write operation (125KHz of WRITE DATA frequency).

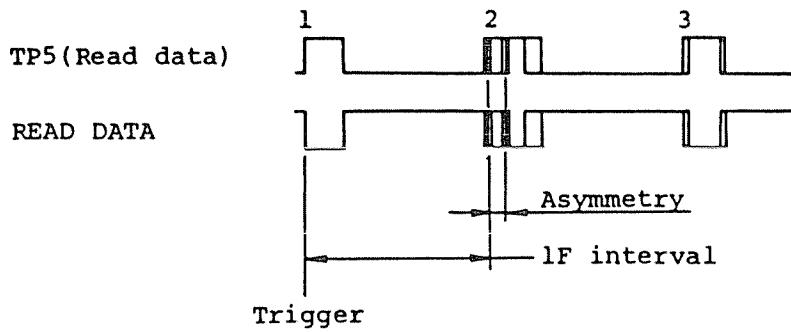
(e) Measure the asymmetry referring to Fig.421.

Note: Oscilloscope should be so set that three read data pulses can be observed. Asymmetry width should be measured at the second read data pulse from the trigger pulse.

(f) Confirm that the asymmetry is within the following range.

Innermost track 1F asymmetry : 0.6 μ sec, Max.

(g) For a double sided FDD, execute items (d) through (f) for the side 0 and the side 1 heads respectively.



(Fig.421) Measurement of asymmetry

- (h) If the value in item (f) or (g) is out of the specified range, adjust according to the following procedure.
- The adjustment can be done only for the PCBA versions or the PCBA revision numbers with the variable resistor R5 on the PCBA MFD control. No adjustment can be done without R5.
- i) Adjust the variable resistor R5 so that the asymmetry takes the minimum value while repeating 1F write and 1F read operations alternately.
 - ii) For a double sided FDD, repeat the operation in item i) for the side 0 and the side 1 heads alternately. The variable resistor shall be so adjusted that both asymmetry for side 1 and side 0 heads take the minimum value.
- (i) If the values in items (f) and (g) are out of the specified range in the PCBA without the variable resistor R5, or if the adjustment in item (i) cannot be done sufficiently even if R5 is mounted, following causes are assumed.
- i) Leakage flux density in the environmental condition of the FDD is high:
If there is some flux source near the FDD such as magnet, transformer, motor, Brown tube, magnetized iron plate, etc., take

it apart from the FDD. Then measure the asymmetry and adjust again.

ii) Inferior disk:

Replace the work disk.

iii) Inferior head:

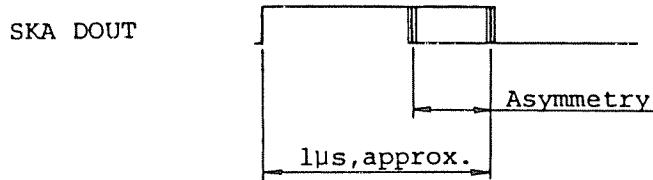
Replace the head carriage Ass'y according to item 4-5-1.

iv) Inferior PCBA MFD control:

Replace the PCBA according to item 4-5-6.

(2) SKA method

- (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Key in "B1F". (1F DUTY)
- (c) Connect an oscilloscope to the DOUT terminal of the SKA.
Oscilloscope range : DC mode, 2V, 0.2 μ sec
- (d) Start the spindle motor by key "5". (MON indicator turns on).
- (e) Install a work disk.
- (f) Execute drive select by key "0". (DS0 indicator turns on).
- (g) Key in "C0" and confirm that the TRACK indicator becomes "00".
(RECALIBRATE)
- (h) Key in "C1". (SEEK TMAX)
- (i) Key in "D4". (WRITE/READ LEVEL PRE 1F)
- (j) Measure the asymmetry as in Fig.422.



(Fig.422) Measurement of asymmetry (SKA)

(k) Confirm that the asymmetry is within the following range.

Innermost track 1F asymmetry : 0.6 μ sec, Max.

(L) For a double sided FDD, depress "4" key and execute items (i) through (k) for the side 0 and the side 1 heads respectively. The side is changed alternately by a depression of "4" key. If side 1 is selected, SIDE 1 indicator of the SKA turns on.

(m) If the value in item (k) or (L) is out of the specified range, adjust according to the following procedure. The adjustment can be done only for the PCBA versions or the PCBA revision numbers with the variable resistor R5 on the PCBA MFD control. No adjustment can be done without R5.

i) Adjust the variable resistor R5 so that the asymmetry takes the minimum value by keying in "D4".

ii) For a double sided FDD, execute the operation in item i) for both sides alternately by changing the side by key "4". The variable resistor shall be so adjusted that both asymmetry for side 1 and side 0 heads take the minimum value.

(n) If the values in items (K) and (L) are out of the specified range in the PCBA without the variable resistor R5, or if the adjustment in item (m) cannot be done sufficiently even if R5 is mounted, refer to item (j) of "General method".

4-4-8. Check of Read Level

(A) Equipment

- (1) Level disk
- (2) SKA or user's system
- (3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP9 and TP10 (Differentiation amp.) on the PCBA MFD control.
Oscilloscope range : AC mode, 0.5V
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and ADD both channels.

(b) Start the spindle motor and install a level disk.

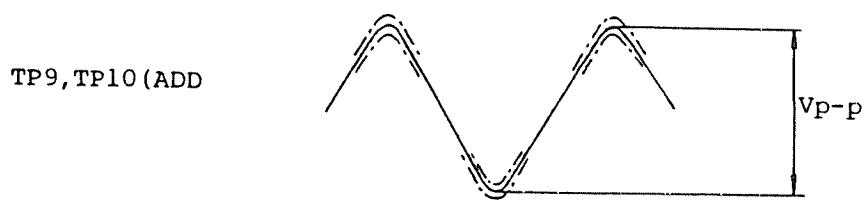
(c) Make the head move to the innermost track.

(d) Execute 2F write operation for one rotation of the disk (250KHz of WRITE DATA frequency).

(e) Measure the average amplitude (V_{p-p}) of the read waveform as in Fig.423.

(f) Calculate the read level by substituting the following expression with the measured value in item (e) and READ LEVEL calibration value (see level disk label).

$$\text{Read level (true value)} = \text{Measured value} \times \frac{100}{\text{Calibration value}}$$



(Fig.423) Measurement of average read level (2F)

(g) Confirm that the true value of the read level is within the following range.

Innermost track read level : $1.4V_{p-p}$, Min.

(h) For a double sided FDD, execute items (d) through (g) for the side 0 and the side 1 heads respectively.

(i) If the value in item (g) or (h) is out of the specified range, following causes are assumed.

i) Inferior disk:

Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

ii) Abnormal disk rotational speed:

Check and adjust according to item 4-4-5.

iii) Inferior head touch:

Check and adjust according to item 4-4-6.

iv) Inferior head:

Replace the head carriage Ass'y according to item 4-5-1.

v) Inferior PCBA MFD control:

Replace the PCBA MFD control according to item 4-5-6.

(k) Eject the level disk and release the Invert and ADD modes of the oscilloscope.

(2) SKA method

- (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Start the spindle motor by key "5". (MON indicator turns on).
- (c) Install a level disk.
- (d) Execute drive select by key "0". (DSO indicator turns on).
- (e) Key in "C0" and confirm that the TRACK indication becomes "00".
(RECALIBRATE)
- (f) Key in "C1". (SEEK TMAX)
- (g) Key in "D7". (WRITE/READ LEVEL DIF 2F)
Calibration value of the level disk should be set previously in the SKA.
- (h) Confirm that the DATA indicator ████ (mVo-p) indicates the value within the following range.
Innermost track read level : 700mVo-p, Min.
- (i) For a double sided FDD, depress key "4" and execute items (g) and (h) for the side 0 and the side 1 heads respectively. The side is changed alternately by a depression of "4" key. If the side 1 is selected, SIDE 1 indicator of the SKA turns on.
- (j) If the value in item (h) or (i) is out of the specified range, refer to item (i) of "General method".
- (k) Eject the level disk.

4-4-9. Check of Resolution

(A) Equipment

- (1) Level disk
- (2) SKA or user's system
- (3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP7 and TP8 (Pre-amp.) on the PCBA MFD control.

Oscilloscope range : AC mode, 50mV ~ 0.1V

Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and ADD both channels.

(b) Start the spindle motor and install a level disk.

(c) Make the head move to the innermost track.

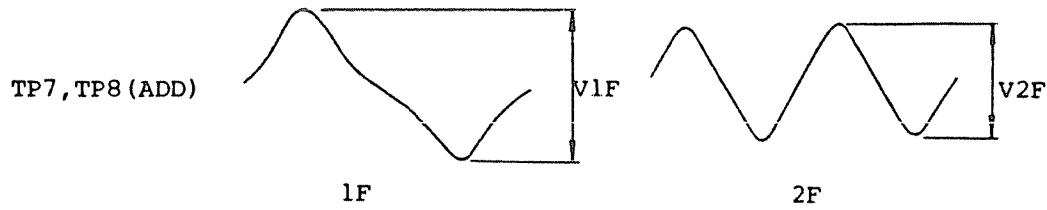
(d) Execute 1F write operation for one rotation of the disk (125KHz of WRITE DATA frequency).

(e) Measure the average amplitude (V1F) as in Fig.424.

(f) Execute 2F write operation as in item (d) (double in frequency to that in item (d)).

(g) Measure the average amplitude (V2F) as in Fig.424.

(h) Calculate the resolution by substituting the following expression with the measured values V1F, V2F, and RESOLUTION calibration value (see level disk label).



(Fig.424) Measurement of resolution

Resolution (true value) = $V2F/V1F \times 100/\text{Calibration value } (\%)$

(i) Confirm that the true value is within the following range.

Innermost track resolution: 55%, Min.

(j) For a double sided FDD, execute items (d) through (i) for the side 0 and the side 1 heads respectively.

(k) If the value in item (i) or (j) is out of the specified range, following causes are assumed.

i) Inferior disk:

Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

ii) Inferior disk rotational speed:

Check and adjust according to item 4-4-5.

iii) Inferior head touch:

Check and adjust according to item 4-4-6.

iv) Inferior head: Replace the head carriage Ass'y according to item 4-5-1.

v) Inferior PCBA MFD control:

Replace the PCBA MFD control according to item 4-5-6.

(L) Eject the level disk and release the Invert and Add modes of the oscilloscope.

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Install a level disk.

(d) Execute drive select by key "0". (DSO indicator turns on).

(e) Key in "C0" and confirm that the TRACK indication becomes "00".
(RECALIBRATE)

(f) Key in "C1". (SEEK TMAX)

(g) Key in "D8". (RESOLUTION)

The calibration value of the level disk should be set previously in the SKA.

(h) Confirm that the DATA indicator (%) indicates the value within the following range.

Innermost track resolution: 55%, Min.

(i) For a double sided FDD, depress key "4" and execute items (g) and (h) for the side 0 head and the side 1 head respectively. The side is changed alternately by a depression of "4" key. If the side 1 is selected, SIDE 1 indicator of the SKA turns on.

(j) If the value in item (h) or (k) is out of the specified range, refer to item (k) of "General method".

(k) Eject the level disk.

4-4-10. Check and Adjustment of Track Alignment

(A) Equipment

- (1) Cross point screwdriver, M3
- (2) Common screwdriver, medium
- (3) Alignment disk
- (4) \SKA or user's system
- (5) Oscilloscope
- (6) Hygrometer.
- (7) Locking paint

(B) Check and adjustment procedure

Note: Check and adjustment of track alignment should be done in an environment of general room temperature and humidity. Even if the environmental condition is within the specified operational condition, extremely high or low temperature, or extremely high or low humidity should be avoided. Check and adjustment should be done after two hours, Min. of storing in the above mentioned condition.

It is recommended that the orientation of the FDD for the track alignment check is the same as when the FDD is actually installed in the user's system.

(1) General method

- (a) Use two channels of an oscilloscope and connect them to TP9 and TP10 (Differentiation amp.) on the PCBA MFD control. Also connect the external trigger of the oscilloscope to TP4 (Index) and apply positive trigger.

Oscilloscope range : AC mode, 0.5V, 20msec

Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and Add both channels.

(b) Start the spindle motor and install an alignment disk.

(c) Set the head to the alignment check track.

Alignment check track: track 16

(d) Confirm that two lobe patterns as in Fig.425 can be observed (it is not necessary that the levels of VA and VB are equal).

If only one lobe pattern can be observed or if two lobes become one pattern, the head is not on the alignment check track.

In such event, execute step-out or step-in operation for 2 tracks space to obtain the most similar waveform to that in Fig.425.

Note: The above number of tracks to be stepped is required to make the alignment track position be fit with the magnetized condition of the basic magnetized phase "A" of the stepping motor. If the stepped track numbers are inassured, set it again from track 00 (TRACK 00 output signal becomes TRUE).

For the FDD, the lobe pattern as in Fig.425 should be observed at the track of even number.

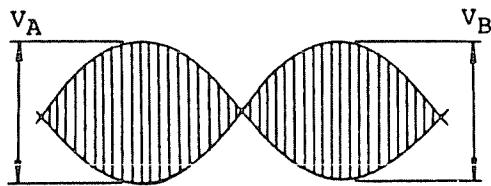
(e) After one or several step-outs from the check track, step in the head to the check track again and measure VA and VB at that time.

(f) Calculate the true value of misalignment by substituting the value in item (e) and ALIGNMENT calibration value (see alignment disk label, attention to the side).

$$\text{Misalignment (true value)} = \frac{\text{VA-VB}}{\text{Larger value in VA & VB}} \times 100 - \text{Calibration value} - (\text{Relative humidity} - 50) \times K$$

K is humidity compensation factor.

K = 0.26



(Fig.425) Alignment check lobe pattern

e.g. VA=0.58V, VB=0.61V, Calibration value= -6(%),
Relative humidity=65%

$$\text{Misalignment (true value)} = \left\{ \frac{0.58 - 0.61}{0.61} \times 100 - (-6) \right\} - (65-50) \\ \times 0.26 \approx -2.8\%$$

If the calculated value is positive, the magnetic head is shifted inward from the reference position, while the head is shifted outward from the reference position when the value is negative.

- (g) Conversely, measure VA and VB when the head is on the alignment check track by stepping-out after one or several step-ins.
- (h) Calculate the true value of misalignment as described in item (f).
- (i) Confirm that both of the calculated values in items (f) and (h) are within the following range.
True value of misalignment: 30%, Max.
- (j) For a double sided FDD, execute items (c) through (i) for the side 0 and the side 1 heads respectively.
- (k) If the value in item (i) or (j) is out of the specified range, adjust the track alignment according to the following procedure:
 - i) Loosen two fixing screws of the stepping motor a little.

- ii) Insert a common screwdriver from the back side of the FDD as shown in Fig.426 and depress it to the geared area of the stepping motor.
- iii) Repeat step-in and step-out operations and adjust the misalignment to be the smallest on the alignment check track during both step-in and step-out operations by the screwdriver (stepping motor moves little by little).

Note: When you adjust the alignment by observing the lobe pattern using the oscilloscope, pay attention to the calibration value on the alignment disk label and the ambient relative humidity.

- ① Calibration value + (Relative humidity - 50) $\times K \geq 0$:
 When the left side lobe pattern level, VA is assumed as "1", lobe pattern ratio should be so adjusted that the right side lobe pattern level VB takes the following value:

$$VB = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

- ② Calibration value + (Relative humidity - 50) $\times K \leq 0$:
 When the right side lobe pattern level, VB is assumed as "1", lobe pattern ratio should be so adjusted that the left side lobe pattern level VA takes the following value.

$$VA = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

e.g. Calibration value = -6%, Relative humidity = 35% :

$$-6 + (35 - 50) \times 0.26 = -9.9 < 0$$

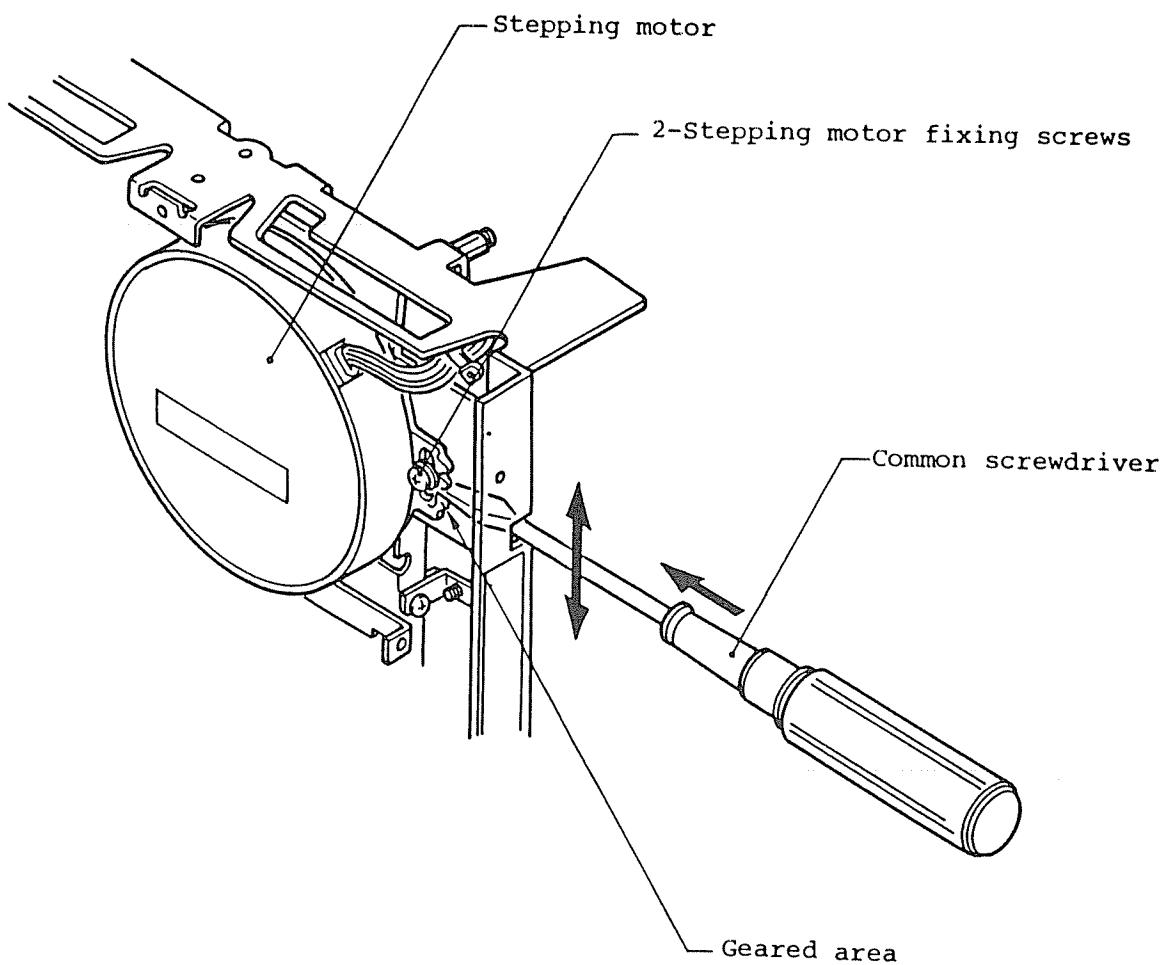
$$VA = 1 - \frac{-6 + (35 - 50) \times 0.26}{100} \approx 0.90$$

- iv) For a double sided FDD, repeat the adjusting operation in item iii) alternately for the side 0 and the side 1 heads until the both

misalignment take the smallest value.

- v) Tighten the two fixing screws of the stepping motor little by little for adjusting the true value of misalignment after tightening the screws with the following specified torque to be within $\pm 20\%$.
Stepping motor fixing torque: 9Kg.cm
- vi) Remove the alignment disk.
- vii) Apply a drop of locking paint to the head of the stepping motor fixing screws.
- viii) Check and adjust the track 00 sensor according to item 4-4-11.
- ix) Check and adjust the track 00 stopper according to item 4-4-12.

(L) Release the Invert and Add modes of the oscilloscope.



(Fig.426) Adjustment of track alignment

(2) SKA method

- (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Use two channels of an oscilloscope. Connect the 1st channel to the DOUT terminal of the SKA and the 2nd channel to the DIF terminal of the SKA. Apply positive trigger by DOUT terminal.
Oscilloscope range
 - The 1st channel: DC mode, 2V, 20msec
 - The 2nd channel: AC mode, 1V, 20msec
- (c) Key in "B9F" (INDEX observation)
- (d) Start the spindle motor by key "5". (MON indicator turns on).
- (e) Install an alignment disk.
- (f) Execute drive select by key "0". (DSO indicator turns on).
- (g) Key in "C0" and confirm that the TRACK indicator becomes "00".
(RECALIBRATE)
- (h) Set the head to the alignment check track.
Key in "C2 16" and confirm that the TRACK indication becomes "16".
- (i) Confirm that two lobe patterns as in Fig.425 can be observed by the oscilloscope (it is not necessary that the levels of VA and VB are equal).
If only one lobe pattern can be observed or if two lobes become one pattern, the head is not on the alignment check track.
In such event, execute step-in or step-out operation for 2 track space to obtain the most similar waveform to that in Fig.425. Step operation can be done by key "8" (STEP-IN) and key "9" (STEP-OUT).

By a depression of these keys, head will move for one track space.

Note: The above number of tracks to be stepped is required to make the alignment track position be fit with the magnetized condition of the basic magnetized phase "A" of the stepping motor.

For the FDD, the lobe pattern as in Fig.425 should be observed at the track of even number.

(j) Confirm that the H GAIN indicator of the SKA is off. If it is on, turn it off by depressing "DD" key.

(k) Key in "E3" (ALIGNMENT)

Calibration value of the alignment disk and environmental relative humidity should be set previously in the SKA.

(L) Confirm all the indications on the DATA (%) indicator are within $\pm 30\%$.

The initial digit of the DATA indicator is the symbol. + (+) mark indicates that the head is shifted inward from the reference position, while - mark indicates that the head is shifted outward.

(m) For a double sided FDD, execute the same check for the side 1 head according to the following procedure.

i) Key in "0" following the operation of item (L) (during execution of E3 command) and confirm that SIDE 1 indicator of the SKA turns on.

ii) Confirm as in item (L).

Note: In order to change the head to side 0, key in "0" again.
(SIDE 1 indicator turns off).

(n) Depress "F" key (STOP).

(o) If the value in items (L) or (m) is out of the specified range, adjust

the track alignment according to the following procedure.

- i) Loosen the two fixing screws of the stepping motor a little.
 - ii) Insert a common screwdriver from the back side of the FDD as shown in Fig.426 and depress it to the geared area of the steppint motor.
 - iii) Key in "E3" and adjust the misalignment so that the DATA indicator  (%) shows the smallest value. The stepping motor moves little by little by the screwdriver.
 - iv) For a double sided FDD, repeat the adjusting operation in item iii) alternately for side 0 and side 1 heads until the both misalignment take the smallest value.
 - v) Tighten the two fixing screws of the stepping motor little by little to obtain the value within ±20% on the DATA indicator when the screws are tightened with the following specified torque.
Stepping motor fixing torque: 9Kg.cm.
 - vi) Remove the alignment disk.
 - vii) Apply a drop of locking paint to the screw head of the stepping motor fixing screws.
 - viii) Check and adjust the track 00 sensor according to item 4-4-11.
 - ix) Check and adjust the track 00 stopper according to item 4-4-12.
- (p) Release the Invert and Add modes of the oscilloscope.

4-4-11. Check and Adjustment of Track 00 Sensor

(A) Equipment

- (1) Common screwdriver, M3
- (2) Work disk
- (3) Alignment disk
- (4) SKA or user's system
- (5) Oscilloscope (or digital voltmeter)
- (6) Locking paint

(B) Check and adjustment procedure

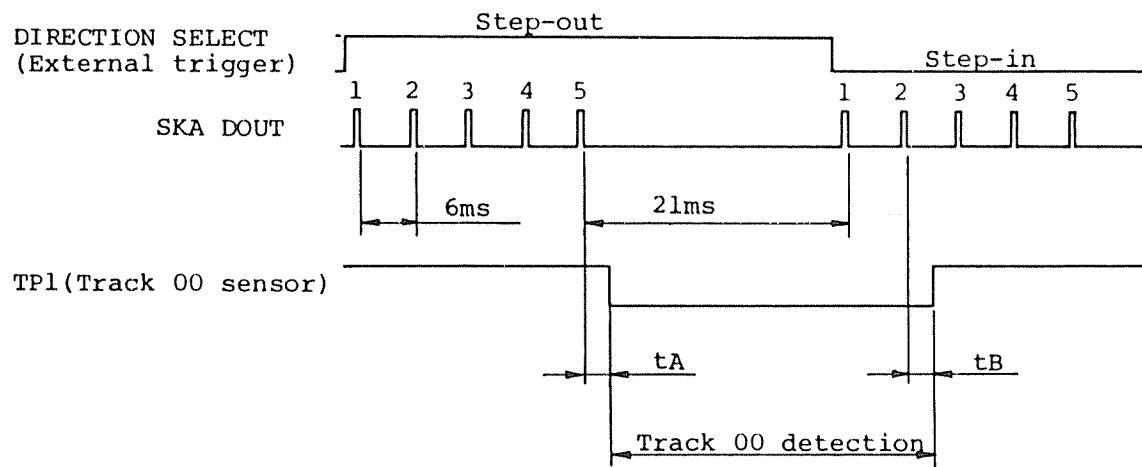
(1) General method

- (a) Use two channels of an oscilloscope and connect them as follows:
 - i) The 1st channel: STEP interface signal (pin No.20) or PCBA MFD control U4, pin 5.
 - ii) The 2nd channel: PCBA MFD control TPl (Track 00 sensor).
1V range
 - iii) External trigger: DIRECTION SELECT interface signal (pin No.18)
or PCBA MFD control U4, pin 11.
(+) trigger
- (b) Start the spindle motor and install a work disk.
- (c) Make the head move to track 00.
- (d) Confirm that the timings tA and tB of the Track 00 sensor signal (TPl) is within the following range when the DIRECTION SELECT (trigger signal) and the STEP signal (6ms interval) as shown in Fig.427 is supplied.

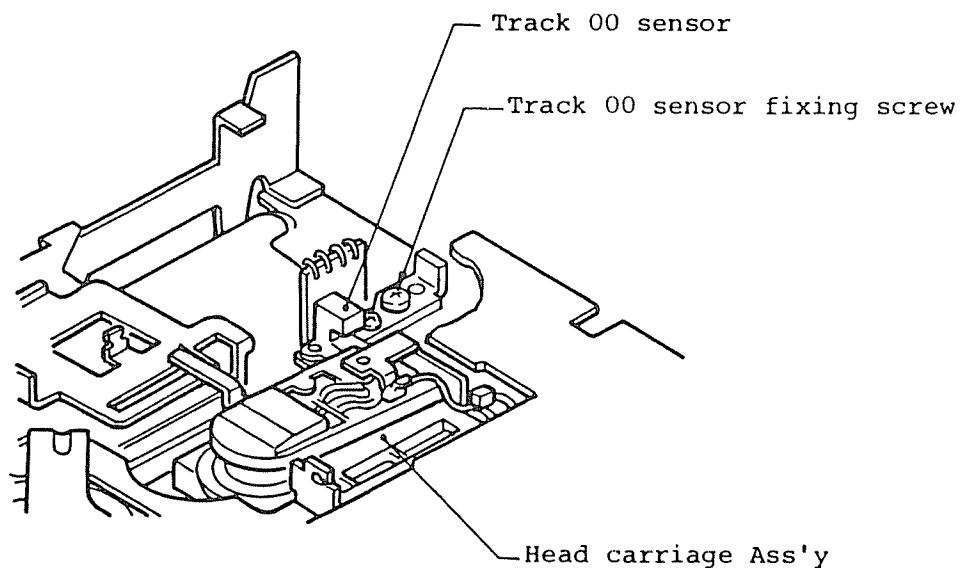
TP1 tA: 3.1 ~ 5.4msec

TP1 tB: 0 ~ 5.8msec

- (e) If the value in item (d) is out of the specified range, adjust the position of the track 00 sensor according to the following procedure.
- i) Loosen the fixing screw of the track 00 stopper (see Fig.429 and shift the stopper in the step-out direction (make apart from the rear side of the head carriage).
 - ii) Connect an oscilloscope to TP9 or TP10 (Differentiation amp.) of the PCBA MFD control.
Oscilloscope range: AC mode, 0.2V, 20msec
 - iii) Install an alignment disk. The track alignment should be adjusted correctly according to item 4-4-10.
 - iv) Make the head move to the position where the lobe pattern as in Fig.425 can be observed.
 - v) Remove the alignment disk.
 - vi) Step out the head for 16 tracks' space. (The head moves to track 00).
 - vii) Change the connection of the oscilloscope as item (a).
 - viii) Loosen the fixing screws of the track 00 sensor (see Fig.428) and move the sensor a little so that the timing tA in Fig.427 falls within the following range.
Adjusting target of TP1 tA: 3.4 ~ 4.6msec
 - ix) Repeat the adjustment of the track 00 sensor position so that the value in item viii) satisfy the specification when the screw has been tightened with the specified torque.
 - x) Apply a drop of locking paint on the fixing screw head.
 - xi) Adjust the track 00 stopper according to item 4-4-12.



(Fig.427) Track 00 sensor waveform



(Fig.428) Adjustment of track 00 sensor

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Use two channels of oscilloscope and connect them as follows:

i) The 1st channel: SKA DOUT terminal

DC mode, 5V, 10msec

ii) The 2nd channel: PCBA MFD control TPl (Track 00 sensor), 1V range

iii) External trigger: DIRECTION SELECT interface signal (Interface connector pin No.18) or Pin 3 of J3 (resistor network RAl for terminator) on the PCBA MFD control.

(+) trigger.

(c) Key in "B8 F". (STEP observation)

(d) Start the spindle motor by key "5". (MON indicator turns on).

(e) Install a work disk.

(f) Execute drive select by key "0". (DS0 indicator turns on).

(g) Set the step rate and the settling time as follows referring to item 4-2-4-3.

Step rate : 6msec

Settling time : 15msec

(h) Key in "C0" and condirm that the TRACK indicator becomes "00".

(i) Key in "C5". (TOC TIMING, SEEK 15)

(j) Measure the tA and tB timings according to Fig.427 and confirm the

timings are within the following range:

tA: 3.1 ~ 5.4msec

tB: 0 ~ 5.8msec

(k) Key in "F". (STOP)

- (L) Turn the FD PWR switch of the SKA off at the track 00 position and then set it again to the PSA side. Confirm that the stop position of the head carriage did not change at power off and on.
- (m) If the value in item (j) or (L) is out of the specified range, adjust the position of the track 00 sensor according to the following procedure.
- i) Loosen the fixing screw of the track 00 stopper (see Fig.429) and shift the stopper in the step-out direction (make apart from the rear side of the head carriage).
 - ii) Connect the 2nd channel of the oscilloscope to TP9 or TP10 (Differentiation amp.) of the PCBA MFD control and change the trigger to this channel.
Oscilloscope range: AC mode, 0.2V, 20msec
 - iii) Install an alignment disk. The track alignment should be correctly adjusted according to item 4-4-10.
 - iv) Key in "C0" and confirm that the track indicator becomes "00". (RECALIBRATE).
 - v) Key in "C2 16" and confirm that two lobe patterns as in Fig.425 can be observed.
If normal lobe pattern cannot be observed, move the head to the track position where the typical lobe pattern can be observed by stepping in by key "8" or by stepping out by key "9".
 - vi) Remove the alignment disk.
 - vii) Key in "E4 16". (SET TRACK NUMBER)
 - viii) Key in "C2 00". (SEEK 00)
Don't key in "C0". (RECALIBRATE)

- ix) Change the connection of the oscilloscope as in item (b).
- x) Key in "C5". (TOO TIMING SEEK ±5)
- xi) Loosen the fixing screw of the track 00 sensor (see Fig.428) and adjust the sensor position so that the timing tA in Fig.427 falls within the following range.
Adjusting target of tA: 3.4 ~ 4.6msec
- xii) Repeat the adjustment so that the values in item xi) fall within the specified range when the fixing screw has been tightened with the specified torque.
- xiii) Apply a drop of locking paint to the fixing screw head.
- xiv) Adjust the track 00 stopper according to item 4-4-12.

4-4-12. Check and Adjustment of Track 00 Stopper

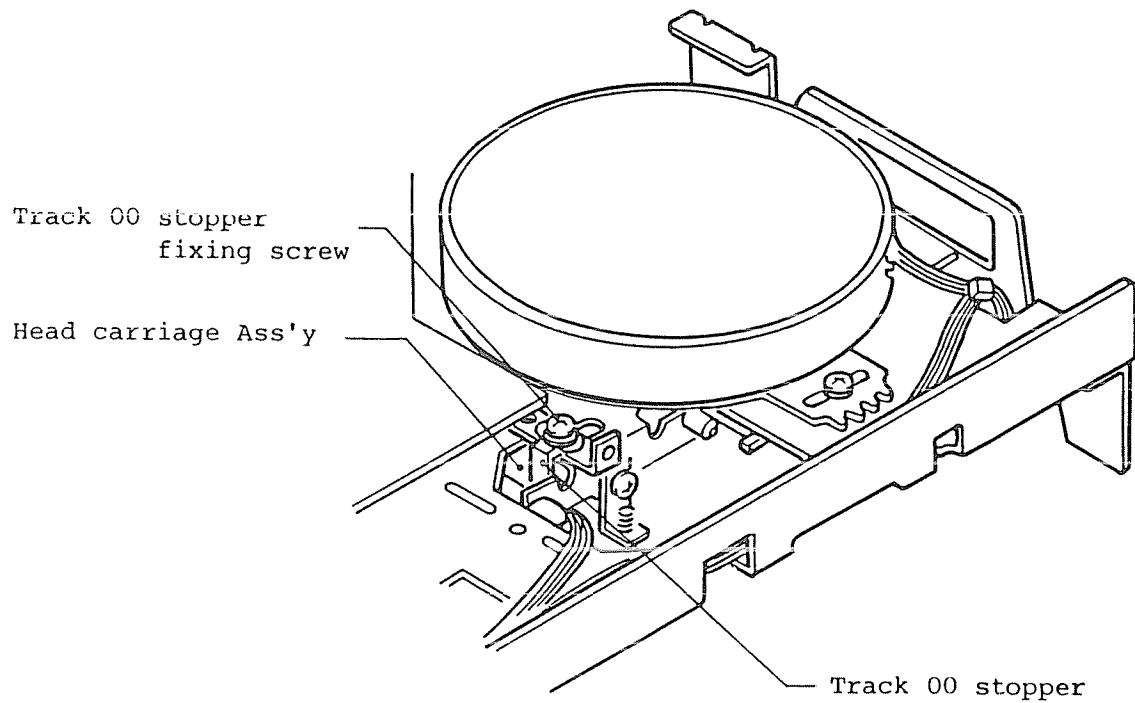
(A) Equipment

- (1) Cross point screwdriver, M3
- (2) SKA or user's system
- (3) Locking paint

(B) Check and adjustment procedure

(1) General method

- (a) Set the head to track 00.
- (b) Step out the head from the track 00 position.
- (c) Confirm that the head carriage does not move by the step-out command (head carriage rests on track 00).
- (d) Confirm that the gap between the head carriage and the extreme end of the track 00 stopper is 0.1 ~ 0.4mm. (See Fig.429).
- (e) Repeat step-in and step-out operations between track 00 and track 05. Confirm that no impact sound can be heard between the head carriage and the track 00 stopper.
- (f) Turn off the FDD power and depress the head carriage lightly against the track 00 stopper with fingers.
- (g) Confirm that the head carriage automatically returns to the initial position (track 00) when the power is turned on again.
- (h) If any one of the items (d), (e), and (g) is not satisfied, adjust the track 00 stopper position according to the following procedure.



(Fig. 429) Adjustment of track 00 stopper

- i) Set the head to track 00.
- ii) Loosen the fixing screw of the track 00 stopper. (See Fig.429).
- iii) Adjust the stopper position so that the gap between the stopper and the head carriage becomes 0.25mm, approx. And then tighten the screw with the specified torque.
- iv) Execute items (a) through (g).
- v) Apply a drop of locking paint on the fixing screw head.

(2) SKA method

- (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Execute drive select by key "0". (DS0 indicator turns on).
- (c) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE).
- (d) Set the step rate and the settling time as follows referring to item 4-2-4-3.
 - Step rate : 6msec
 - Settling time : 15msec
- (e) Key in "9". (STEP OUT)
- (f) Confirm that the head carriage does not move even if "9" is keyed in (head carriage rests on track 00).
- (g) Confirm that the gap between the head carriage and the extreme end of the track 00 stopper is 0.1 ~ 0.4mm. (See Fig.429).
- (h) Key in "C0" and key in "C5". (STEP TIMING, SEEK ±5)
- (i) Confirm that no impact sound can be heard between the head carriage and the track 00 stopper.
- (j) Turn off the FD PWR switch of the SKA and depress the head carriage lightly against the track 00 stopper.
- (k) Confirm that the head carriage automatically returns to the initial position (track 00) when the FD PWR switch is set to the PSA side again.

(L) If any one of the items (g), (i), and (k) is not satisfied, adjust the track 00 stopper position according to the following procedure.

- i) Key in "C0" and confirm that the TRACK indicator becomes "00"
(RECALIBRATE)
- ii) Loosen the fixing screw of the track 00 stopper. (See Fig.429).
- iii) Adjust the stopper position so that the gap between the stopper and the head carriage becomes 0.25mm, approx.
And then tighten the screw with the specified torque.
- iv) Execute items (a) ~ (k).
- v) Apply a drop of locking paint on the fixing screw head.

4-4-13. Check and Adjustment of Index Burst Timing

(A) Equipment

- (1) Cross point screwdriver, M3
- (2) Alignment disk
- (3) SKA or user's system
- (4) Oscilloscope (not required when the SKA is used)
- (5) Locking paint

(B) Check and adjustment procedure

(1) General method

- (a) Use two channels of the oscilloscope. Connect the 1st channel to TP4 (Index) on the PCBA MFD control and the 2nd channel to TP7 or TP8 (Pre-amp.). Apply positive trigger by TP4.

Oscilloscope range

The 1st channel: DC mode, 2V, 50 μ sec

The 2nd channel: AC mode, 1V, 50 μ sec

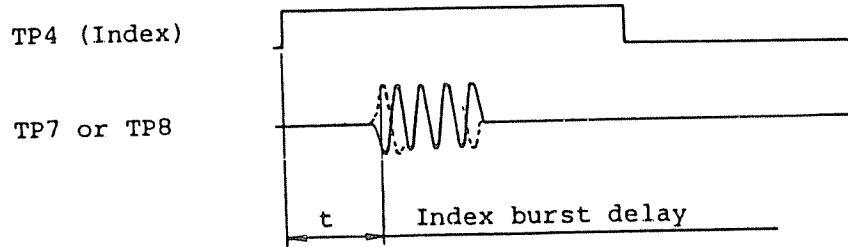
- (b) Start the spindle motor and install an alignment disk.

- (c) Set the head to track 01.

- (d) Measure "t" in Fig.430.

- (e) Substitute the following equation with the measured value in item (d) and INDEX TIMING calibration value (see alignment disk label).

Index burst timing (true value) = Measured value - Calibration value(μ s)



(Fig.430) Index burst timing

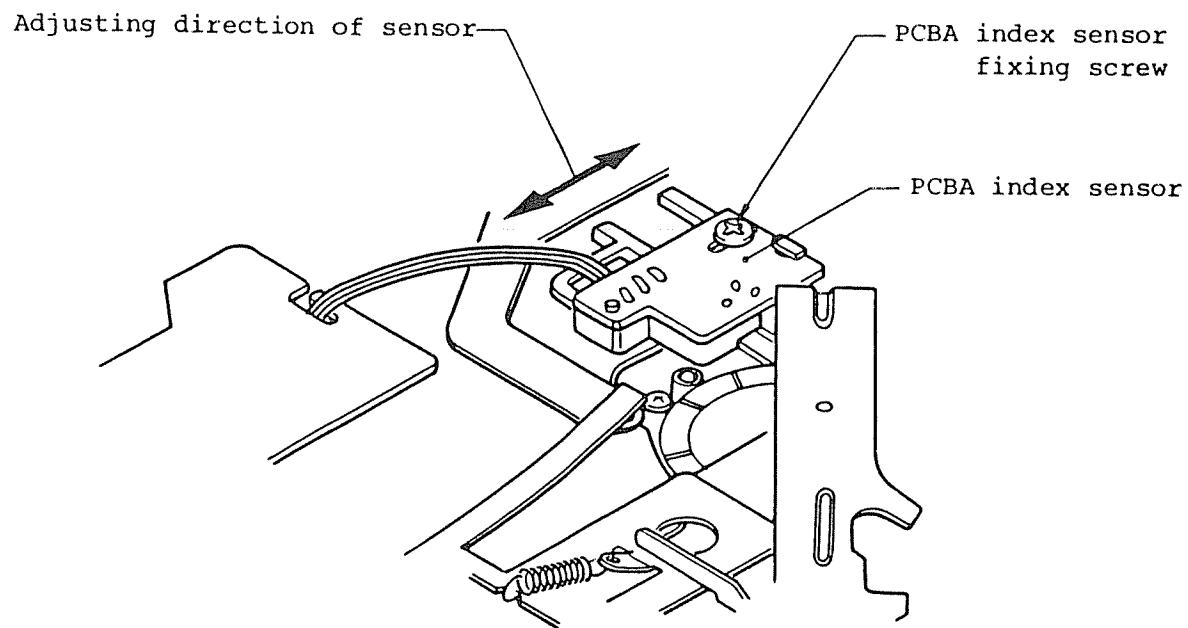
- (f) Confirm that the true value of the index burst timing is within the following range.

Index burst timing : $200 \pm 200 \mu\text{sec}$

- (g) If the value in item (f) is out of the specified range, adjust the index sensor Ass'y position according to the following procedure.

- i) Loosen the fixing screws (see Fig.431) of the PCBA index sensor and adjust its position to make the true value of the index burst timing fall in the specified range in item (f).
- ii) Repeat the adjustment so that the true value of the index burst timing falls in the range of item (f) when the fixing screw has been tightened with the specified torque.
- iii) Apply a drop of locking paint on the fixing screw head.

- (h) Remove the alignment disk.



(Fig.431) Adjustment of index sensor

(2) SKA method

- (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.
- (b) Start the spindle motor by key "5". (MON indicator turns on).
- (c) Install an alignment disk.
- (d) Execute drive select by key "0". (DSO indicator turns on).
- (e) Key in "C0" and confirm that the TRACK indicator becomes "00".
(RECALIBRATE)
- (f) Set the head to the index check track.
Key in "C2 01" and confirm that the TRACK indication becomes "01".
- (g) Key in "E6". (INDEX TIMING)
The calibration value of the index timing should be set previously in the SKA.
- (h) Confirm that the DATA indicator (μs) indicates the value within the following range.
Index burst timing: 200±200μsec
- (i) Key in "F". (STOP)
- (j) If the value in item (h) is out of the specified range, adjust the index sensor Ass'y position according to the following procedure.
 - i) Loosen the fixing screws (see Fig.431) of the PCBA index sensor and its position so that the DATA indication under execution shows the median value in the specified range of item (h).

- ii) Repeat the adjustment so that the DATA indication takes the median value when the fixing screw has been tightened with the specified torque.
 - iii) Depress "F" key. (STOP).
 - iv) Apply a drop of locking paint on the fixing screw head.
- (k) Remove the alignment disk.

4-5. MAINTENANCE PARTS REPLACEMENT

4-5-1. Replacement of Head Carriage Ass'y

(A) Tools

- (1) Cross point screwdriver, M3
- (2) Cross point screwdriver, M2.6
- (3) Hexagon wrench key, 1.5mm
- (4) Box screwdriver for hexagon nut, M3
- (5) A pair of tweezers
- (6) Lubricant, Kantoh Kasei 946P
- (7) Alcohol and gauze (several sheets)
- (8) Locking paint
- (9) SKA or user's system

(B) Replacement procedure

- (1) Turn the front lever (Fig.505, No.42) to close position and remove the fixing screw (Fig.505, S11).
- (2) Turn the front lever to open position and draw out the front lever Ass'y.
- (3) Remove the fixing screws (Fig.505, S5) of the front bezel Ass'y (Fig. 505, No.41) to remove the Ass'y.
- (4) Remove the fixing screw (Fig.505, S1) of the cord clamper to remove the clamper (Fig.505, No.39).
- (5) Remove two fixing screws (Fig.505, S1) of the shield cover (Fig.505, No.44) to remove the cover.
- (6) Remove three fixing screws (Fig.505, No.37 and S1) of the PCBA MFD

control (Fig.505, No.35) and lift it up.

- (7) Disconnect all of the connectors mounted on the PCBA MFD control and remove the PCBA.
- (8) Pull out the head cable from the disk guide U-groove and cable clamper and draw it out to the head carriage Ass'y (Fig.505, No.13) side.
- (9) Holding the top of the band fixing plate B (Fig.505, No.17) and the head carriage Ass'y with your fingers to release the hook of the steel belt (Fig.505, No.19) and the band fixing plate B.
- (10) Pull out the band fixing plate B and the band spring (Fig.505, No.18) at the same time from the head carriage Ass'y.
- (11) Separate the steel belt from the hook of the band fixing plate A (Fig.505, No.16) to remove the band fixing plate A from the head carriage Ass'y.
When removing the band fixing plate A from the head carriage, it will be removed easily if it is shifted toward the front bezel side and then drawn out in a right angle.
- (12) Remove the belt fixing screw (Fig.505, S8) on the capstan of the stepping motor Ass'y (Fig.505, No.12) and then remove the band washer (Fig.505, No.20) and the steel belt.
- (13) Remove one of the two guide shaft clips (Fig.505, No.15) which fix the guide shafts. The clip for the rear side one should be removed.
- (14) Draw out two guide shafts (Fig.505, No.14) toward the rear of the FDD and remove them from the fixing area of the front side chassis (Fig.505, No.1).
Then remove the head carriage Ass'y with two guide shafts and the front

side clip. Refer to Fig.432.

(15) Draw out two shafts from the head carriage and remove the front guide shaft clip.

(16) Prepare a new head carriage Ass'y and two guide shafts for installation.

Note: When replacing the head carriage Ass'y, replace the guide shafts at the same time because of matching the hole diameter of the carriage with that of the guide shaft. Guide shafts are to be designated in combination with the head carriage Ass'y. (Refer to item 4-1-3, (2)).

Guide shaft which goes through the hole of the head carriage smoothly with a little clearance is considered to be the best.

(17) Apply specified lubricant to the surface of one guide shaft. Then install it again to the new head carriage as it was.

Note: When applying the lubricant to the guide shaft, dip a piece of gauze to the lubricant and wipe the shaft and then wipe it again lightly with a dry and clean gauze.

The most appropriate quantity of the lubricant for the surface of the shafts forms a thin oil coating.

(18) Apply the lubricant to the another guide shaft and install it to the new head carriage as it was.

(19) Attach the guide shaft clip to the front bezel side groove of the shafts.

(20) Attach the new head carriage Ass'y in item (19) in the reverse order of items (13) and (14).

Note: Pre-load is applied between the two guide shafts to make them approach each other by the guide shaft clip in order to reduce the

variety of the installation position of the head carriage Ass'y.
For installing the two guide shafts to the chassis, mount them with
pressure to separate them.

- (21) Install the steel belt (C) to the capstan of the stepping motor Ass'y
in the reverse order of item (12).

Note: If the surface of steel belt or capstan is smeared, clean it
carefully with alcohol and gauze.

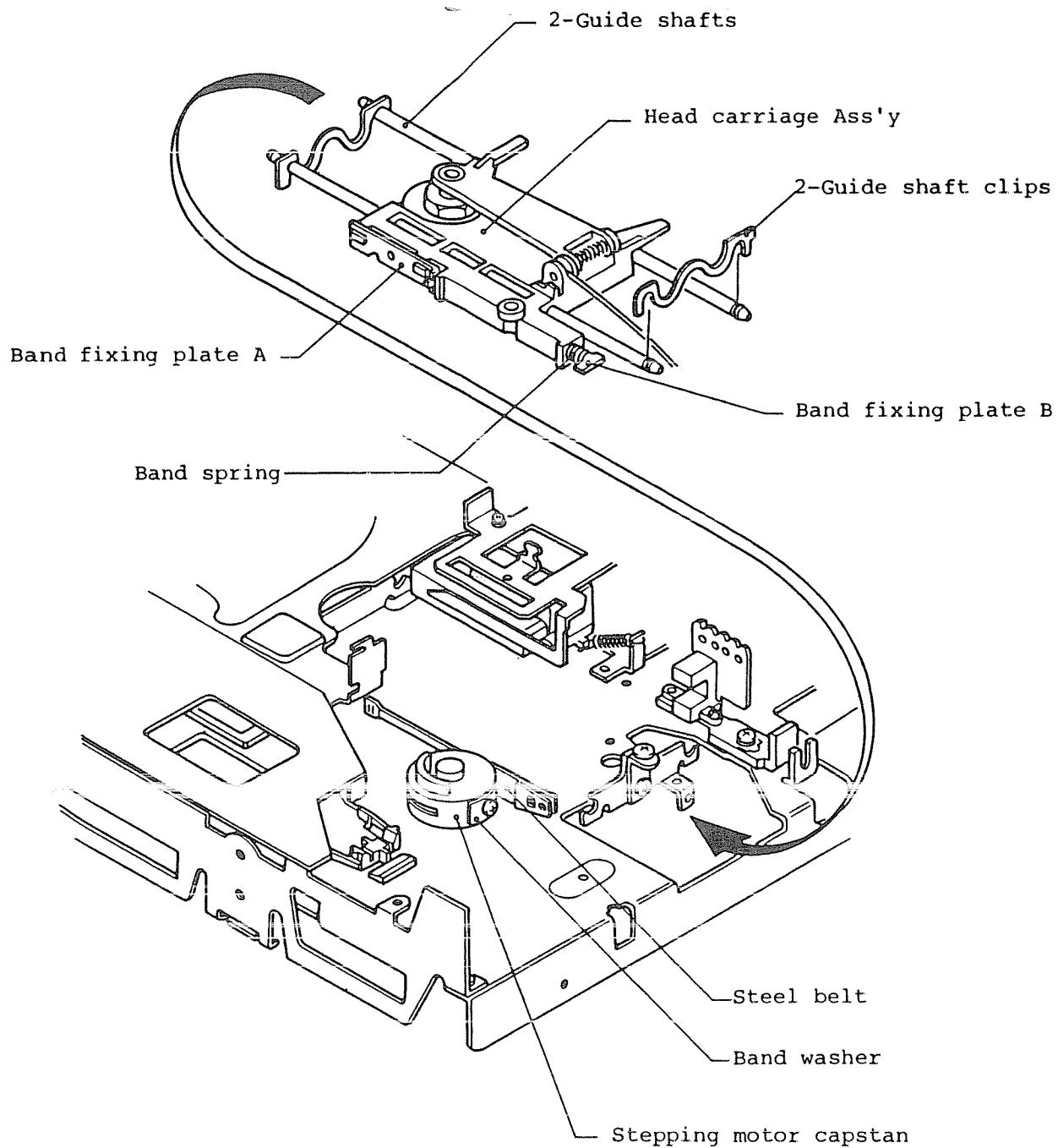
- (22) Connect the steel belt to the head carriage Ass'y using the band fixing
plates A and B and band spring in the reverse order of items (9) through
(11).
- (23) Tighten the fixing screw of the steel belt slightly to the stepping
motor Ass'y.
- (24) After moving the head carriage several times manually, tighten the steel
belt fixing screw carefully with the specified torque. At this time,
be careful that the belt is tensioned straightly. Pay attention not to
damage the surface of the belt or the capstan.
- (25) Form the head cable in the reverse order of items (4) and (6) through
(8) and attach the PCBA MFD control. Refer to item 4-2-3 as to the
details of the head cable treatment.
- (26) Loosen the fixing screw (Fig.505, S4) of the track 00 stopper (Fig.505,
No.6) and shift the stopper toward the rear side of the FDD.
- (27) Attach the front lever temporarily for the following check and
adjustment.
- (28) Make the head seek continuously between the track 00 and the innermost
track and confirm that the steel belt does not meander nor undulate.

When the SKA is used, key in "C6" for this check and key in "F" for stop.

If the steel belt does meander or undulate, readjust the belt to run straightly by the screw in item (12). After the adjustment, tighten the screw carefully with the specified torque.

- (29) Check for the head touch according to item 4-4-6.
- (30) Check and adjust the asymmetry according to item 4-4-7. (Adjustment is applied only for the FDD with the variable resistor, R5 on the PCBA MFD control).
- (31) Adjust the track alignment according to item 4-4-10.
- (32) Adjust the track 00 sensor position according to item 4-4-11.
- (33) Adjust the track 00 stopper position according to item 4-4-12.
- (34) Check and adjust the index burst timing according to item 4-4-13.
- (35) Check for the read level according to item 4-4-8.
- (36) Check for the resolution according to item 4-4-9.
- (37) Attach the shield cover in the reverse order of item (5).
- (38) Remove the fixing screw of the front lever to remove the lever.
- (39) Attach the front bezel Ass'y and the front lever Ass'y in the reverse order of items (1) through (3).
- (40) Adjust the front lever position according to item 4-4-2.
- (41) It is recommended to connect the FDD to the system for overall test.

Refer to item 4-2-5 (1)).



(Fig.432) Replacement of head carriage Ass'y

4-5-2. Replacement of Stepping Motor Ass'y and Steel Belt

(A) Tools

- (1) Cross point screwdriver, M3
- (2) Cross point screwdriver, M2.6
- (3) Hexagon wrench key, 1.5mm
- (4) Box screwdriver for hexagon nut
- (5) A pair of tweezers
- (6) Alcohol and gauze
- (7) Locking paint
- (8) SKA or user's system

(B) Replacement procedure

- (1) Remove the shield cover (Fig.505, No.44) by removing the two fixing screws (Fig.505, S1).
- (2) Lift the PCBA MFD control (Fig.505, No.35) by removing the three fixing screws (Fig.505, No.37 and S1).
- (3) Disconnect all the connectors mounted on the PCBA MFD control and remove the PCBA.
- (4) Holding the top of the band fixing plate B (Fig.505, No.17) and the head carriage Ass'y with your fingers to release the hook of the steel belt (Fig.505, No.19) and the band fixing plate B.
- (5) Pull out the band fixing plate B and the band spring (Fig.505, No.18) at the same time from the head carriage Ass'y.
- (6) Separate the steel belt from the hook of the band fixing plate A (Fig.505, No.16) to remove the band fixing plate A from the head carriage Ass'y.

When removing the band fixing plate A from the head carriage, it will be removed easily if it is shifted toward the front bezel side and then drawn out in a right angle

- (7) Remove the belt fixing screw (Fig.505, S8) on the capstan of the stepping motor Ass'y (Fig.505, No.12) and then remove the band washer (Fig.505, No.20) and the steel belt.
- (8) Remove the stepping motor Ass'y by removing the fixing screws (Fig.505, S4).
- (9) Install a new stepping motor Ass'y as it was.
- (10) Fix a new α-shape steel belt temporarily to the capstan of the new stepping motor with the band washer and the screw in item (7).

Note: Fundamentally, the steel belt and the band spring should be replaced with the stepping motor. However, if there is no inferior points for these belt and spring, they may be used after cleaning the surface carefully with alcohol and gauze.

- (11) Connect the steel belt and the head carriage using the band fixing plates A and B and band spring in the reverse order of items (4) through (6).
- (12) After moving the head carriage several times manually, tighten the steel belt fixing screw in item (10) carefully with the specified torque. At this time, be careful so that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.
- (13) Install the PCBA MFD control in the reverse order of items (2) and (3).
- (14) Loosen the fixing screw (Fig.505, S4) of the crack or stopper (Fig.505, No.6) and shift the stopper toward the rear side of the FDD.

- (15) Make the head seek continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate. When the SKA is used, key in "C6" for this check and key in "F" for stop the operation.
- If the steel belt meanders or undulates, readjust the belt to run straightly by the screw in item (10). After the adjustment, tighten the screw carefully with the specified torque.
- (16) Execute the continuous seek operation for five minutes. When the SKA is used, key in "C6" and key in "F" for stopping the operation.
- (17) Attach the shield cover with two fixing screws.
- (18) Adjust the track alignment according to item 4-4-10.
- (19) Adjust the track 00 sensor position according to item 4-4-11.
-
- (20) Adjust the track 00 stopper position according to item 4-4-12.

4-5-3. Replacement of DD Motor Ass'y (Spindle motor)

(A) Tools

- (1) Cross point screwdriver, M3
- (2) A pair of tweezers
- (3) Cutting pliers
- (4) SKA or user's system

(B) Replacement procedure

- (1) Remove the shield cover (Fig.505, No.44) by removing the two fixing screws (Fig.505, S1).
- (2) Disconnect the spindle motor connector (J7).
- (3) Cut and remove the cable tie (Fig.505, No.40) for binding the wiring. Throw away the removed cable tie.
- (4) Draw out the PCB holder (Fig.505, No.38) which holds the PCBA servo of the DD motor Ass'y (C) (Fig.505, No.7) from the chassis (Fig.505, No.1).
- (5) Remove three fixing screws (Fig.505, S2, S7) of the DD motor from the upper side of the FDD and remove the DD motor Ass'y from the lower side of the FDD.
- (6) Install a new DD motor Ass'y in the reverse order of items (2) through (5).

Notes: 1. The spindle area of the DD motor Ass'y (clamping cup of the disk) is precisely machined. For installing the motor to the frame, place the spindle in parallel to the frame and push into the frame slowly. Handle the spindle very carefully not to damage

the spindle surface.

2. Collar B (Fig.505, No.5) is attached to the screw of the disk insertion side. Confirm that the collar B is not taken out in the process of tightening the screw.

(7) Adjust the collet shaft plate (Fig.505, No.29) position according to item 4-4-1.

(8) Bind a new bundle of cables to the chassis made of DD motor cable, T00 sensor Ass'y cable, and front OPT Ass'y cable using a new cable tie.

(9) Check for the file protect sensor according to item 4-4-4.

(10) Check or adjust the disk rotation speed according to item 4-4-5.
(Adjustment is applied only for the motor with the variable resistor, R1 on the PCBA DD motor servo).

(11) Check and adjust the track alignment according to item 4-4-10.

(12) Check and adjust the index burst timing according to item 4-4-13.

(13) Attach the shield cover in the reverse order of item (1).

4-5-4. Replacement of Collet Ass'y

(A) Equipment

- (1) Cross point screwdriver, M3
- (2) A pair of tweezers
- (3) Locking paint
- (4) SKA or user's system

(B) Replacement procedure

- (1) Remove the shield cover (Fig.505, No.44) by removing the two fixing screws (Fig.505, S1).
- (2) Remove the collet shaft plate Ass'y (Fig.505, No.29) by removing two fixing screws (Fig.505, S3).

Note: For the drive with eject Ass'y (Option), remove the hooks of the eject spring A and eject spring B from the collet shaft plate. Then remove the collet shaft plate Ass'y.

- (3) Pull out the collet Ass'y (Fig.505, No.30) from the U-groove of the clamp spring (Fig.505, No.27) to remove it.
- (4) Install a new collet Ass'y in the reverse order. For installation at this step screw the collet shaft plate Ass'y temporarily.
- (5) Adjust the collet shaft plate position according to item 4-4-1.
- (6) Check and adjust the track alignment according to item 4-4-10.
- (7) Attach the shield cover in the reverse order of item (1).

4-5-5. Replacement of PCBA T00 Sensor

(A) Tools

- (1) Cross point screwdriver, M3
- (2) Cross point screwdriver, M2
- (3) A pair of tweezers
- (4) Cutting pliers
- (5) Locking paint
- (6) SKA or user's system

(B) Replacement procedure

- (1) Disconnect the track 00 connector (J4).
- (2) Cut and remove the cable tie (Fig.505, No.40) for binding the wiring.
Throw away the removed tie.
- (3) Remove the PCBA T00 sensor (Fig.505, No.9) by removing the fixing screw (Fig.505, S10).
- (4) Install a new PCBA T00 sensor in the reverse order of item (1) through (3).
- (5) Loosen the fixing screw (Fig.505, S6) of the T00 bracket (Fig.505, No.8) and shift it toward the rear side of the FDD.
- (6) Loosen the fixing screw (Fig.505, S4) of the track 00 stopper (Fig.505, No.6) and shift it toward the rear side of the FDD.
- (7) Adjust the track 00 position sensor according to item 4-4-11.
- (8) Adjust the track 00 stopper position according to item 4-4-12.

4-5-6. Replacement of PCBA MFD Control (C)

(A) Tools

- (1) Cross point screwdriver, M3
- (2) Box screwdriver for hexagon nut, M3
- (3) SKA or user's system

(B) Replacement procedure

- (1) Remove the shield cover (Fig.505, No.44) by removing two fixing screws (Fig.505, S1).
- (2) Remove three fixing screws of the PCBA MFD control (Fig.505, No.35) and lift up the PCBA.
- (3) Disconnect all of the connectors mounted to the PCBA MFD control and remove the PCBA.
- (4) Install a new PCBA MFD control in the reverse order of items (2) and (3).
- (5) Set the straps as they were on the old PCBA.
- (6) Check and adjust the asymmetry according to item 4-4-7. (Adjustment is applied only for the PCBA MFD control with the variable resistor, R5.)
- (7) Check for the read level according to item 4-4-8.
- (8) Check for the resolution according to item 4-4-9.
- (9) Check for the track 00 sensor according to item 4-4-11.
- (10) Attach the shield cover in the reverse order of item (1).

(11) It is recommended to connect the FDD to the system for overall test.
(Refer to item 4-2-5, (1)).

4-5-7. Replacement of Front OPT Ass'y

(A) Tools

- (1) Cross point screwdriver, M3
- (2) Hexagon wrench key, 1.5mm
- (3) Box screwdriver for hexagon nut, M3
- (4) Cutting pliers
- (5) Locking paint
- (6) SKA or user's system

(B) Replacement procedure

- (1) Turn the front lever (Fig.505, No.42) to close position and remove the fixing screw (Fig.505, S11).
- (2) Turn the front lever to open position and draw out the front lever Ass'y.
- (3) Remove the front bezel Ass'y (Fig.505, No.41) by removing two fixing screws (Fig.505, S5).
- (4) Remove the shield cover (Fig.505, No.44) by removing two fixing screws (Fig.505, S5).
- (5) Cut and remove the cable tie (Fig.505, No.40) for binding the wiring.
Throw away the removed tie.
- (6) Disconnect the front OPT connector (J5).
- (7) Draw out the cable from the space between the chassis (Fig.505, No.1) and the PCBA DD motor servo and then draw it out from the U-groove of the disk guide (Fig.505, No.3).
- (8) Remove two separate fixing screws (Fig.505, S1 and S5) of the front OPT

Ass'y (Fig.505, No.34) to remove the Ass'y.

- (9) Install a new front OPT Ass'y in the reverse order of item (6) through (8).
- (10) Check for the file protect sensor according to item 4-4-4.
- (11) Adjust the index burst timing according to item 4-4-13.
- (12) Form the cables as they were using a new cable tie.
- (13) Attach the shield cover in the reverse order of item (4).
- (14) Attach the front bezel Ass'y and the front lever Ass'y in the reverse order of items (1) through (3).
- (15) Adjust the front lever position according to item 4-4-2.

4-5-8. Replacement of Head Pad (Single sided only)

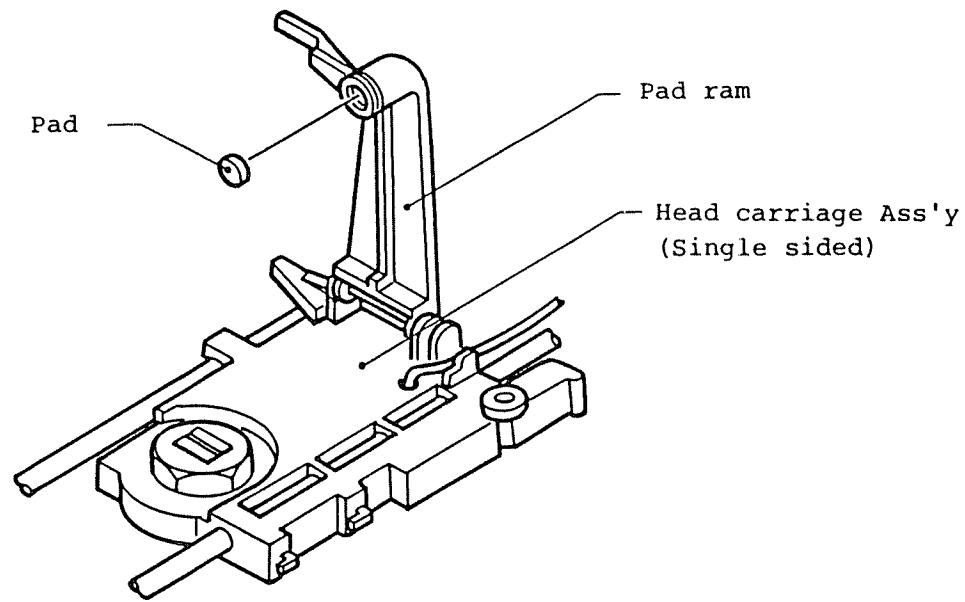
This item applies only to the single sided FDD.

(A) Tools

- (1) A pair of tweezers
- (2) Alcohol and gauze

(B) Replacement procedure

- (1) Remove the shield cover (Fig.505, No.44) by removing two fixing screws (Fig.505, S5).
- (2) Lift up the pad arm manually and peel the pad carefully with a pair of tweezers. (See Fig.433).
- (3) Apply a new pad to the initial position. Be careful not to press the pad surface strongly.
- (4) Clean the magnetic head surface according to item 4-3-2.
- (5) Adjust the head pad position according to item 4-4-6.
- (6) Check for the read level according to item 4-4-8.
- (7) Check for the resolution according to item 4-4-9.
- (8) Attach the shield cover in the reverse order of item (1).



(Fig.433) Replacement of head pad

4-5-9. Replacement of Front Bezel Ass'y

(A) Tools

- (1) Cross point screwdriver, M3
- (2) Hexagon wrench key, 1.5mm

(B) Replacement procedure

- (1) Turn the front lever (Fig.505, No.42) to close position and remove a fixing screw (Fig.505, S11).
- (2) Turn the front lever to open position and draw out the front lever Ass'y.
- (3) Remove the fixing screws (Fig.505, S5) of the front bezel Ass'y (Fig. 505, No.41) and draw out the front bezel.
- (4) Install a new front bezel Ass'y in the reverse order of item (2) and (3).

Note: For the installation of the front bezel, be sure to hold the four installation and support arms of the upper and the lower chassis (Fig.505, No.1 and No.21) and press the longitudinal sides of the bezel against the chassis and tighten the fixing screws with the specified torque.

- (5) Adjust the front lever position according to item 4-4-2.

4-5-10. Replacement of Front Lever Ass'y

(A) Tools

- (1) Hexagon wrench key, 1.5mm

(B) Replacement procedure

(1) Turn the front lever (Fig.505, No.42) to close position and remove a fixing screw (Fig.505, S11).

(2) Turn the front lever to open position and draw out the front lever Ass'y.

(3) Install a new front lever Ass'y in the reverse order.

Note: For installation of the front lever Ass'y, match the slot of the lever to the pin of the lever shaft.

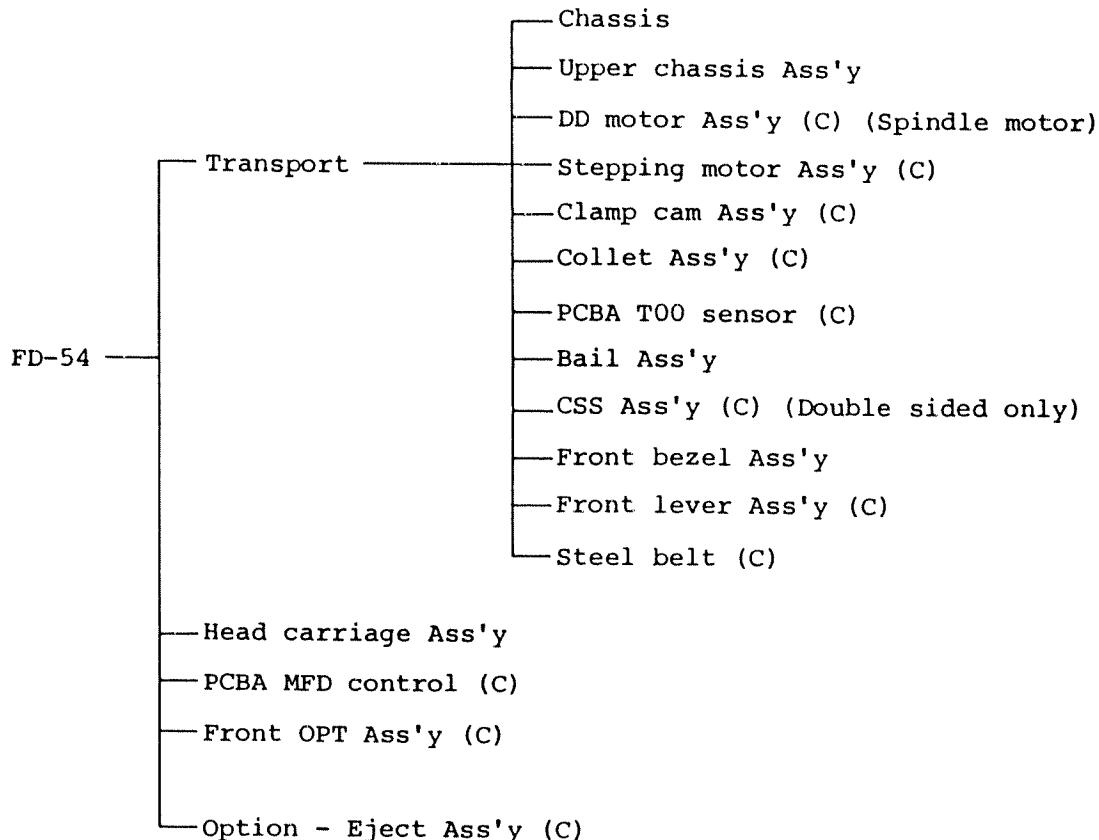
(4) Adjust the front lever position according to item 4-4-2.

SECTION 5

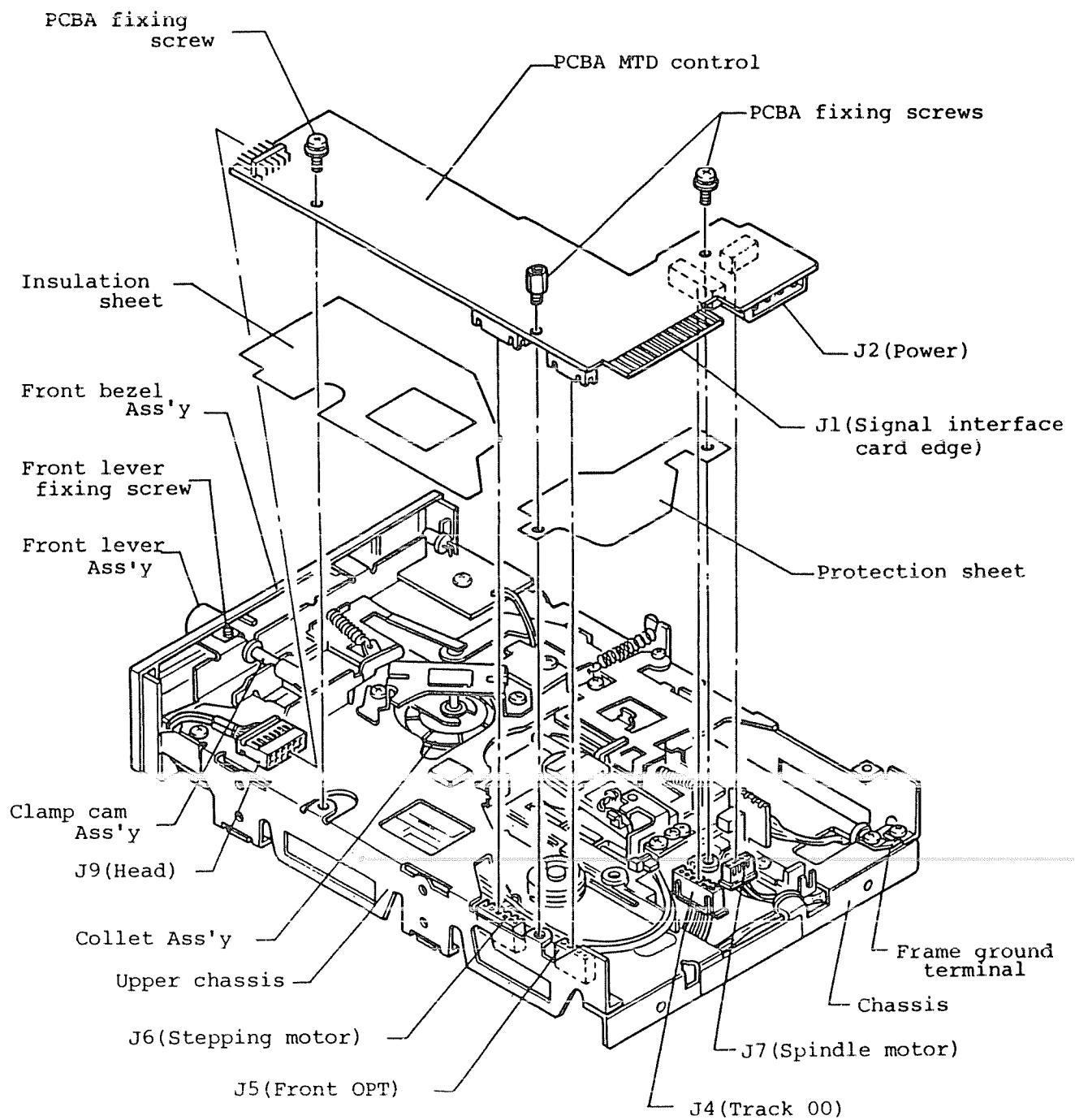
DRAWINGS & PARTS LIST

5-1. CONFIGURATION

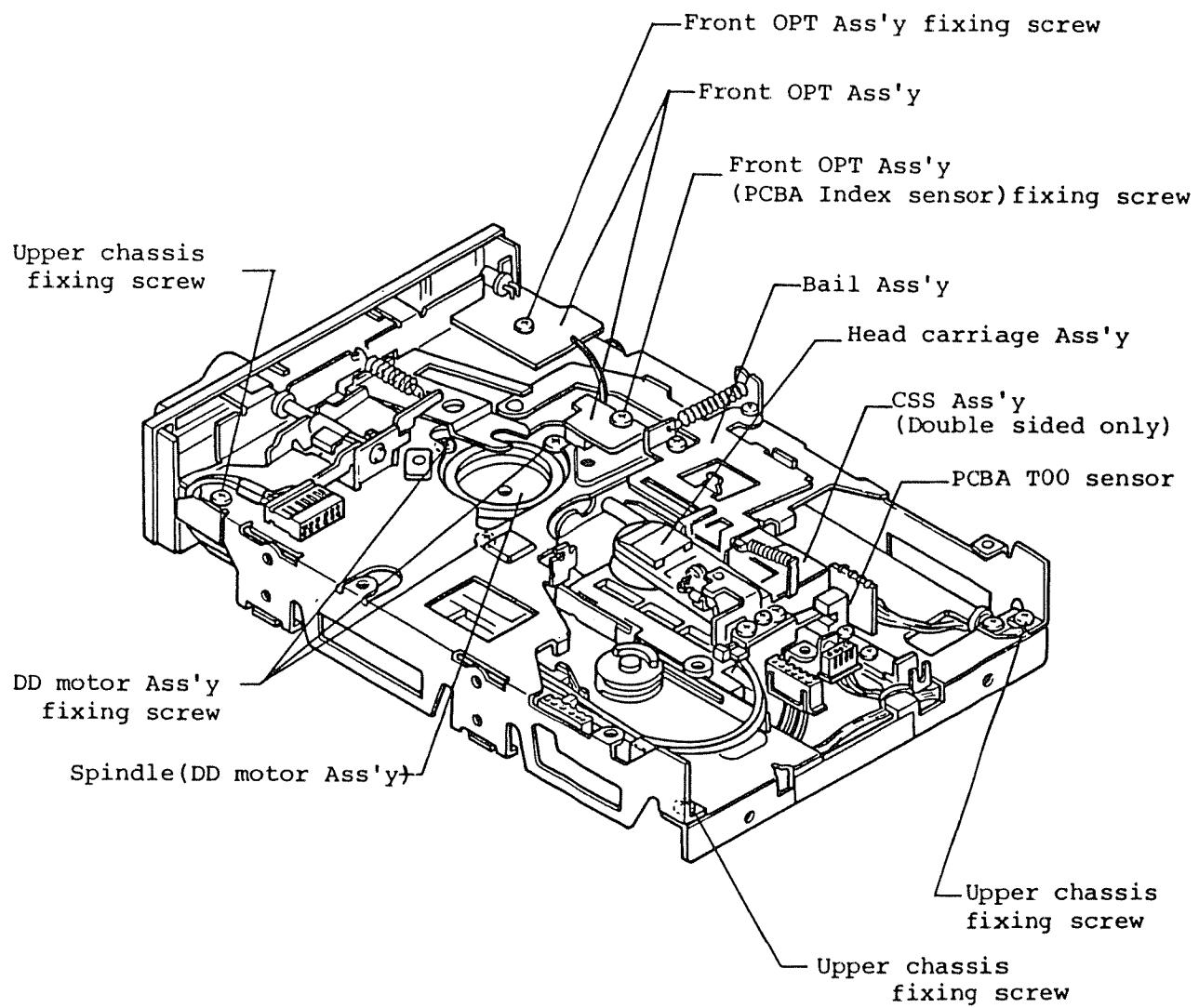
Following shows the configuration of the main parts of FD-54. (Refer to Fig.501 Fig.504). Refer to items 5-2 and 5-3 as to detailed break-downs.



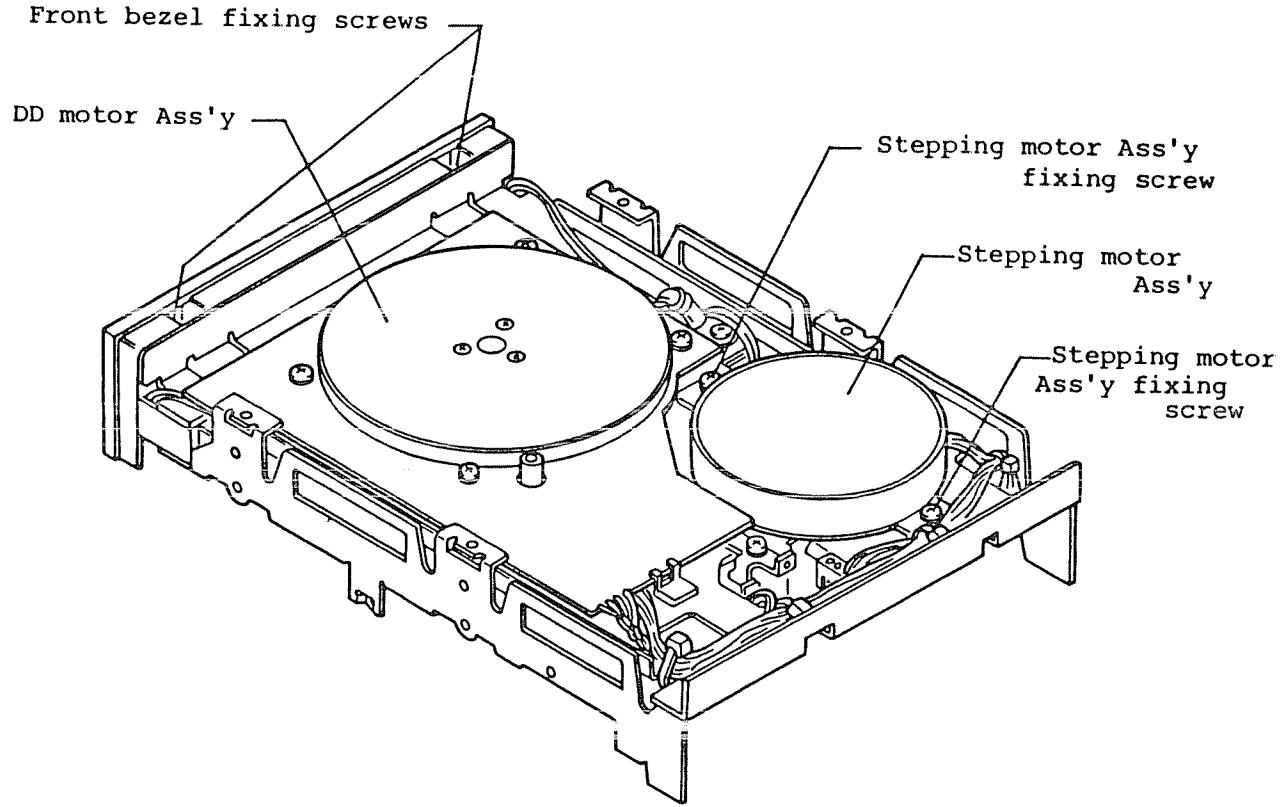
(Table 501) Main parts configuration of FD-54



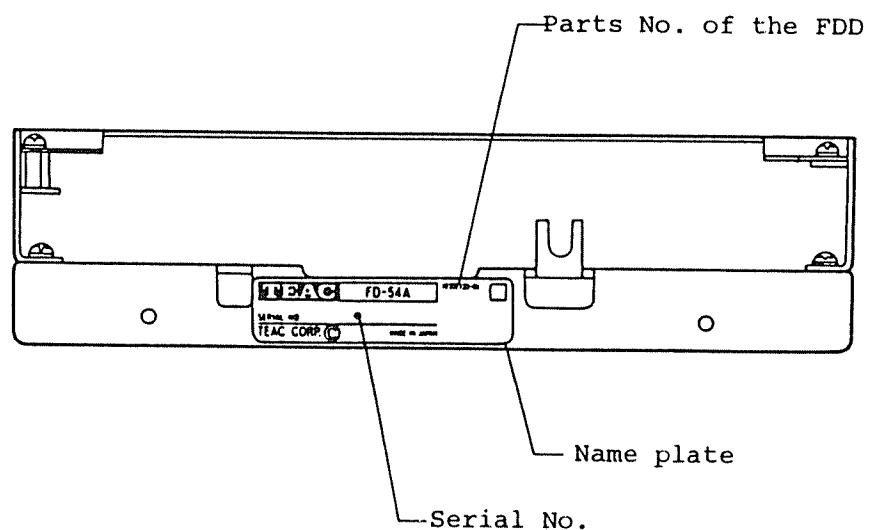
(Fig.501) External view (No.1)



(Fig.502) External view (No.2)



(Fig.503) External view (No.3)



(Fig.504) External view (No.4)

5-2. MECHANICAL BREAK-DOWN AND PARTS LIST

5-2-1. FDD (Refer to Fig.505)

Nos.	Parts Nos.	Parts name	Q'ty	Description
1	16152892-00	Chassis	1	
2	16802621-00	PCB fixing plate	1	
3	16787144-00	Disk guide	1	
4	16730435-00	Collar	2	
5	16730433-00	Collar B	1	
6	16802622-00	T00 stopper	1	
7	14733780-00	DD motor Ass'y(C)(Spindle motor)	1	
8	16757130-00	T00 bracket	1	
9	15532004-00	PCBA T00 sensor(C)	1	
10	17966927-00	CSS Ass'y(C)	1	FD-54B
11	13189135	Terminal	1	
12	14733770-00	Stepping motor Ass'y(C)	1	
13	17966912-00	Head carriage Ass'y(C)]*1	FD-54A
	17966663-00	Head carriage Ass'y(C)		FD-54B
14	16766631-XX	Guide shaft(C)	2	Note 4
15	16766638-00	Guide shaft clip	2	
16	16802624-00	Band fixing plate A	1	
17	16802623-00	Band fixing plate B	1	
18	16385130-00	Band spring	1	
19	16792300-00	Steel belt (C)	1	
20	16766636-00	Band washer	1	

(Table 502) FDD parts list (1/3)

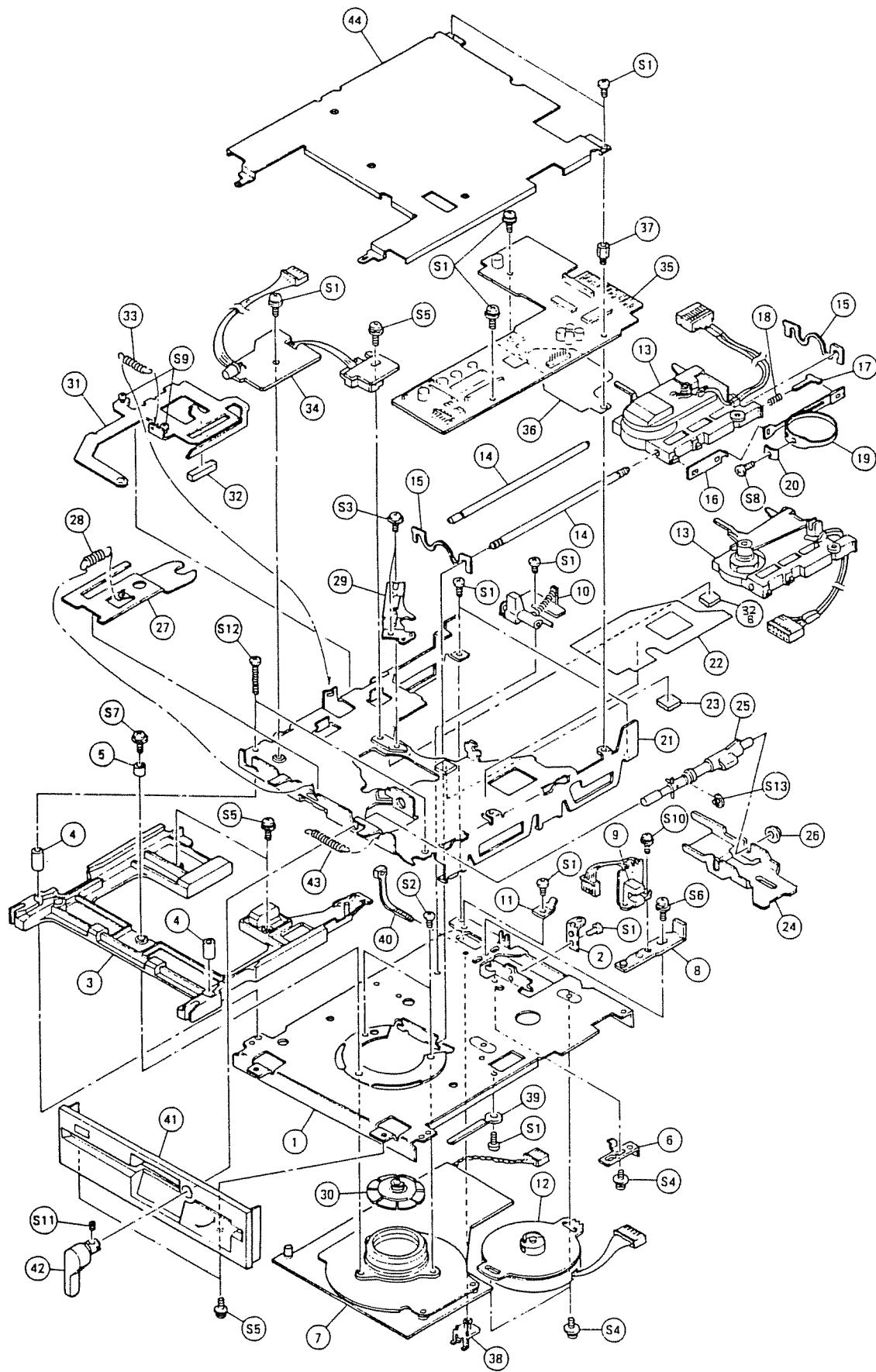
Nos.	Parts Nos.	Parts name	Q'ty	Description
21	16152891-00	Upper chassis	1	
22	16787150-00	Insulation sheet	1	
23	16787151-00	Disk pad B	1	Note 3
24	16802616-00	Set arm	1	
25	17966929-00	Clamp cam Ass'y(C)	1	
26	16787148-00	Clamp shaft holder	1	
27	16392019-00	Clamp spring	1	
28	16381104-00	Clamp return spring	1	
29	17966933-00	Collet shaft plate Ass'y	1	
30	17966923-00	Collet Ass'y(C)	1	
31	17966935-00	Bail Ass'y(A)	*1	FD-54A
	17966936-00	Bail Ass'y(B)		FD-54B
32	16787157-00	Disk pad A-2	1	Note 3
32B		Disk pad	1	Note 3
33	16381106-00	Disk pad lever spring	1	
34	15090730-00	Front OPT Ass'y(C)	1	
35	15532006-XX	PCBA MFD control(C)	1	Note 5
36	16787152-00	Protection sheet	1	
37	16730434-00	Fixing shaft	1	
38	16787149-00	PCB holder	1	
39	16322054-00	Cord clamper	1	
40	16362418-00	Cable tie	4	

(Table 502) FDD parts list (2/3)

Nos.	Parts Nos.	Parts name	Q'ty	Description
41	17966807-50	Front bezel Ass'y	1	Note 6
42	17966924-00	Front lever Ass'y(C)	1	Note 6
43	16381109-00	Front lever spring	1	
44	17966937-00	Shield cover Ass'y	1	

(Table 502) FDD parts list (3/3)

- Notes:
1. As to the parts with an asterisk in the Q'ty column, select appropriate one for the model.
 2. As to the parts with model name of FD-54 in the Description column, the parts is used only for the model.
 3. Disk pads are included in the Ass'y No.21 and No.31.
 4. Guide shafts are always used in combination with the head carriage Ass'y due to make the corresponding diameter match with the hole of the head carriage. When you replace the head carriage Ass'y, be sure to replace the guide shafts together.
 5. The parts number versions of the PCBA MFD control (C) are different depending on each model. Refer to the name plate on the actual PCBA installed to designate the same version.
 6. The parts numbers of the front bezel Ass'y and the front lever Ass'y are those of FD-54, standard color, black.



(Fig.505) Mechanical section break-down

5-2-2. Screw, Washer

Nos.	Parts Nos.	Parts name	Description
S1	16410304	Screw,bind,3x4,S,ZMC	
S2	16411304	Screw,bind,3x4, B,BNM	
S3	16400304	Screw,pan,three pieces,3x4,S,ZMC	
S4	16498647	Screw,pan,three pieces,3x5,S,ZMC	
S5	16410306	Screw,bind,3x6,S,ZMC	
S6	16498579	Screw,pan,three pieces,3x6,S,ZMC	
S7	16476308	Screw,pan,flat,flat washer,3x8,B,BNM	
S8	16470004	Screw,pan,sems,2.6x4,S,ZMC	
S9	16400004	Screw,pan,2.6x4,S,ZMC	
S10	16400204	Screw,bind,2x4,S,ZMC	
S11	16498260-00	Set screw,3x3	
S12	16410316	Screw,bind,3x16,S,ZMC	
S13	16351140	E-ring, 3J	

(Table 503) Parts list of screw & washer

5-3. PCBA PARTS LIST

Following shows all the parts mounted on the PCBAs of FD-54 series.

5-3-1. PCBA MFD Control (C)

Parts Nos.	Parts name & rating	Location
13447358-00	LSI TEAC 7358-00	U1
13441922-00	LSI TEAC 1922-00	U2
13441983	TTL IC 74LS368A	U3
13441235	TTL IC 74LS04	U4
13428139	Transistor array, M54578P	U5
13424286	Transistor, 2SC2021R	Q3, Q4
13421211	Transistor, 2SA881 Q.R	Q1
13411378	Diode, pair, MA154WA	CRA1, CRA2, CRA5, CRA6, **CRA3, **CRA4
13411406	Diode, pair, MA154WK	CRA7
13411243	Diode, 1S954	CR1, CR4~CR8
13411339	Diode, DS442X	CR8
13415408	Diode, zener, RD6.8EN2	CR2
13497262	Resistor array, SA 9-1KΩ, J	RA1
13497310	Resistor array, SA 5-15KΩ, J	RA3

(Table 504) PCBA MFD control (C) parts list (1/4)

Parts Nos.	Parts name & rating	Location
13497266	Resistor array,SA 3-4.7KΩ,J	RA4
13497286	Resistor array,SC 4-2.2KΩ,J	RA2
13497228-00	Resistor array,T-7228	RA5
13497227-00	Resistor array,T-7227	RA7
13497229-00	Resistor array,T-7229	RA6
11187105	Resistor,RD,1/6W,1MΩ,J	R16
11187473	Resistor,RD,1/6W,47KΩ,J	**R15,R18
11187682	Resistor,RD,1/6W,6.8KΩ,J	R17
11187222	Resistor,RD,1/6W,2.2KΩ,J	R20
11198104	Resistor,RD,1/4W,100KΩ,J	R10
11198497	Resistor,RN,1/4W,1.24KΩ,F	R19
11051121	Resistor,RN,1W,120Ω,J	R21
11051390	Resistor,RN,1W,390Ω,J	R13,R14
13040341	Jumping wire	**S1
12903343	Capacitor,CE,10V,100μF,M	C2
12903353	Capacitor,CE,25V,47μF,M	C24
12903345	Capacitor,CE,16V,22μF,M	C6,C8
12903227	Capacitor,CS,20V,15μF,M	C7,C9
12903154	Capacitor,CS,16V,47μF,M	**C33,C34
12903152	Capacitor,CS,16V,2.2μF,K	C36
12903178	Capacitor,CS,35V,0.22μF,K	C13,C14
12903177	Capacitor,CS,35V,0.15μF,M	C11,C12
12903375	Capacitor,CS,16V,1μF,M	C17

(Table 504) PCBA MFD control (C) parts list (2/4)

Parts Nos.	Parts name & rating	Location
12903372	Capacitor,CS,16V,0.33μF,M	C5
12903080	Capacitor,CC,25V,YU,0.1μF,M	C26,C28
12903335	Capacitor,CC,25V,X,0.022μF,Z	C3,C4,C10,C15,C16,C20 C27,C31,C32
12902530	Capacitor,CC,500V,F,0.01μF,Z	C1
12901421	Capacitor,CC,50V,B,2200PF,K	C25
12901417	Capacitor,CC,50V,B,1000PF,K	C29
12900771	Capacitor,CC,50V,SL,180PF,J	C18,C19
12902588	Capacitor,CC,50V,CH,56PF,J	C22
12902578	Capacitor,CC,50V,CH,22PF,J	C23
12454222	Capacitor,CQ,100V,2200PF,G	C30
12454152	Capacitor,CQ,100V,1500PF,G	C35
12454101	Capacitor,CQ,100V,100PF,G	C21
13295084-00	Ceramic oscillator,480KHz	Y1
14723507	Coil,chalk,330μH,J	L1~L3
13121234	Connector,S6P,polarizing	*J9
13121152	Connector,W12P,polarizing	
13121361	Connector,S5P	TP7~10,G
13121363	Connector,S7P	TPI~6,G
13121332	Connector,W14P	HS~1U

(Table 504) PCMB MFD control (C) parts list (3/4)

Parts No.s	Parts name & rating	Location
13121109	Connector, 4P	J2
16322368	Connector, clamp	for J2 installation
13121175	Connector, 4P	J7
13121176	Connector, 5P	J5
13121177	Connector, 6P	J4,J6
13121149	Short bar	HSM, HL, IU, HS, DS003, HM straps
16271169-XX	Name plate	

(Table 504) PCBA MFD control (C) parts list (4/4)

- Notes:
1. Parts with an asterisk are different depending on the PCBA versions. Select either of them.
 2. Parts with a double asterisks are not used in some PCBA versions.
 3. Refer to the schematic diagram of the PCBA as to the details of the parts with asterisks.
 4. Name plate version is different depending on the PCBA version used.

Parts No.s	Parts name & rating	Location
13121109	Connector,4P	J2
16322368	Connector,clamp	for J2 installation
13121175	Connector,4P	J7
13121176	Connector,5P	J5
13121177	Connector,6P	J4,J6
13121149	Short bar	HSM,HL,IU,HS,DSO~3,HM straps
16271169-XX	Name plate	

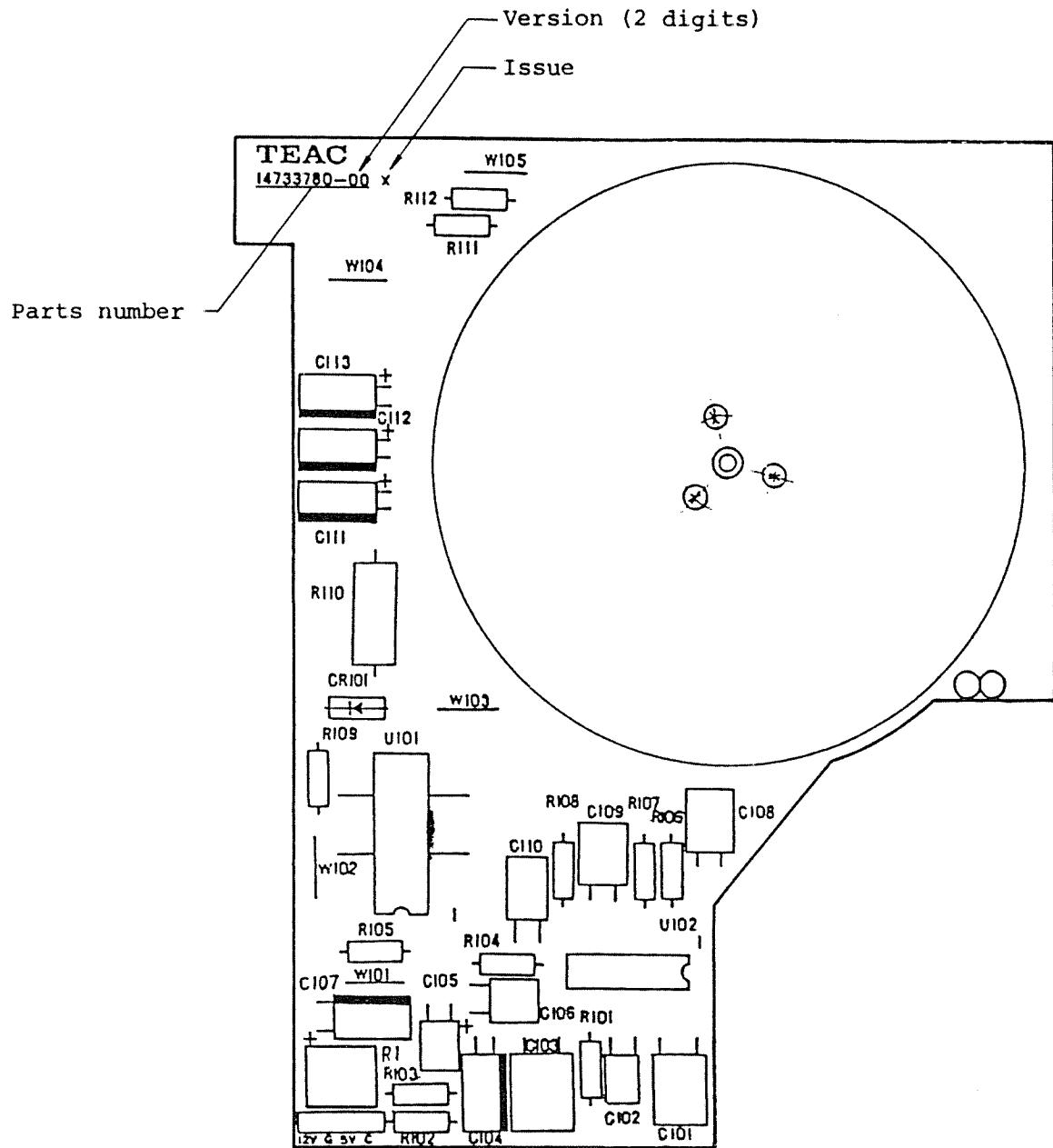
(Table 504) PCBA MFD control (C) parts list (4/4)

- Notes:
1. Parts with an asterisk are different depending on the PCBA versions. Select either of them.
 2. Parts with a double asterisks are not used in some PCBA versions.
 3. Refer to the schematic diagram of the PCBA as to the details of the parts with asterisks.
 4. Name plate version is different depending on the PCBA version used.

5-4. SCHEAMTIC DIAGRAMS AND PARTS LOCATION

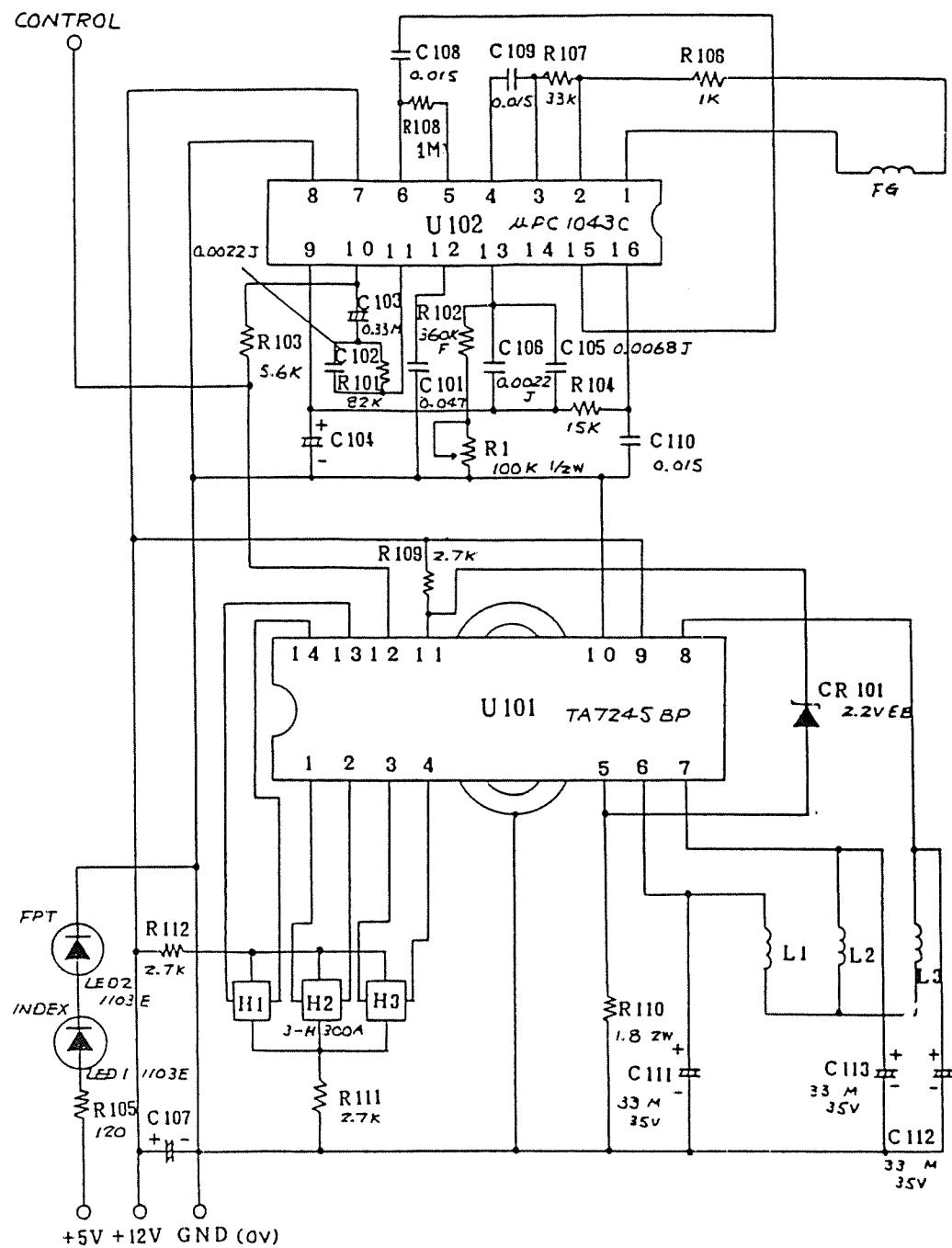
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SPARE PAGE



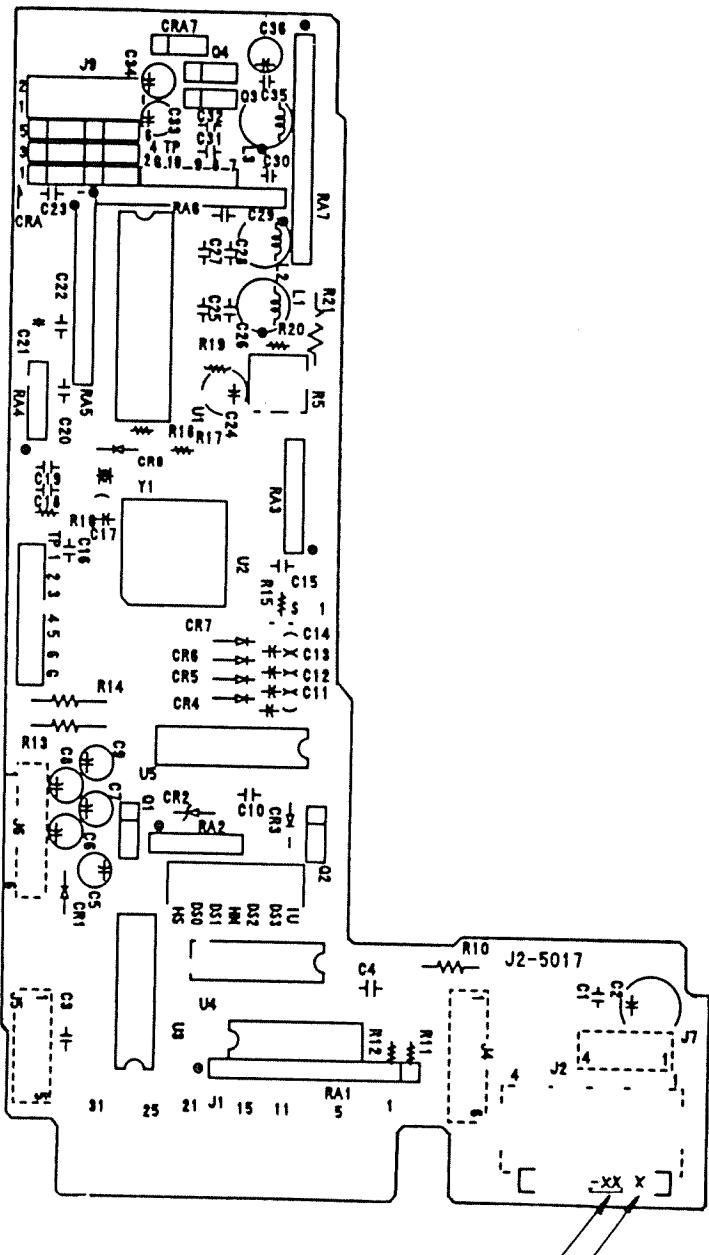
PCBA DD MOTOR SERVO (Type C)

PARTS LOCATION



PCBA DD MOTOR SERVO (Type C)

SCHEMATIC DIAGRAM



Version (2 digits)

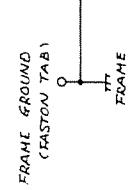
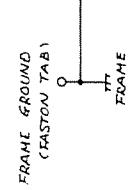
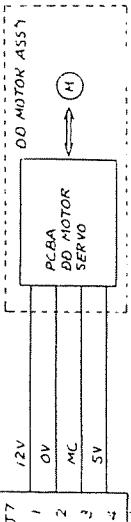
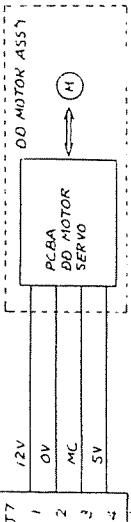
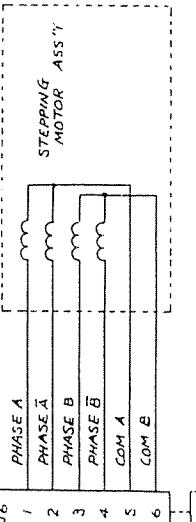
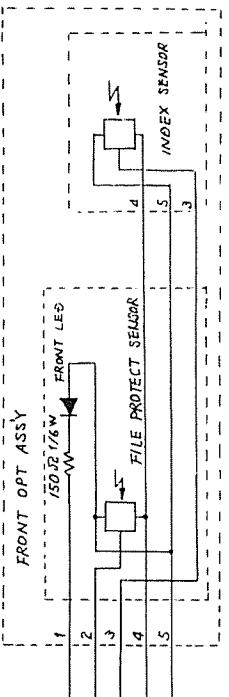
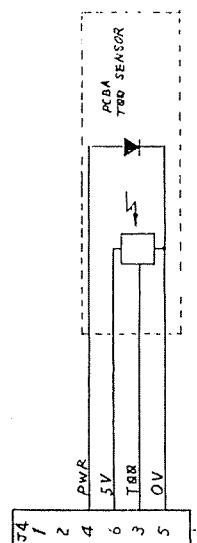
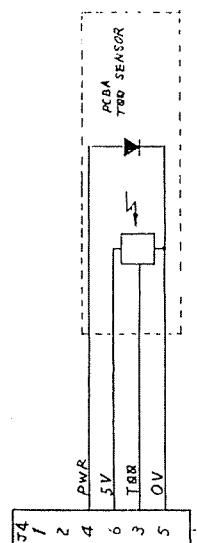
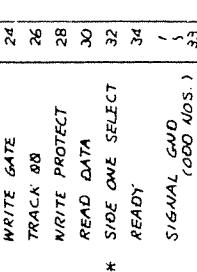
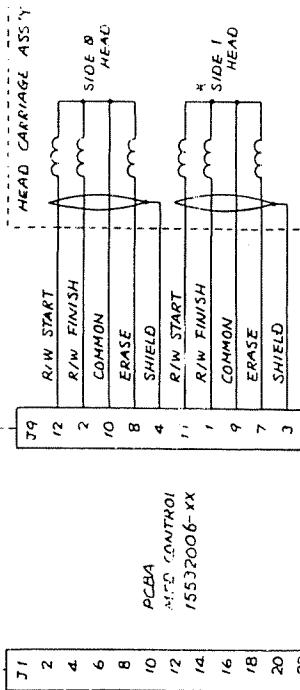
Issue

PCBA MTD CONTROL, PARTS LOCATION

3024624

VERSION TABLE

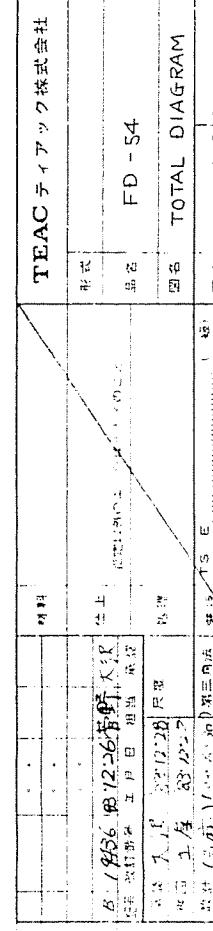
		FDD VERSION	MAIN SPEC	* PARTS & SIGNALS	NOTE
RESERVED	2	J9	R/W START	S SIDE	
IN USE	4	1/2	R/W FINISH	S SIDE	
DRIVE SELECT 3	6	2	COMMON	S HEAD	SIDE ONE SELECT
INDEX / SECTOR	8	10	ERASE	6 - 02	D SIDE
DRIVE SELECT 8	10	8	SHIELD	A - 04	S SIDE
DRIVE SELECT 1	12	4	R/W START	Mechanism Only (WITHOUT PCBA)	
DRIVE SELECT 2	14	11	R/W FINISH	MFD CONTROL & TQD SENSOR	
MOTOR ON	16	1	COMMON		
DIRECTION SELECT	18	9	ERASE		
STEP P	20	7	SHIELD		
WRITE DATA	22	2	POWER		
WRITE GATE	24	4	SV	PCBA TQD SENSOR	
TRACK #8	26	6	TQD		
WRITE PROTECT	28	3	OV		
READ DATA	30	5	OV		
* SIDE ONE SELECT	32				
READY	34				
SIGNAL GND (000 AND 5.)	33				



2. ABBREVIATED NAMES ARE AS FOLLOWS
S SIDE : SINGLE SIDE
D SIDE : DOUBLE SIDE
SI HEAD : SIDE ONE HEAD

NOTE 1. PARTS AND SIGNALS WITH AN ASTERISK (*) ARE USED
ONLY FOR THE DOUBLE SIDE MODEL.

P/N 19307120-XX



10409304

10409304

10409304

部品名		規格		寸法		仕様		備考																																		
PCBA VERSIONS	MAIN SPEC.	* PARTS																																								
-00	48tpn S.Side A.STD	R19 (1.24K), R21 (120) Si																																								
-01	48tpn D.Side B.STD	R19 (1.24K), R21 (120), R15 (47K) CRA3, CRA4, C33, J9 (12P) SIDE / HEAD																																								
<p>6. POLARIZING KEY POSITIONS FOR CONNECTORS (J) ARE: J_1: BETWEEN PIN4 AND 6 J_9: PIN6</p> <p>5. REFER TO SHORT BAR SELECTION TABLE (HSM~DS3) AS TO THE SHIPPING POSITIONS.</p> <p>4. TOLERANCE SYMBOLS FOR R, RA, AND C ARE: $R: \pm 1\%$, $G: \pm 2\%$, $J: \pm 5\%$, $K: \pm 10\%$, $M: \pm 20\%$, $Z: +80-20\%$</p> <p>3. CAPACITOR (C) VALUES ARE IN MICROFARADS. SOV OR HIGHER, $\pm 10\%$ (K), UNLESS OTHERWISE SPECIFIED.</p> <p>2. RESISTOR (R) AND RESISTOR ARRAY (RA) VALUES ARE IN OHMS. 1/BW OR GREATER, $\pm 5\%$ (J). UNLESS OTHERWISE SPECIFIED.</p> <p>1. PARTS WITH AN ASTERISK (*) ARE DIFFERENT IN EACH PCBA VERSION. REFER TO VERSION TABLE.</p> <p>NOTES</p> <p>6. POLARIZING KEY POSITIONS FOR CONNECTORS (J) ARE: J_1: BETWEEN PIN4 AND 6 J_9: PIN6</p> <p>5. REFER TO SHORT BAR SELECTION TABLE (HSM~DS3) AS TO THE SHIPPING POSITIONS.</p> <p>4. TOLERANCE SYMBOLS FOR R, RA, AND C ARE: $R: \pm 1\%$, $G: \pm 2\%$, $J: \pm 5\%$, $K: \pm 10\%$, $M: \pm 20\%$, $Z: +80-20\%$</p> <p>3. CAPACITOR (C) VALUES ARE IN MICROFARADS. SOV OR HIGHER, $\pm 10\%$ (K), UNLESS OTHERWISE SPECIFIED.</p> <p>2. RESISTOR (R) AND RESISTOR ARRAY (RA) VALUES ARE IN OHMS. 1/BW OR GREATER, $\pm 5\%$ (J). UNLESS OTHERWISE SPECIFIED.</p> <p>1. PARTS WITH AN ASTERISK (*) ARE DIFFERENT IN EACH PCBA VERSION. REFER TO VERSION TABLE.</p> <p>NOTES</p> <p>6. POLARIZING KEY POSITIONS FOR CONNECTORS (J) ARE: J_1: BETWEEN PIN4 AND 6 J_9: PIN6</p> <p>5. REFER TO SHORT BAR SELECTION TABLE (HSM~DS3) AS TO THE SHIPPING POSITIONS.</p> <p>4. TOLERANCE SYMBOLS FOR R, RA, AND C ARE: $R: \pm 1\%$, $G: \pm 2\%$, $J: \pm 5\%$, $K: \pm 10\%$, $M: \pm 20\%$, $Z: +80-20\%$</p> <p>3. CAPACITOR (C) VALUES ARE IN MICROFARADS. SOV OR HIGHER, $\pm 10\%$ (K), UNLESS OTHERWISE SPECIFIED.</p> <p>2. RESISTOR (R) AND RESISTOR ARRAY (RA) VALUES ARE IN OHMS. 1/BW OR GREATER, $\pm 5\%$ (J). UNLESS OTHERWISE SPECIFIED.</p> <p>1. PARTS WITH AN ASTERISK (*) ARE DIFFERENT IN EACH PCBA VERSION. REFER TO VERSION TABLE.</p> <p>NOTES</p>																																										
<p>P/N 15532006 - XX</p> <p>VERSION TABLE</p> <table border="1"> <thead> <tr> <th>部品番号</th> <th>基板番号</th> <th>基板名</th> <th>仕様</th> <th>基板外のエッジ</th> <th>仕上</th> <th>基板外のエッジ</th> <th>仕上</th> <th>部品番号</th> <th>部品名</th> <th>仕様</th> </tr> </thead> <tbody> <tr> <td>302462</td> <td>302462</td> <td>302462</td> <td>FD-54</td> <td>FD-54</td> <td>FD-54</td> <td>FD-54</td> <td>FD-54</td> <td>302462</td> <td>PCBA MFQ CONTROL PCB</td> <td>TEAC ティアック株式会社</td> </tr> <tr> <td>302462</td> <td>302462</td> <td>302462</td> <td>FD-54</td> <td>FD-54</td> <td>FD-54</td> <td>FD-54</td> <td>FD-54</td> <td>302462</td> <td>SCHEMATIC</td> <td>TEAC ティアック株式会社</td> </tr> </tbody> </table> <p>10409305</p> <p>10409305</p>										部品番号	基板番号	基板名	仕様	基板外のエッジ	仕上	基板外のエッジ	仕上	部品番号	部品名	仕様	302462	302462	302462	FD-54	FD-54	FD-54	FD-54	FD-54	302462	PCBA MFQ CONTROL PCB	TEAC ティアック株式会社	302462	302462	302462	FD-54	FD-54	FD-54	FD-54	FD-54	302462	SCHEMATIC	TEAC ティアック株式会社
部品番号	基板番号	基板名	仕様	基板外のエッジ	仕上	基板外のエッジ	仕上	部品番号	部品名	仕様																																
302462	302462	302462	FD-54	FD-54	FD-54	FD-54	FD-54	302462	PCBA MFQ CONTROL PCB	TEAC ティアック株式会社																																
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TANDY®

Service Manual

25-1000

**56 Watt Power Supply
Part Number 8790070
Supplement To
Tandy 1000 Service Manual
Catalog No. 25-1000**

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

The 56W Power Supply (8790070) is electrically the same as the 54W Power Supply used in the Tandy 1000 Computer. The only exception is the following.

	Minimum Load			Maximum Load			
	Output	Current (A)	Resistor Value(Ohm)	Safe Power Rating (WT)	Current (A)	Resistor Value(Ohm)	Safe Power Rating (WT)
Condition I	+ 5V	2.0	2.5	20	7.5	0.67	50
	+ 12V	0.2	60	5	1.25	9.6	30
	-12V	0	0	0	.25	48	5
Condition II	+ 5V	2.0	2.5	20	6.0	0.83	50
	+ 12V	0.2	60	5	*1.8	6.67	30
	-12V	0	0	0	0.25	48	5

*Note: 2.0A surge for 15 seconds.

RADIO SHACK, A DIVISION OF TANDY CORPORATION

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CANADA: BARRIE, ONTARIO L4M 4W5**

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