NCR 8496 SOUND GENERATOR

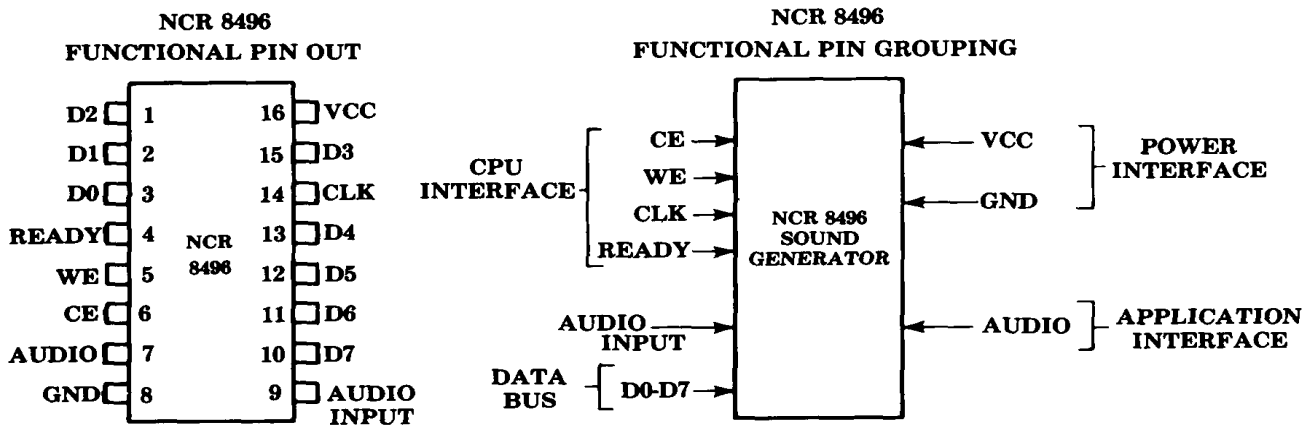## TABLE OF CONTENTS

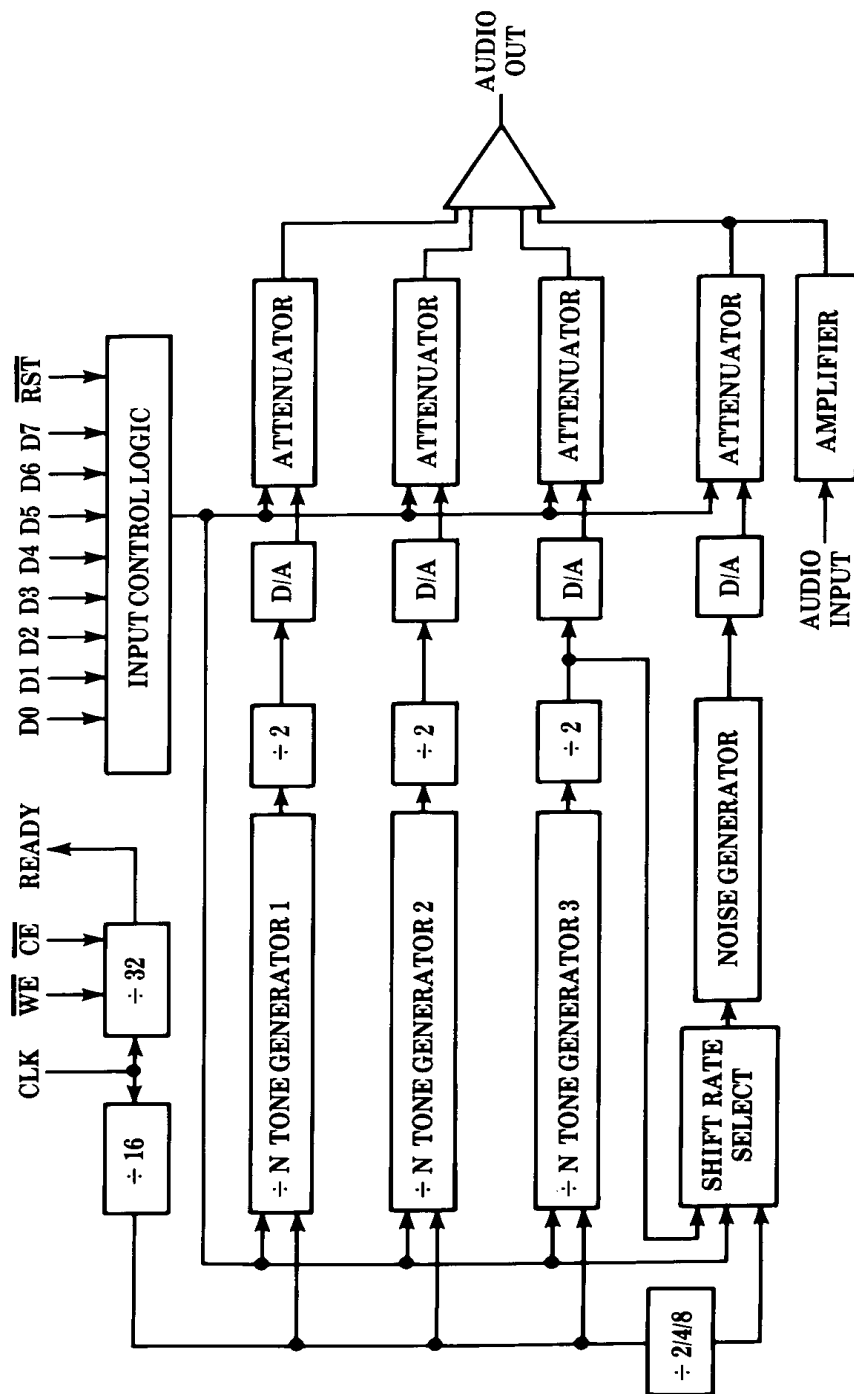## LIST OF ILLUSTRATIONS

SECTION 1

GENERAL DESCRIPTION

The NCR 8496 is an NMOS digital sound generator capable of providing applications with a low cost solution for noise and sound generation.

FEATURES

- Functionally and Pin compatible with the SNR76496
- Programmable white or periodic noise generator
- Three programmable tone generators
- Programmable attenuation values
- Simultaneous multiple sound generation
- TTL compatible
- 4 MHz maximum clock input
- External audio input added to Internal Generators

NCR 8496
FUNCTIONAL PIN OUT

```
        D2 ⊏ 1        16 ⊐ VCC
        D1 ⊏ 2        15 ⊐ D3
        D0 ⊏ 3        14 ⊐ CLK
     READY ⊏ 4   NCR  13 ⊐ D4
        WE ⊏ 5   8496 12 ⊐ D5
        CE ⊏ 6        11 ⊐ D6
     AUDIO ⊏ 7        10 ⊐ D7
       GND ⊏ 8         9 ⊐ AUDIO
                          INPUT
```

NCR 8496
FUNCTIONAL PIN GROUPING

```
              ⎡ CE  →                          ⎤
    CPU       | WE  →      NCR 8496    ← VCC    | POWER
 INTERFACE  ⎨  CLK →        SOUND              ⎬ INTERFACE
              ⎣ READY →    GENERATOR   ← GND    ⎦

    AUDIO ────→                       ← AUDIO ⎤ APPLICATION
    INPUT                                     ⎦ INTERFACE

    DATA   ⎡
    BUS    ⎣ D0-D7 →
```

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NCR 8496 FUNCTIONAL BLOCK DIAGRAM

SECTION 2

FUNCTIONAL DESCRIPTIONS

2.1 Control Registers

The NCR 8496 Sound Generator has eight (8) internal
registers used to control three (3) tone generators and one
(1) noise generator. A three (3) bit data word used to
determine the destination control register is contained in
the first byte of data for all data transfers. The internal
register designations are as follows:

Address Bits			Register Destination
RO	R1	R2	Description
0	0	0	Tone 1: Frequency
0	0	1	Tone 1: Attenuation
0	1	0	Tone 2: Frequency
0	1	1	Tone 2: Attenuation
1	0	0	Tone 3: Frequency
1	0	1	Tone 3: Attenuation
1	1	0	Noise : Control
1	1	1	Noise : Attenuation

Note: RO is the most significant address bit

2.2 Tone Generation

The NCR 8496 sound generator has three (3) programmable tone
generators, each with separate frequency synthesis and
attenuation sections. The frequency synthesis section
requires ten (10) bits of data (F0 to F9) to define half the
period of the desired frequency. This data is entered into
a ten (10) stage tone counter, which is decremented at a
rate of N/16 where N is the clock input frequency. A signal
is produced when this tone counter decrements to one, which
toggles a divide by two counter and reloads the tone
counter. Therefore, the period of the desired frequency is
twice the value of the tone generator.

The frequency of each tone generation is calculated using the equation:

$$f = N/32n$$

N = the clock input frequency
n = a 10 bit binary number [2 < n < 1023]

The divide by two counter is directly connected to a four stage attenuator whose values and bit position in the data word are shown in the following table:

ATTENUATION CONTROL

Data				Value	Data				Value
A0	A1	A2	A3	dB	A0	A1	A2	A3	dB
0	0	0	0	0	1	0	0	0	-16
0	0	0	1	-2	1	0	0	1	-18
0	0	1	0	-4	1	0	1	0	-20
0	0	1	1	-6	1	0	1	1	-22
0	1	0	0	-8	1	1	0	0	-24
0	1	0	1	-10	1	1	0	1	-26
0	1	1	0	-12	1	1	1	0	-28
0	1	1	1	-14	1	1	1	1	OFF

Note: A0 is the most significant bit of data

2.3 Noise Generation

The NCR Sound Generator has two (2) noise sources (periodic and white), which share a common attenuator. These noise sources are shift registers with an exclusive NOR feedback network. One (1) of four (4) noise generator shift rates, each rate being derived from the input clock, will be controlled by the two (2) NF bits, as is shown in the following table:

NOISE GENERATOR FREQUENCY CONTROL

NF BITS		FREQUENCY CONTROL
NFO	NF1	SHIFT RATE
0	0	N/512
0	1	N/1024
1	0	N/2048
1	1	Tone Generator #3 Output

Note: NFO is the most significant bit

The choice of either periodic or white noise is controlled by the noise feedback control bit FB, as is shown in the following table:

NOISE FEEDBACK CONTROL

FB	CONFIGURATION
0	Periodic Noise
1	White Noise

2.4 Data Transfer

The NCR 8496 Sound Generator is enabled by the CPU by asserting a low logic level to $\overline{CE}$. $\overline{WE}$ strobes the contents of the data bus to the appropriate control register. Data bus contents must be valid at this time. Data transfers cannot occur unless $\overline{CE}$ is true.

Thirty two (32) clock cycles are required by the NCR 8496 to load data into the control register. The READY output used as a handshake signal to synchronize the CPU, is asserted to a low logic level immediately following the leading edge of $\overline{CE}$. READY assumes a true state via an external pull up register once the data transfer has been completed.

Formats for Data Transfer are as follows:

FREQUENCY UPDATE (Double Byte Transfer)

FIRST BYTE   SECOND BYTE

DATA				REGISTER ADDRESS			BIT 0
F9	F8	F7	F6	R2	R1	R0	1

D7   D0

DATA							BIT O
F5	F4	F3	F2	F1	F0	X	0

D7   D0

NOISE SOURCE UPDATE (Single Byte Transfer)

SHIFT RATE		FEEDBACK		REGISTER ADDRESS			BIT O
NF1	NF0	FB	X	R2	R1	R0	1

D7   D0

ATTENUATOR UPDATE (Single Byte Transfer)

| DATA				REGISTER ADDRESS			BIT 0
A3	A2	A1	A0	R2	R1	R0	1

D7   D0

2.5 CPU INTERFACE

Eight (8) data lines (D0-D7) and three (3) control lines ($\overline{WE}$, $\overline{CE}$, READY) interface the NCR 8496 Sound Generator to the CPU. As indicated in Section 2.2, Tone Generation, ten (10) bits of data are required by each tone generator in selecting frequency values. Frequency updates require double byte data transfers. An additional four (4) bits of data are required to select the attenuation values. Attenuation updates require only single byte data transfers. (See Section 2.4: Data Transfer).

Tone generators can be quickly updated by initially sending both bytes of frequency and register data, followed by only the second byte of data for succeeding values only if no other control registers are accessed at the time of generator updating. This action is accomplished by latching the register address and permitting the continued transfer of data into the same register. This updating feature permits the expedited modification of the six (6) most significant bits of data needed for frequency sweeps.

2.6 OUTPUT CIRCUITRY

The NCR 8496 Sound Generator output circuitry, emulating a conventional op amp summing circuit, sums the three (3) tone and one (1) noise generator outputs, and will source/sink current to 2 mA. The 0 dB output signal per generator is nominally a 450 mV square in the negative direction from a 2V quiescent level. The output should be OR coupled into the application audio circuit via a filtering network similar to the following:
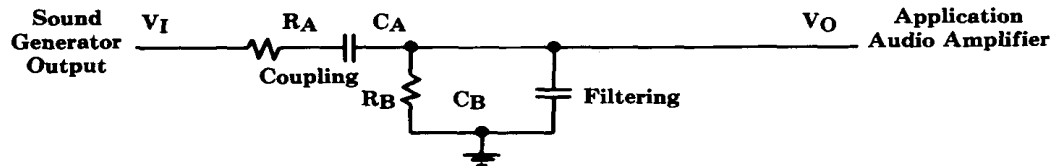
The upper and lower frequency poles for the application are determined from the following equations:

Lower Pole

$$f \cong \frac{1}{2\pi(R_A + R_B) C_A}$$

Upper Pole

$$f \cong \frac{1}{2\pi(R_A // R_B) C_B}$$

Attenuation of the output signal is:

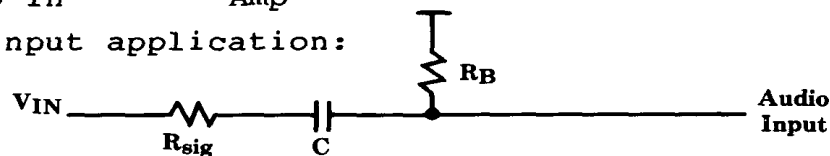$$\frac{V_O}{V_I} = \frac{R_B}{R_A + R_B}$$

Typically $R_B \geq 10 R_A$ so that the attenuation can be small while achieving desired filtering at the same time.

2.7 AUDIO INPUT CIRCUIT

This input node can be biased on with a current to give an approximate transfer function at the output of :

$V_O = R_{Amp}I_{in}$ where R_{Amp} is on the order of 1K Ohms

Typical input application:

R_B provides the bias current to put the amplifier in the linear range.

R_{sig} controls the input current causing the signal swing.

SECTION 3

INTERFACE DEFINITION

3.1 MICROPROCESSOR INTERFACE

Signal	Pin	Description
READY	4	OUTPUT: Open collector, READY indicates that data has been read when true (high). The CPU must be placed in a wait state until READY is true.
$\overline{\text{WE}}$	5	INPUT: Write Enable $\overline{\text{WE}}$ indicates that data is available to the NCR 8496 when true (low).
$\overline{\text{CE}}$	6	INPUT: Chip Enable $\overline{\text{CE}}$ indicates that data may be transferred to the NCR 8496.
$\overline{\text{RST}}$	9	INPUT: Master Reset $\overline{\text{RST}}$ is used for testing purposes only. This pin is a no connect on the SN 76489A and is internally pulled high.
D7	10	Inputs: D0-D7 is the data bust through which data is transferred. D0 is the most significant data bit. D7 is the least significant data bit.
D6	11	
D5	12	
D4	13	
D3	15	
D2	1	
D1	2	
D0	3	
CLK	14	Input Clock

3.2 AUDIO APPLICATION INTERFACE

Signal	Pin	Description
Audio	7	OUTPUT: Audio signal to application. Refer to section 2.6. Output Circuitry for recommended output connections.
Audio In	9	INPUT: Audio input signal from application. Refer to section 2.7.

3.3 POWER INTERFACE

Signal	Pin	Description
VCC	16	Supply Voltage
GND	8	Ground Reference