

8185/8185-2

1024 x 8-BIT STATIC RAM FOR MCS®-85

- Multiplexed Address and Data Bus
- Directly Compatible with 8085AH and 8088 Microprocessors
- Low Operating Power Dissipation
- Low Standby Power Dissipation
- Single +5V Supply
- High Density 18-Pin Package

The Intel 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085AH and 8088 microprocessors to provide a maximum level of system integration.

The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185 that is compatible with the 5 MHz 8085AH-2 and the 5 MHz 8088.

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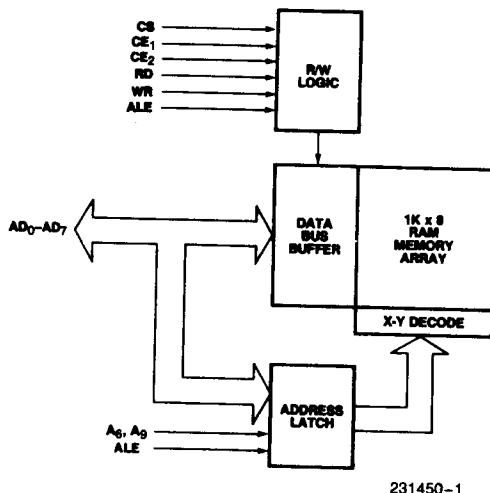


Figure 1. Block Diagram

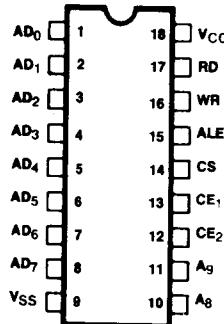


Figure 2. Pin Configuration

Pin Names

| | |
|----------------------------------|----------------------|
| AD ₀ -AD ₇ | Address/Data Lines |
| A ₈ , A ₉ | Address Lines |
| CS | Chip Select |
| CE ₁ | Chip Enable (I/O/M) |
| CE ₂ | Chip Enable |
| ALE | Address Latch Enable |
| WR | Write Enable |

FUNCTIONAL DESCRIPTION

The 8185 has been designed to provide for direct interface to the multiplexed bus structure and bus timing of the 8085A microprocessor.

At the beginning of an 8185 memory access cycle, the 8-bit address on AD_{0-7} , A_8 and A_9 , and the status of \overline{CE}_1 and CE_2 are all latched internally in the 8185 by the falling edge of ALE. If the latched status of both \overline{CE}_1 and CE_2 are active, the 8185 powers itself up, but no action occurs until the \overline{CS} line goes low and the appropriate RD or WR control signal input is activated.

The \overline{CS} input is not latched by the 8185 in order to allow the maximum amount of time for address decoding in selecting the 8185 chip. Maximum power consumption savings will occur, however, only when \overline{CE}_1 and CE_2 are activated selectively to power down the 8185 when it is not in use. A possible connection would be to wire the 8085A's IO/M line to the 8185's \overline{CE}_1 input, thereby keeping the 8185 powered down during I/O and interrupt cycles.

Table 1. Truth Table for Power Down and Function Enable

| \overline{CE}_1 | CE_2 | \overline{CS} | $(CS^*)^{(2)}$ | 8185 Status |
|-------------------|--------|-----------------|----------------|--|
| 1 | X | X | 0 | Power Down and Function Disable ⁽¹⁾ |
| X | 0 | X | 0 | Power Down and Function Disable ⁽¹⁾ |
| 0 | 1 | 1 | 0 | Powered Up and Function Disable ⁽¹⁾ |
| 0 | 1 | 0 | 1 | Powered Up and Enabled |

NOTES:

X = Don't Care.

1: Function Disable implies Data Bus in high impedance state and not writing.

2: $CS^* = (\overline{CE}_1 = 0) \times (CE_2 = 1) \times (\overline{CS} = 0)$.

CS^* = 1 signifies all chip enables and chip select active.

Table 2. Truth Table for Control and Data Bus Pin Status

| (CS^*) | RD | WR | AD ₀₋₇ During Data Portion of Cycle | 8185 Function |
|----------|------|------|--|-----------------------------------|
| 0 | X | X | Hi-Impedance | No Function |
| 1 | 0 | 1 | Data from Memory | Read |
| 1 | 1 | 0 | Data to Memory | Write |
| 1 | 1 | 1 | Hi-Impedance | Reading, but not Driving Data Bus |

NOTE:

X = Don't Care.

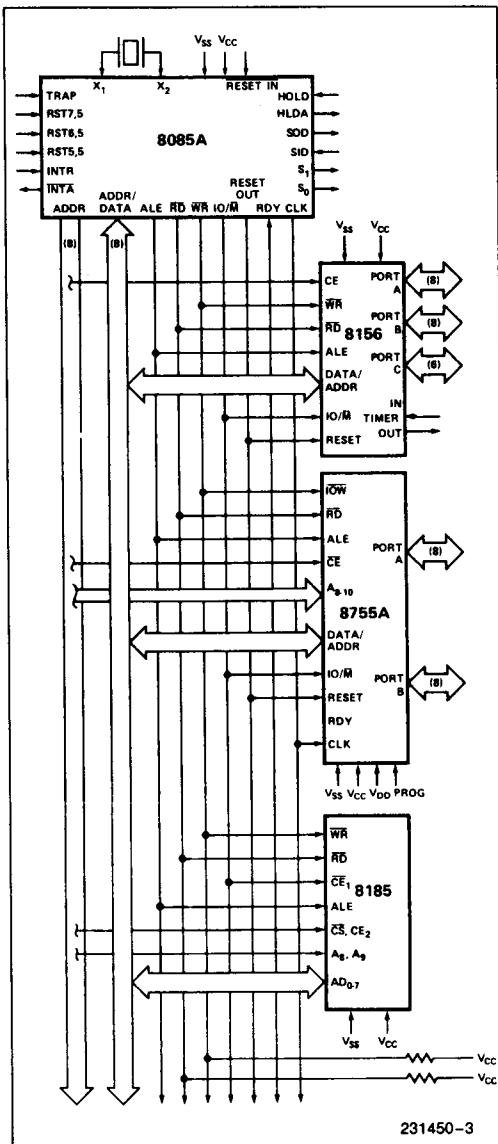


Figure 3. 8185 in an MCS®-85 System

4 Chips:

2K Bytes EPROM

1.25K Bytes RAM

38 I/O Lines

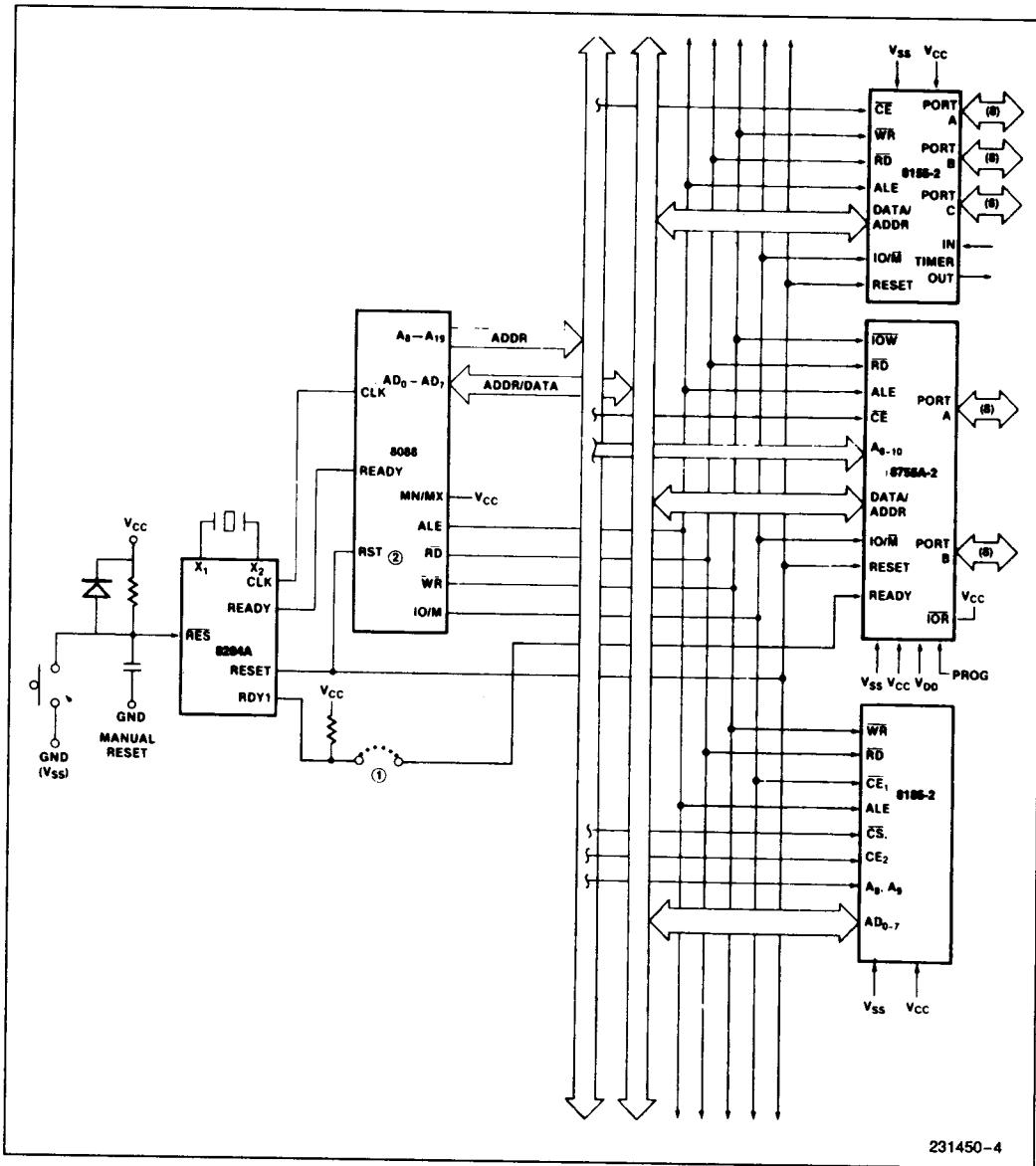
1 Counter/Timer

2 Serial I/O Lines

5 Interrupt Inputs

IAPX 88 FIVE CHIP SYSTEM:

- 1.25K Bytes RAM
- 2K Bytes EPROM
- 38 I/O Pins
- 1 Internal Timer
- 2 Interrupt Levels

**Figure 4. IAPX 88 Five Chip System Configuration**

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias 0°C to + 70°C
 Storage Temperature -65°C to + 150°C
 Voltage on Any Pin
 with Respect to Ground -0.5V to + 7V
 Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

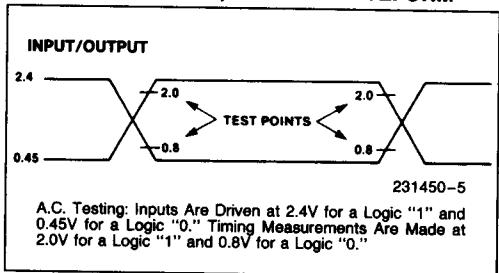
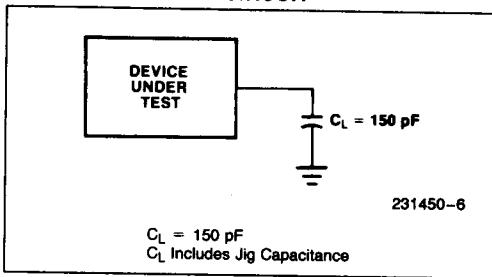
* **WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|--------|----------------------------------|------|-----------|-------|--------------------|
| VIL | Input Low Voltage | -0.5 | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | VCC + 0.5 | V | |
| VOL | Output Low Voltage | | 0.45 | V | IOL = 2 mA |
| VOH | Output High Voltage | 2.4 | | | IOH = -400 μA |
| UIL | Input Leakage | | ±10 | μA | 0V ≤ VIN ≤ VCC |
| UOL | Output Leakage Current | | ±10 | μA | 0.45V ≤ VOUT ≤ VCC |
| ICC | VCC Supply Current Powered Up | | 100 | mA | |
| | Powered Down | | 35 | mA | |

A.C. CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

| Symbol | Parameter | 8185 | | 8185-2 | | Units |
|--------|--|------|-----|--------|-----|-------|
| | | Min | Max | Min | Max | |
| tAL | Address to Latch Set Up Time | 50 | | 30 | | ns |
| tLA | Address Hold Time After Latch | 80 | | 30 | | ns |
| tLC | Latch to READ/WRITE Control | 100 | | 40 | | ns |
| tRD | Valid Data Out Delay from READ Control | | 170 | | 140 | ns |
| tLD | ALE to Data Out Valid | | 300 | | 200 | ns |
| tLL | Latch Enable Width | 100 | | 70 | | ns |
| tRDF | Data Bus Float After READ | 0 | 100 | 0 | 80 | ns |
| tCL | READ/WRITE Control to Latch Enable | 20 | | 10 | | ns |
| tCC | READ/WRITE Control Width | 250 | | 200 | | ns |
| tDW | Data In to WRITE Set Up Time | 150 | | 150 | | ns |
| tWD | Data In Hold Time After WRITE | 20 | | 20 | | ns |
| tSC | Chip Select Set Up to Control Line | 10 | | 10 | | ns |
| tCS | Chip Select Hold Time After Control | 10 | | 10 | | ns |
| tALCE | Chip Enable Set Up to ALE Falling | 30 | | 10 | | ns |
| tLACE | Chip Enable Hold Time After ALE | 50 | | 30 | | ns |

A.C. TESTING INPUT, OUTPUT WAVEFORM**A.C. TESTING LOAD CIRCUIT**

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WAVEFORM