GRAPHIC DISPLAY MODULE

GP1006C02B INSTRUCTION MANUAL

GENERAL DESCRIPTION

FUTABA GP1006C02B is a graphic display module using a FUTABA 256×64 VFD.
Consisting of a VFD, display drivers, a control circuit and power supply, the module can be driven by connecting to the host system through a simple interface.

CONTENTS

1.FEATURES

1-1. High luminance permitted by the triple anode matrix driving system.

1-2. Compact and light-weight unit by using flat packed display drivers and one-chip VFD controller.

1-3. Driven through a simple interface.

1-4. High speed 8bit data write-in capability.

1-5. Luminance adjustment available by software.

2. GENERAL SPECIFICATIONS

2-1. DIMENSIONS, WEIGHT (Refer APPENDIX-1)

TABLE-1

ITEM	SPECIFICATION	UNIT
OUTER DIMENSIONS	(L) 215 ± 1 (W) 85 ± 1 (T) 41MAX	mm
WEIGHT	370 APPROX.	g

2-2. SPECIFICATIONS OF THE DISPLAY PANEL

TABLE-2

ITEM	SPECIFICATION	UNIT
DISPLAY AREA	166.2 × 41.4	mm
NUMBER OF DOT	256 × 64	DOT
DOT PITCH (H × W)	0.65 × 0.65	mm
DOT SIZE (H × W)	0.45 × 0.45	mm
COLOR OF ILLUMINATION	Green (505nm)	–

(Note)
By using a filter, uniform color ranging from blue to orange (including white) can be obtained.

2-3. ENVIRONMENTAL CONDITIONS

TABLE-3

ITEM	SYMBOL	MIN.	MAX.	UNIT
OPERATING TEMPERATURE	Topr	0	+ 50	°C
STORAGE TEMPERATURE	Tstg	– 20	+ 70	°C
OPERATING HUMIDITY	Hopr	20	85	%
STORAGE HUMIDITY	Hstg	20	90	%
VIBRATION(10 to 55 Hz)	-	-	4	G
SHOCK	-	-	40	G

NOTE) Avoid operations and or storage in moist environmental conditions.

2-4. ABSOLUTE MAXIMUM RATINGS

TABLE-4

ITEM	SYMBOL	MIN.	MAX.	UNIT
SUPPLY VOLTAGE	Vcc	-0.4	7.0	V
INPUT SIGNAL VOLTAGE	V_{IS}	-0.4	5.5	V

2-5. RECOMMENDED OPERATING CONDITIONS

TABLE-5

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE	Vcc	-	4.5	5.0	5.5	V
H-LEVEL INPUT VOLTAGE	V_{IH}	Vcc = 5V	2.0	-	5.25	V
L-LEVEL INPUT VOLTAGE	V_{IL}	Vcc = 5V	-	-	0.8	V

2-6. ELECTRICAL CHARACTERISTICS

TABLE-6

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY CURRENT	Icc	Vcc = 5V All on	-	2.1	2.5	A
POWER CONSUMPTION	-		-	10.5	-	W
LUMINANCE	-		270 (80)	540 (160)	-	cd/m² (fL)
H-LEVEL INPUT CURRENT	I_{IH}	V_{IH} = 2.4V		-	10	μA
L-LEVEL INPUT CURRENT	I_{IL}	V_{IL} = 0.8V	-	-	-0.6	mA
H-LEVEL OUTPUT VOLTAGE	V_{OH}	I_{OH} = -3mA	2.4	-	-	V
L-LEVEL OUTPUT VOLTAGE	V_{OL}	I_{OL} = 11.8mA	-	-	0.4	V

NOTE) The surge current can be approx. 5 times the specified supply current at power on.

3. BASIC FUNCTIONS

- 3-1. Data Write-in
- 3-2. Data Read-out
- 3-3. Selection of Displaying Page
- 3-4. Luminance Adjustment

Function Table

TABLE-7

ADDRESS	$\overline{CS}$	$\overline{MERQ}$	$\overline{WR}$	$\overline{RD}$	MODE
n000H~n7FFH	L	L	L	H	Write-in
n000H~n7FFH	L	L	H	L	Read-out
(n + 1)000H~(n + 1)7FFH	L	L	L	H	Page Selection
(n + 1)800H~(n + 1)FFFH	L	L	L	H	Luminance Adjustment
x	H	x	x	x	Display

(Note1) "n" in the table represents the figure of 0 to E, even number of the hexadecimal system.

(Note2) x = irrelevant (any input, including transitions)

3-1. DATA WRITE-IN

The display area corresponds to a 2-kbytes area memory map.
Write-in data operates with 8bits at a time.

Write-in of 8-bit data to addresses of n000H thru n7FFH occurs when $\overline{CS}$ = "L", $\overline{WR}$ = "L", $\overline{MERQ}$ = "L" and $\overline{RD}$ = "H".

Data "H" = ON(light on), Data "L" = OFF(light off).

Relationship of the display dot to address and data is shown in FIG. 1 and FIG. 2.

3-2. DATA READ-OUT

The 8-bit data of the displayed pattern can be read-out by selecting addresses of n000H thru n7FFH when $\overline{CS}$ = "L", $\overline{MERQ}$ = "L", $\overline{WR}$ = "H" and $\overline{RD}$ = "L".

Relationship of the display dot to address and data

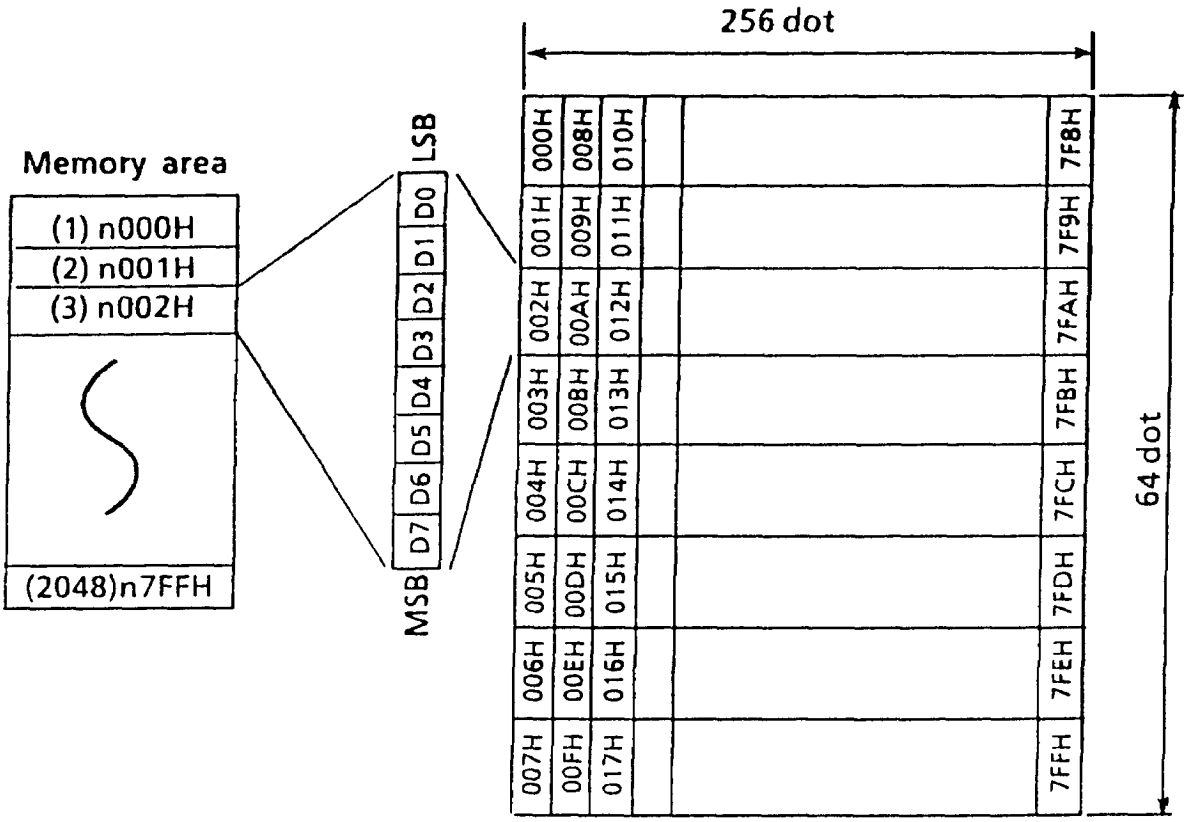


FIG.1 DISPLAY DOT TO ADDRESS AND DATA

Example of data write-in

To display a letter A on the left top of the screen, data are input in the following way.

ADDRESS	DATA
n000H	F8H
n008H	24H
n010H	22H
n018H	24H
n020H	F8H

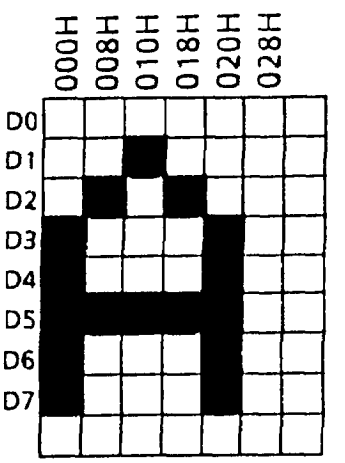


FIG.2 EXAMPLE OF DATA WRITE-IN

3-3. DISPLAY PAGE

This module is equipped with 4 displaying pages.

The desired page can be selected by writing-in any 1 byte to addresses of (n + 1)000H thru (n + 1)7FFH when $\overline{CS}$ = "L", $\overline{MERQ}$ = "L", $\overline{WR}$ = "L" and $\overline{RD}$ = "H".

In this case, the data of D7 thru D4 becomes invalid.

TABLE-8

D3	D2	D1	D0	MODE
×	×	L	L	Displaying page 0.
×	×	L	H	Displaying page 1.
×	×	H	L	Displaying page 2.
×	×	H	H	Displaying page 3.
L	L	×	×	RD/WR allowed for page 0.
L	H	×	×	RD/WR allowed for page 1.
H	L	×	×	RD/WR allowed for page 2.
H	H	×	×	RD/WR allowed for page 3.

(Note1) × = irrelevant (any input, including transitions)

3-4. LUMINANCE ADJUSTMENT

Input data (00H, 06H-0FH) allows luminance to be adjusted in 11 uniform levels.

Adjustment is performed by writing-in any 1 byte to addresses of (n + 1)800H thru (n + 1)FFFH , when $\overline{CS}$ = "L", $\overline{MERQ}$ = "L", $\overline{WR}$ = "L" and $\overline{RD}$ = "H".

The data of D7 thru D4 becomes invalid.

TABLE-9

D3	D2	D1	D0	HEX	LUMINANCE (%)
H	H	H	H	F	100.0
H	H	H	L	E	92.9
H	H	L	H	D	85.7
H	H	L	L	C	78.6
H	L	H	H	B	71.4
H	L	H	L	A	64.3
H	L	L	H	9	57.1
H	L	L	L	8	50.0
L	H	H	H	7	42.9
L	H	H	L	6	35.7
L	L	L	L	0	0

4. INTERFACE CONNECTION

4-1. CONNECTOR PIN ASSIGNMENT

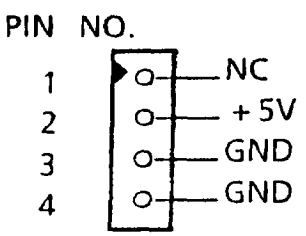
(1) CN1 for power supply

Connector :5045-04A (MOLEX)
Applicable mating Connector :5251-04 (MOLEX)
or equivalent

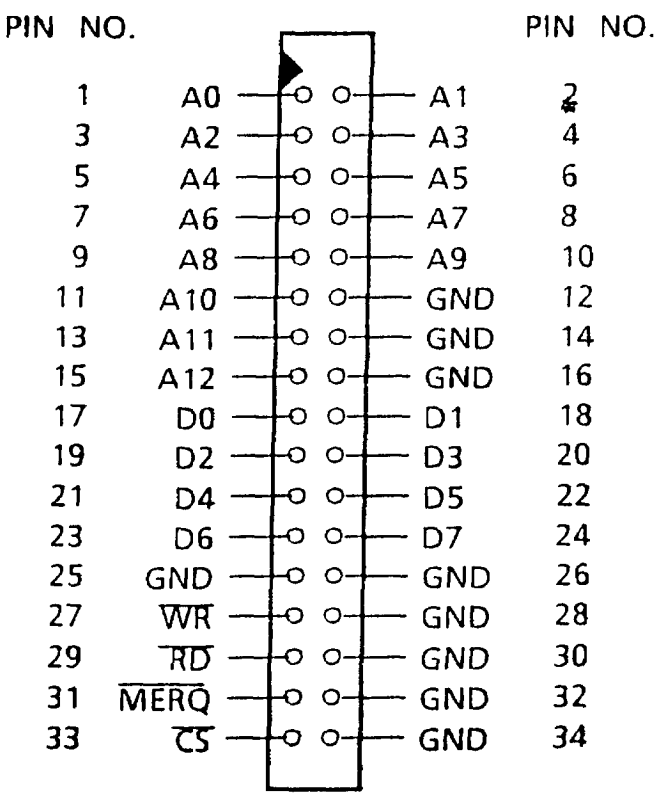
(2) CN2 for Signal

Connector :HIF3FC-34PA-2.54DSA (HIROSE)
Applicable mating Connector :HIF3BA-34D-2.54R (HIROSE)
or equivalent

(CN 1)



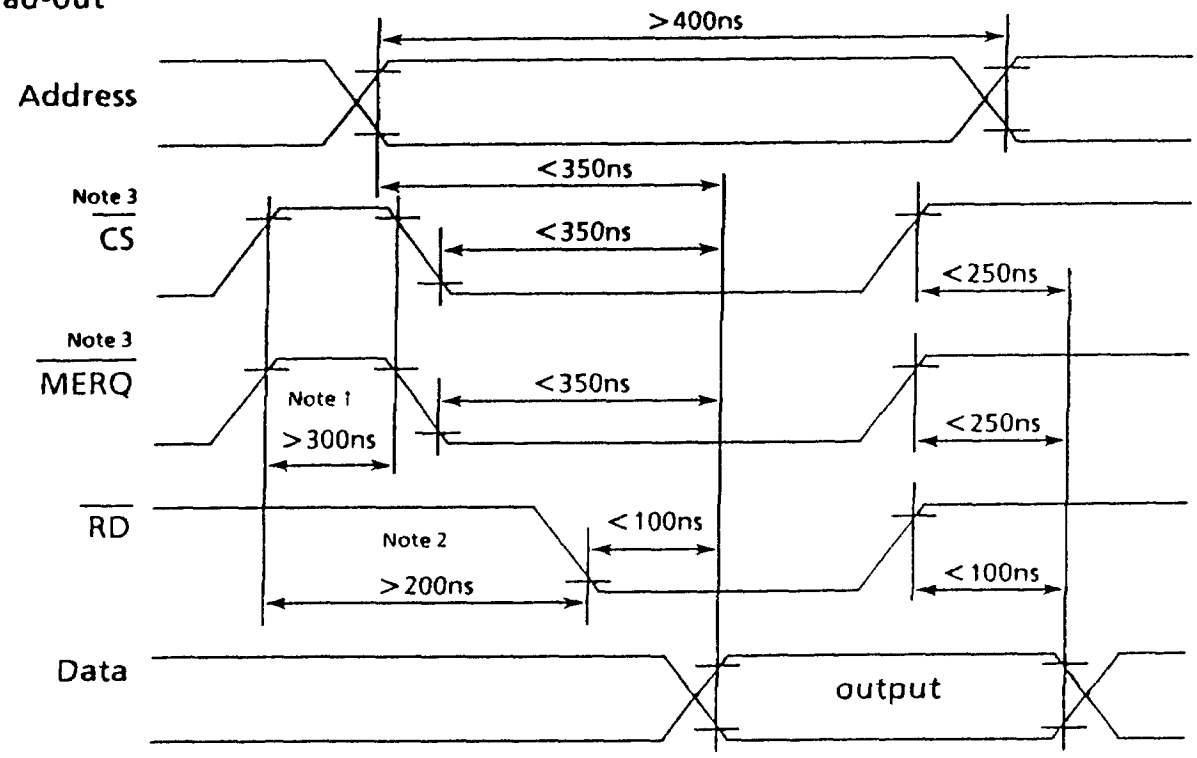
(CN 2)



NOTE 1)
All GND terminal are connected together on the PWB.

4-2. TIMING CHART FOR WRITE-IN AND READ-OUT

(1)Read-out



(2)Write-in

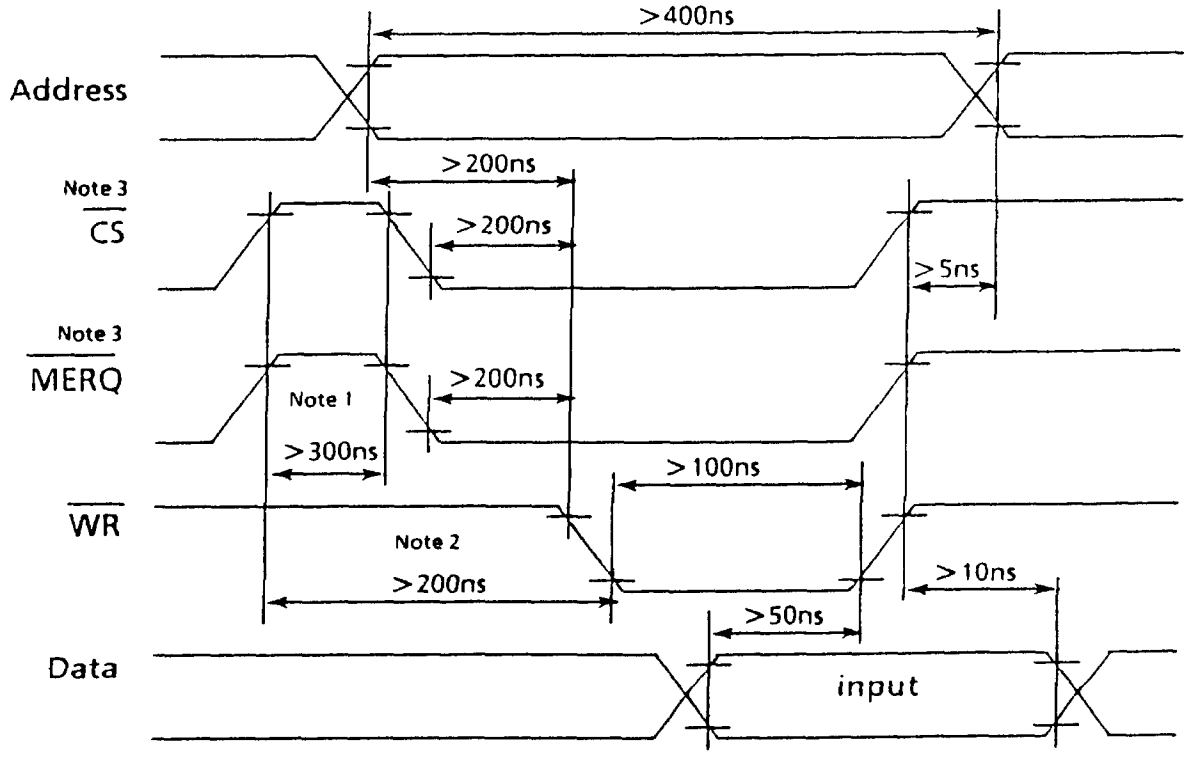


FIG.3 TIMING CHART FOR WRITE-IN AND READ-OUT

Note 1) At each one byte access, the hold-time of high level of $\overline{CS}$ or $\overline{MERQ}$ signal is necessary.

Note 2) Several units are controlled by the $\overline{CS}$ signal, $\overline{RD}$ or $\overline{WR}$ signal shall be kept high-level for 200ns after the rising edge of $\overline{CS}$ signal.

Note 3) Don't apply less than 300 nsec. low signal to $\overline{CS}$ and $\overline{MERQ}$ at the same time.

4-3. EXAMPLE OF INTERFACE CONNECTION

This module can be connected to the host system CPU bus.

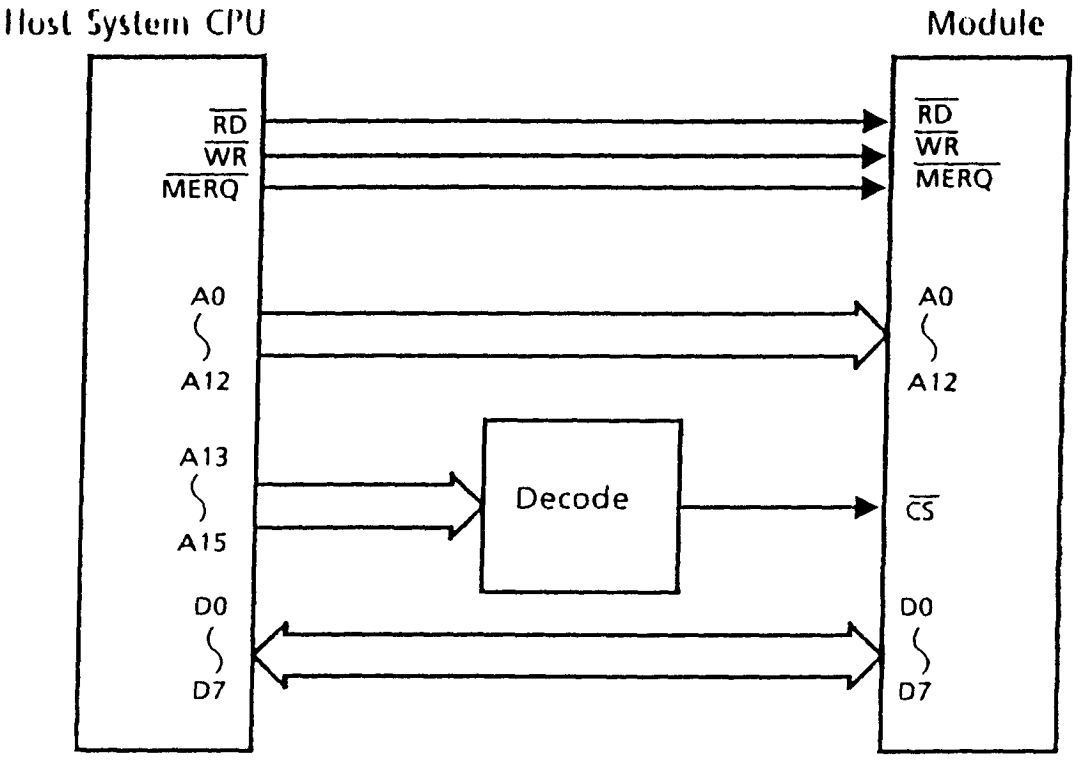


FIG.4 EXAMPLE OF INTERFACE CONNECTION

4-4. ADDRESS DECODING

The module requires the allocation of 8kbytes of memory.
Memory allocation is performed using the chip select signal (CS) which is obtained by the combination of addresses A13 thru A15.

TABLE-10

A15	A14	A13	Memory Area for Module Drive
0	0	0	0000H ~ 1FFFH
0	0	1	2000H ~ 3FFFH
0	1	0	4000H ~ 5FFFH
0	1	1	6000H ~ 7FFFH
1	0	0	8000H ~ 9FFFH
1	0	1	A000H ~ BFFFH
1	1	0	C000H ~ DFFFH
1	1	1	E000H ~ FFFFH

4-5. EXAMPLE OF DRIVING MODULE

Initial setting by the host CPU is required for page selection and luminance adjustment at power on.

[Example] Using Z80 as the host CPU, module driving is explained.

(1) By allocating the addresses 8000H thru 9FFFH (8kbytes) to the memory area the following division will result : (Ref.Page) (3, 4-4)

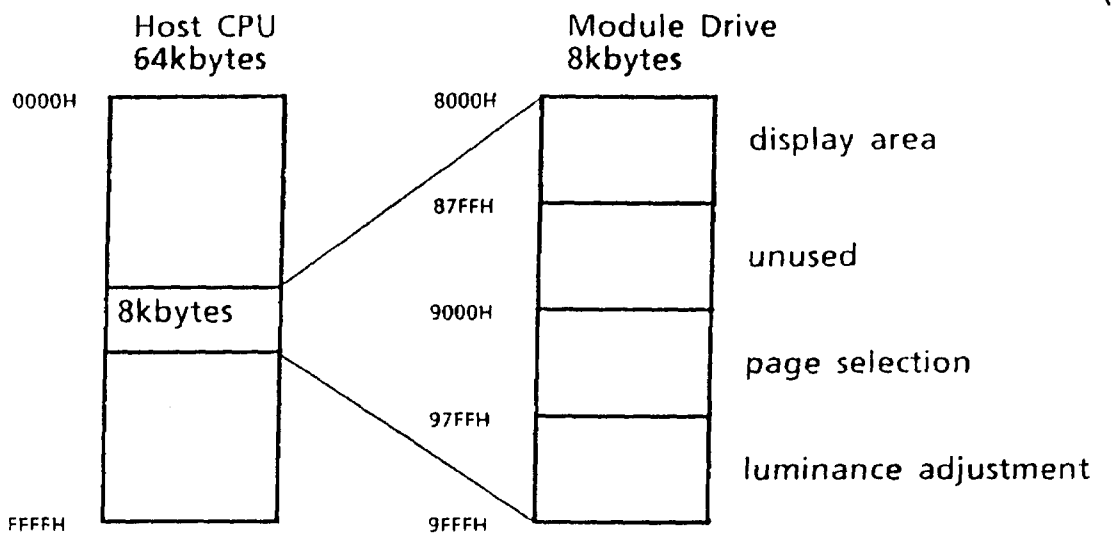
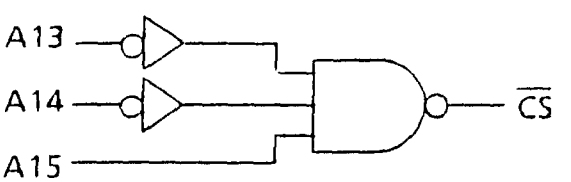


FIG.5 EXAMPLE OF DRIVING MODULE

(2) To generate the CS signal :

→ To make CS signal, $\overline{CS}$ = "L" when A15 = "H", A14 = A13 = "L".



(3) Power on (+ 5V, CN1)

→ The luminance adjustment is set to 0% when power is on.

(4) Write-in 00H to 9000H. (3-3)

→ The display-page, write-in, and read-out page will be set to page 0.

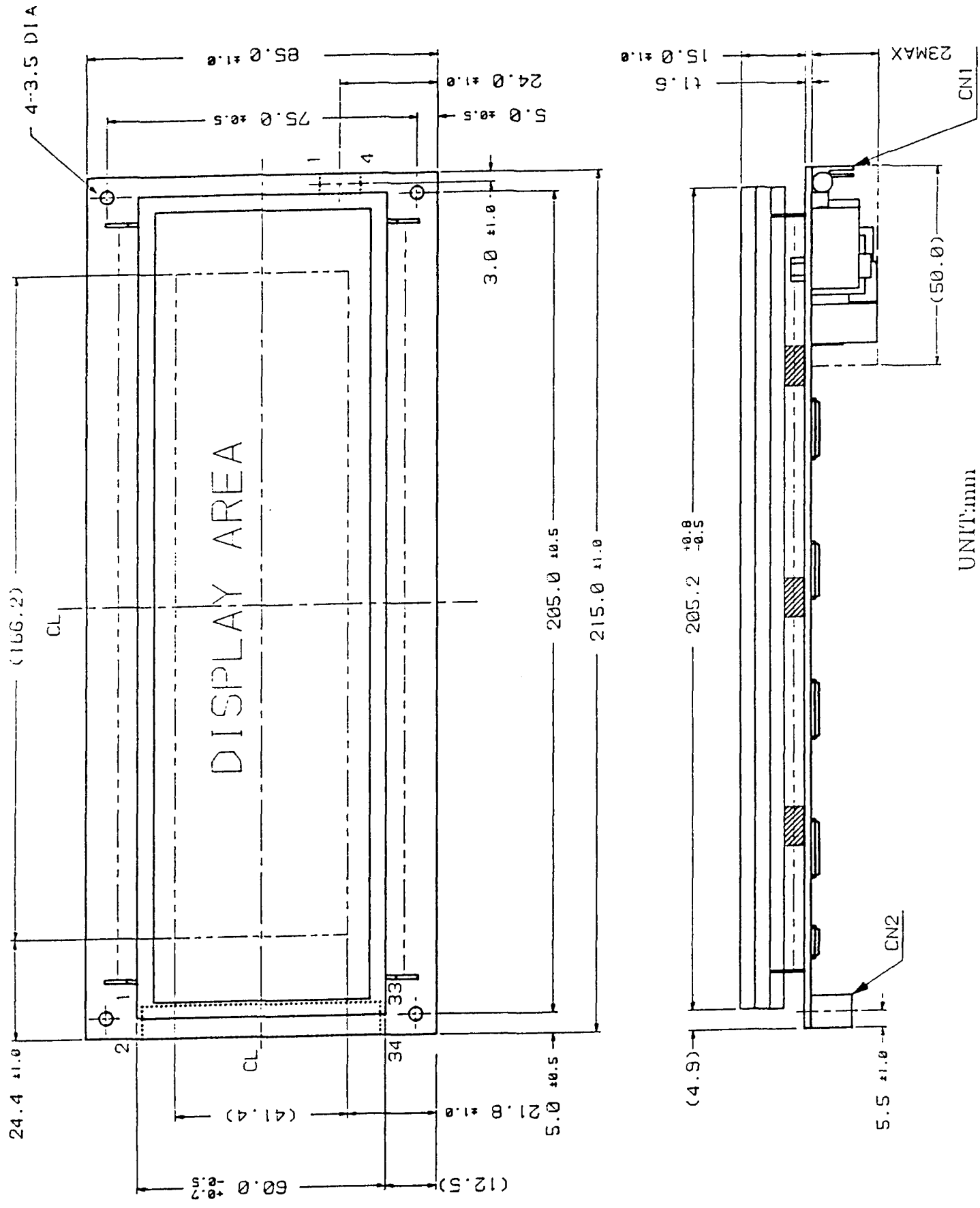
(5) Write-in display data to 8000H thru 87FFH. (3-1)

(6) Write-in 0FH to 9800H. (3-4)

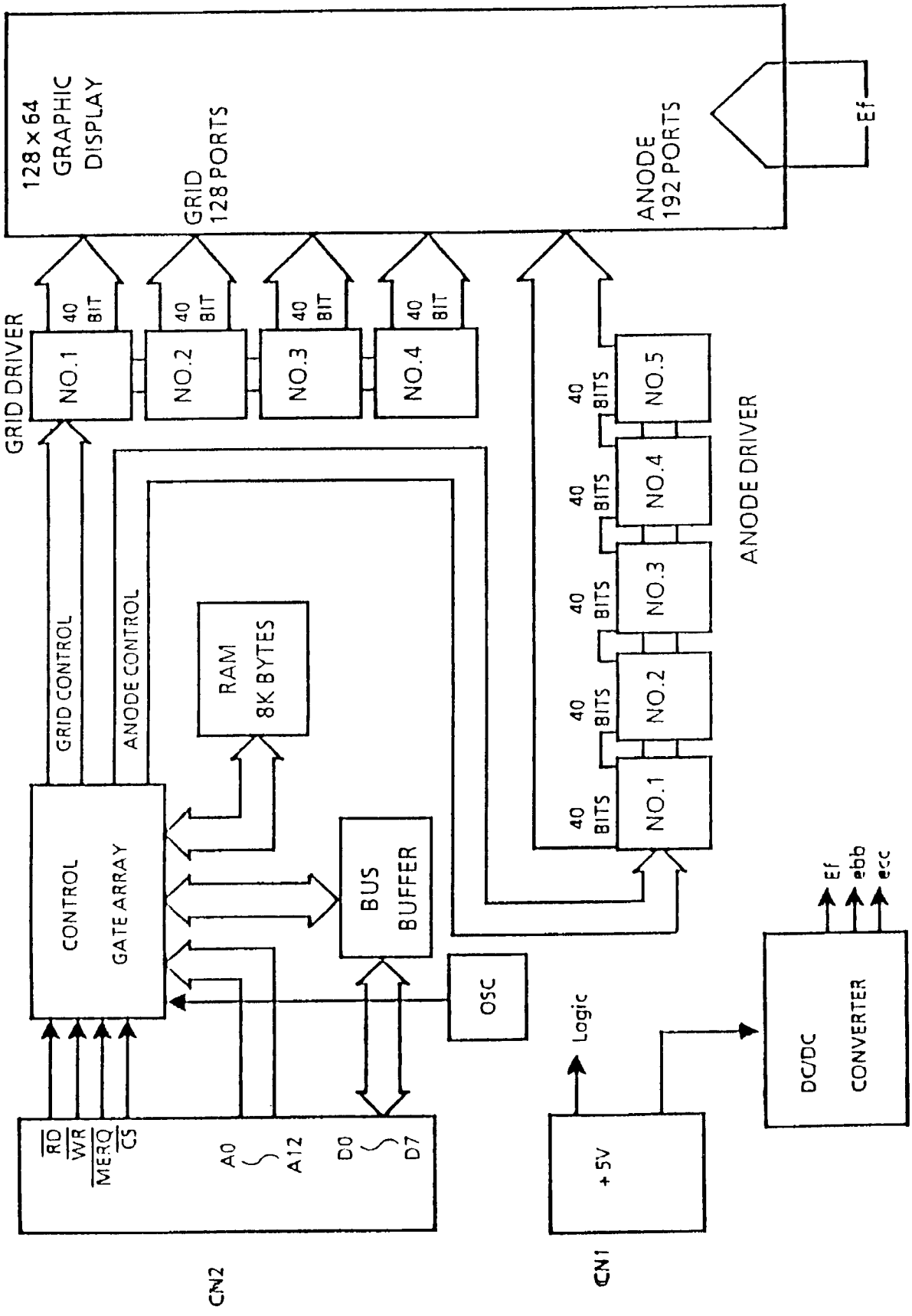
→ Luminance adjustment becomes 100% (the typical rated luminance), the display data written by the item (5) will be displayed.

If the item (6) is executed before the item (5), random pattern may be displayed.

APPENDIX-1 OUTER DIMENSIONS



APPENDIX-2 CIRCUIT BLOCK DIAGRAM



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