

Programmable logic array

(22 × 42 × 10)

PLS173

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement (\bar{I} , \bar{B}) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes for this device are listed below.

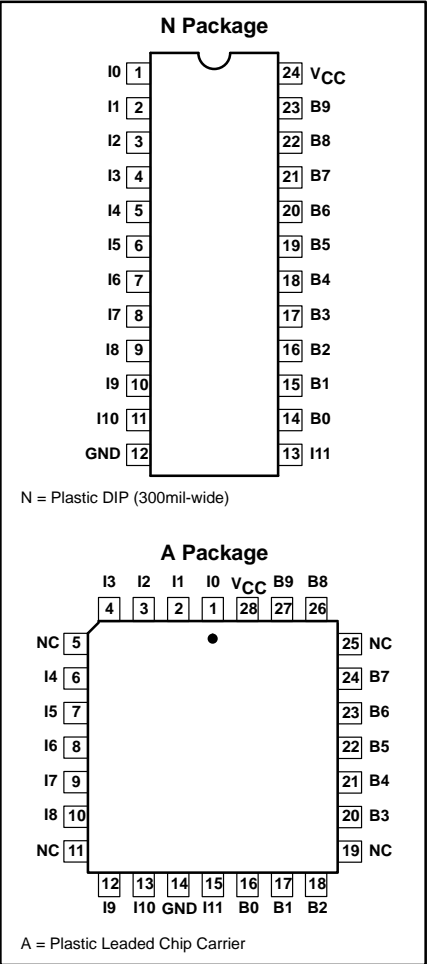
FEATURES

- I/O propagation delay: 30ns (max.)
- 12 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 product terms:
 - 32 logic terms
 - 10 control terms
- Ni-Cr programmable links
- Input loading: –100µA (max.)
- Power dissipation: 750mW (typ.)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

PIN CONFIGURATIONS



ORDERING INFORMATION

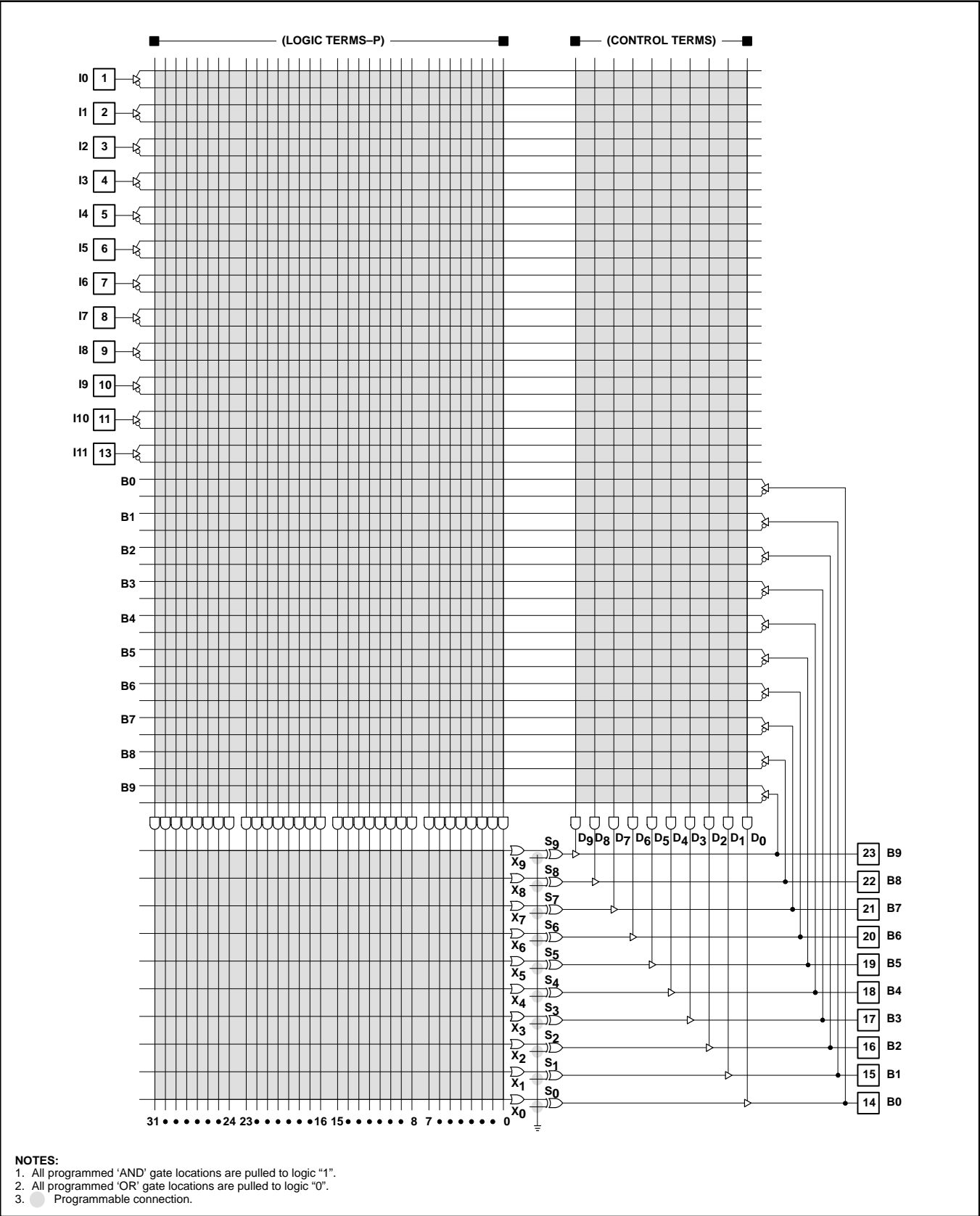
DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Dual-In-Line 300mil-wide	PLS173N	0410D
28-Pin Plastic Leaded Chip Carrier	PLS173A	0401F

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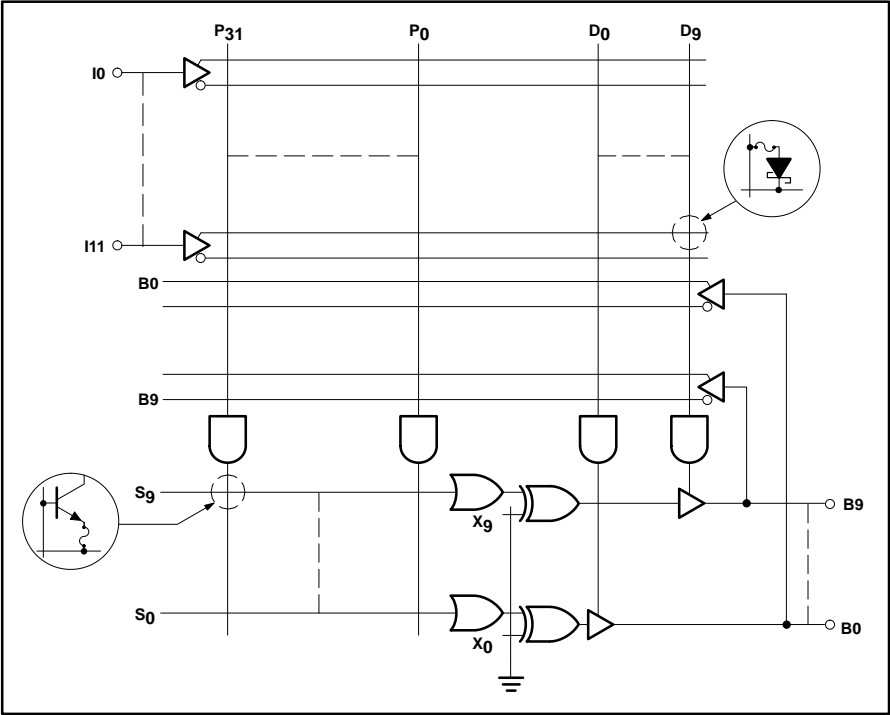
LOGIC DIAGRAM



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FUNCTIONAL DIAGRAM



LOGIC FUNCTION

TYPICAL PRODUCT TERM:
 $P_n = A \cdot \bar{B} \cdot C \cdot D \cdot \dots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
 $Z = P_0 + P_1 + P_2 \dots$

AT OUTPUT POLARITY = L
 $Z = \overline{P_0 + P_1 + P_2 \dots}$
 $Z = \overline{P_0} \cdot \overline{P_1} \cdot \overline{P_2} \dots$

NOTES:

1. For each of the 10 outputs, either function Z (Active-High) or \bar{Z} (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.

2. ZX, A, B, C, etc. are user defined connections to fixed inputs (I), and bidirectional pins (B).

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V _{CC}	Supply voltage		+7	V _{DC}
V _{IN}	Input voltage		+5.5	V _{DC}
V _{OUT}	Output voltage		+5.5	V _{DC}
I _{IN}	Input currents	−30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{amb}	Operating free-air temperature range	0	+75	°C
T _{stg}	Storage temperature range	−65	+150	°C

- NOTES:**
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS173 is also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Philips Semiconductors Military Data Handbook.

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DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +75^{\circ}\text{C}$, $4.75 \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage ²						
V _{IL}	Low	V _{CC} = MIN	2.0		0.8	V
V _{IH}	High	V _{CC} = MAX			V	
V _{IC}	Clamp ³	V _{CC} = MIN, I _{IN} = −12mA			V	
Output voltage ²						
V _{OL}	Low ⁴	V _{CC} = MIN I _{OL} = 15mA	2.4		0.5	V
V _{OH}	High ⁵	I _{OH} = −2mA			V	
Input current ⁹						
I _{IL}	Low	V _{CC} = MAX V _{IN} = 0.45V			−100	μA
I _{IH}	High	V _{IN} = V _{CC}			40	μA
Output current						
I _{O(OFF)}	Hi-Z state ⁸	V _{CC} = MAX V _{OUT} = 5.5V V _{OUT} = 0.45V	−15		80 −140	μA
I _{OS}	Short circuit ^{3, 5, 6}	V _{OUT} = 0V			−70	mA
I _{CC}	V _{CC} supply current ⁷	V _{CC} = MAX		150	170	mA
Capacitance						
I _{IN}	Input	V _{CC} = 5V V _{IN} = 2.0V		8		pF
C _B	I/O	V _B = 2.0V		15	pF	

NOTES:

1. All typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^{\circ}\text{C}$.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs V_{IL} applied to I_{11} . Pins 1–5 = 0V, Pins 6–10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V.
5. Same conditions as Note 4 except Pin 11 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0 and $I_1 = 0\text{V}$, and $I_2 - I_{11}$ and $B_0 - B_9 = 4.5\text{V}$. Part in Virgin State.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 - I_{11}$).

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AC ELECTRICAL CHARACTERISTICS

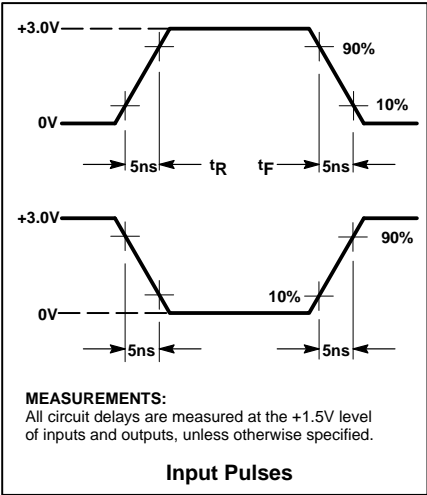
0°C ≤ T_{amb} ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V, R₁ = 470Ω, R₂ = 1kΩ

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS			UNIT
					MIN	TYP	MAX	
t _{PD}	Propagation delay ²	Input ±	Output ±	C _L = 30pF		20	30	ns
t _{OE}	Output enable ¹	Input ±	Output –	C _L = 30pF		20	30	ns
t _{OD}	Output disable ¹	Input ±	Output +	C _L = 5pF		20	30	ns

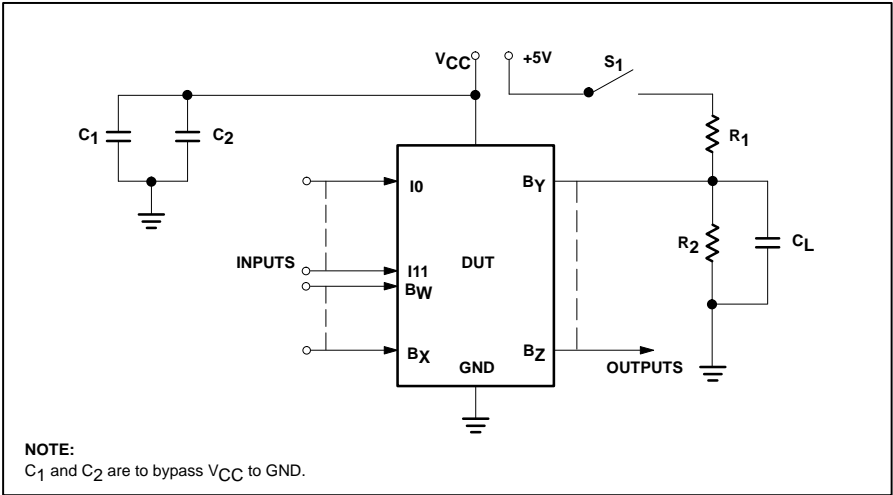
NOTES:

- For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S₁ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} – 0.5V) with S₁ open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S₁ closed.
- All propagation delays are measured and specified under worst case conditions.

VOLTAGE WAVEFORM



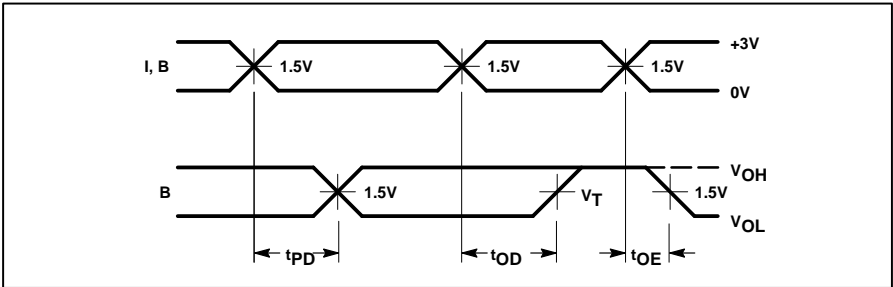
TEST LOAD CIRCUIT



TIMING DEFINITIONS

SYMBOL	PARAMETER
t _{PD}	Propagation delay between input and output.
t _{OD}	Delay between input change and when output is off (Hi-Z or High).
t _{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



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LOGIC PROGRAMMING

The PLS173 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP, Data I/O Corporation's ABEL™, and Logical Devices Incorporated's CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

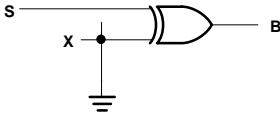
PLS173 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

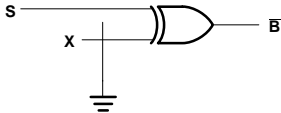
PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Third-Party Programmer/Software Support*) of this data handbook for additional information.

OUTPUT POLARITY – (B)

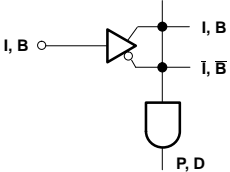


ACTIVE LEVEL	CODE
HIGH ¹ (NON-INVERTING)	H

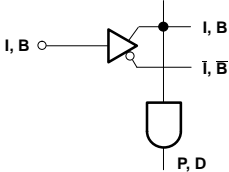


ACTIVE LEVEL	CODE
LOW (INVERTING)	L

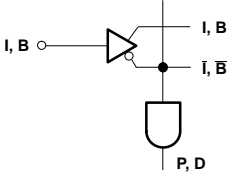
AND ARRAY – (I, B)



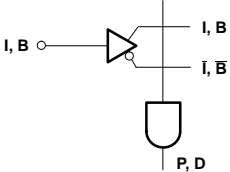
STATE	CODE
INACTIVE ^{1, 2}	O



STATE	CODE
I, B	H

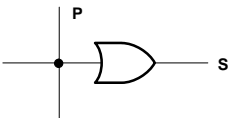


STATE	CODE
I, B̄	L

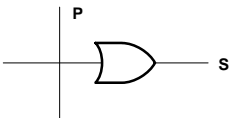


STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P _n STATUS	CODE
ACTIVE ¹	A



P _n STATUS	CODE
INACTIVE	•

NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the True and Complement of any input (I, B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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CUPL is a trademark of Logical Devices, Inc.

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PROGRAM TABLE

CUSTOMER NAME

PHILIPS DEVICE #

PROGRAM TABLE # REV DATE

NOTES

1. The PLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table.
(Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (—).
3. Unused product terms can be left blank.

OR

ACTIVE

INACTIVE

A

B(0)

CONTROL

(POL)

H

L

AND

INACTIVE

0

I, B

H

I, B

L

DON'T CARE

—

TER M

0

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3

4

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VARIABLE NAME

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POLARITY

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October 22, 1993

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SNAP RESOURCE SUMMARY DESIGNATIONS

