

SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

SLLS005B – OCTOBER 1980 – REVISED MAY 1995

- Meets IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multiple Controllers
- High-Speed, Low-Power Schottky Circuitry
- Low Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)

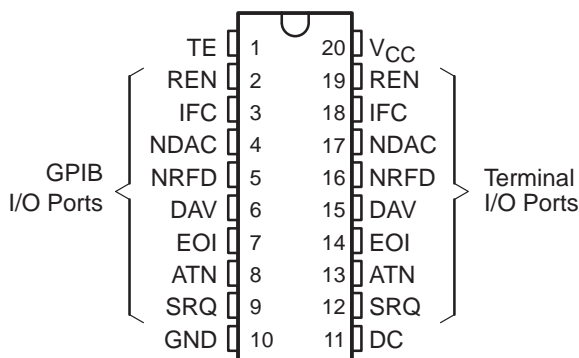
description

The SN75161B and SN75162B eight-channel, general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE-488 bus.

The SN75161B and SN75162B feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power-up/-down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power up and power down.

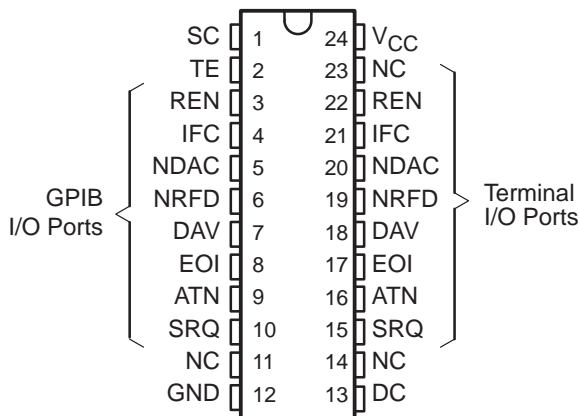
SN75161B . . . DW OR N PACKAGE

(TOP VIEW)



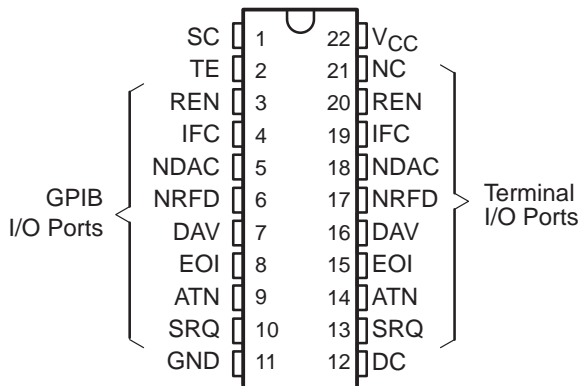
SN75162B . . . DW PACKAGE

(TOP VIEW)



SN75162B . . . N PACKAGE

(TOP VIEW)



NC—No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN75161B, SN75162B

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description (continued)

The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

Function Tables

SN75161B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

SN75162B RECEIVE/TRANSMIT

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



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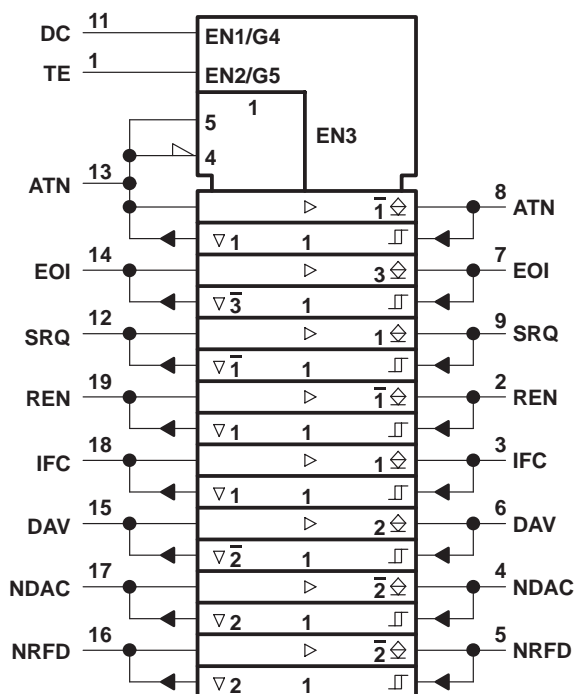
SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162B only)	
ATN	Attention	
SRQ	Service Request	
REN	Remote Enable	Bus Management
IFC	Interface Clear	
EOI	End of Identity	
DAV	Data Valid	
NDAC	Not Data Accepted	Data Transfer
NRFD	Not Ready for Data	

SN75161B logic symbol†

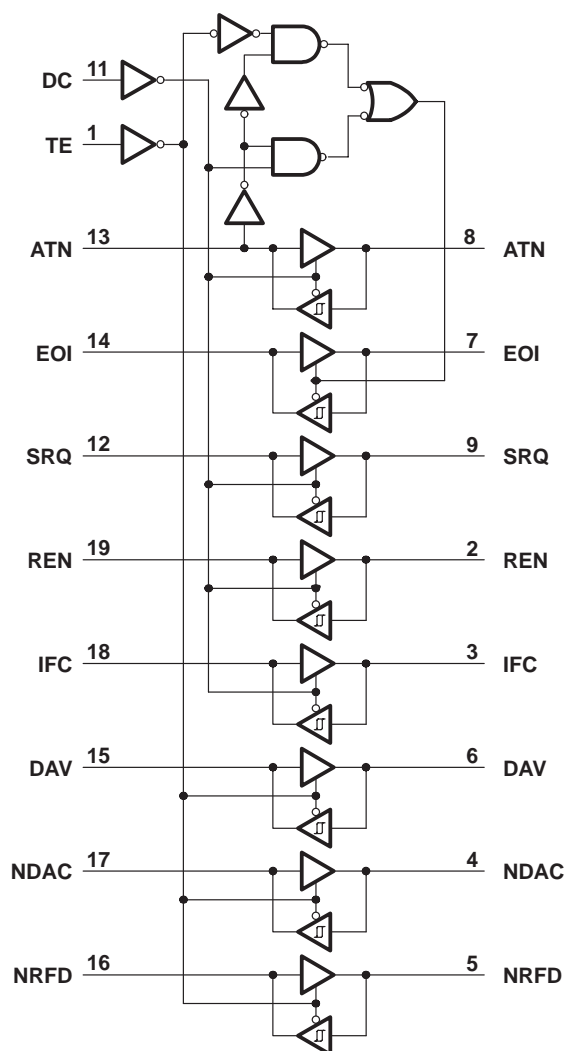


† This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

⊗ Designates passive-pullup outputs

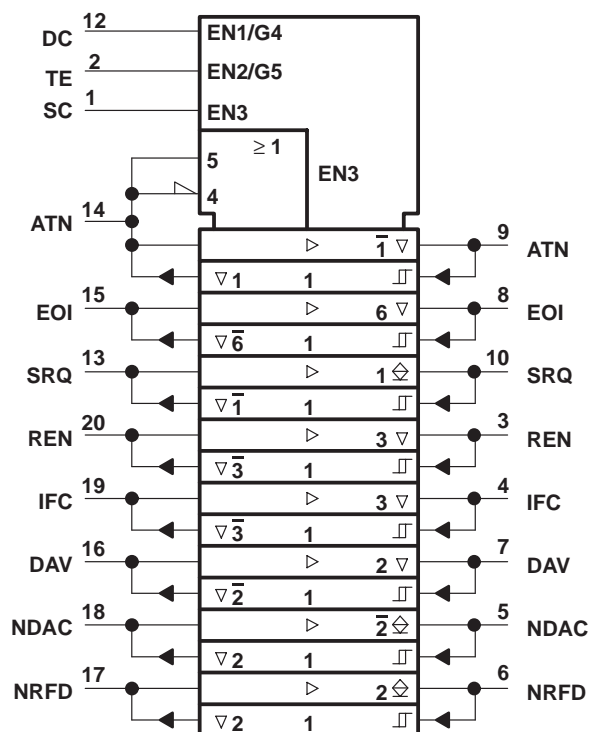
SN75161B logic diagram (positive logic)



SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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SN75162B logic symbol†

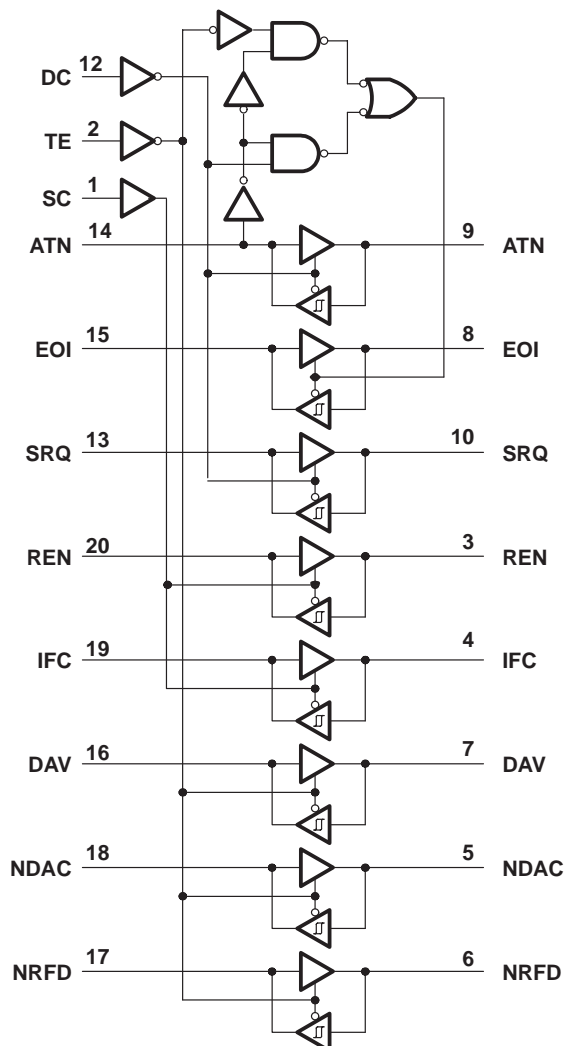


†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

⊗ Designates passive-pullup outputs

SN75162B logic diagram (positive logic)



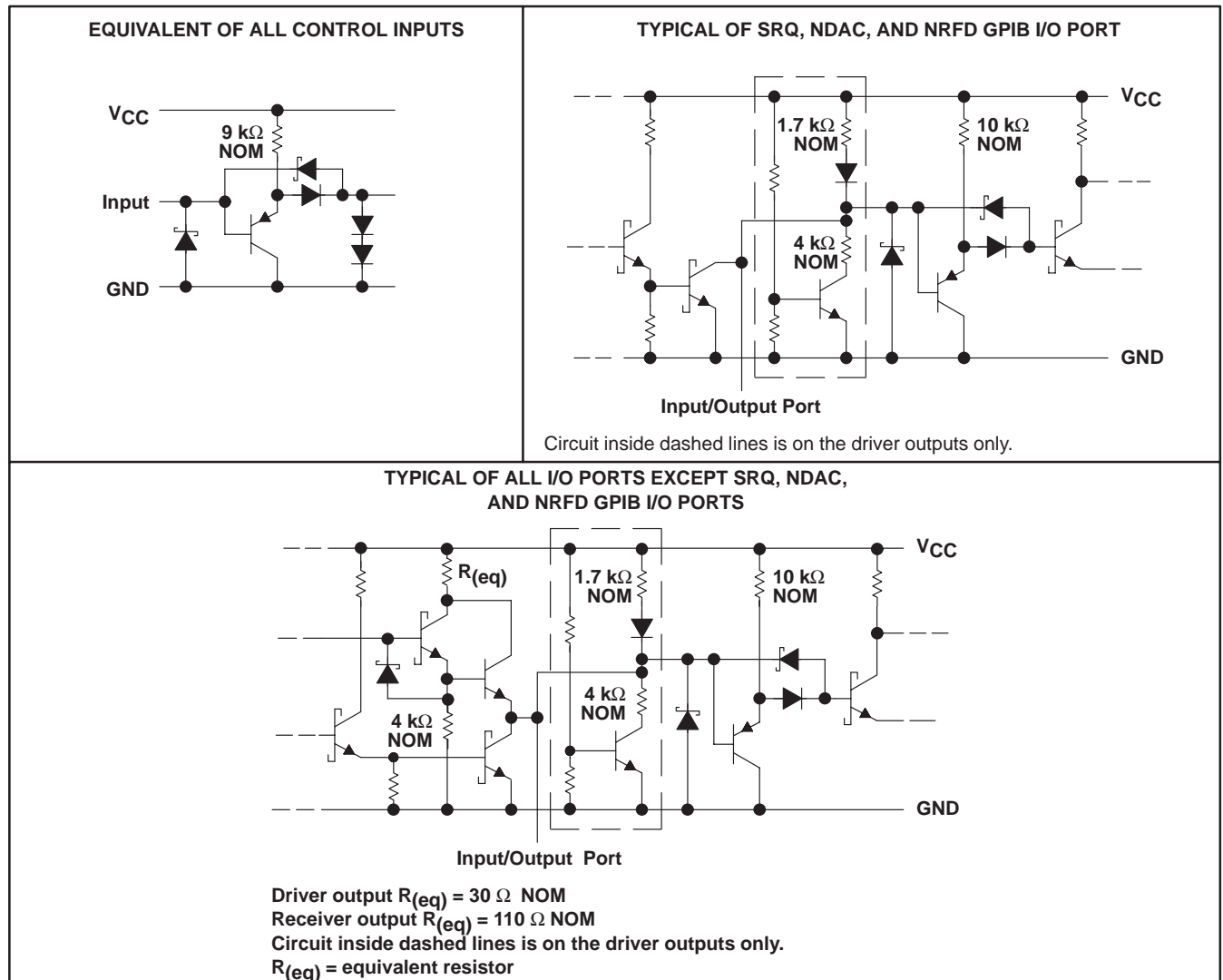
Pin numbers shown are for the N package.

SN75161B, SN75162B

OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Low-level driver output current, I_{OL}	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

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OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW (20 pin)	1125 mW	9.0 mW/ $^\circ\text{C}$	720 mW
DW (24 pin)	1350 mW	10.8 mW/ $^\circ\text{C}$	864 mW
N (20 pin)	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW
N (22 pin)	1700 mW	13.6 mW/ $^\circ\text{C}$	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			-5.2	mA
	Terminal ports			-800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	$^\circ\text{C}$



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18 \text{ mA}$	-0.8	-1.5		V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus	See Figure 7	0.4	0.65		V
V_{OH}^{\ddagger}	High-level output voltage	Terminal	$I_{OH} = -800 \mu\text{A}$	2.7	3.5		V
		Bus	$I_{OH} = -5.2 \text{ mA}$	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16 \text{ mA}$		0.3	0.5	V
		Bus	$I_{OL} = 48 \text{ mA}$		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5 \text{ V}$		0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7 \text{ V}$		0.1	20	μA
I_{IL}	Low-level input current		$V_I = 0.5 \text{ V}$		-10	-100	μA
$V_{I/O(\text{bus})}$ Voltage at bus port		Driver disabled	$I_{I(\text{bus})} = 0$	2.5	3.0	3.7	V
			$I_{I(\text{bus})} = -12 \text{ mA}$			-1.5	
$I_{I/O(\text{bus})}$ Current into bus port	Current into bus port	Power on	Driver disabled	$V_{I(\text{bus})} = -1.5 \text{ V to } 0.4 \text{ V}$		-1.3	mA
				$V_{I(\text{bus})} = 0.4 \text{ V to } 2.5 \text{ V}$		0	
				$V_{I(\text{bus})} = 2.5 \text{ V to } 3.7 \text{ V}$			
				$V_{I(\text{bus})} = 3.7 \text{ V to } 5 \text{ V}$		0	
				$V_{I(\text{bus})} = 5 \text{ V to } 5.5 \text{ V}$		0.7	
		Power off	$V_{CC} = 0, V_{I(\text{bus})} = 0 \text{ V to } 2.5 \text{ V}$			-40	μA
I_{OS}	Short-circuit output current	Terminal		-15	-35	-75	mA
		Bus		-25	-50	-125	
I_{CC}	Supply current		No load, TE, DE, and SC low			110	mA
$C_{I/O(\text{bus})}$	Bus-port capacitance		$V_{CC} = 5 \text{ V to } 0, V_{I/O} = 0 \text{ to } 2 \text{ V}, f = 1 \text{ MHz}$		16		pF

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ V_{OH} applies for 3-state outputs only.

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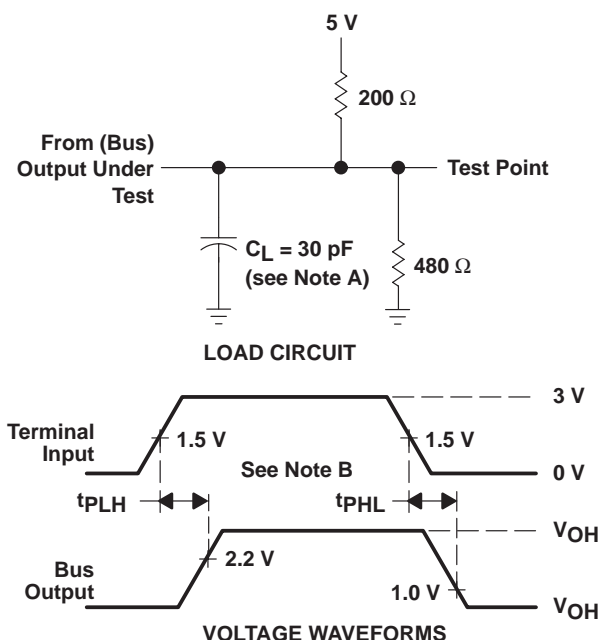
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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

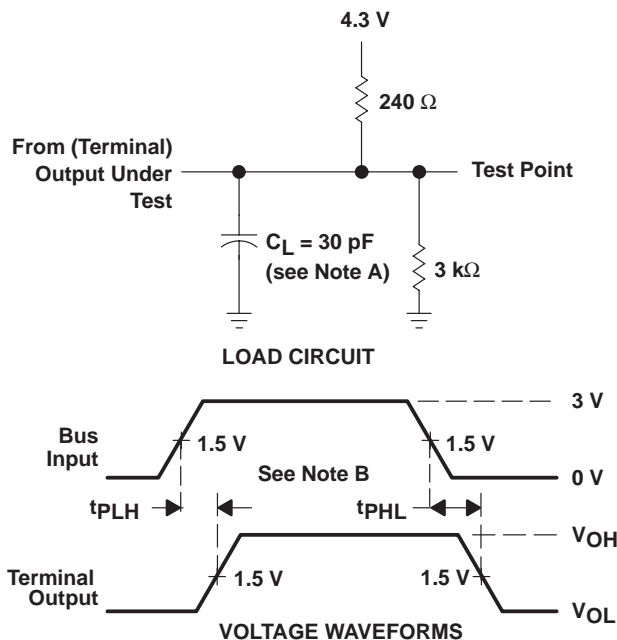
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	Terminal	Bus	$C_L = 30\text{ pF}$, See Figure 1		14	20	ns
t_{PHL} Propagation delay time, high- to low-level output					14	20	
t_{PLH} Propagation delay time, low- to high-level output	Terminal	Bus (SRQ, NDAC, NRFD)	$C_L = 30\text{ pF}$, See Figure 1		29	35	ns
t_{PLH} Propagation delay time, low- to high-level output	Bus	Terminal	$C_L = 30\text{ pF}$, See Figure 2		10	20	ns
t_{PHL} Propagation delay time, high- to low-level output					15	22	
t_{PZH} Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t_{PHZ} Output disable time from high level						45	
t_{PZL} Output enable time to low level						60	
t_{PLZ} Output disable time from low level						55	
t_{PZH} Output enable time to high level	TE, DC, or SC	Terminal	See Figure 4			55	ns
t_{PHZ} Output disable time from high level						50	
t_{PZL} Output enable time to low level						45	
t_{PLZ} Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms



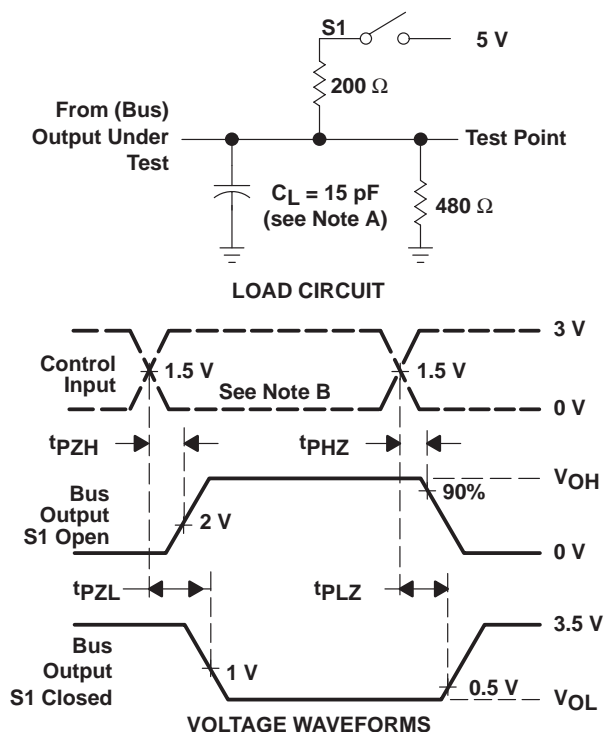
- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

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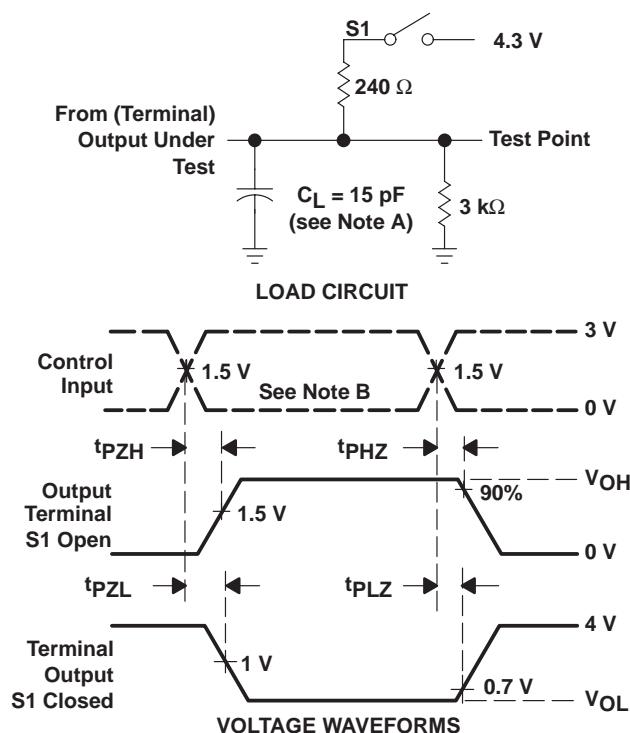
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 3. Bus Enable and Disable Times Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The Input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, t_r \leq 6 ns, t_f \leq 6 ns, Z_O = 50 Ω .

Figure 4. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

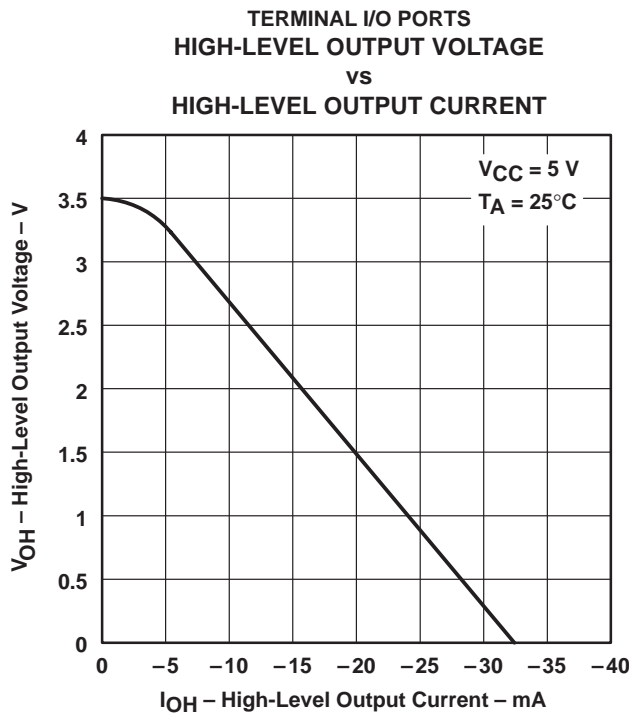


Figure 5

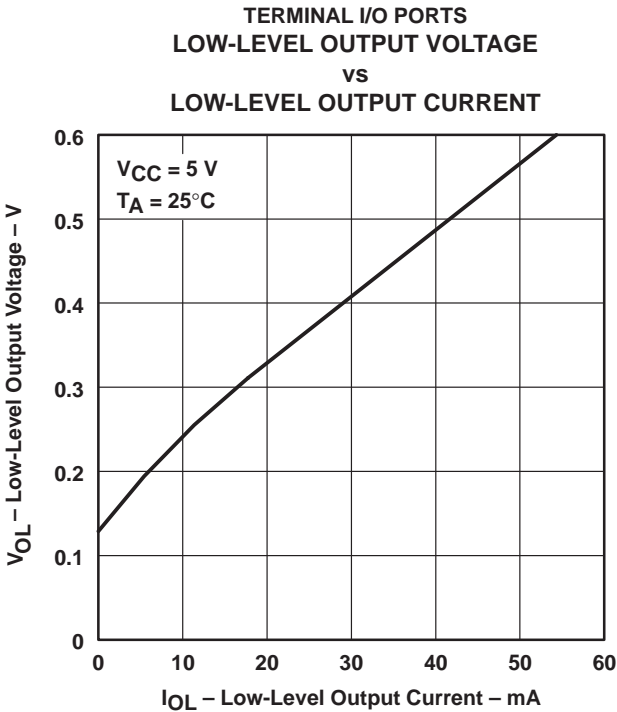


Figure 6

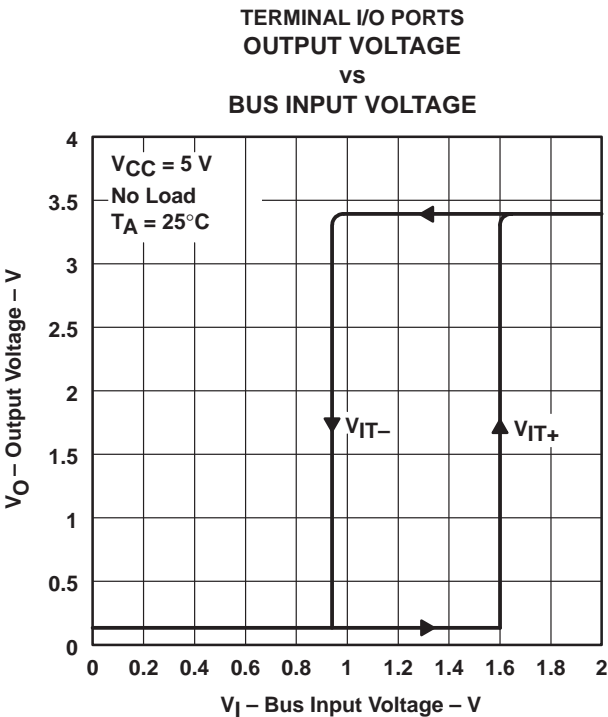


Figure 7

SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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TYPICAL CHARACTERISTICS

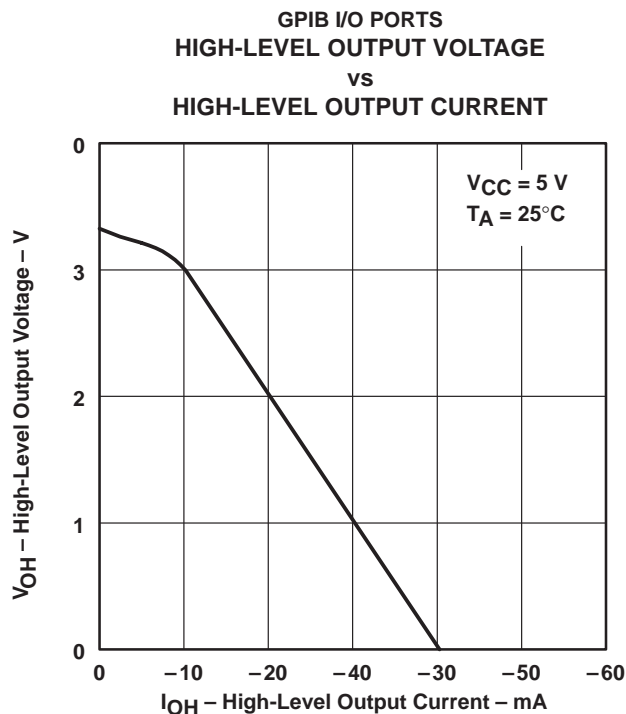


Figure 8

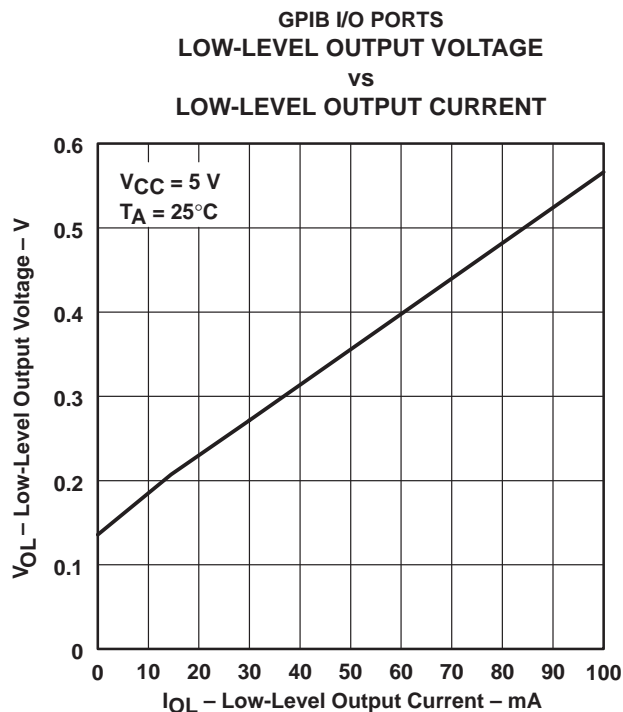


Figure 9

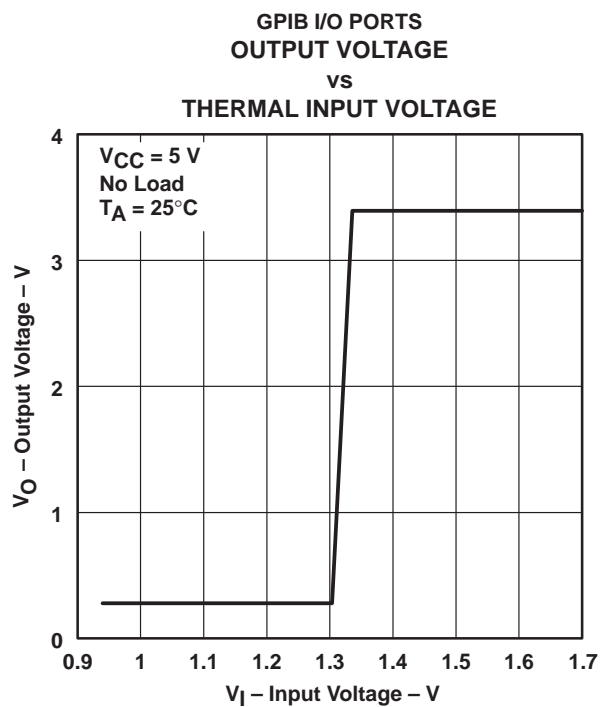


Figure 10

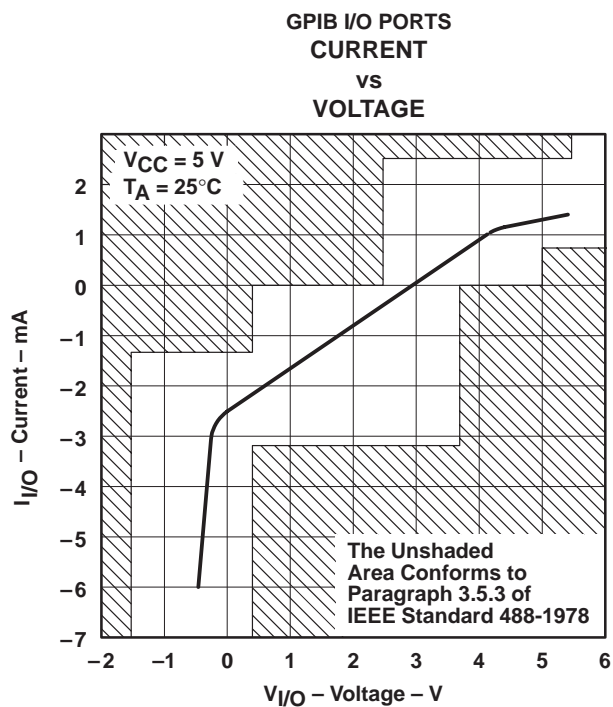


Figure 11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75161BDW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B
SN75161BDW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B
SN75161BDWG4	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B
SN75161BDWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B
SN75161BDWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B
SN75161BDWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B
SN75161BN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75161BN
SN75161BN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75161BN
SN75161BNE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75161BN
SN75162BDW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B
SN75162BDW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B
SN75162BDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B
SN75162BDWR.A	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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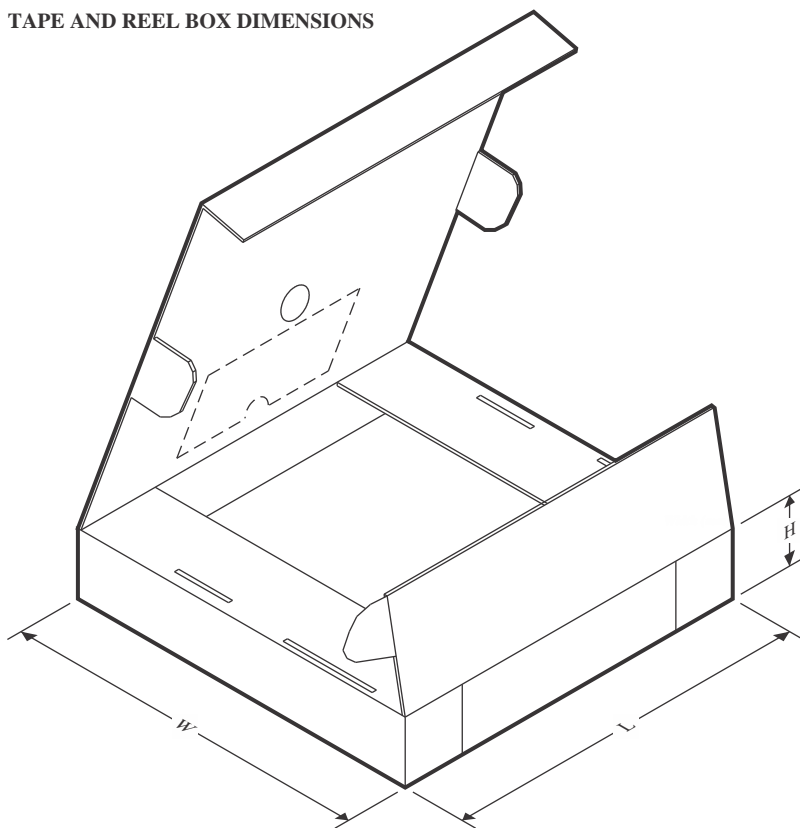
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75161BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75162BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

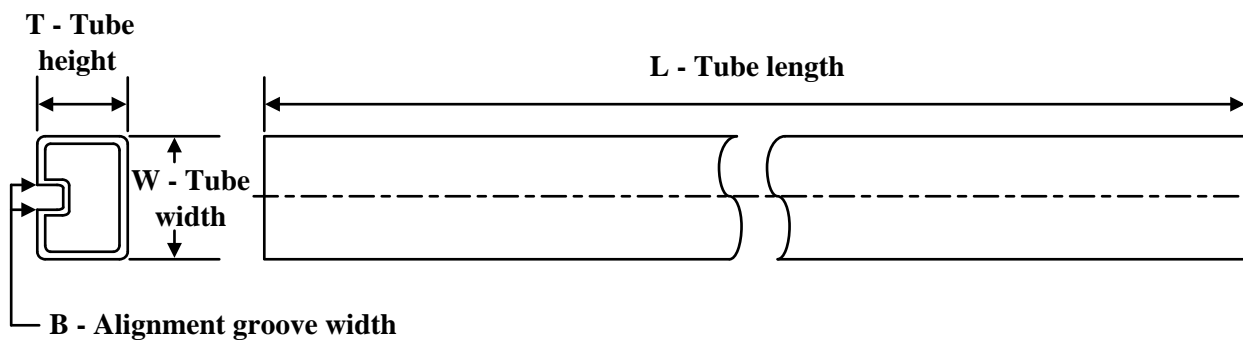
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75161BDWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN75162BDWR	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE

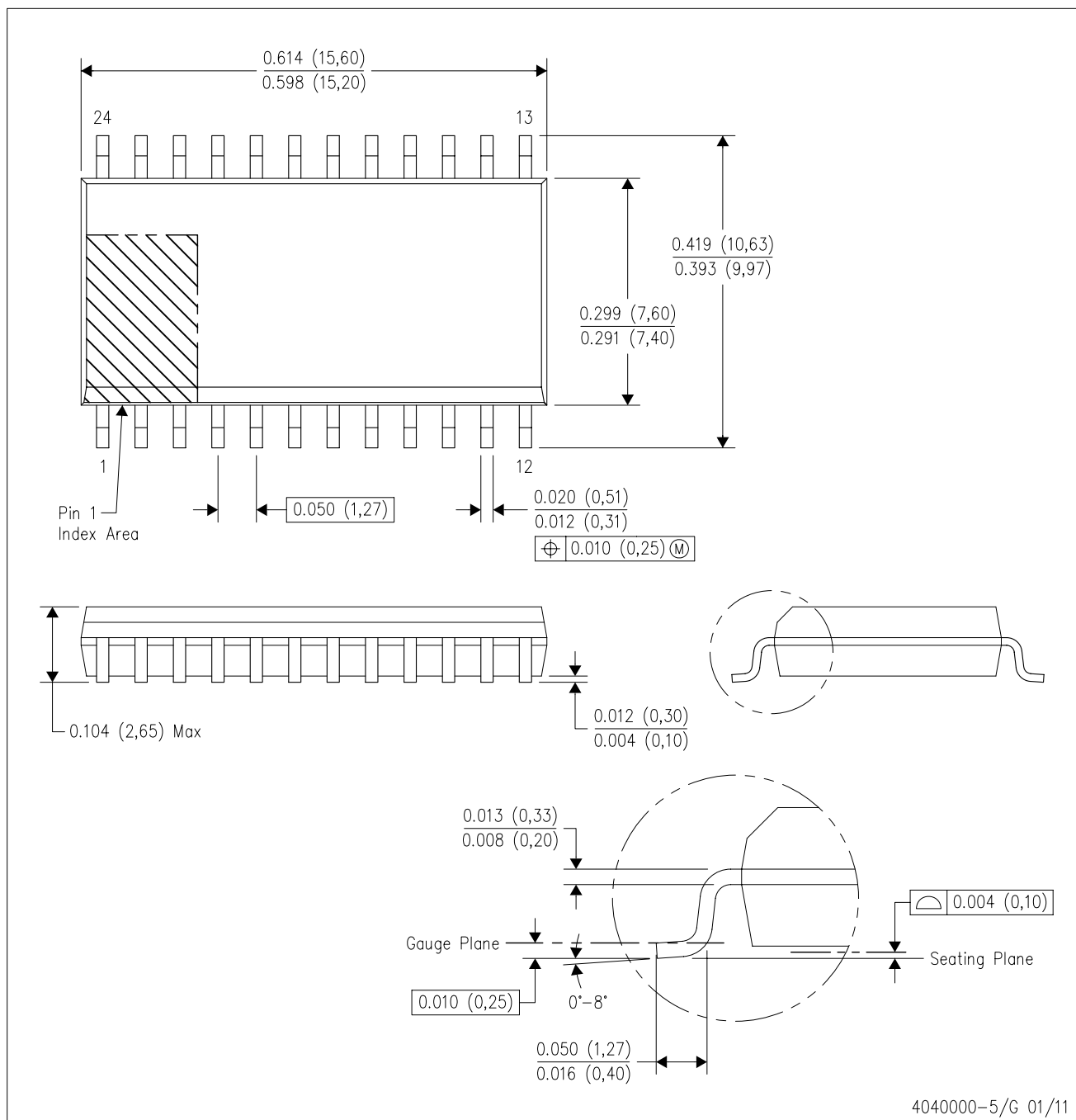


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75161BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75161BDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75161BDW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75161BDW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN75161BDWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN75161BDWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75161BN	N	PDIP	20	20	506	13.97	11230	4.32
SN75161BN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN75161BNE4	N	PDIP	20	20	506	13.97	11230	4.32
SN75162BDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN75162BDW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

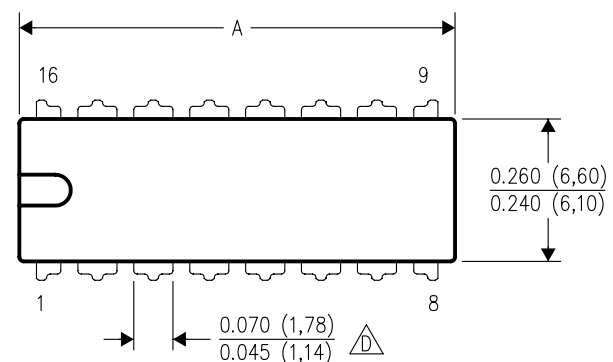


- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

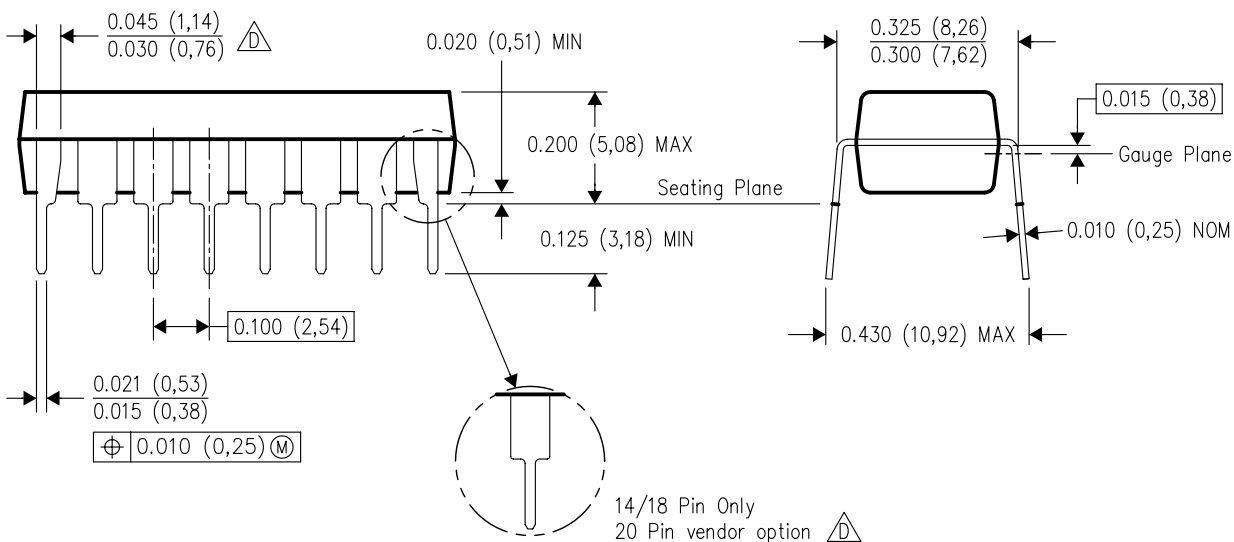
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





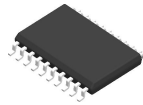
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



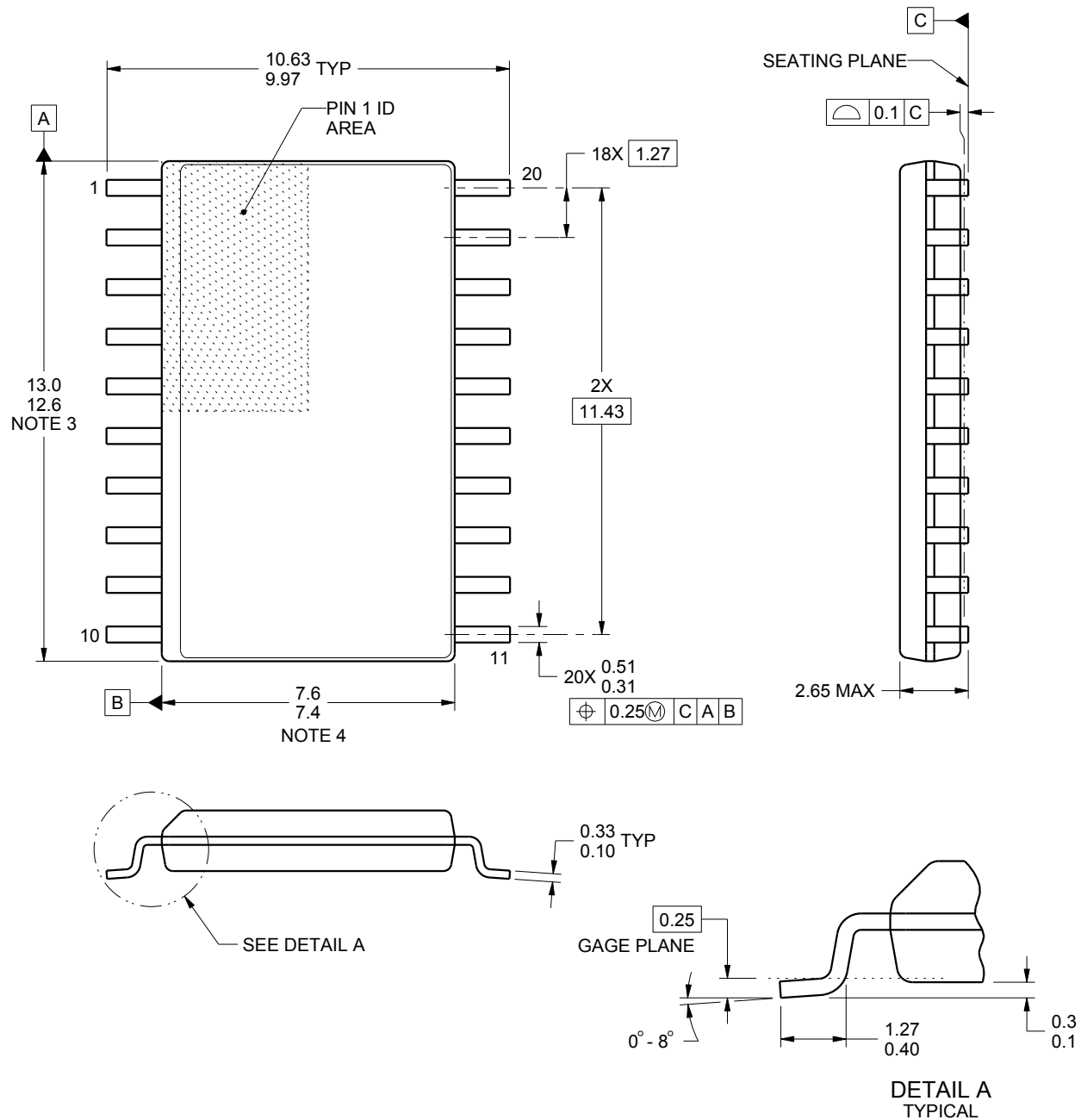
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A**PACKAGE OUTLINE****SOIC - 2.65 mm max height**

SOIC



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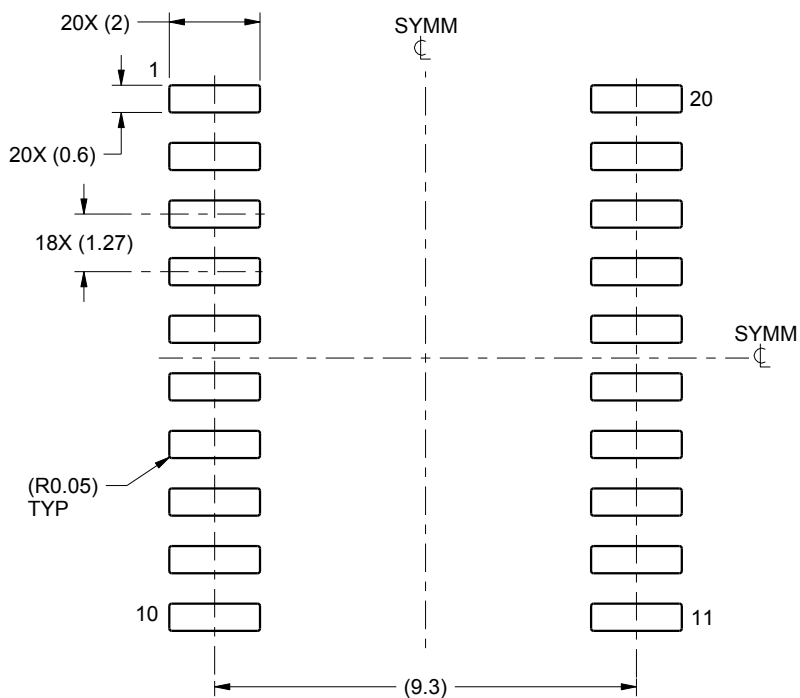
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

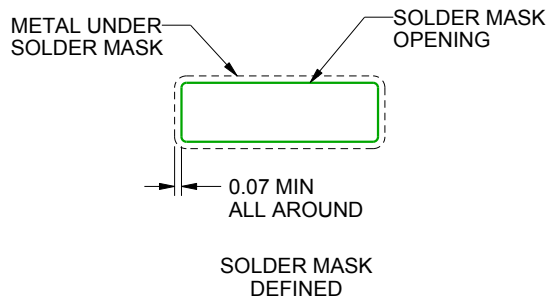
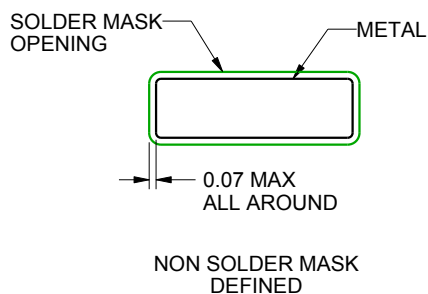
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

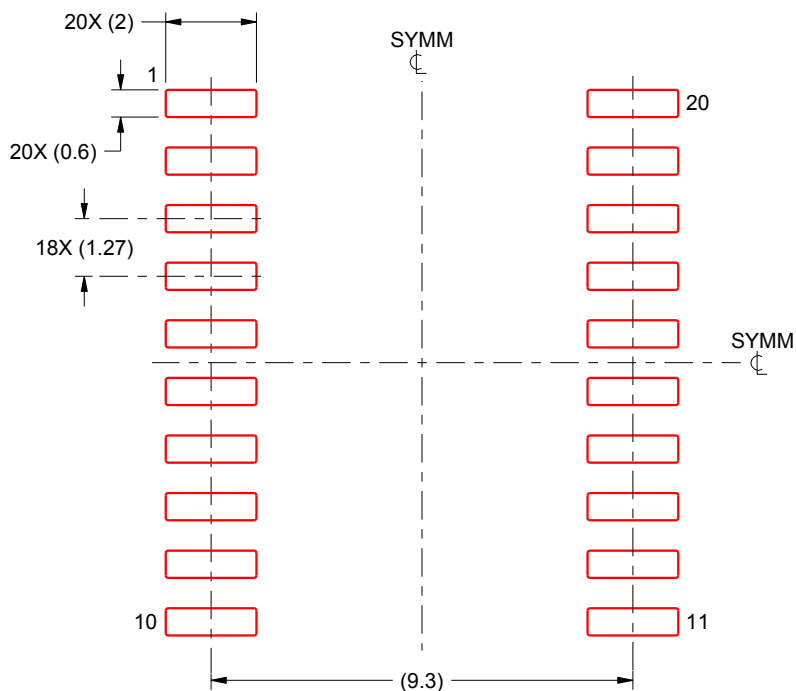
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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