

TC5118165BJ/BFT-60/70

PRELIMINARY

1,048,576 WORD X 16 BIT HYPER PAGE (EDO) DYNAMIC RAM

Description

The TC5118165BJ/BFT is the hyper page (EDO) dynamic RAM organized 1,048,576 words by 16 bits. The TC5118165BJ/BFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5118165BJ/BFT to be packaged in a standard 42 pin plastic SOJ and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

B DRAM
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Features

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power
 - 990mW MAX. Operating (TC5118165BJ/BFT-60)
 - 825mW MAX. Operating (TC5118165BJ/BFT-70)
 - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} -only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC5118165BJ: SOJ42-P-400
TC5118165BFT: TSOP50-P-400

Note: For packaging details see Mechanical Dimensions section.

Key Parameters

ITEM		TC5118165BJ/BFT	
		-60	-70
t_{RAC}	\overline{RAS} Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	\overline{CAS} Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

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Pin Name

A0 ~ A9	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Column Address Strobe/ Upper Byte Control
$\overline{\text{LCAS}}$	Column Address Strobe/ Lower Byte Control
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O1 ~ I/O16	Data Input/Output
V_{CC}	Power (+5.0V)
V_{SS}	Ground
NC	No Connection

Pin Connection (Top View)

Plastic SOJ

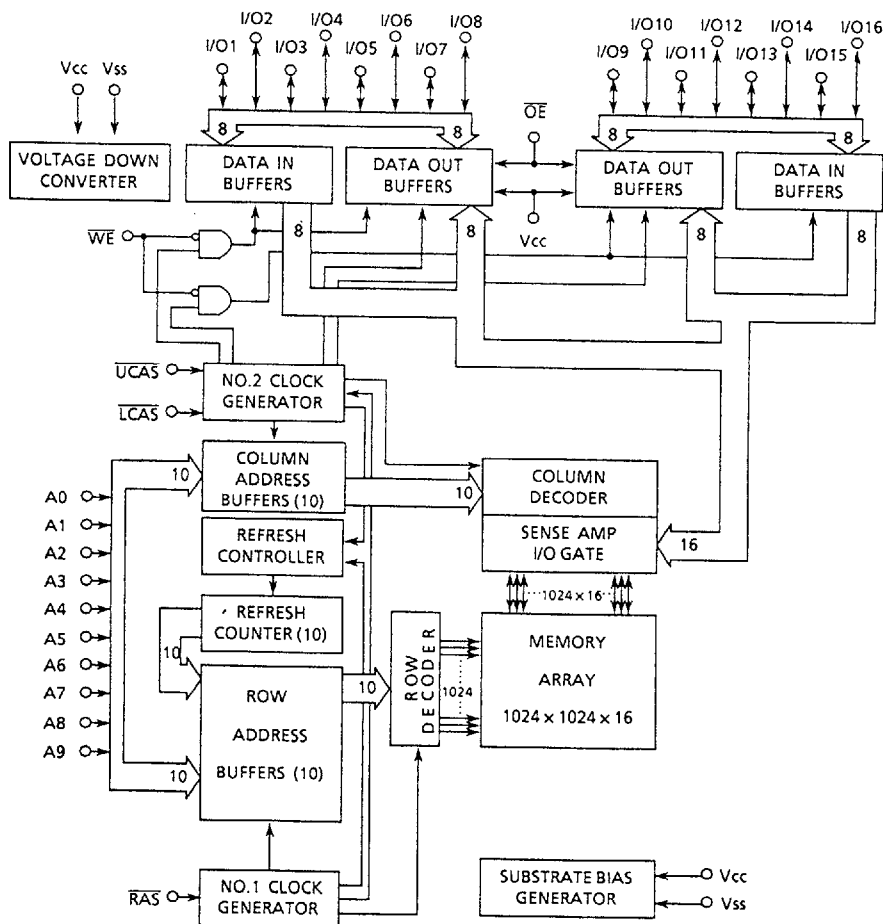
V_{CC}	1	42	V_{SS}
I/O1	2	41	I/O16
I/O2	3	40	I/O15
I/O3	4	39	I/O14
I/O4	5	38	I/O13
V_{CC}	6	37	V_{SS}
I/O5	7	36	I/O12
I/O6	8	35	I/O11
I/O7	9	34	I/O10
I/O8	10	33	I/O9
NC	11	32	NC
NC	12	31	$\overline{\text{LCAS}}$
$\overline{\text{WE}}$	13	30	$\overline{\text{UCAS}}$
$\overline{\text{RAS}}$	14	29	$\overline{\text{OE}}$
NC	15	28	A9
NC	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
V_{CC}	21	22	V_{SS}

Plastic TSOP

V_{CC}	1	50	V_{SS}
I/O1	2	49	I/O16
I/O2	3	48	I/O15
I/O3	4	47	I/O14
I/O4	5	46	I/O13
V_{CC}	6	45	V_{SS}
I/O5	7	44	I/O12
I/O6	8	43	I/O11
I/O7	9	42	I/O10
I/O8	10	41	I/O9
NC	11	40	NC
NC	15	36	NC
NC	16	35	$\overline{\text{LCAS}}$
$\overline{\text{WE}}$	17	34	$\overline{\text{UCAS}}$
$\overline{\text{RAS}}$	18	33	$\overline{\text{OE}}$
NC	19	32	A9
NC	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
V_{CC}	25	26	V_{SS}

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Block Diagram



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Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	$0 \sim 70$	$^{\circ}C$	1
Storage Temperature	T_{STG}	$-55 \sim 150$	$^{\circ}C$	1
Soldering Temperature (10s)	T_{SOLDER}	260	$^{\circ}C$	1
Power Dissipation	P_D	1.3	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

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Recommended DC Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	-	V _{CC} + 0.5*	V	2
V _{IL}	Input Low Voltage	-0.5**	-	0.8	V	2

*V_{CC} + 2.0V at pulse width ≤ 20ns (pulse width is measured at V_{CC}).**-2.0V at pulse width ≤ 20ns (pulse width is measured at V_{SS}).DC Electrical Characteristics (V_{CC} = 5V±10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I _{CC1}	OPERATING CURRENT Average Power Supply Operating Current (RAS, UCAS, ULAS, Address Cycling: t _{RC} =t _{RC} MIN.)	TC5118165BJ/BFT-60	-	180	mA	3, 4, 5
		TC5118165BJ/BFT-70	-	150	mA	
I _{CC2}	STANDBY CURRENT Power Supply Standby Current (RAS=UCAS=ULAS=V _{IH})			2	mA	
I _{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, UCAS=ULAS=V _{IH} : t _{RC} =t _{RC} MIN.)	TC5118165BJ/BFT-60	-	180	mA	3, 5
		TC5118165BJ/BFT-70	-	150	mA	
I _{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode (RAS=V _{IL} , UCAS, ULAS, Address Cycling: t _{HPC} =t _{HPC} MIN.)	TC5118165BJ/BFT-60	-	110	mA	3, 4, 5
		TC5118165BJ/BFT-70	-	100	mA	
I _{CC5}	STANDBY CURRENT Power Supply Standby Current (RAS=UCAS=ULAS=V _{CC} -0.2V)		-	1	mA	
I _{CC6}	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS, UCAS, ULAS Cycling: t _{RC} =t _{RC} MIN.)	TC5118165BJ/BFT-60	-	180	mA	3, 4, 5
		TC5118165BJ/BFT-70	-	150	mA	
I _{I (L)}	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V _{IN} ≤0.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
I _{O (L)}	OUTPUT LEAKAGE CURRENT (D _{OUT} is disabled, (0V≤V _{OUT} ≤V _{CC}))		-10	10	μA	
V _{OH}	OUTPUT LEVEL Output "H" Level Voltage (I _{OUT} = -5mA)		2.4	-	V	
V _{OL}	OUTPUT LEVEL Output "L" Level Voltage (I _{OUT} =4.2mA)		-	0.4	V	

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Electrical Characteristics and Recommended AC Operating Conditions ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

(Notes 6,7,8)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t _{RC}	Random Read or Write Cycle Time	104	-	124	-	ns	
t _{RMW}	Read-Modify-Write Cycle	135	-	157	-	ns	
t _{RAC}	Access Time from RAS	-	60	-	70	ns	9, 14, 15
t _{CAC}	Access Time from CAS	-	17	-	20	ns	9, 14
t _{AA}	Access Time from Column Address	-	30	-	35	ns	9, 15
t _{CPA}	Access Time from CAS Precharge	-	35	-	40	ns	9
t _{CLZ}	CAS to Output in Low-Z	0	-	0	-	ns	9
t _{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10, 16
t _T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t _{RP}	RAS Precharge Time	40	-	50	-	ns	
t _{RAS}	RAS Pulse Width	60	10,000	70	10,000	ns	
t _{RASP}	RAS Pulse Width (Hyper Page Mode)	60	100,000	70	100,000	ns	
t _{RSH}	RAS Hold Time	10	-	12	-	ns	
t _{RHCP}	RAS Hold Time from CAS Precharge (Hyper Page Mode)	35	-	40	-	ns	
t _{CSH}	CAS Hold Time	40	-	50	-	ns	
t _{CAS}	CAS Pulse Width	10	10,000	12	10,000	ns	
t _{RCD}	RAS to CAS Delay Time	14	43	14	50	ns	14
t _{RAD}	RAS to Column Address Delay Time	12	30	12	35	ns	15
t _{CRP}	CAS to RAS Precharge Time	5	-	5	-	ns	
t _{CP}	CAS Precharge Time	10	-	10	-	ns	
t _{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t _{RAH}	Row Address Hold Time	10	-	10	-	ns	
t _{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t _{CAH}	Column Address Hold Time	10	-	12	-	ns	
t _{RAL}	Column Address to RAS Lead Time	30		35		ns	
t _{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t _{RRH}	Read Command Hold Time referenced to RAS	0	-	0	-	ns	11
t _{WCH}	Write Command Hold Time	10	-	12	-	ns	

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Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t _{WP}	Write Command Pulse Width	10	-	12	-	ns	
t _{RWL}	Write Command to RAS Lead Time	10	-	12	-	ns	
t _{CWL}	Write Command to CAS Lead Time	10	-	12	-	ns	
t _{DS}	Data Set-Up Time	0	-	0	-	ns	12
t _{DH}	Data Hold Time	10	-	12	-	ns	12
t _{REF}	Refresh Period	-	16	-	16	ms	
t _{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t _{CWD}	CAS to WE Delay Time	36	-	39	-	ns	13
t _{RWD}	RAS to WE Delay Time	79	-	89	-	ns	13
t _{AWD}	Column Address to WE Delay Time	49	-	54	-	ns	13
t _{CPWD}	CAS Precharge to WE Delay Time	54	-	59	-	ns	13
t _{CSR}	CAS Set-Up Time (CAS before RAS Cycle)	5	-	5	-	ns	
t _{CHR}	CAS Hold Time (CAS before RAS Cycle)	10	-	15	-	ns	
t _{RPC}	RAS to CAS Precharge Time	5	-	5	-	ns	
t _{CPT}	CAS Precharge Time (CAS before RAS Counter Test Cycle)	20	-	20	-	ns	
t _{ROH}	RAS Hold Time referenced to OE	10	-	10	-	ns	
t _{OEA}	OE Access Time	-	15	-	20	ns	9
t _{OED}	OE to Data Delay	15	-	15	-	ns	
t _{OLZ}	OE to Output in Low-Z	0	-	0	-	ns	
t _{OEZ}	Output buffer turn off Delay Time from OE	0	15	0	15	ns	10
t _{OEH}	OE Command Hold Time	10	-	12	-	ns	
t _{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	



Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	TC5118165BJ/BFT				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t _{RNCD}	RAS to next CAS Delay Time (Hyper Page Mode)	60	-	70	-	ns	
t _{HPC}	Hyper Page Mode Cycle Time	25	-	30	-	ns	
t _{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	68	-	75	-	ns	
t _{COH}	Output Data Hold Time	5	-	5	-	ns	
t _{REZ}	Output Buffer Turn-off Delay from RAS	0	15	0	15	ns	10, 16
t _{WEZ}	Output Buffer Turn-off Delay from WE	0	15	0	15	ns	10
t _{WED}	WE to Data Delay	15	-	15	-	ns	
t _{OE}	OE Pulse Width	15	-	20	-	ns	
t _{OEP}	OE Precharge Time	10	-	12	-	ns	
t _{CPO}	CAS to OE Precharge Time	5	-	5	-	ns	

Capacitance (V_{CC} = 5V±10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C _{I1}	Input Capacitance (A0 ~ A9)	-	5	pF
C _{I2}	Input Capacitance (RAS, UCAS, LCAS, WE, OE)	-	7	
C _O	Input Capacitance (I/O1 ~ I/O16)	-	7	

Note: Please refer to Timing Diagrams Number 2.

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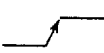
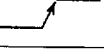
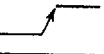
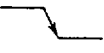
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Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of t_{CC4} , it can be changed once or less during a hyper page mode cycle (t_{HPC}).
6. An initial pause of 500 μ s is required after power-up followed by 8 \overline{RAS} only refresh cycles before proper device operation is achieved. When the internal refresh counter is used, a minimum of 8 \overline{CAS} before \overline{RAS} refresh cycles instead of 8 \overline{RAS} only refresh cycles are required.
7. AC measurements assume $t_f=2$ ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. This parameter is measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.), t_{OEZ} (max.), t_{REZ} (max.) and t_{WEZ} (max.), define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to \overline{UCAS} , \overline{LCAS} leading edge in early write cycles and to \overline{WE} leading edge in Read-Modify-Write cycles.
13. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{min.})$ (Hyper Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\text{max.})$ limit insures that t_{RAC} can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
15. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
16. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going (t_{OFF}). If \overline{CAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going (t_{REZ}).




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Data Out Hi-Z Control Logic

RAS	CAS	OE	WE	Timing Specification
"H"		"L"	"H"	t _{OFF}
	"H"	"L"	"H"	t _{REZ}
"L"	"L"		"H"	t _{OEZ}
"L"	"H"	"L"		t _{WEZ}

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Data Out Lo-Z Control Logic

RAS	CAS	OE	WE	Timing Specification
"L"		"L"	"H"	t _{CLZ}
"L"	"L"		"H"	t _{OLZ}
"L"	"L"		"H"	t _{OLZ}

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