DIC-Serielle Kommunikation mit einem µC

Fabio Plunser

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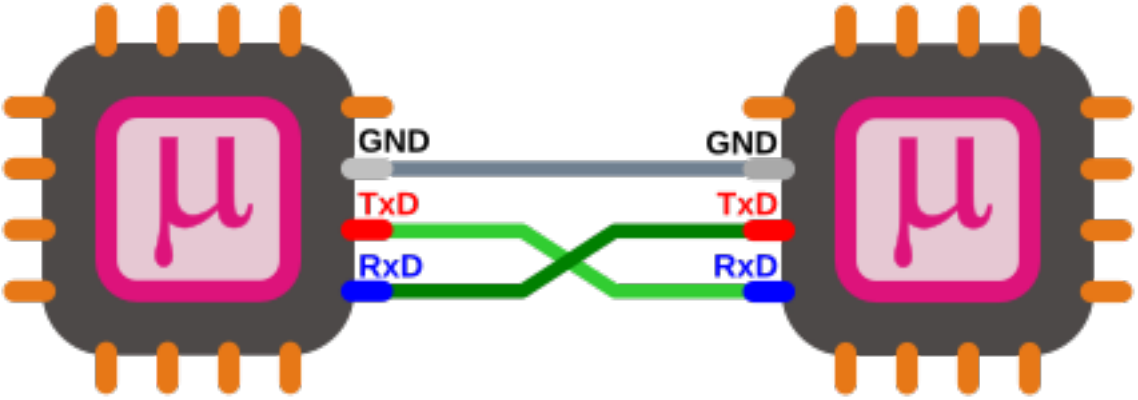

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Code

1 Aufgabenstellung

Die Aufgabe ist es auf dem STM32F030F4 Chip die UART3 so zu programmieren, dass sie den Wert eines eingebauten ADC per interrupt ausgibt.
Die richtige Aufgabe ist es die STM32F030F4 UART3 zu programmieren dass sie wenn sie ein zeichen erhält 10 Bytes zurückschickt.
Da dieses spezielle Package des STM32 keine UART3 besitzt ist die Aufgabenstellung so nicht möglich somit wird einfach die vorhandene UART1 Schnittstelle verwendet.
Der STM UART Ausgang wird mit einem MAX485 auf RS485 übersetzt.
UART einstellungen:
Baudrate: 38400 mit ODD parity

Dieser Arbeitsauftrag kann in dieser GIT-Repo verfolgt werden: `https://github.com/FabioPlunser/DIC-Lezuo`

2 RS485

2.1 Generelles

Ist ein Industriestandard der eine asynchrone serielle Datenübertragung ermöglicht.
Der Standard verwendet ein symmetrisches Leitungspaar, dass für eine höhere elektromagnetische Resistenz sorgt.

2.2 Wie funktioniert es?

Betriebsspannung 5V oder 3.3V
Der empfänger wertet die die Differenz beider Leitungen aus und kann Pegel ab $\pm 200mV$ erkennen.
Senderpegel können von $\pm 1.5V bis \pm 6V$
Logik:
Wenn $U_+ - U_- < -0.3V$ = MARK = OFF = Logisch 1
Wenn $U_+ - U_- > +0.3V$ = SPACE = ON = Logisch 0

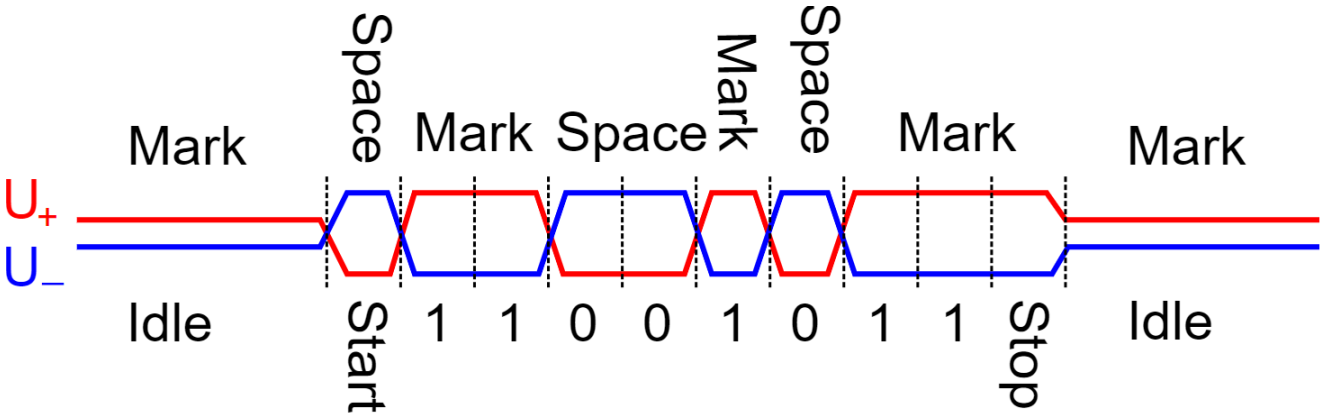

Abbildung 1: RS485-Diagramm

2.3 Wie wird der MAX485 angeschlossen

Unten ist ein Beispiel mit einem Arduino UNO
Anschluss:
DI → TX
RO → RX
DE, RE auf einen GPIO Pin. Da wenn DE + RE = 1 → Daten können nur gesendet werden.
Wenn DE + RE = 0 → Daten können nur empfangen werden.

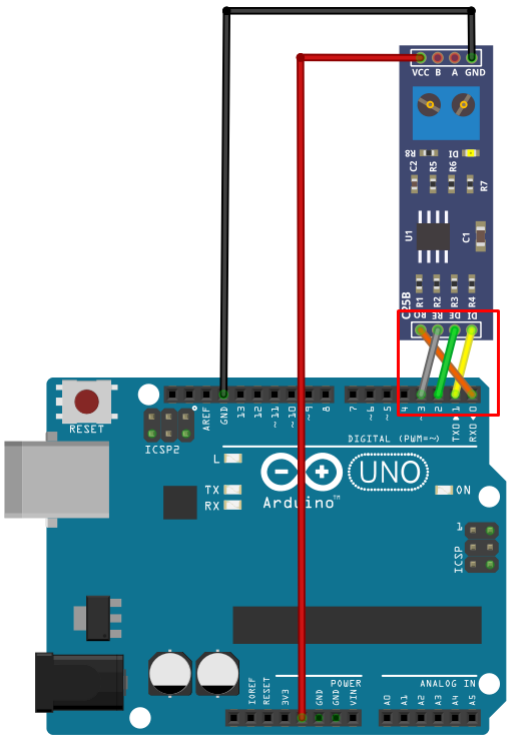

Abbildung 2: MAX485-Arduino-Anschluss-BSP

Ebenso muss dann der MAX485 and dem STM angeschlossen werden. Das untere Bild ist das Demo Board des STM32F030F4, eines der wenigen Boards, dass man zum Testen des Programmes für den STM Chip kaufen kann.

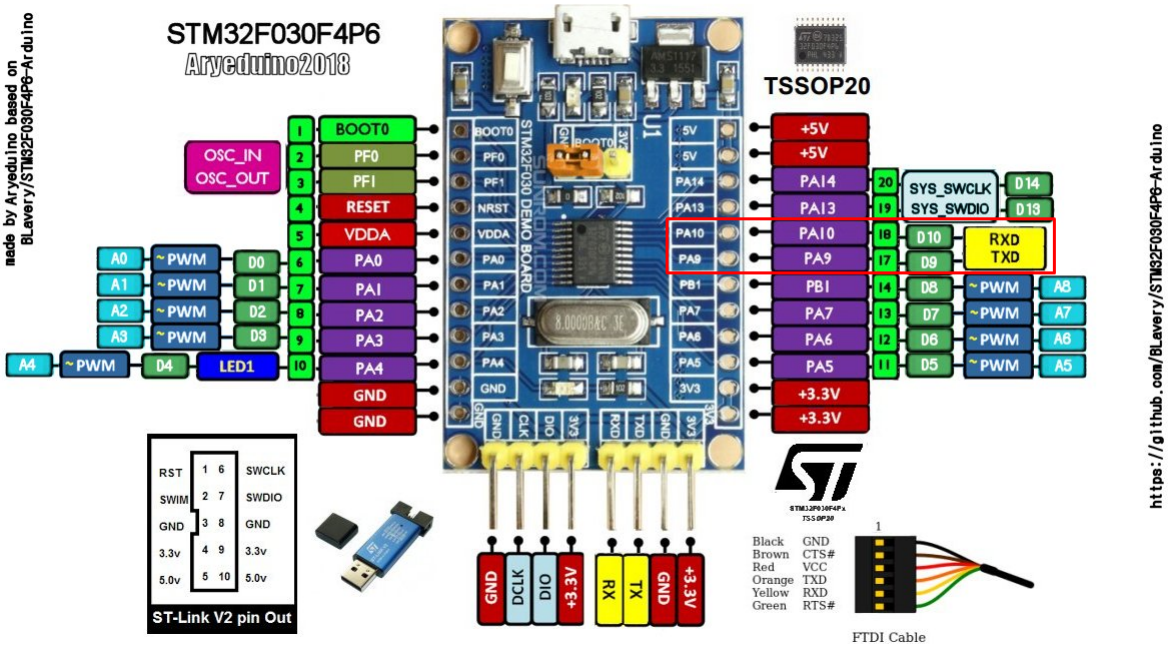

Abbildung 3: STM32F030F4P6-Pinout

3 Einteilung — Was man wissen muss

- Clock aufbau / einstellen
- GPIO Pins register finden / GPIO Pins einstellen
- UART Register suchen / UART aktivieren und einstellen
- Verstehen wie NVIC funktioniert

4 Clock

Die Clock wird am einfachsten, passend aus der gewollten Baudrate für die USART ausgewählt. Damit die Baudrate richtig berechnet wird.
Die HSI Clock von 8MHz ist standard mäßig aktiviert.
Weiterhin werden im APB2 Bus die Clocks für die USART1 und für den ADC und im AHB Bus für die GPIO Ports aktiviert. Die weiteren Clock einstellungen wie z.B. für die USART sind in der jeweilign Initiallisierungs Funktion enthalten.

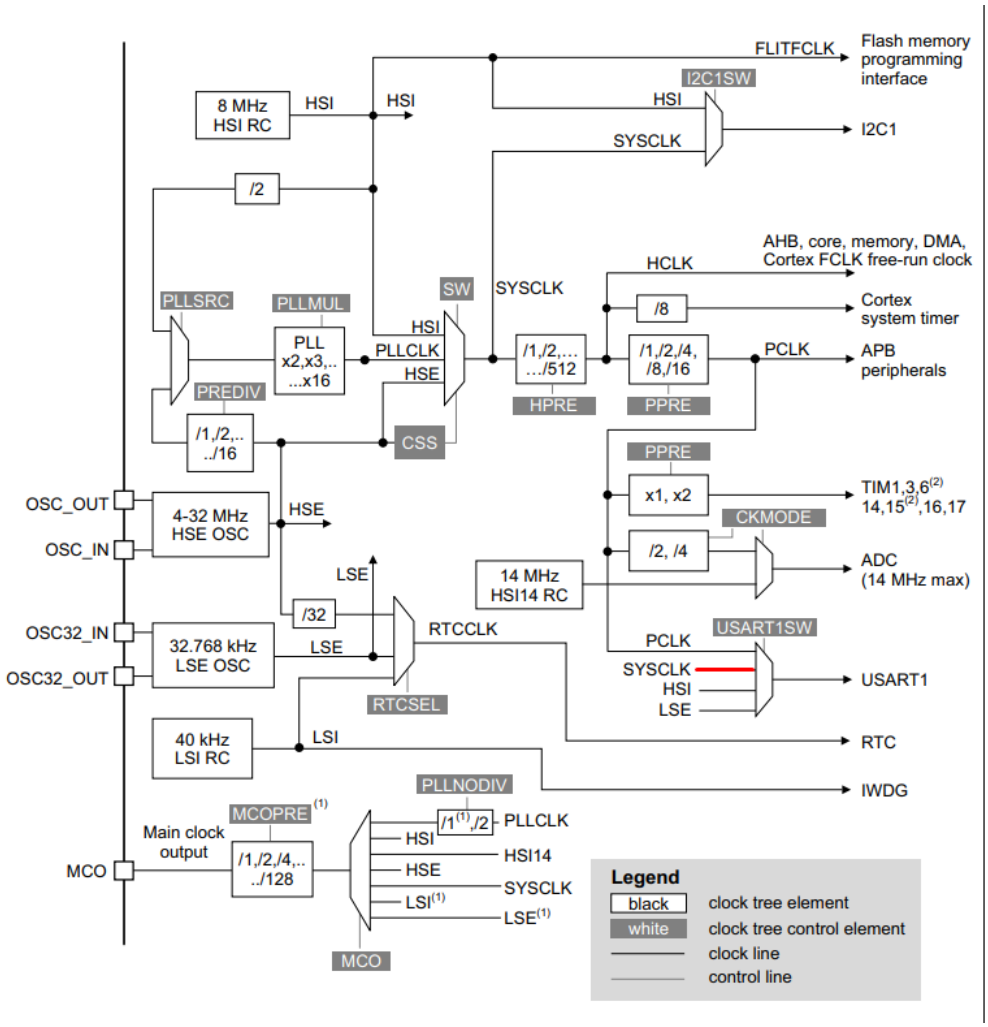

Abbildung 4: Clock-Tree

4.1 Clock-Code

```
int init_CLOCK()
{
    uint32_t reg_content;
    uint32_t* rcc_ahbenr = RCC_AHBENR;
    uint32_t* rcc_apb2enr = RCC_APB2ENR;
    uint32_t* rcc_cfgr = RCC_CFGR;

    //GPIO A port clock enable
    reg_content = *rcc_ahbenr;
    reg_content |= 0x00020000;
    *rcc_ahbenr = reg_content;

    //USART1 clock enable
    reg_content = *rcc_apb2enr;
    reg_content |= 0x00004200;
    *rcc_apb2enr = reg_content;

    //set AHB Clock to not divided so same clock as sysclock
    reg_content = *rcc_cfgr;
    reg_content |= 0x00000000;
    *rcc_cfgr = reg_content;
}
```

Listing 1: init-CLOCK

5 GPIO

5.1 GPIO-Erklärung

Wie man bei der Abbildung 5 sehen kann, sind die GPIOs am BUS AHB2 verbunden. Da das verwendete Paket nur GPIO A verwendet müssen dementsprechend die GPIO-A Register richtig konfiguriert werden
Das Register um die GPIOs als output einzustellen ist **GPIOA_MODER im Addressraum 0x4800 0000 (des AHB2 Buses) mit dem Address offset: 0x00**
Um Pins für die UART verwenden zu können müssen diese Pins noch als ”alternate functions” konfiguriert werden im Register **GPIOA_AFRH mit Address offset: 0x24**. Welche Pin Nummer man Programmieren muss, sieht man in der Abbildung 6, man benötigt PA9 (Pin:17) und PA10 (Pin:18), da diese als alternate function die USART_1 TX und RX hinterlegt haben. Wie das alternate function Register konfiguriert werden muss sieht man in den Abbildungen 7 und 8

Weiterhin müssen noch zwei GPIO Pins Für die DE und RE Pins des MAX485 als output konfiguriert werden. Ich verwend PA7 und PA8.
Ebenfalls wird ein GPIO Pin als analog konfiguriert um diesen als ADC Eingang zu verwenden.

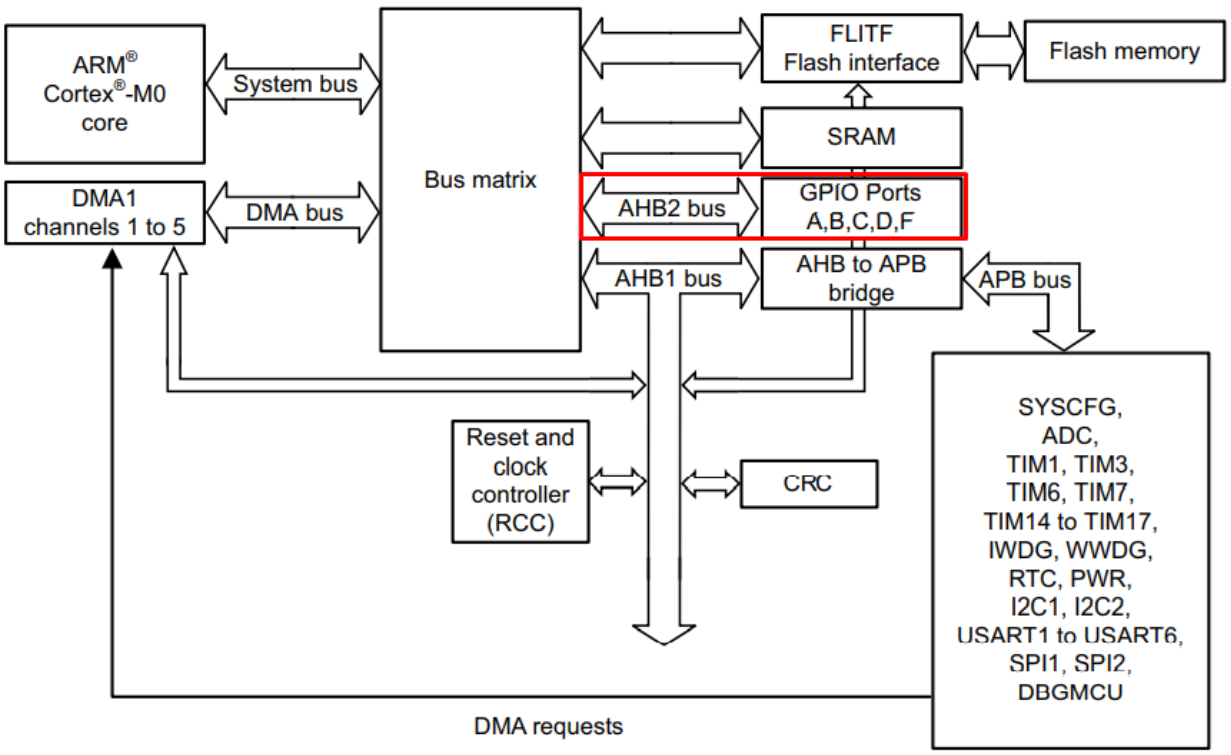

Abbildung 5: System-Architektur

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
34	26	-	-	PB13	I/O	FT	-	SPI1_SCK(2), SPI2_SCK(3)(5), I2C2_SCL(5), TIM1_CH1N, USART3_CTS(5)	-
35	27	-	-	PB14	I/O	FT	-	SPI1_MISO(2), SPI2_MISO(3)(5), I2C2_SDA(5), TIM1_CH2N, TIM15_CH1(3)(5), USART3_RTS(5)	-
36	28	-	-	PB15	I/O	FT	-	SPI1_MOSI(2), SPI2_MOSI(3)(5), TIM1_CH3N, TIM15_CH1N(3)(5), TIM15_CH2(3)(5)	RTC_REFIN, WKUP7(5)
37	-	-	-	PC6	I/O	FT	-	TIM3_CH1	-
38	-	-	-	PC7	I/O	FT	-	TIM3_CH2	-
39	-	-	-	PC8	I/O	FT	-	TIM3_CH3	-
40	-	-	-	PC9	I/O	FT	-	TIM3_CH4	-
41	29	18	-	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	30	19	17	PA9	I/O	FT	-	USART1_TX, TIM1_CH2, TIM15_BKIN(3)(5) I2C1_SCL(2)(5)	-
43	31	20	18	PA10	I/O	FT	-	USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA(2)(5)	-
44	32	21	-	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT, I2C2_SCL(5)	-
45	33	22	-	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT, I2C2_SDA(5)	-

Abbildung 6: GPIO-UART-PIN-Table

Table 12. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART1_CTS(2)	-	-	USART4_TX(1)	-	-
		USART2_CTS(1)(3)					
PA1	EVENTOUT	USART1_RTS(2)	-	-	USART4_RX(1)	TIM15_CH1N(1)	-
		USART2_RTS(1)(3)					
PA2	TIM15_CH1(1)(3)	USART1_TX(2)	-	-	-	-	-
		USART2_TX(1)(3)					
PA3	TIM15_CH2(1)(3)	USART1_RX(2)	-	-	-	-	-
		USART2_RX(1)(3)					
PA4	SPI1_NSS	USART1_CK(2)	-	-	TIM14_CH1	USART6_TX(1)	-
		USART2_CK(1)(3)					
PA5	SPI1_SCK	-	-	-	-	USART6_RX(1)	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	USART3_CTS(1)	TIM16_CH1	EVENTOUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-
PA9	TIM15_BKIN(1)(3)	USART1_TX	TIM1_CH2	-	I2C1_SCL(1)(2)	MCO(1)	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA(1)(2)	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	SCL	-

Abbildung 7: GPIO-AF

8.4.10 GPIO alternate function high register (GPIOx_AFRH) (x = A..D, F)

Address offset: 0x24

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFSEL15[3:0]				AFSEL14[3:0]				AFSEL13[3:0]				AFSEL12[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFSEL11[3:0]				AFSEL10[3:0]				AFSEL9[3:0]				AFSEL8[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:0 **AFSELy[3:0]:** Alternate function selection for port x pin y (y = 8..15)
These bits are written by software to configure alternate function I/Os

AFSELy selection:

0000: AF0	1000: Reserved
0001: AF1	1001: Reserved
0010: AF2	1010: Reserved
0011: AF3	1011: Reserved
0100: AF4	1100: Reserved
0101: AF5	1101: Reserved
0110: AF6	1110: Reserved
0111: AF7	1111: Reserved

Abbildung 8: GPIO-AF-Register

5.2 GPIO-Code

```
int init_GPIO()
{
    //Set GPIO pins PA9 and PA10 alternate function for USART TX and RX,
    //set PA7 and PA6 output for DE and RE of MAX485
    //PA0 ADC_IN0 so set it to analog and then in DAC register set PA0 as
       ADC_IN0
    uint32_t reg_content;
    uint32_t* gpioa_moder = GPIOA_MODER;
    uint32_t* gpioa_afrh = GPIOA_AFRH;
    uint32_t* gpioa_odr = GPIOA_ODR;

    reg_content = *gpioa_moder;
    reg_content |= 0x00285003;
    *gpioa_moder = reg_content;

    //Set GPIO PA9 as AF=TX and PA10 as AF = RX
    reg_content = *gpioa_afrh;
    reg_content |= 0x00000110;
    *gpioa_afrh = reg_content;

    //Ensure that output gpios are 0 for MAX, to read all the time
    //and only send, when needing to send
    reg_content = *gpioa_odr;
    reg_content |= 0x00000000;
    *gpioa_odr = reg_content;
}
```

Listing 2: GPIO-Code

6 USART

USART Addressraum: **0x4001 3800 - 0x4001 3BFF** Für die USART muss, die Clock, die Bautrate, Parity, Wordlenght und die Interrupts eingestellt werden.

6.1 Baudrate-Berechnung-Register-Setzen

Um die Baudrate einstellen zu können muss in das Register **USART_BRR** die richtige Hexadezimal Zahl geschrieben werden.

Berechnung: $\frac{Clock}{Baudrate}$, $\frac{8MHz}{38400} = 208{,}3_{dezimal}$ bzw. $D0_{hex}$
Zurückgerechnet $208 * 38400 = 7.98MHz$. $\frac{8MHz}{208}$ =Baudrate von 38461.

Da der Systemclock gleich der HSI clock ist, kann dafür im Register **RCC_CFGR3 bei der Addresse offset: 0x30** die USART1SW entweder mit 01 für Systemclock oder mit 11 für HSI

clock beschrieben werden. Zusätzlich muss im Register **USART_BRR mit Address offset: 0x0C** D0 geschrieben Werden.

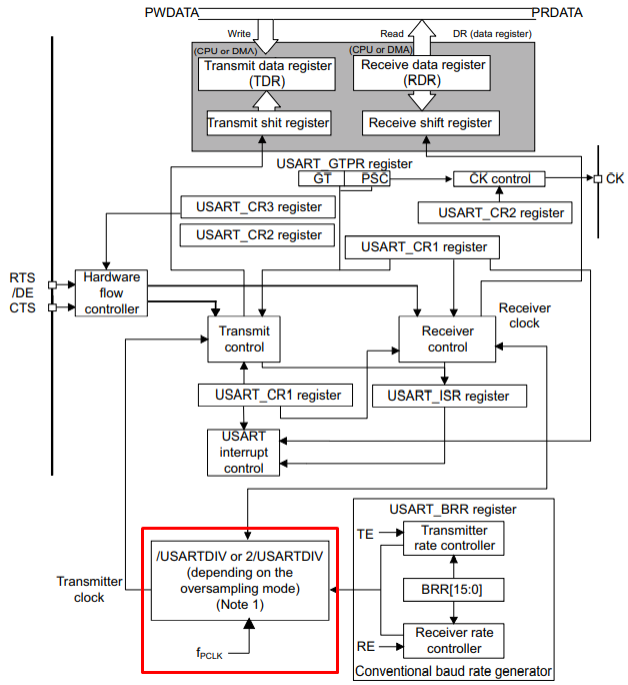

Abbildung 9: USART-Aufbaug

23.7.4 Baud rate register (USART_BRR)

This register can only be written when the USART is disabled (UE=0). It may be automatically updated by hardware in auto baud rate detection mode.

Address offset: 0x0C

Reset value: 0x0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:4 **BRR[15:4]**
BRR[15:4] = USARTDIV[15:4]

Bits 3:0 **BRR[3:0]**
When OVER8 = 0, BRR[3:0] = USARTDIV[3:0].
When OVER8 = 1:
BRR[2:0] = USARTDIV[3:0] shifted 1 bit to the right.
BRR[3] must be kept cleared.

Abbildung 10: USART_BRR

6.2 Weitere USART einstellungen

Die Eistellungen der USART müssen getroffen werden, bevor sie aktiviert wird. Laut angabe wird noch eine ODD Parity verwendet diese kann in dem Register **USART_CR1** auf Bit9: festgelegt werden. Weiterhin müssen dort unter Bit3 und Bit2, TX und RX aktivieren.

6.3 USART-Initiallisierung/Konfiguration—Code

```
int init_UART()
{
    uint32_t reg_content;
    uint32_t* rcc_cfr3 = RCC_CFGR3;
    uint32_t* usart1_brr = USART1_BRR;
    uint32_t* usart1_cr1 = USART1_CR1;

    //Use SYSCLK for USART and use Baudrate 38400
    reg_content = *rcc_cfr3;
    reg_content |= 0x00000001;
    *rcc_cfr3 = reg_content;

    reg_content = *usart1_brr;
    reg_content = 0x00000D00;
    *usart1_brr = reg_content;

    //Wordlenght, Parity control enable, Parity selection, interrupt enable,
        Transmission complete interrupt enable, RXNE interrupt enable
    reg_content = *usart1_cr1;
    reg_content |= 0x000006EC;
    *usart1_cr1 = reg_content;

    reg_content = *usart1_cr1;
    reg_content |= 0x00000001; //enable UART
    *usart1_cr1 = reg_content;
}
```

Listing 3: Init-UART

6.4 USART-InterruptHandler

```
void USART1_IRQHandler(void)
{
    uint32_t* usart1_isr = USART1_ISR;
    uint32_t usart1_isr_rxne = USART1_ISR_RXNE;
    uint32_t usart1_isr_tc = USART1_ISR_TC;
    uint32_t* usart1_tc = USART1_ICR;
    uint32_t* usart1_tc_tcce = USART1_ICR_TCCF;
    uint32_t* usart1_tdr =  USART1_TDR;
    uint32_t* gpioa_odr = GPIOA_ODR;
    uint32_t reg_content;
```

```
    if ((*usart1_isr & usart1_isr_tc) == usart1_isr_tc)
    {
        if (send == sizeof(USART_write_data))
        {
            //set MAX to listen
            reg_content = *gpioa_odr;
            reg_content |= 0x00000000;
            *gpioa_odr = reg_content;
            send=0;
            *usart1_tc |= *usart1_tc_tcce; /* Clear transfer complete flag
               */
        }
        else
        {
            /* clear transfer complete flag and fill TDR with a new char */
            *usart1_tdr = USART_write_data[send++];
        }
    }

    if ((*usart1_isr & usart1_isr_rxne) == usart1_isr_rxne)
    {
        USART_READ = *((char *)USART1_RDR);
    }
}
```

Listing 4: Init-UART

7 ADC

7.1 Erklärung

Der STM hat einen ADC eingebaut, dieser kann bei den größeren Packages sogar als Temperatursensor verwendet werden. Alle GPIOs können als ADC Eingang verwendet werden solange sie als analog GPIO konfiguriert werden.

7.2 Register

Die Register für den ADC beginnen bei 0x4001 2400 bis 0x4001 27FF. Für die Konfiguration werden folgende Register benötigt:

7.2.1 ADC_ISR — ADC Interrupts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	AWD	Res.	Res.	OVR	EOSEQ	EOC	EOSMP	ADRDY
								rc_w1			rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Abbildung 11: ADC-ISR-Register

- EOC (End of conversion):
  0: Channel conversion not complete (or the flag event was already acknowledged and cleared by software)
  1: Channel conversion complete
- ADRDY (ADC ready): 0: ADC not yet ready to start conversion (or the flag event was already acknowledged and cleared by software)
  1: ADC is ready to start conversion

7.2.2 ADC_IER — ADC enable Interrupts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	AWD IE	Res.	Res.	OVRIE	EOSEQ IE	EOCIE	EOSMP IE	ADRDY IE
								rw			rw	rw	rw	rw	rw

Abbildung 12: ADC-IER-Register

Benötigt wird:

- EOCIE(End of conversion interrupt enable):
  0: EOC interrupt disabled
  1: EOC interrupt enabled. An interrupt is generated when the EOC bit is set.
- ADRDYIE (ADC ready interrupt enable): 0: ADRDY interrupt disabled.
  1: ADRDY interrupt enabled. An interrupt is generated when the ADRDY bit is set.

7.2.3 ADC_CR — ADC kalibrieren, aktivieren, starten

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AD CAL	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
rs															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ADSTP	Res.	ADSTART	ADDIS	ADEN
											rs		rs	rs	rs

Abbildung 13: ADC-CR-Register

Benötigt wird:

- ADCAL (ADC calibration):
  0: Calibration complete
  1: Write 1 to calibrate the ADC. Read at 1 means that a calibration is in progress.
- ADEN (ADC enable command)
  0: ADC is disabled (OFF state)
  1: Write 1 to enable the ADC.
- ADSTART (ADC start conversion command)
  0: No ADC conversion is ongoing.
  1: Write 1 to start the ADC. Read 1 means that the ADC is operating and may be converting

7.2.4 ADC_CFGR2 — Clock Einstellung

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CKMODE[1:0]		Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
rw	rw														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.

Abbildung 14: ADC-CFGR2-Register

Benötigt wird:

- CKMODE[1:0] (ADC clock mode):
  00: ADCCLK (Asynchronous clock mode), generated at product level (refer to RCC section)
  01: PCLK/2 (Synchronous clock mode)
  10: PCLK/4 (Synchronous clock mode)
  11: Reserved

7.2.5 ADC_CHSELR — ADC Input Channel

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CHSEL 17	CHSEL 16
														rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL 15	CHSEL 14	CHSEL 13	CHSEL 12	CHSEL 11	CHSEL 10	CHSEL 9	CHSEL 8	CHSEL 7	CHSEL 6	CHSEL 5	CHSEL 4	CHSEL 3	CHSEL 2	CHSEL 1	CHSEL 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Abbildung 15: ADC-CHSELR-Register

Benötigt wird:

- CHSELx: Channel-x selection
  0: Input Channel-x is not selected for conversion
  1: Input Channel-x is selected for conversion

7.2.6 ADC_DR — 16 Bit Ergebniss der Umnwandlung

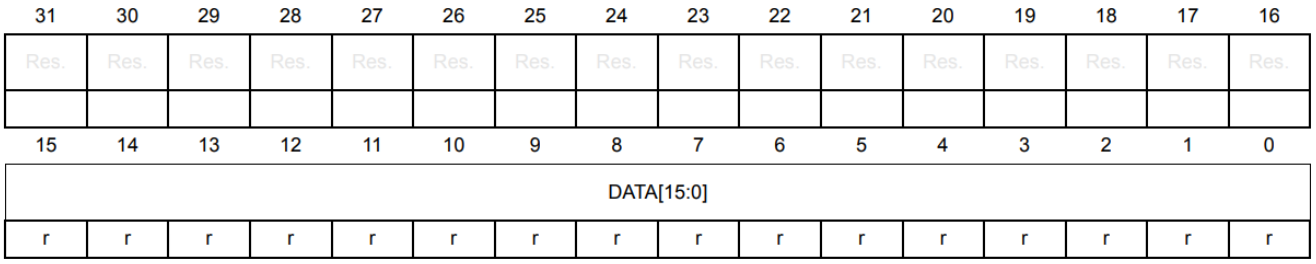

Abbildung 16: ADC-DR-Register

Benötigt wird:

- DATA[15:0]: Converted data

7.3 Konfiguration

Um den ADC zu konfigurieren, wird zuerst der ADC Clock eingestellt → der ADC kalibriert → ADC aktiviert → GPIO als ADC Input einstellen.
Wenn die Kalibrierung fertig ist, ist das ADCAL Bit 0. Dann kann der ADC und Interrupts aktiviert werden und eingestellt werden welcher GPIO Pin als Input verwendet wird. Weiterhin wird der ADC im vortlaufenden (continuous) Modus betrieben, sodass im EOC Interrupt die Umwandlung nicht wieder gestartet werden muss.

Danach wenn der ADC bereit ist wird im Interrupt Register die ADC_ADRDY (ADC Ready) flag gesetzt, dieses wird im ADC-Interrupt-Handler abgefragt und dann eine Umwandlung gestartet.
Wenn eine Umwandlung fertig ist wird im Interrupt Register das ADC_TC (Transmission complete) flag gesetzt. Im ADC-Interrupt-Hanlder wird dann aus dem ADC_DR Register das Ergebniss der Umwandlung weitergeben um dies dann an der USART senden zu können.

7.4 ADC-Initiallisierungs-Code

```
int init_ADC()
{
    uint32_t reg_content;
    uint32_t* adc_chselr = ADC_CHSELR;
    uint32_t* adc_isr = ADC_ISR;
    uint32_t* adc_cr = ADC_CR;
    uint32_t* adc_cfgr1 = ADC_CFGR1;
    uint32_t adc_cr_adcal = ADC_CR_ADCAL;
    uint32_t* adc_ier = ADC_IER;
    uint32_t* adc_cfgr2 = ADC_CFGR2;
    uint32_t adc_isr_adrdy = ADC_ISR_ADRDY;

    //set ADC clock to PCLK so thats is synchronous with sysclock
    reg_content = *adc_cfgr2;
    reg_content |= 0x40000000;
    *adc_cfgr2 = reg_content;
    //before starting callibrate ADC
    reg_content = *adc_cr;
    reg_content |= adc_cr_adcal;
    *adc_cr = reg_content;

    //if calibration is complete enable ADC
    //enable Interrupts
    //set correct channel
    //when ADC is ready, a ad ready interrupt occurs and the interrupt
       handler
    //will then start the ADC convertion
    while((*adc_cr & adc_cr_adcal) == adc_cr_adcal); // wait till
       callibration is complete

    //enable ADC and ensure ADSTART=0 for further configuration and enable
       ADC
    reg_content = *adc_cr;
    reg_content |= 0x00000001;
    *adc_cr = reg_content;
    //set ADC to continues convertion so, that convertion doesn't to start
       again in Interrupt
    reg_content = *adc_cr;
    reg_content |= 0x0000200;
    *adc_cr = reg_content;
    //enable Interrupts of ADC
    reg_content = *adc_ier;
    reg_content |= 0x00000005;
    *adc_ier = reg_content;
    //Set ADC Channel to channel 0 because PA0 is ADC_IN0
    reg_content = *adc_chselr;
    reg_content |= 0x00000001;
    *adc_chselr = reg_content;
}
```

Listing 5: ADC-Initiallisierungs-Code

7.5 ADC-Interrupt-Handler-Code

```
void ADC1_IRQHandler(void)
{
    uint32_t* adc_isr = ADC_ISR;
    uint32_t* adc_cr = ADC_CR;

    uint32_t adc_isr_eoc = ADC_ISR_EOC;
    uint32_t adc_isr_adrdy = ADC_ISR_ADRDY;
    uint32_t* adc_dr = ADC_DR;
    uint32_t adc_dr_data = ADC_DR_DATA;
    uint32_t* gpioa_odr = GPIOA_ODR;
    uint32_t* usart1_tdr =  USART1_TDR;

    uint32_t adc_cr_adstart = ADC_CR_ADSTART;
    uint16_t ADC_Value;

    uint32_t reg_content;

    //if ADC Ready start convertion
    if((*adc_isr & adc_isr_adrdy) == adc_isr_adrdy)
    {
        reg_content = *adc_cr;
        reg_content |= adc_cr_adstart;
        *adc_cr = reg_content;
    }

    //if convertion complete send ADC value
    if((*adc_isr & adc_isr_eoc) == adc_isr_eoc)
    {
        send=0;
        ADC_Value = (*adc_dr & adc_dr_data);
        //Set PA7 and PA6 high for max to send data
        reg_content = *gpioa_odr;
        reg_content |= 0x000000C0;
        *gpioa_odr = reg_content;

        sprintf(USART_write_data, "%d", ADC_Value);

        //write something into the USART Buffer for USART
        //interrupt where rest of adc value gets put into the buffer
        *usart1_tdr = 'n';
    }
}
```

Listing 6: ADC-Interrupt-Handler-Code

8 NVIC

8.1 Wir wird er verwendet

Beim Programmieren des STM muss der Vector Table beschrieben werden mit einem Assembler File und Linker Skript, diese werden von der Cube IDE erstellt.
Im Vector Table sind alle Interrupts mit dem entsprechenden Funktionnamen für das Programm hinterlegt. Im NVIC_ISER Register können die Interrupts durch ihre Interrupt Position aktiviert werden.

Die IRQ_Handler Positionen werden beim programmieren des uC in den Flash geschrieben.

Table 32. Vector table (continued)

Position	Priority	Type of priority	Acronym	Description	Address
3	10	settable	FLASH	Flash global interrupt	0x0000 004C
4	11	settable	RCC	RCC global interrupts	0x0000 0050
5	12	settable	EXTI0_1	EXTI Line[1:0] interrupts	0x0000 0054
6	13	settable	EXTI2_3	EXTI Line[3:2] interrupts	0x0000 0058
7	14	settable	EXTI4_15	EXTI Line[15:4] interrupts	0x0000 005C
8			Reserved		0x0000 0060
9	16	settable	DMA_CH1	DMA channel 1 interrupt	0x0000 0064
10	17	settable	DMA_CH2_3	DMA channel 2 and 3 interrupts	0x0000 0068
11	18	settable	DMA_CH4_5	DMA channel 4 and 5 interrupts	0x0000 006C
12	19	settable	ADC	ADC interrupts	0x0000 0070
13	20	settable	TIM1_BRK_UP_ TRG_COM	TIM1 break, update, trigger and commutation interrupt	0x0000 0074
14	21	settable	TIM1_CC	TIM1 capture compare interrupt	0x0000 0078
15			Reserved		0x0000 007C
16	23	settable	TIM3	TIM3 global interrupt	0x0000 0080
17	24	settable	TIM6	TIM6 global interrupt	0x0000 0084
18			Reserved		0x0000 0084
19			Reserved		0x0000 0088
19	26	settable	TIM14	TIM14 global interrupt	0x0000 008C
20	27	settable	TIM15	TIM15 global interrupt	0x0000 0090
21	28	settable	TIM16	TIM16 global interrupt	0x0000 0094
22	29	settable	TIM17	TIM17 global interrupt	0x0000 0098
23	30	settable	I2C1	I^2C1 global interrupt	0x0000 009C
24	31	settable	I2C2	I^2C2 global interrupt	0x0000 00A0
25	32	settable	SPI1	SPI1 global interrupt	0x0000 00A4
26	33	settable	SPI2	SPI2 global interrupt	0x0000 00A8
27	34	settable	USART1	USART1 global interrupt	0x0000 00AC
28	35	settable	USART2	USART2 global interrupt	0x0000 00B0
29	36	settable	USART3_4_5_6	USART3, USART4, USART5, USART6 global interrupts	0x0000 00B4
30			Reserved		0x0000 00B8
31	38	settable	USB	USB global interrupt (combined with EXTI line 18)	0x0000 00BC

Abbildung 17: NVIC-Vector-Table

```
124   g_pfnVectors:
125     .word  _estack
126     .word  Reset_Handler
127     .word  NMI_Handler
128     .word  HardFault_Handler
129     .word  0
130     .word  0
131     .word  0
132     .word  0
133     .word  0
134     .word  0
135     .word  0
136     .word  SVC_Handler
137     .word  0
138     .word  0
139     .word  PendSV_Handler
140     .word  SysTick_Handler
141     .word  WWDG_IRQHandler                   /* Window WatchDog              */
142     .word  0                                 /* Reserved                     */
143     .word  RTC_IRQHandler                    /* RTC through the EXTI line    */
144     .word  FLASH_IRQHandler                  /* FLASH                        */
145     .word  RCC_IRQHandler                    /* RCC                          */
146     .word  EXTI0_1_IRQHandler                /* EXTI Line 0 and 1            */
147     .word  EXTI2_3_IRQHandler                /* EXTI Line 2 and 3            */
148     .word  EXTI4_15_IRQHandler               /* EXTI Line 4 to 15            */
149     .word  0                                 /* Reserved                     */
150     .word  DMA1_Channel1_IRQHandler          /* DMA1 Channel 1               */
151     .word  DMA1_Channel2_3_IRQHandler        /* DMA1 Channel 2 and Channel 3 */
152     .word  DMA1_Channel4_5_IRQHandler        /* DMA1 Channel 4 and Channel 5 */
153     .word  ADC1_IRQHandler                   /* ADC1                         */
154     .word  TIM1_BRK_UP_TRG_COM_IRQHandler    /* TIM1 Break, Update, Trigger and Commutation */
155     .word  TIM1_CC_IRQHandler                /* TIM1 Capture Compare         */
156     .word  0                                 /* Reserved                     */
157     .word  TIM3_IRQHandler                   /* TIM3                         */
158     .word  0                                 /* Reserved                     */
159     .word  0                                 /* Reserved                     */
160     .word  TIM14_IRQHandler                  /* TIM14                        */
161     .word  0                                 /* Reserved                     */
162     .word  TIM16_IRQHandler                  /* TIM16                        */
163     .word  TIM17_IRQHandler                  /* TIM17                        */
164     .word  I2C1_IRQHandler                   /* I2C1                         */
165     .word  0                                 /* Reserved                     */
166     .word  SPI1_IRQHandler                   /* SPI1                         */
167     .word  0                                 /* Reserved                     */
168     .word  USART1_IRQHandler                 /* USART1                       */
169     .word  0                                 /* Reserved                     */
170     .word  0                                 /* Reserved                     */
171     .word  0                                 /* Reserved                     */
172     .word  0                                 /* Reserved                     */
```

Abbildung 18: Ausschnit-Assembler-File

4.2.2 Interrupt set-enable register (ISER)

Address offset: 0x00

Reset value: 0x0000 0000

The ISER register enables interrupts, and shows which interrupts are enabled

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETENA[31:16]															
rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETENA[15:0]															
rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs

Bits 31:0 **SETENA**: Interrupt set-enable bits.

Write:

0: No effect

1: Enable interrupt

Read:

0: Interrupt disabled

1: Interrupt enabled.

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

Abbildung 19: NVIC-ISER-Register

8.2 NVIC-Code

```
void NVIC_enable_interrupts(void)
{
    uint32_t* nvic_iser =  NVIC_ISER;
    uint32_t reg_content;
    reg_content = *nvic_iser;
    reg_content |= 0x08001000;
    *nvic_iser = reg_content;
}
```

Listing 7: NVIC-enable-interrupts

9 Gesamtes-Programm

9.1 Headerfile

```
#ifndef __header_H
#define __header_H

//boundary addresses at page 37 - 41
/*
General boundaries
*/
#define PERIPHALS       ((uint32_t*)0x40000000)     //Peripherals
#define APBPERIPHALS    PERIPHALS                   //APBPeriphals
#define AHBPERIPHALS    (PERIPHALS + 0x00020000)
#define AHB2PERIPHALS   (PERIPHALS + 0x08000000)

/*
USART1
*/
#define USART1_BASE (APBPERIPHALS+0x00013800) //USART 1 Base Address
//Base + Address offset + Comment + Page in reference Manual
#define USART1_CR1      (USART1_BASE+0x00)   //USART Control Register 1  --
   at Page 625
#define USART1_CR2      (USART1_BASE+0x04)   //USART Control Register 2  --
   at Page 628
#define USART1_CR3      (USART1_BASE+0x08)   //USART Control Register 3  --
   at Page 630
#define USART1_BRR      (USART1_BASE+0x0C)   //USART Baudrate Register   --
   at page 632
#define USART1_RQR      (USART1_BASE+0x18)   //USART Request register

#define USART1_ISR      (USART1_BASE+0x1c)   //USART Interrupt and status
   register   -- at Page 635
#define USART1_ISR_TXE  ((uint32_t)0x00000080)
#define USART1_ISR_TC   ((uint32_t)0x00000040)
#define USART1_ISR_RXNE ((uint32_t)0x00000020)

#define USART1_ICR       (USART1_BASE+0x20)   //USART Interrupt and flag
   Clear register -- at Page 638
#define USART1_ICR_TCCF  ((uint32_t) 0x00000040) //USART transmission
   complete clear flag -- at Page 639
#define USART1_RDR       (USART1_BASE+0x24)   //USART Receive Data register
     --  at Page 639
#define USART1_TDR       (USART1_BASE+0x28)   //USART Transmit Data register
     --  at Page 640

/*
RCC
*/
//From boundary addresses at page 39
#define RCC (AHBPERIPHALS+0x00001000)
//All found from RCC Register Map on Page 125
```

```
#define RCC_CR          (RCC+0x00)          //RCC Control register -- at
    Page 99
#define RCC_CFGR        (RCC+0x04)          //RCC Clock configuration
    register -- at Page 101
#define RCC_CIR         (RCC+0x08)          //RCC Clock interrupt register
    -- at Page 104
#define RCC_APB2RSTR    (RCC+0x0C)          //RCC APB peripheral reset
    register 2 -- at Page 106
#define RCC_APB1RSTR    (RCC+0x010)         //RCC APB peripheral reset
    register 1 -- at Page 108
#define RCC_AHBENR      (RCC+0x14)          //RCC AHB peripheral clock
    enable register -- at Page 111
#define RCC_APB2ENR     (RCC+0x18)          //RCC APB peripheral clock
    enable register 2-- at Page 112
#define RCC_APB1ENR     (RCC+0x1C)          //RCC APB peripheral clock
    enable register 1-- at Page 114
#define RCC_BDCR        (RCC+0x20)          //RCC RTC domain control
    register -- at Page 117
#define RCC_CSR         (RCC+0x24)          //RCC Control/status register --
     at Page 119
#define RCC_AHBRSTR     (RCC+0x28)          //RCC AHB peripheral reset
    register -- at Page 120
#define RCC_CFGR2       (RCC+0x2C)          //RCC Clock configuration
    register 2 -- at Page 122
#define RCC_CFGR3       (RCC+0x30)          //RCC Clock configuration
    register 3 -- at Page 123
#define RCC_CR2         (RCC+0x34)          //RCC Clock control register 2
    -- at Page 123


/*
GPIOA
*/
#define GPIO_A (AHB2PERIPHALS + 0x00000000)
//Page 142
#define GPIOA_MODER     (GPIO_A+0x00)       //GPIO port moder register -- at
     Page 136
#define GPIOA_OTYPER    (GPIO_A+0x04)       //GPIO port output type register
     -- at Page 136
#define GPIOA_OSPEEDR   (GPIO_A+0x08)       //GPIO port output speed
    register -- at Page 137
#define GPIOA_PUPDR     (GPIO_A+0x0C)       //GPIO port pull-up/pull-down
    register -- at Page 137
#define GPIOA_IDR       (GPIO_A+0x10)       //GPIO port input data register
    -- at Page 138
#define GPIOA_ODR       (GPIO_A+0x14)       //GPIO port output data register
     -- at Page 138
#define GPIOA_BSRR      (GPIO_A+0x18)       //GPIO port bis set/reset
    register -- at Page 138
#define GPIOA_LCKR      (GPIO_A+0x1c)       //GPIO port configuration lock
    register -- at Page 139
#define GPIOA_AFRL      (GPIO_A+0x20)       //GPIO alternate function low
    register -- at Page 140
```

```
#define GPIOA_AFRH      (GPIO_A+0x024)      //GPIO alternate function high
    register -- at Page 141
#define GPIOA_BRR       (GPIO_A+0x28)       //GPIO port bit reset register
    -- at Page 141


/*
ADC
*/
//boundary address at page 40
#define ADC (APBPERIPHALS+0x00012400)
//Page 220
#define ADC_ISR         (ADC+0x00)                  //ADC interrupt and
    status register -- at Page 207
#define ADC_ISR_AWD     ((uint32_t)0x00000080)       //Analog watchdog flag
#define ADC_ISR_OVR     ((uint32_t)0x00000010)       //Overrun flag
#define ADC_ISR_EOSEQ   ((uint32_t)0x00000008)       //End of Sequence flag
#define ADC_ISR_EOC     ((uint32_t)0x00000004)       //End of Conversion
#define ADC_ISR_EOSMP   ((uint32_t)0x00000002)       //End of sampling flag
#define ADC_ISR_ADRDY   ((uint32_t)0x00000001)       //ADC Ready

#define ADC_IER         (ADC+0x04)      //ADC interrupt enable register --
    at Page 208

#define ADC_CR          (ADC+0x08)      //ADC control register -- at Page
    210
#define ADC_CR_ADCAL    ((uint32_t)0x80000000)  //ADC Calibration
#define ADC_CR_ADSTP    ((uint32_t)0x00000010)  //ADC stop of conversion
    command
#define ADC_CR_ADSTART  ((uint32_t)0x00000004)  //ADC start of conversion
#define ADC_CR_ADDIS    ((uint32_t)0x00000002)  //ADC disable command
#define ADC_CR_ADEN     ((uint32_t)0x00000001) //ADC enable control


#define ADC_CFGR1       (ADC+0x0C)      //ADC configuration register 1 -- at
     Page 212
#define ADC_CFGR2       (ADC+0x10)      //ADC configuration register 2 -- at
     Page 216
#define ADC_SMPR        (ADC+0x14)      //ADC sampling time register -- at
    Page 216
#define ADC_TR          (ADC+0x20)      //ADC watchdog threshold register --
     at Page 217
#define ADC_CHSELR      (ADC+0x28)      //ADC channel selection register --
    at Page 218

#define ADC_DR          (ADC+0x40)      //ADC data register -- at Page 218
#define ADC_DR_DATA     ((uint32_t)0x0000FFFF)       //ADC Data Mask
#define ADC_CCR         (ADC+0x308)     //ADC common configuration register
    -- at Page 219
```

```
//Interrupt ant Page 171
#define ADC_IRQn    12          //Address 0x0000 0070
#define USART1_IRQn 27      //Address 0x0000 00AC
//in ARMv6 and stm32f0xx-cortexm0-programming-manual-- at Page 70
#define NVIC_ISER   ((uint32_t*)0xE000E100)   //Interrupt Set-Enable
   Register page B3-284
#define NVIC_ICER   ((uint32_t*)0xE000E180)   //Interrupt Clear Enable
   Register page B3-285
#define NVIC_ISPR   ((uint32_t*)0xE000E200)   //Interrupt Set-Pending
   Register page B3-286
#define NVIC_ICPR   ((uint32_t*)0xE000E280)   //Interrupt Clear-Pending
   Register page B3-287
#define NVIC_IPRN   ((uint32_t*)0xE000E400)   //-0xE000E43C Interrupt
   Priority Registers NVIC_IPR0-NVICIPR7 B3-288


#endif
```

Listing 8: Headerfile

9.2 Main

```
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <sys/time.h>
#include <unistd.h>
#include <fcntl.h>
#include <stdint.h>

#include "header.h"

char USART_READ;
uint32_t ADC_Value;

//Prototypes
char USART_write_data[32];
int send=0;
//ADC Interrupt Handler
void ADC1_IRQHandler(void)
{
    uint32_t* adc_isr = ADC_ISR;
    uint32_t* adc_cr = ADC_CR;

    uint32_t adc_isr_eoc = ADC_ISR_EOC;
    uint32_t adc_isr_adrdy = ADC_ISR_ADRDY;
    uint32_t* adc_dr = ADC_DR;
    uint32_t adc_dr_data = ADC_DR_DATA;
    uint32_t* gpioa_odr = GPIOA_ODR;
    uint32_t* usart1_tdr =  USART1_TDR;

    uint32_t adc_cr_adstart = ADC_CR_ADSTART;
    uint16_t ADC_Value;

    uint32_t reg_content;

    //if ADC Ready start convertion
    if((*adc_isr & adc_isr_adrdy) == adc_isr_adrdy)
    {
        reg_content = *adc_cr;
        reg_content |= adc_cr_adstart;
        *adc_cr = reg_content;
    }

    //if convertion complete send ADC value
    if((*adc_isr & adc_isr_eoc) == adc_isr_eoc)
    {
        send=0;
        ADC_Value = (*adc_dr & adc_dr_data);
        //Set PA7 and PA6 high for max to send data
        reg_content = *gpioa_odr;
        reg_content |= 0x000000C0;
        *gpioa_odr = reg_content;
```

```
        sprintf(USART_write_data, "%d", ADC_Value);

        //write something into the USART Buffer for USART
        //interrupt where rest of adc value gets put into the buffer
        *usart1_tdr = 'n';
    }
}

//Enable Interrupts in NVIC
void NVIC_enable_interrupts(void)
{
    uint32_t* nvic_iser =  NVIC_ISER;
    uint32_t reg_content;
    reg_content = *nvic_iser;
    reg_content |= 0x08001000;
    *nvic_iser = reg_content;
}


//USART Interrupt Handler
void USART1_IRQHandler(void)
{
    uint32_t* usart1_isr = USART1_ISR;
    uint32_t usart1_isr_rxne = USART1_ISR_RXNE;
    uint32_t usart1_isr_tc = USART1_ISR_TC;
    uint32_t* usart1_tc = USART1_ICR;
    uint32_t* usart1_tc_tcce = USART1_ICR_TCCF;
    uint32_t* usart1_tdr =  USART1_TDR;
    uint32_t* gpioa_odr = GPIOA_ODR;
    uint32_t reg_content;

    if ((*usart1_isr & usart1_isr_tc) == usart1_isr_tc)
    {
        if (send == sizeof(USART_write_data))
        {
            //set MAX to listen
            reg_content = *gpioa_odr;
            reg_content |= 0x00000000;
            *gpioa_odr = reg_content;
            send=0;
            *usart1_tc |= *usart1_tc_tcce; /* Clear transfer complete flag
                */
        }
        else
        {
            /* clear transfer complete flag and fill TDR with a new char */
            *usart1_tdr = USART_write_data[send++];
        }
    }

    if ((*usart1_isr & usart1_isr_rxne) == usart1_isr_rxne)
    {
```

```
        USART_READ = *((char *)USART1_RDR);
    }
}

//Initialize ADC
int init_ADC()
{
    uint32_t reg_content;
    uint32_t* adc_chselr = ADC_CHSELR;
    uint32_t* adc_isr = ADC_ISR;
    uint32_t* adc_cr = ADC_CR;
    uint32_t* adc_cfgr1 = ADC_CFGR1;
    uint32_t adc_cr_adcal = ADC_CR_ADCAL;
    uint32_t* adc_ier = ADC_IER;
    uint32_t* adc_cfgr2 = ADC_CFGR2;
    uint32_t adc_isr_adrdy = ADC_ISR_ADRDY;

    //set ADC clock to PCLK so thats is synchronous with sysclock
    reg_content = *adc_cfgr2;
    reg_content |= 0x40000000;
    *adc_cfgr2 = reg_content;

    //before starting callibrate ADC
    reg_content = *adc_cr;
    reg_content |= adc_cr_adcal;
    *adc_cr = reg_content;

    //if calibration is complete enable ADC
    //enable Interrupts
    //set correct channel
    //when ADC is ready, a ad ready interrupt occurs and the interrupt
       handler
    //will then start the ADC convertion
    while((*adc_cr & adc_cr_adcal) == adc_cr_adcal); // wait till
       callibration is complete


    //enable ADC and ensure ADSTART=0 for further configuration and enable
       ADC
    reg_content = *adc_cr;
    reg_content |= 0x00000001;
    *adc_cr = reg_content;

    //set ADC to continues convertion so, that convertion doesn't to start
       again in Interrupt
    reg_content = *adc_cr;
    reg_content |= 0x0000200;
    *adc_cr = reg_content;

    //enable Interrupts of ADC
    reg_content = *adc_ier;
    reg_content |= 0x00000005;
    *adc_ier = reg_content;
```

```
    //Set ADC Channel to channel 0 because PA0 is ADC_IN0
    reg_content = *adc_chselr;
    reg_content |= 0x00000001;
    *adc_chselr = reg_content;
}

//Initialize needed clocks
int init_CLOCK()
{
    uint32_t reg_content;
    uint32_t* rcc_ahbenr = RCC_AHBENR;
    uint32_t* rcc_apb2enr = RCC_APB2ENR;
    uint32_t* rcc_cfgr = RCC_CFGR;

    //GPIO A port clock enable
    reg_content = *rcc_ahbenr;
    reg_content |= 0x00020000;
    *rcc_ahbenr = reg_content;

    //USART1 clock enable
    reg_content = *rcc_apb2enr;
    reg_content |= 0x00004000;
    *rcc_apb2enr = reg_content;

    //set AHB Clock to not divided so same clock as sysclock
    reg_content = *rcc_cfgr;
    reg_content |= 0x00000000;
    *rcc_cfgr = reg_content;
}

//Initialize GPIOs
int init_GPIO()
{
    //Set GPIO pins PA9 and PA10 alternate function for USART TX and RX,
    //set PA7 and PA6 output for DE and RE of MAX485
    //PA0 ADC_IN0 so set it to analog and then in DAC register set PA0 as
       ADC_IN0
    uint32_t reg_content;
    uint32_t* gpioa_moder = GPIOA_MODER;
    uint32_t* gpioa_afrh = GPIOA_AFRH;
    uint32_t* gpioa_odr = GPIOA_ODR;

    //set above mentioned Pins
    reg_content = *gpioa_moder;
    reg_content |= 0x00285003;
    *gpioa_moder = reg_content;

    //Set GPIO PA9 as AF=TX and PA10 as AF = RX
    reg_content = *gpioa_afrh;
    reg_content |= 0x00000110;
    *gpioa_afrh = reg_content;
```

```
    //Set GPIO PA9 as AF=TX and PA10 as AF = RX
    reg_content = *gpioa_afrh;
    reg_content |= 0x00000110;
    *gpioa_afrh = reg_content;


    //Ensure that output gpios are 0 for MAX, to read all the time
    //and only send, when needing to send
    reg_content = *gpioa_odr;
    reg_content |= 0x00000000;
    *gpioa_odr = reg_content;
}

//Initialize USART
int init_UART()
{
    uint32_t reg_content;
    uint32_t* rcc_cfr3 = RCC_CFGR3;
    uint32_t* usart1_brr = USART1_BRR;
    uint32_t* usart1_cr1 = USART1_CR1;

    //Use SYSCLK for USART and use Baudrate 38400
    reg_content = *rcc_cfr3;
    reg_content |= 0x00000001;
    *rcc_cfr3 = reg_content;

    reg_content = *usart1_brr;
    reg_content = 0x00000D00;
    *usart1_brr = reg_content;

    //Wordlenght, Parity control enable, Parity selection, interrupt enable,
        Transmission complete interrupt enable, RXNE interrupt enable
    reg_content = *usart1_cr1;
    reg_content |= 0x000006EC;
    *usart1_cr1 = reg_content;

    reg_content = *usart1_cr1;
    reg_content |= 0x00000001; //enable UART
    *usart1_cr1 = reg_content;
}

int main()
{
    init_CLOCK();
    init_GPIO();
    init_UART();
    init_ADC();
    NVIC_enable_interrupts();

    for(;;);
}
```

Listing 9: Gesamter-Code

10 Anhang

10.1 Verlinkungen

Abbildung: 0
`http://www.mathe-mit-methode.com/schlaufuchs_web/elektrotechnik/mikrocontroller_lernmaterial/microcontroller_allgemein/mikrocontroller_ext_hardware/mikrocontroller_uart_bild_001.html`

Abbildung: 1
`https://de.wikipedia.org/wiki/EIA-485`

Abbildung: 3
https://user-images.githubusercontent.com/20950920/48240567-e985c080-e3db-11e8-8775-68a216485b59.jpg von aryeguetta