ANDANTE

AI for **N**ew **D**evices **An**d **T**echnologies at the **E**dge

ANDANTE

CPS&IoT'2023 Summer School on
Cyber-Physical Systems and Internet-of-Things

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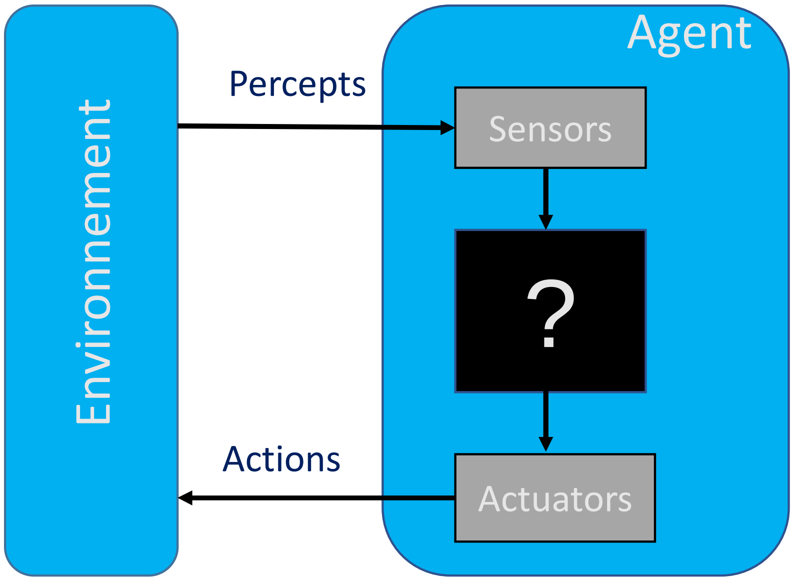
Outline

Data Analytics : Cloud or/and Edge

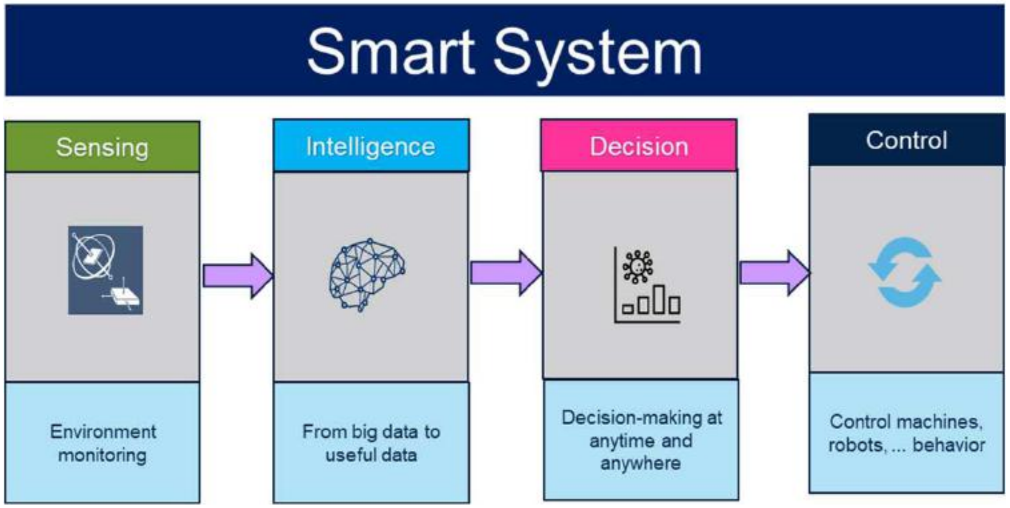
Agent, IOT & CPS

- **Agents** interacts with **environments** through **sensors** and **actuators**
- **IoT** (Internet of Things) enables to **monitor devices to take decisions and optimize actuators** and generate results
- **CPS** (Cyber-Physical Systems) consists of **computation and control components** tightly **combined with physical**



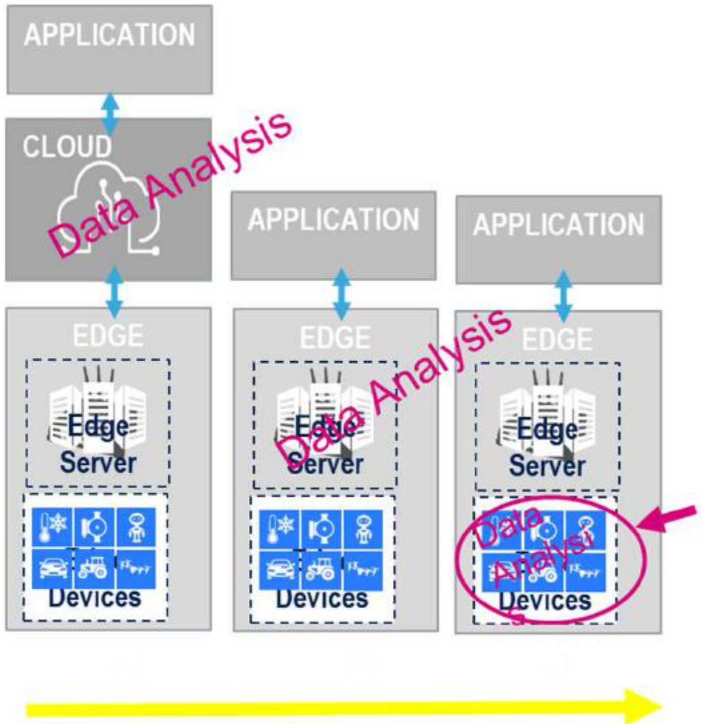
AI and IOT & CPS

- IoT and CPS are evolutions of existing monitoring / control systems.
- IoT and CPS are a revolution for the applications in multiples areas
- IoT and CPS bring higher system flexibility, accuracy, precision, distributed computing power, real-time, … at cost effective



Data Analytics from Cloud to Edge

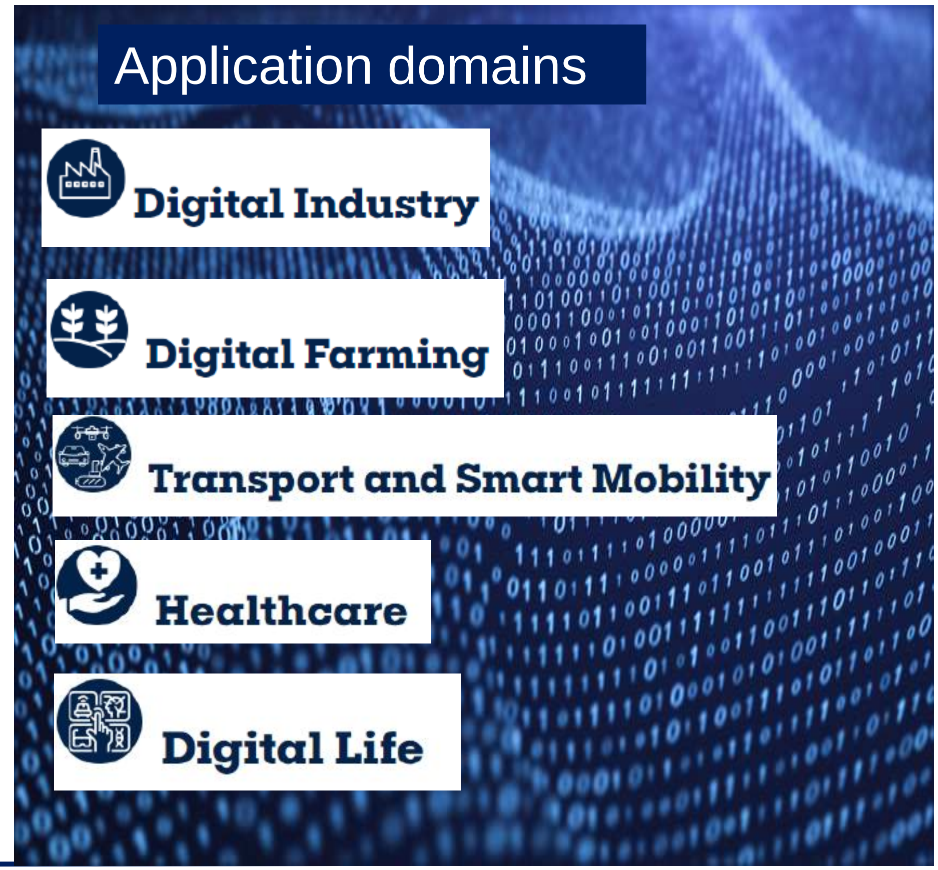
- Nowadays, **AI** is strongly penetrating large market segments.
- **Data analysis** is moving from the **Cloud** to the **Edge** creating new opportunities for the European industry
- At the **Edge**, innovative, efficient, and cost-effective **IC solutions** are required



What is the ANDANTE Motivation ?

Provide Efficient AI Solutions

- Digitalization is bringing many advantages in many application domains
- An important **drawback** is the **electricity consumed** with the use of **cloud computing solutions**
- Bloomberg estimated that about **1% of the world's electricity** goes to cloud computing and for 2030 will increase **conservatory to 8%** to power the future cloud
- New solutions should be found at **all levels** to remediate this unsustainability



IoT & CPS System Requirements

Technologies

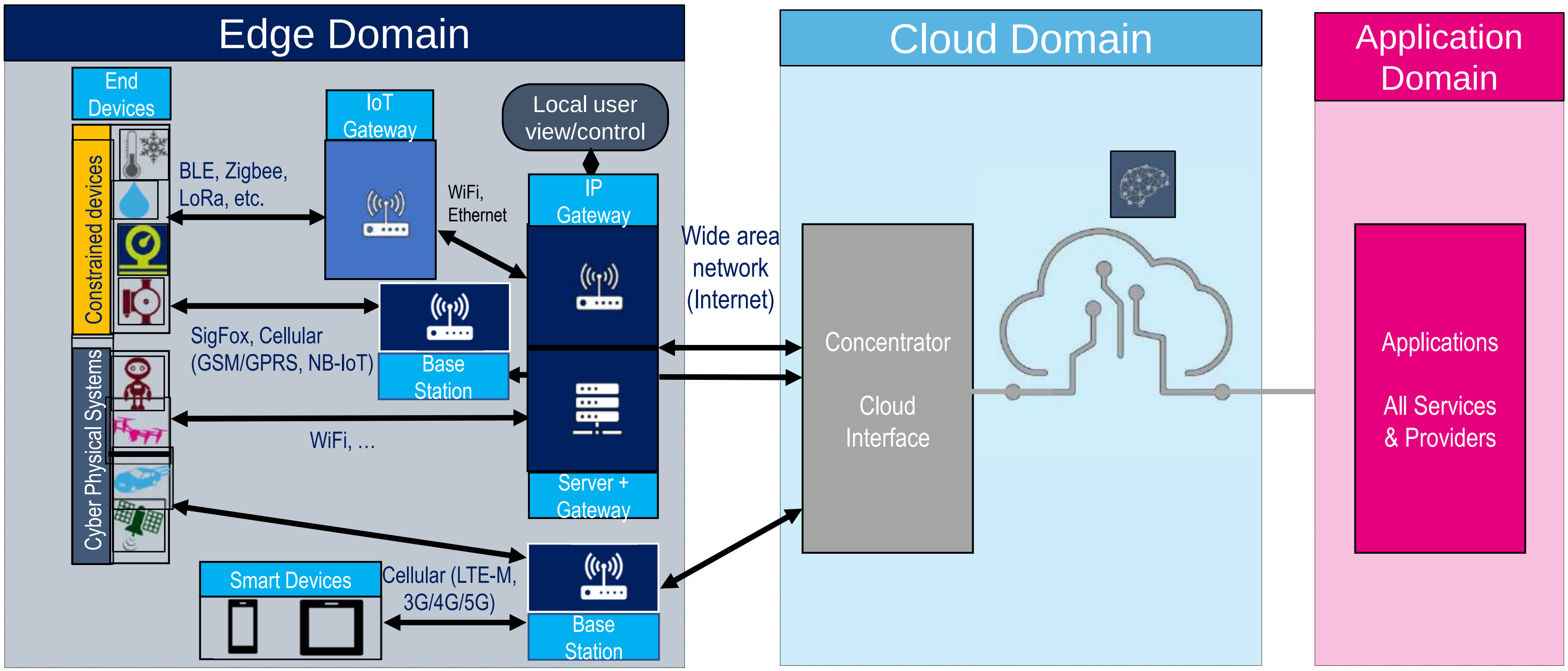
- Multi-sensors and actuators, robots, UVA, satellites
- Efficient Edge / Cloud computing capabilities
- Data analysis: AI, Machine Learning, Deep Learning
- Security and privacy
- Adapted connectivity
- Low-power consumption
- Reliable technology
- Computer vision
- Tools for Modeling, data analysis, SW development, prediction, verification, system debug and validation

Applications

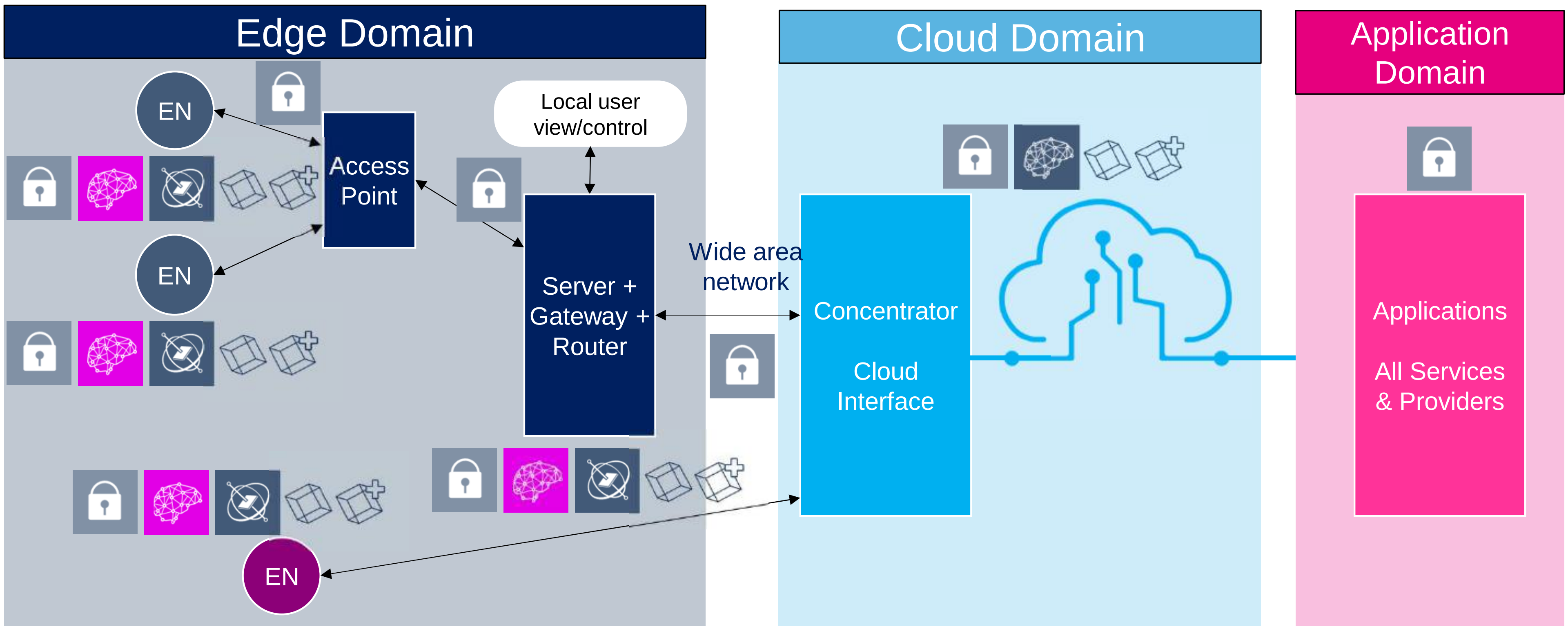
- Autonomy
- Reliable
- Large coverage
- Easy to use
- Integration
- Availability
- Cost
- Flexibility
- Robustness
- Support and Maintenance

- Digital Twin for prediction: maintenance, production, ….

IoT Reference Architecture



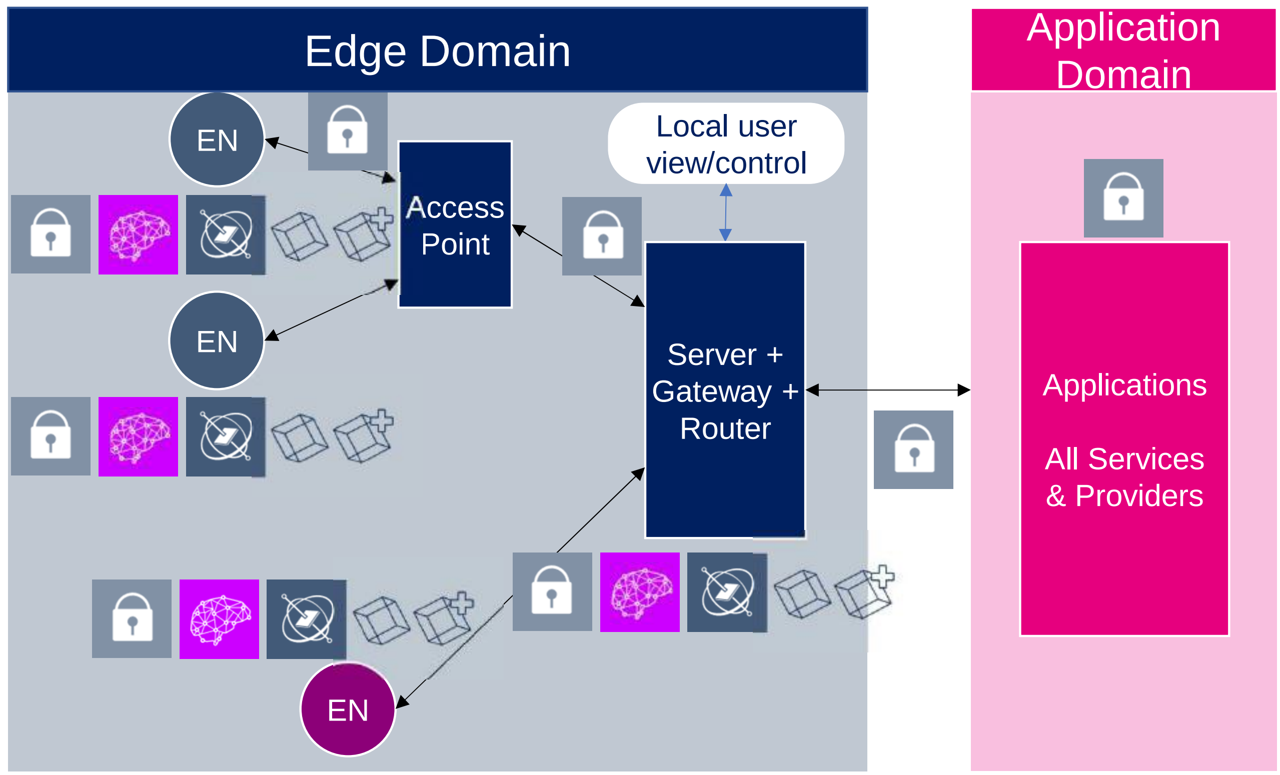
IoT & CPS System evolution



Move from Cloud to Edge → Edge computing

Benefits

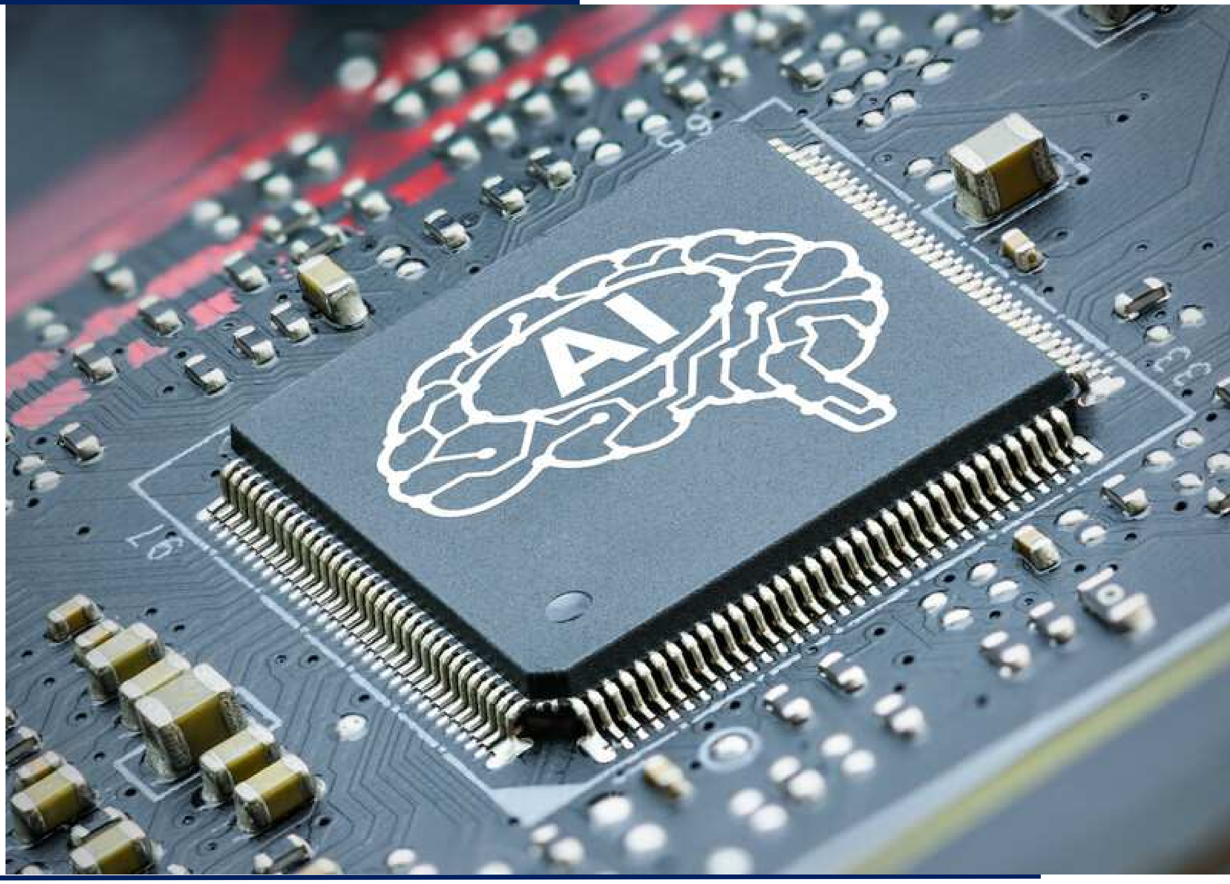
- Reduced latency
  → Real-time applications
- Reduced bandwidth
- Higher cyber-security and privacy
- Lower power consumption
- Local Private Network



WHAT is the ANDANTE Project?

Main Goal

To leverage innovative **IC designs** to build powerful **HW&SW platforms** supporting **artificial and spiking** neural networks



Main Activities

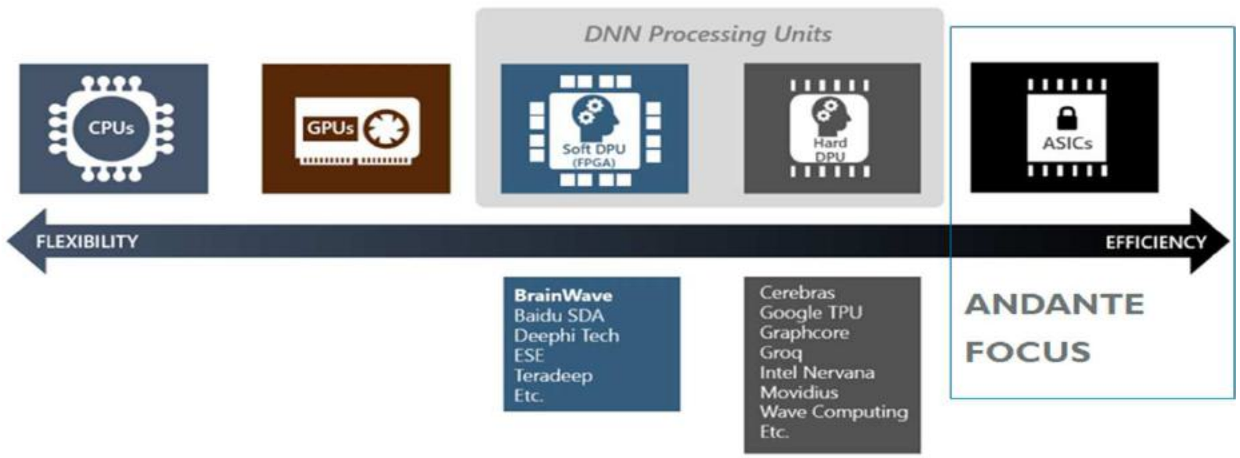
Emerging eNVM memories	Tools & Methodologies	Neuromorphic ASICs & FPGAs	AI Platforms & Applications
• OxRAM, • PCM • FeFET, • SOT-MRAM	• SW-HW co-design • Training, profiling and mapping a neural network on a HW target	• SNN and ANN architectures • Digital, mixed-design strategies	• Measure **KPI** • Validate, and evaluate **solutions pertinence**

ANDANTE Edge Application Areas

Innovative solutions in the Edge with **strong Market Impact**

Main Focus

Highly efficient artificial and spiking neural networks implemented in **ASICs, SoCs and FPGAs** to perform inference and/or classification



ANDANTE Consortium Members

ANDANTE Facts and Figures

Start
June 2020

End
Feb. 2024

Duration
45 Months

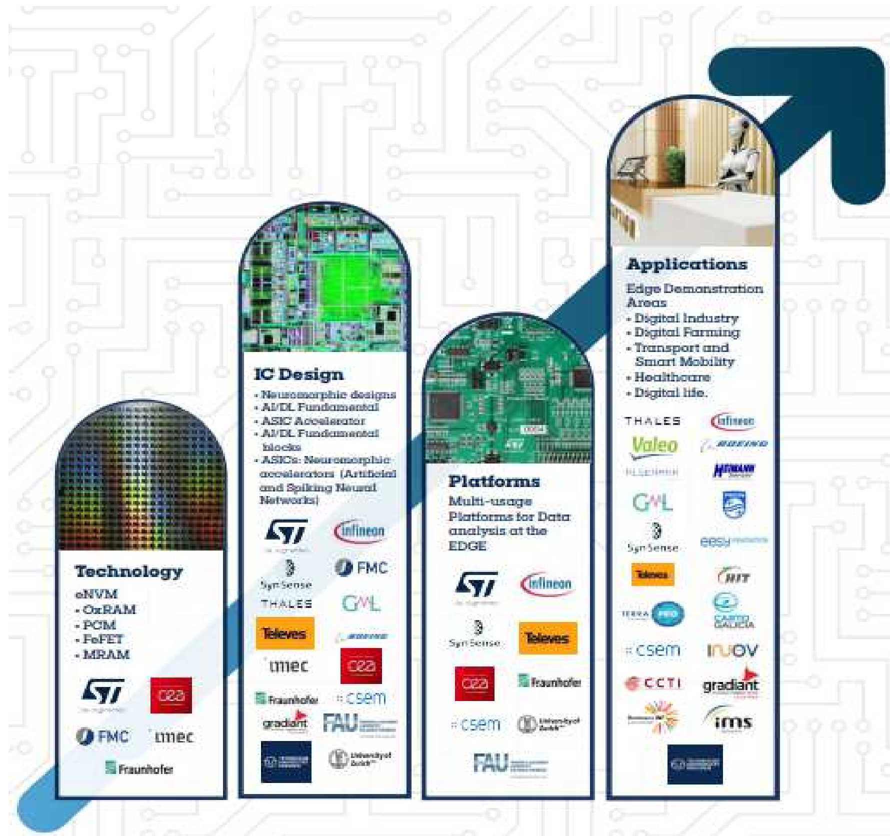
Budget
40 €M

Partners
30

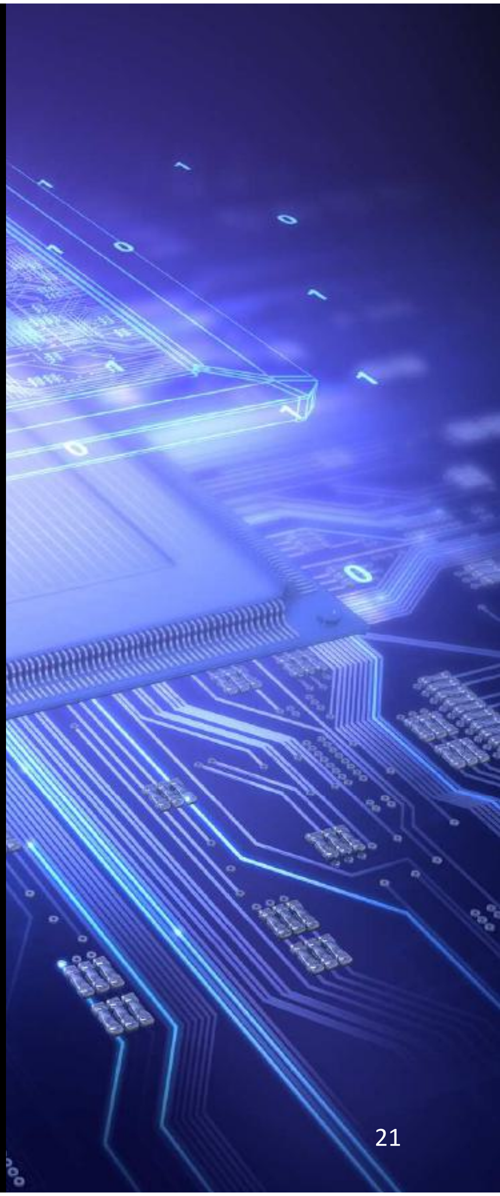
Countries
7

ANDANTE Value Chain

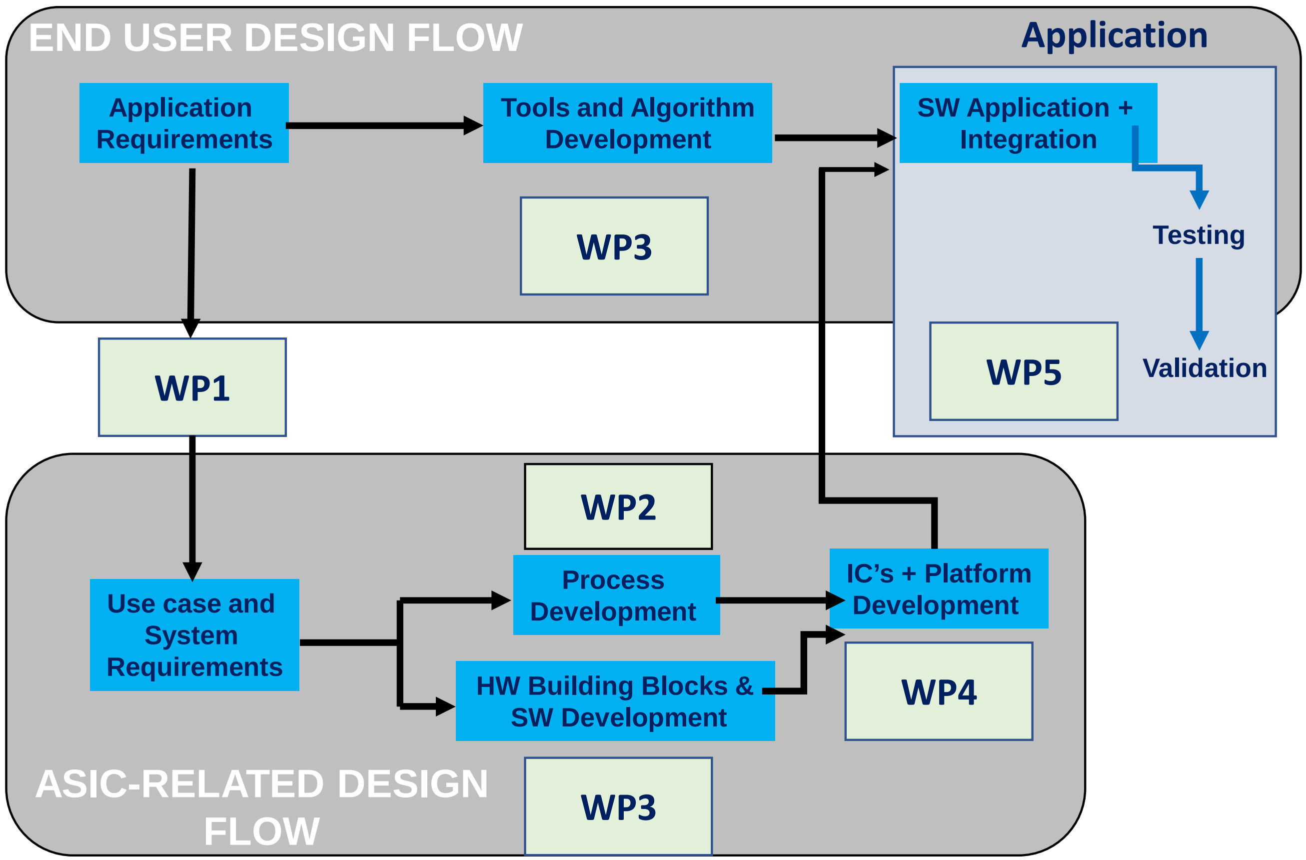
Complete value chain covered from technology formulation towards system realization



ANDANTE Work plan and activities



Project Structure

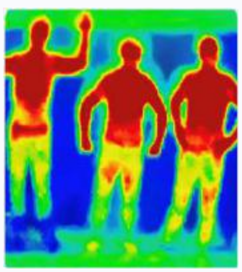


Applications

Digital Industry

UC1.1: Indoor Positioning, Recognition and People Counting

Partners: IFAG, EESY, TUD, FHG, HEI



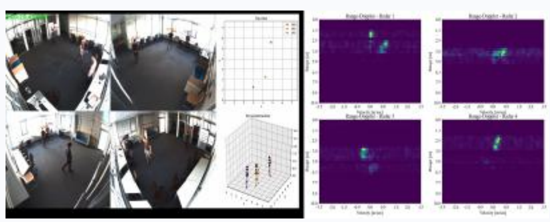
Description: Indoor positioning recognition and people counting for smart laboratory/factory applications (e.g., robot co-working)

Challenges:

- Real time computation
- Scaling to handle input of multiple sensors

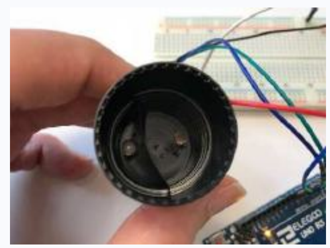
Positioning vs State-of-the-Art:

- Existing solutions are too slow to fulfill the safety requirement of a smart factory/laboratory



UC 1.2: Color Classification at the Edge for Quality Control

Partners: IFAG



Description: Integration of simple neuronal networks for color classification into color sensor nodes for real time control and monitoring devices at the edge

Challenges:

- Size of the AI solution
- Energy consumption and cost of the overall solution

Positioning vs State-of-the-Art:

- Existing solutions are too big, consume too much energy and are too costly to be integrated into color sensors

Digital Farming

UC2.1: Autonomous Weeding System

Partners: Bordeaux-INP, CEA and STGNB

Description:

- Crops and weeds detection
- Intra-row weeding
- Mechanically: alternative to chemical weeding
- Autonomous: limiting human intervention

Challenges:

- Computation in real-time
- High precision needed to differentiate crops and weeds

Positioning vs State-of-the-art

- To date, for most crops, only inter-row mechanized/autonomous weeding solutions exists

UC2.2: Tomato pests and diseases forecast

Partners: CCTI, Italagro, TPRO-Tech., CEA, STGNB

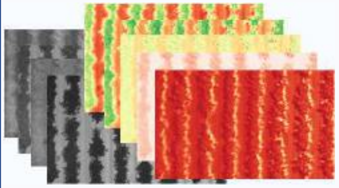
Description: Pest and disease detection model for the tomato agriculture industry.

Challenges:

- Collecting enough and good quality data
- Time-series analysis for forecasting
- Model selection and development for edge devices

Positioning vs State-of-the-art

- State-of-the-art solutions do not resort to image analysis with ANNs, which produce many false positive events.



Transport and Smart Mobility

Partners: Thales, CEA, STGNB

UC3.1: Drones/USV

Description: detection, classification and segmentation of high-altitude images using either ANN, SNN or hybrid technology

Challenges:

- Real time computation
- High resolution inputs
- Power consumption

Positioning vs State-of-the-Art:

- Existing solutions are not compatible with drone constraints

Partners:
ALSEAMAR, CEA, STGNB, Synsense

UC3.2: Underwater Acoustic Signal Classification

Description: The ocean soundscape is a continuously changing mosaic of sounds that originate from various sources. This is of primary interest to recognize in real time the components of the soundscape. Study on marine mammals classification.

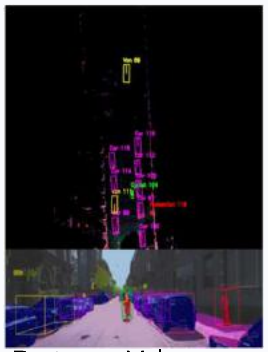
Challenges:

- Real time computation
- Low power

Positioning vs State-of-the-Art:

- Long-term monitoring
- Real time communication with shore

Transport and Smart Mobility



Partners: Valeo, CEA, STGNB, UZH

UC3.3: 3D Object Detection and Classification of Road Users based on LiDAR and camera

Description: Object detection on lidar point clouds that will be fused with camera semantic image data implemented on ANDANTE Platform

Challenge:

- Real time computation with received sensor data (bandwidth bottlenecks)
- Scaling to handle input of multiple sensors

Positioning vs State-of-the-Art:

- No fusion of both sensors/sensor data yet done on neuromorphic hardware

Partners: BR&T-E, Gradiant, TVES, CARTO

UC 3.4: Robust Autonomous Landing

Description: Four critical functionalities are considered: 1) image-based runway relative localization for navigation, 2) image registration for navigation, 3) foreign object detection on runway, 4) robust communications.

Challenges:

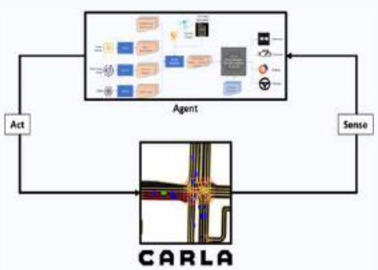
- Real time computation
- Adaptation of large networks to efficient hardware without sacrificing performance levels
- Learning on the edge

Positioning vs State-of-the-Art:

- Many smaller aircraft cannot permit energy cost of large number of conventional AI algorithms in standard hardware, which on the other hand, are necessary to enable autonomous operations.

Transport and Smart Mobility

Partners: GML, Valeo



UC3.5: Path Planning for Autonomous steering

Description: Continuously calculate trajectories, based on deltas in world map, avoid intersects, while optimally steering the vehicle, e.g., by solving many diff equations

Challenges :

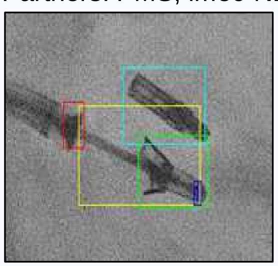
- 100Hz world map update rates and <10ms latency ➔ huge comp. loads
- Small form-factor (<200x200mm) and power consumption (<2W)

Positioning vs State-of-the-Art:

- Reduce power by 100x over SotA
- Reduce latency by 10x over SotA

Healthcare

Partners: PMS, imec-NL



UC 4.1: Multi-modal image processing and device tracking in medical X-ray & ultrasound images

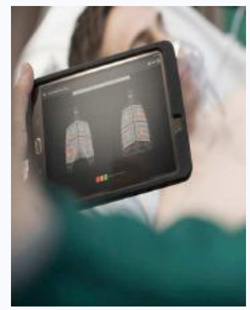
Description: Navigating a medical device like a Mitral Clip to the right location in the heart is challenging and requires accurate and intuitive image guidance.

Challenges:

- Detection accuracy → placement of device
- System latency → eye-hand coordination

Positioning vs State-of-the-art

- Benchmark the SNN version of the detection algorithm against an implementation in state-of-the-art GPU HW



Partners: PRE, imec-NL and GML

UC 4.2: Ultrasound acquisition or processing

Description: Lung ultrasound can detect healthy/unhealthy (Covid-19, Pneumonia) patients. We create a neural network to automatically detect healthy/unhealthy lungs

Challenges:

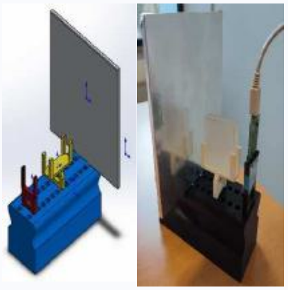
- Make NN fit on the two platforms

Positioning vs State-of-the-Art:

- Automatic detection
- Need low power consumption for mobile ultrasound

Healthcare

Partners: EESY, IFAG



Use Case 4.3: Glucose Monitoring

Description: Apply SNN algorithms to high-frequency sensor data to classify different glucose level in water dilutions.

Challenges:

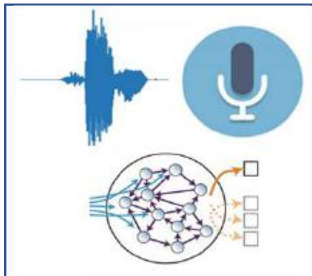
- To distinguish standard human body glucose concentrations

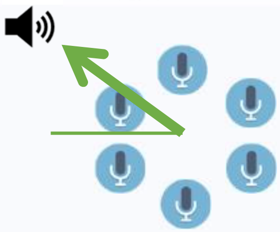
Positioning vs State-of-the-art

- Leverage the faster computation of the SNN to reach accurate results of the glucose level using less time and energy resources.

Digital Life

UC5.1: Consumer Auditory Processing





Overall Challenges:

- Continuous real time computation
- Low-latency, low-power requirements

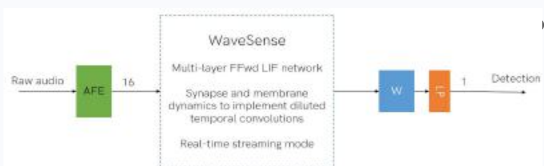
5.1a: Continuous audio scene classification. The audio environment is monitored continually, to assist in selecting a noise reduction scheme appropriate for the environment.

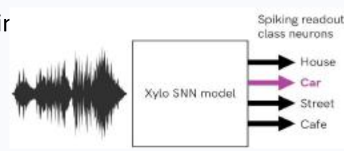
5.1b: Audio event detection: Continuous monitoring of audio signals for pre-defined trigger events, such as glass break (for security purposes) or distress call (for health monitoring purposes).

5.1c: Multi-microphone auditory processing: A low-power sensory processing task designed for multiple simultaneous input channels (i.e., a microphone array), to assist in noise reduction in smart home devices.

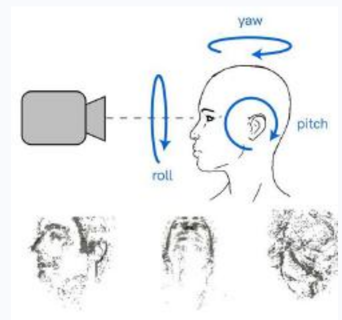
5.1d: Voice Activity Detection: Monitoring of audio scene for detection of voiced speech which acts as a wake up signal for smart devices.

Partners: Synsense, UZH, FHG, STGNB





UC5.2: Vision -based human computer interaction application



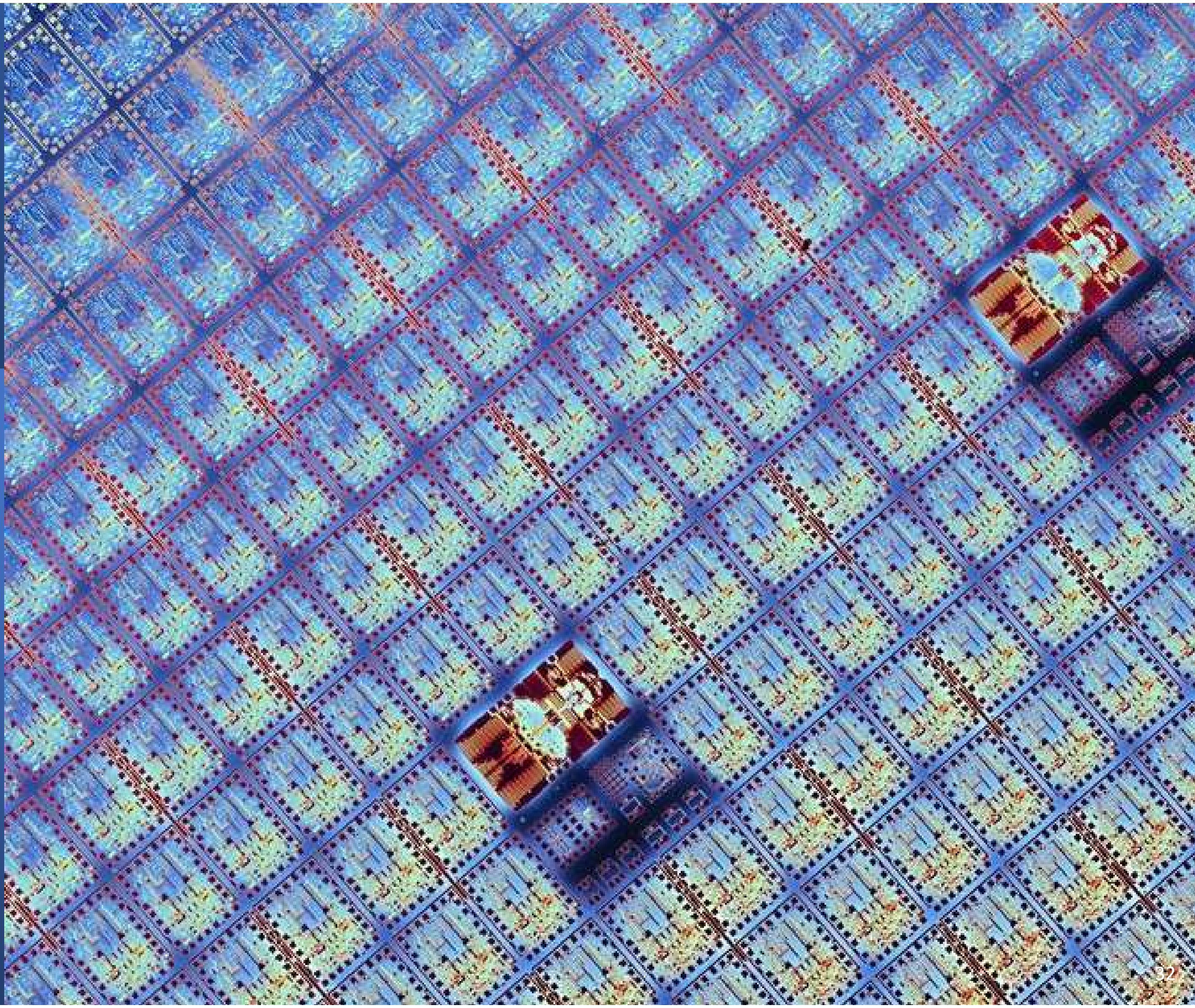
Description: Glance detection for mobile hand-held devices, to be used as a smart wake-up trigger

Challenges:

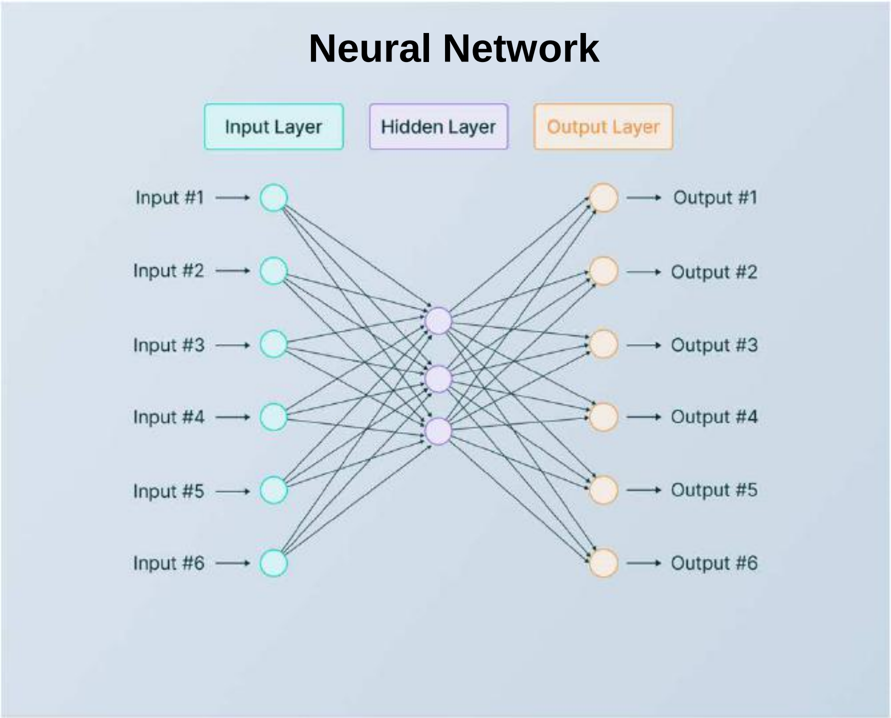
- Low-latency and low-energy requirements
- Low false-reject rate requirements

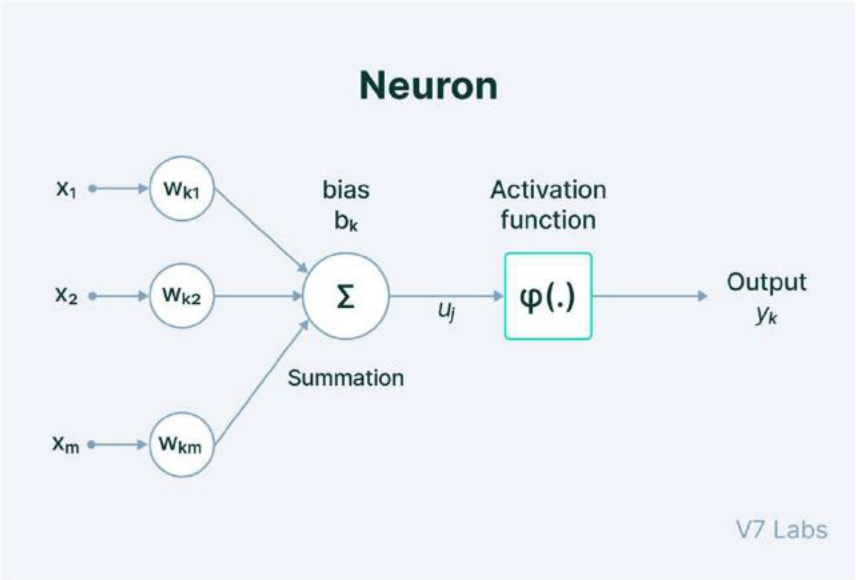
Partners: Synsense, UZH, CSEM, STGNB

New Memory Technologies for AI Applications



Deep Learning : Key concepts

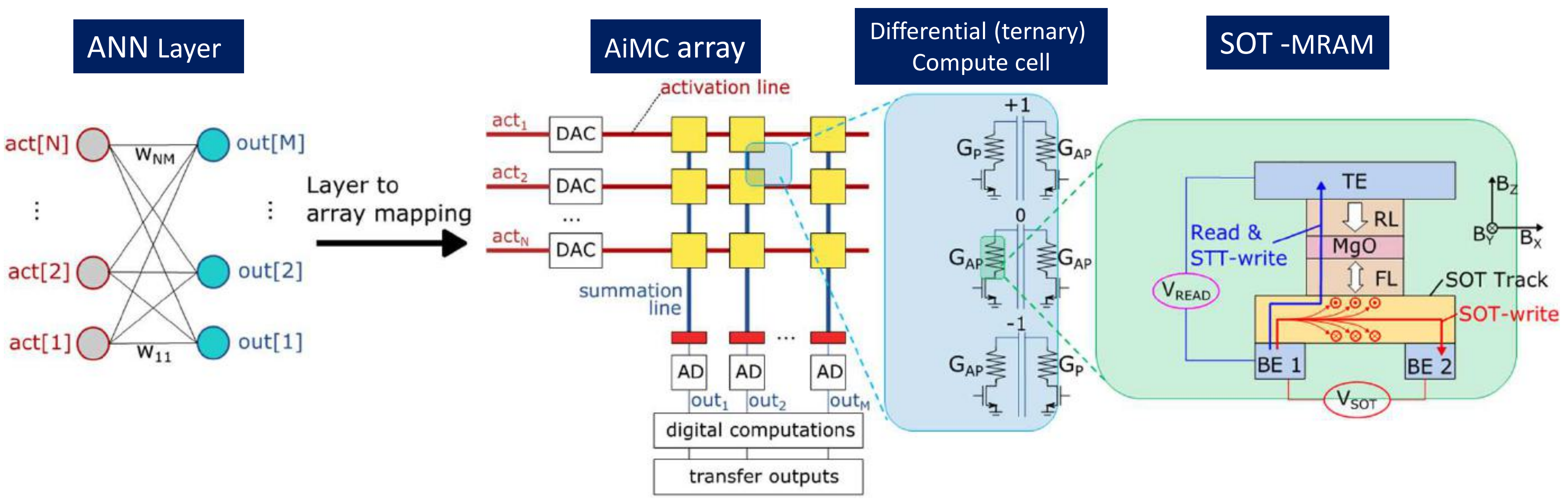




https://www.v7labs.com/blog/neural-networks-activation-functions#h1

eNVM Features

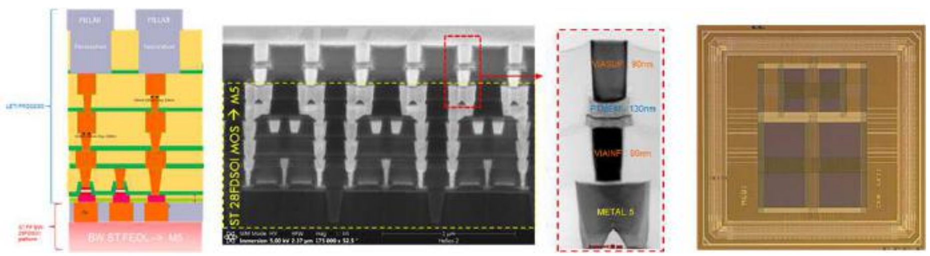
- Matrix vector multiplications (MVMs).
- Minimizing the data movement between through IMC (In Memory Computing techniques) and the high storage density of eNVM.



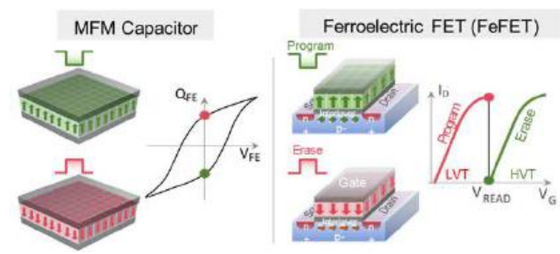
eNVM: OxRAM, PCM, FeFET, SOT-RAM

- New low-power architectures for edge AI applications.
- New memory technology options for In Memory Computing (IMC) and high storage density.

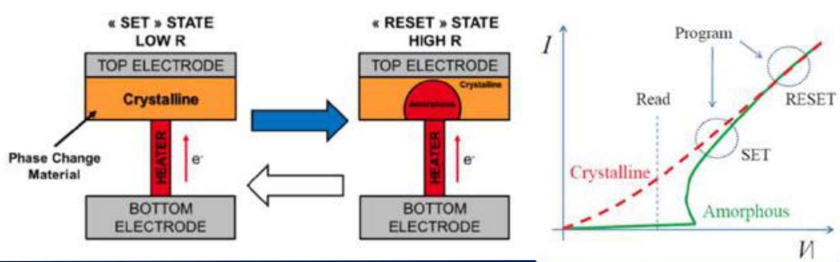
Large scale integration in OxRAM



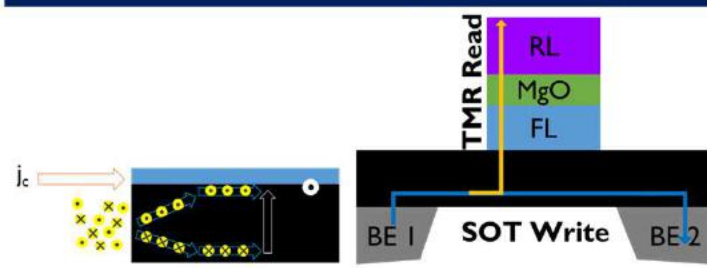
High endurance of Ferroelectric FET (FeFET)



Reliability and Large scale integration Phase Change Memory



“Unlimited endurance” Spin-Orbit Torque MRAM



eNVM Technologies : Score card

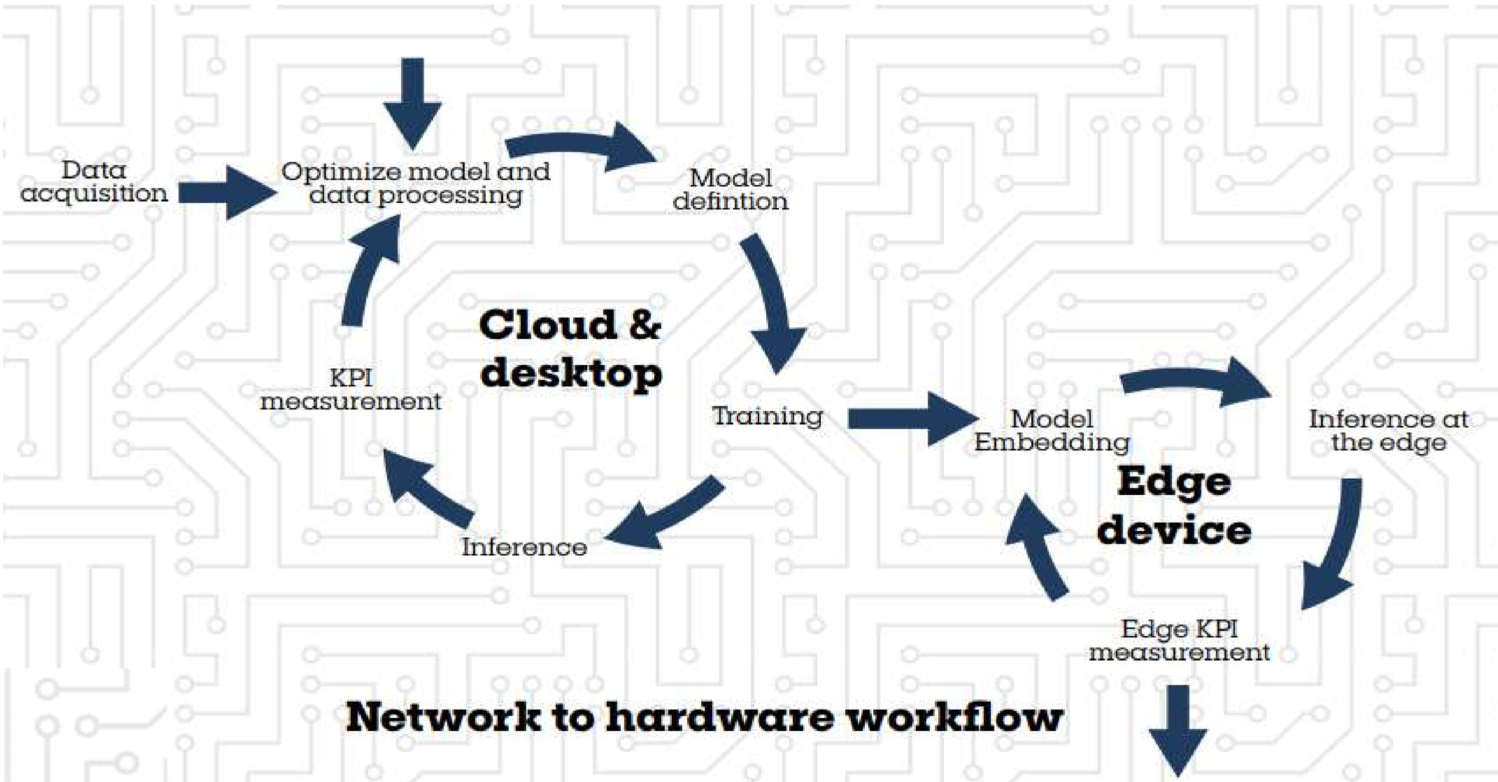
	SOT-MRAM	2T1C BEOL TFT	FeFET	PCM	PCM (2)	ReRAM
Evaluation current	10 µA .. 100 nA (tuneable)	100nA	10 µA .. 100 nA (tuneable)	10 – 20 µA	10 – 20 µA	100..10 µA
Device-to-device (D2D) variation	5%	10%	5%	<10%	<10%	30%
Cycle-to-cycle (C2C) variation	5%	10%	5%	<10%	<10%	30%
On/off ratio	2 .. 3	> 1e9	1E3...1E8	> 100	> 100	5 .. 20
Read voltage	0.8 V	0.8 V	0.8 V	MOS: 0.5-0.6 V	BJT: 1.5-1.6 V	0.1 .. 0.4 V
Write current	100µA	1µA	0	< 300µA	300µA	200 ..100 µA
Write voltage	0.1V	1V	2.5 ... 5 V	MOS: ~2.5 V	BJT: ~4.5 V	1.5 .. 2.5 V
Write time (pulse)	1 ns	10 ns	10 ns ... 1ms	GST225: < 100ns / < 400ns	Ge-rich-GST: <100ns / < 2us	100 ns ... 1µs
Area (full cell size)	0.15 μm^2	0.26 μm^2	0.007 ... 0.25 μm^2	MOS: 0.036 µm2	BJT: 0.019 µm2	0.11 .. 0.2 μm^2
Write endurance (full swing)	1.00E+15	Infinite	1.00E+05	> 1.00E+5	> 1.00E+5	> 1E+5
Number of levels (with σ)	2	8	8	GST225: 2-4	Ge-rich-GST: 2	8
Retention (@temp)	Infinite	1 min	10 year @120°C	GST225: 10y@95°C	Ge-rich-GST: 10y@150°C	10 year @120°C
Write energy	10 fJ	50 fJ	< 1 fJ	~ 10 pJ	~ 100 pJ	2 pj
Read energy	1 fJ	1 fJ	1 fJ	~ 10 fJ	~ 10 fJ	30 fj (dynamic differential reading mode)

eNVM Technologies: Strengths & Challenges

		Flash reference	MRAM type	PCM type	ReRAM type	FeFET	Hf based FERAM 1T1C
Performance	Programming power	<200pJ/bit - # 100pJ/bit (eSTM)	~20pJ/bit	~90pJ/bit	~100pJ/bit	<~20pJ/bit	<pJ/bit
	Reading access time	HV devices ~15ns	Core oxide device ~1ns	No HV devices ~5ns	No HV devices ~5ns	No HV devices ~5ns	Write after read (Destr. Read)
	Erasing granularity	FN mechanism Full page erasing	bit-2-bit erasing Fine granularity	bit-2-bit erasing Fine granularity	bit-2-bit erasing Fine granularity	bit-2-bit? Depend on archi	bit-2-bit erasing
Reliability	Endurance	Mature technology	High capability 10^15 ?	500Kcy	10^5 trade Off with BER	10^5 Gate stress sensibility	10^11 #10^6 with write after read
	Retention	Mature technology	Main weakness Trade-off with Taa	150°C auto compliant	Demonstrated Trade Off with power	To be proven	To be proven
	Soldering reflow	Mature technology	High risk To be proven	pass	possible	To be proven	To be proven
Cost	Extra masks	Very high (>10)	Limited (3-5)	Limited (3-5)	Limited (3-5)	Low (1-3)	Low (1-3)
	Process flow	Complex	Complex	Simple	Simple	Simple	Simple
	New assets vs CMOS	Shared	New _ manufacturable	New _manufacturable	BE High-k material	FE High k material	BE High-k material

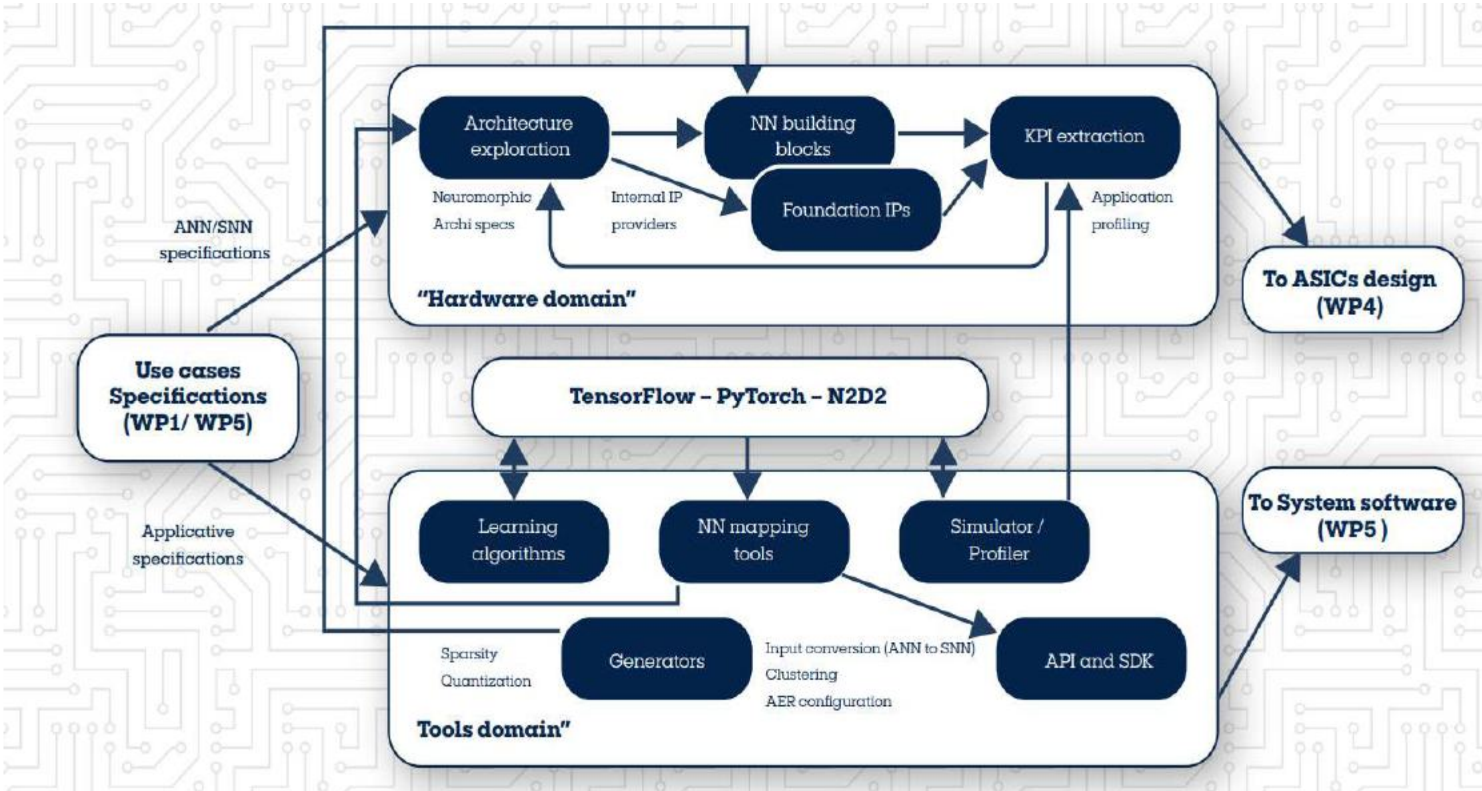
Tools and Methods for training, profiling and mapping NN on a HW target

Workflow for embedded neural networks



Design Challenges of Edge AI processors

SW-HW co-design methodology pursued in ANDANTE.



Application dependent high-level design choices

What coding style to use?

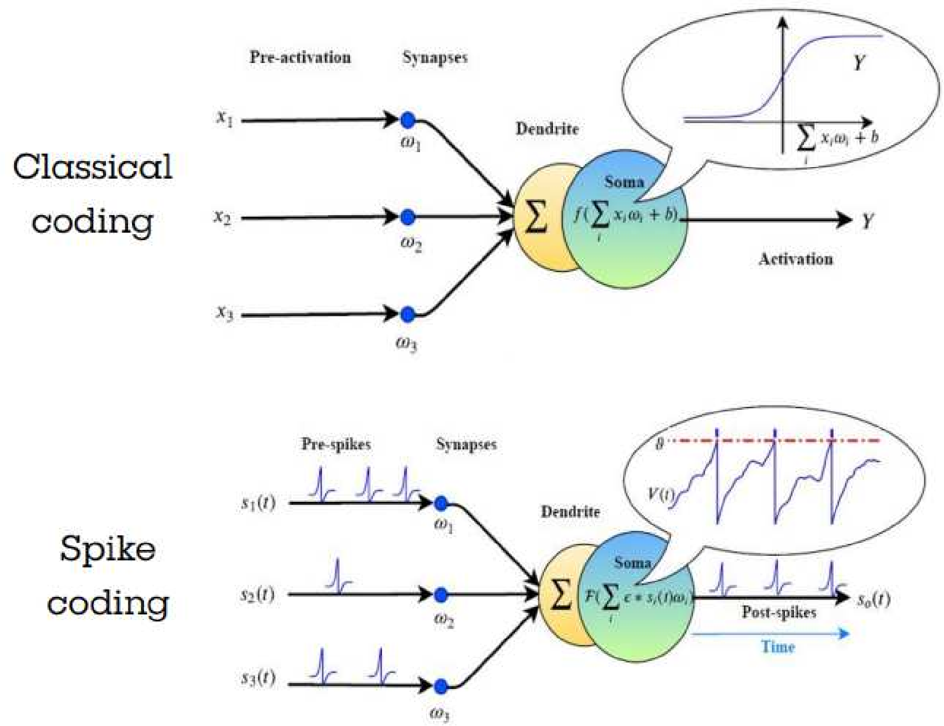
- Classical for still inputs (e.g., images)
- Event / Spike for always-on, low-activity inputs (e.g. surveillance)
    - o Rate code is to for “Frame-type” inputs
    - o Temporal code is best on Temporal series (e.g. audio)

What network topology?

- A Deep, Feed Forward for high accuracy and fixed inputs applications
- A Shallow, recurrent for temporal series (e.g., audio)

What implementation strategy?

- A fully digital for very deep, large, networks
- An analog mixed-signal for shallower networks



Tools

Training Tools

❑ Spike-Coding

- ANN-to-SNN conversion
- Direct SNN training (offline and On-chip learning)

❑ Classical coding

- Transfer learning
- Quantization Aware (QAT) Training: reduces memory footprint and enables the use of embedded NVM

❑ HW aware training (HAT) for mixed-signal implementations of ANN ASICs

- Takes non-idealities into account during the training phase

Generation, Mapping and Simulation Tools

❑ Hardware generator

- Writes RTL (for digital NN)
- Generates schematic and layout (for analog NN)

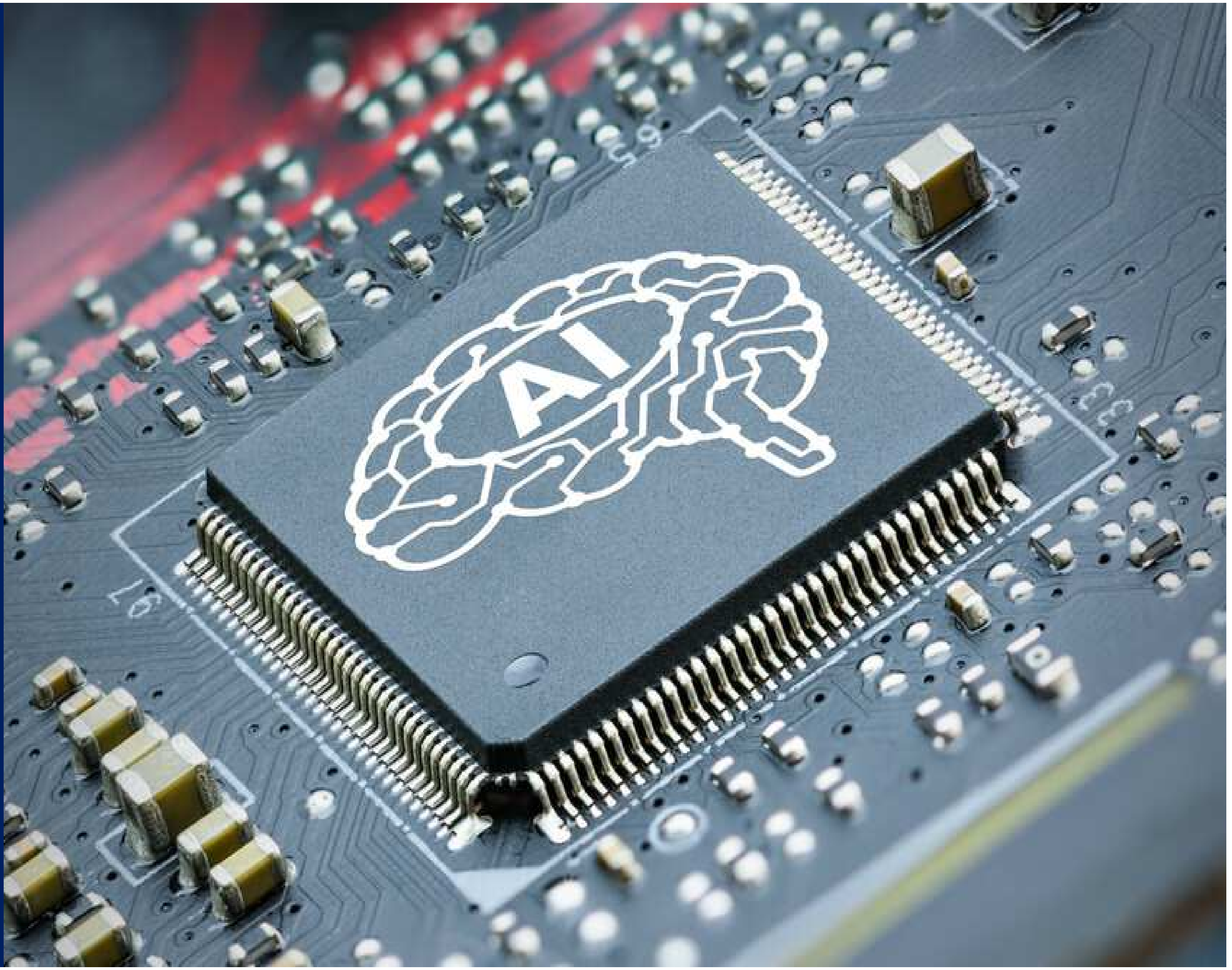
❑ Neural Network Mapper on Hardware

- Maps onto Processing engines or NVM arrays

❑ Simulation

- Estimates power dissipation

Design of Neuromorphic SoCs, ASICs and FPGAs, and Platforms



Objectives and Challenges

- Design : **inference, classification, segmentation accelerators** based on **analog, digital and spiking neurons**
- Design **ASICS, SoCs, FPGAs and dedicated platforms** for **5** application domains
- Performance evaluation through **14 use cases**

- Managing several **design types** and in advanced technologies
- Managing efficiently HW/SW **co-design tools** of neuromorphic hardware
- Managing the support of **various applications in the same platform**

Design of Edge AI processors (1/2)

6 FPGA Designs

Designs

- 16 SpiNNaker2 processing element
  Hybrid inference accelerator
- Neuromorphic accelerator, SENeCA
- Accelerated inference of DNN for runway detection, Yolo v4
- Accelerated inference of DNN for object detection and image registration, RetinaNet and VGG19
- Accelerated inference of DNN for process communication parameters MobilNet V1

Benefits

- High level of (HW/SW) programmability
- Design Flexibility
- Easy to update and Optimize

Xilinx Platforms

Applications

- Smart Mobility and Healthcare application areas
- Validation
- KPIs measurement

VCU118

ZCU102

ZCU1

Design of Edge AI processors (2/2)

8 ASIC Designs

Designs

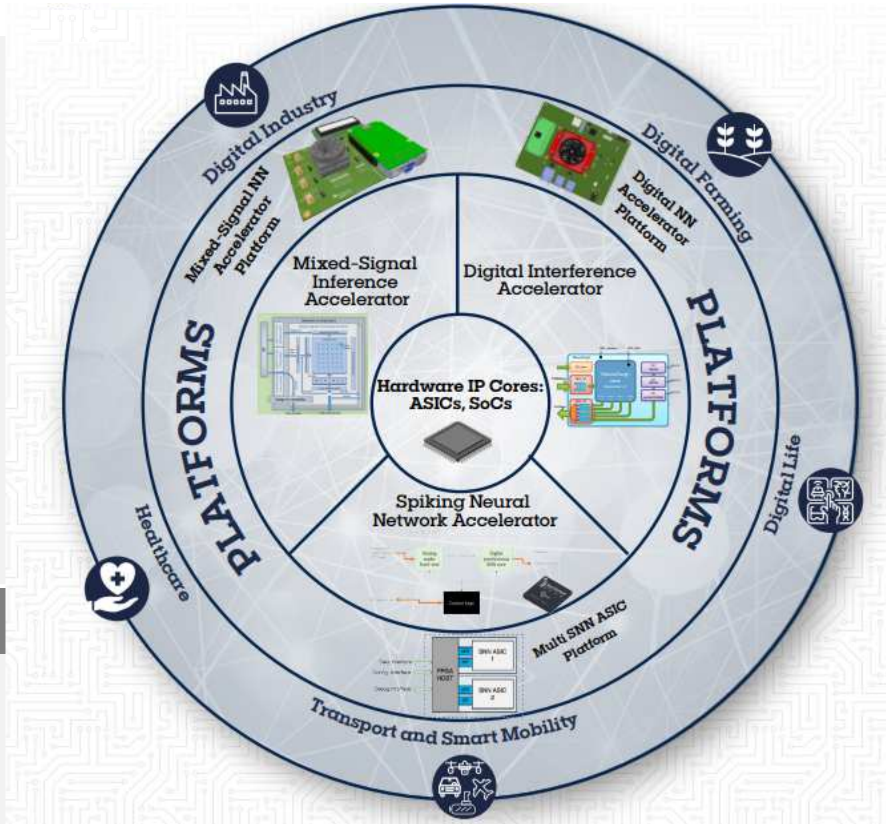
- 2 Mixed-signal SNN
- 1 Digital ANN (inference accelerator)
- 1 Digital CNN (smart vision)
- 3 Mixed-signal inference accelerators with in-memory computing
- 1 SoC (MCU + NPU (AI accelerator)

Benefits

- High energy efficiency
- Low latency
- High integration

6 Platforms

- 14 Applications in 5 Application areas
- Validation
- KPIs measurement
- Evaluation

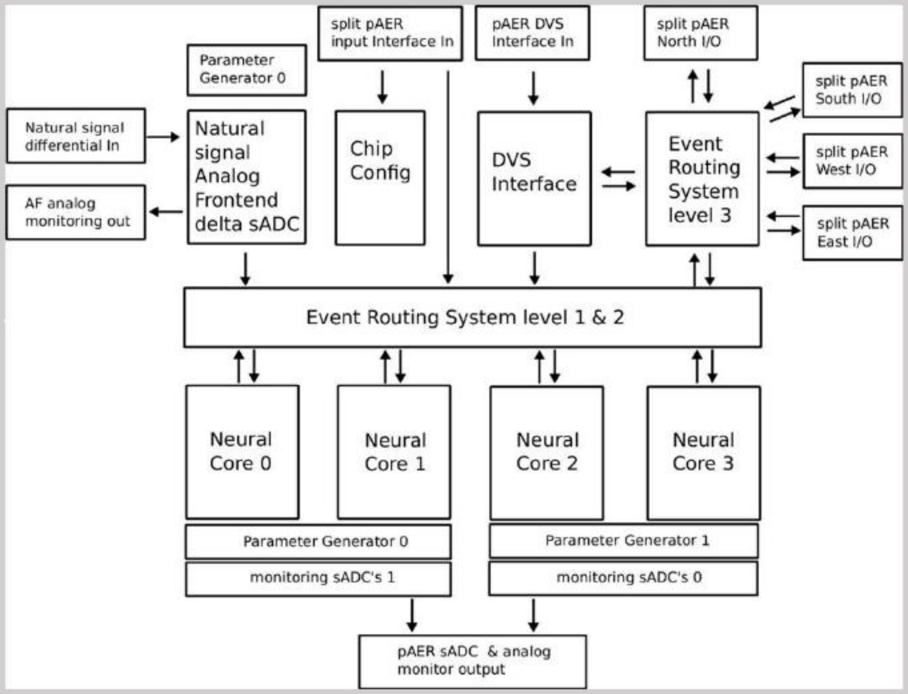


UZH: Multi-Core Mixed Signal SNN

ASIC 1.2 Mixed Signal SNN

- **Target**: low-dimensional signal representations, such as auditory signals, vibrations, or bio-signals not related to machine vision
- **Technology** : PCM/ 28 nm ST/P28
- **Memory type**: PCM
- **NN Type**: Spiking
- **Status** : Under design
- **Silicon**: Jan/Feb 2024
- **Use case:** Embedded AI for heterogenous sensor processing (Sound, ultrasound, ECG, Keyword spotting, etc.)

Block Diagram of Multi-Core Mixed Signal SNN

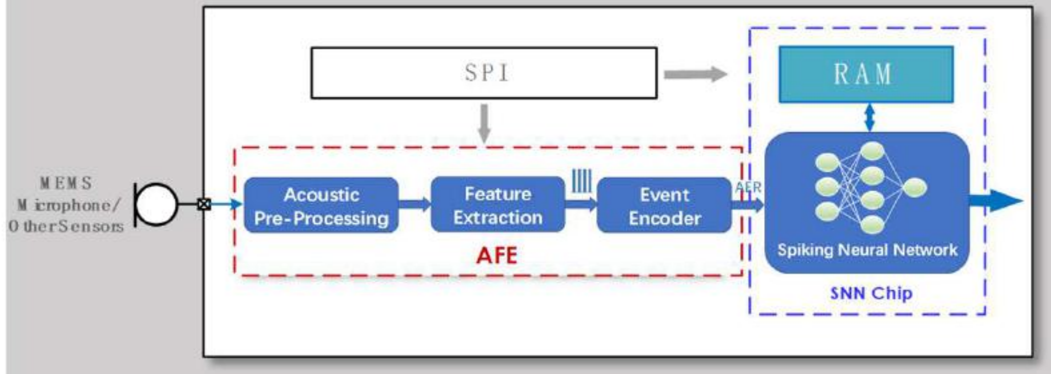


SynSense: Audio Front-end

ASIC 1.3 Audio Processing

- **Target**: Low -power analog audio front-end tailored for human speech applications. It performs analog filtering via a set of tuneable bandpass filters for its processing by a Spiking Neural Network. not related to machine vision
- **Technology**: 40 nm TSMC
- **Input bandwidth : 100 – 20 kHz**
- **Expected power consumption** : < 300 uW
- **Status** : Silicon available
- **Use case**: 3.2 Under water signal classification, 5.1 Consumer Auditory processing

Architecture of AFE interfacing with an SNN Chip

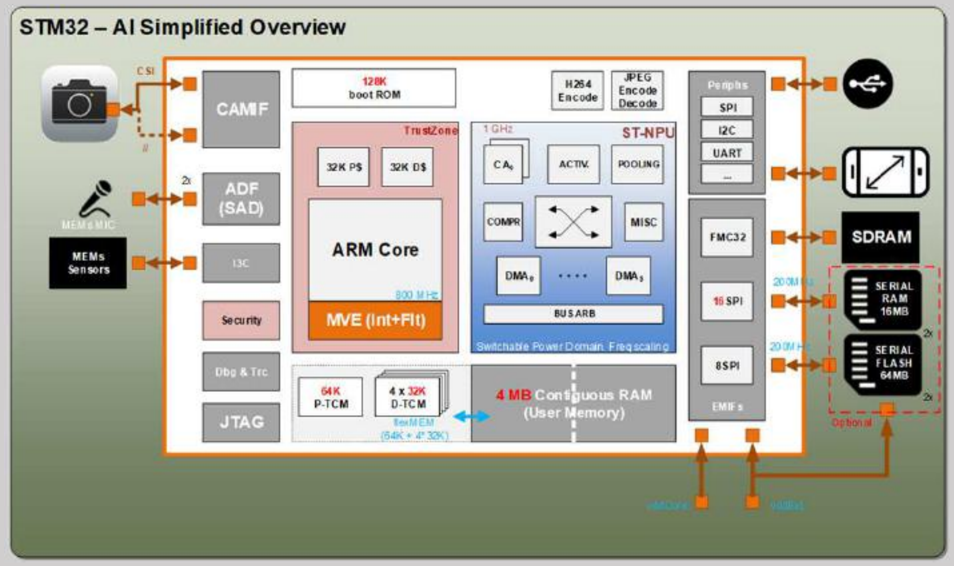


ST: Digital MCU with AI (1/2)

SoC 1.1 ST32 –AI MCU

- **Target:** SoC combining a Microcontroller STM32 microcontroller with AI acceleration via a neural processing unit for consumer applications
- **Technology**: 16 nm FinFET TSCM / SRAM
- **Memory**: SRAM, 4.2 Mbyte
- **NN type**: ANN/CNN/Yolo V3
- **Expected efficiency** : 3.3 TOPS/W
- **Expected power consumption** : TBD
- **Status** : Silicon available
- **Use case:** consumer applications

Block diagram of STM32 AI SoC

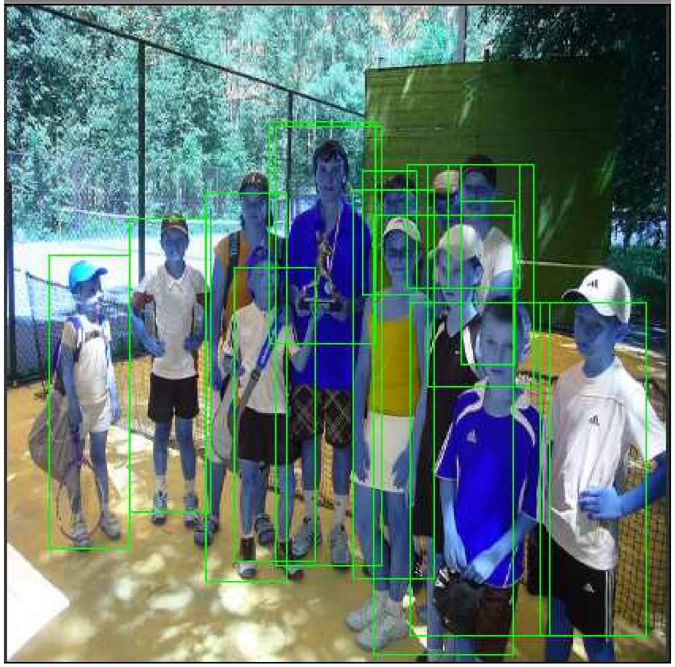


ST: Digital MCU with AI (2/2)

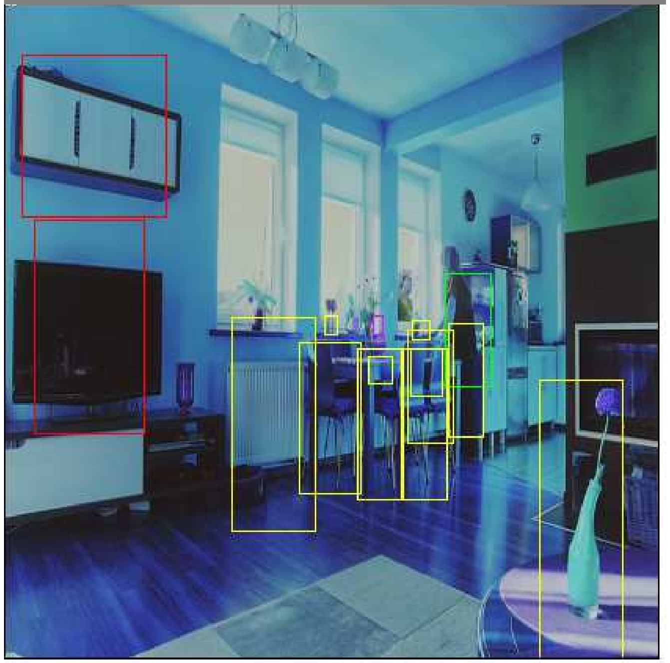
Measurements

- 314 fps
- 1 to 2 order of magnitude > SW solution on STM32H7 (Arm Cortex A7)

YOLO : Inference of Persons



YOLO : Inference of Persons & objects



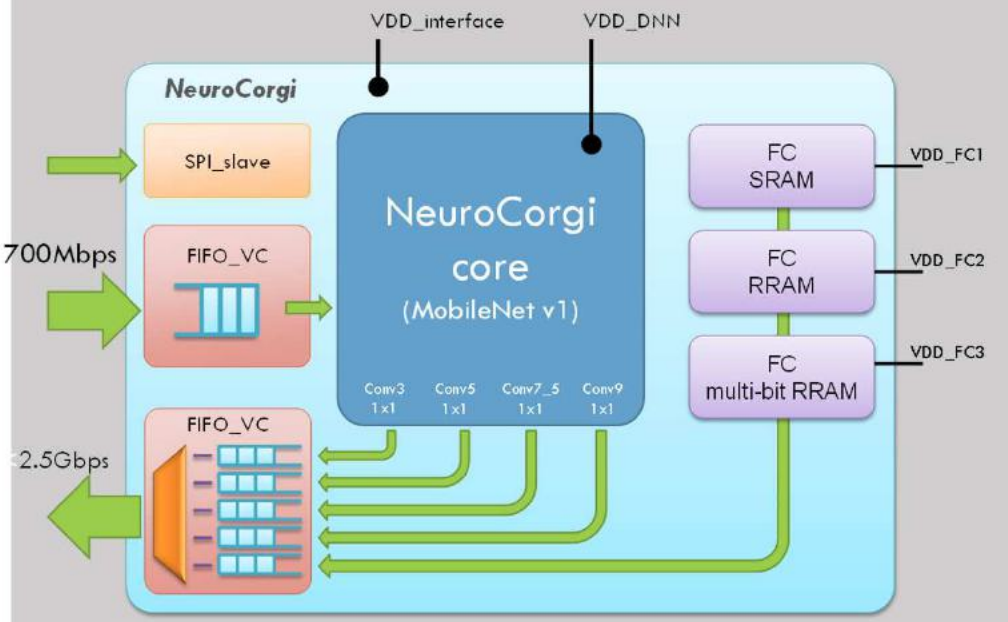
Demos done at Embedded World March 2023

CEA: Digital ANN

ASIC 2.1 NeuroCorgi

- **Target**: Feature extractor circuit to address image classification, segmentation and detection for ANN applications minimizing the energy required per inference while having an extremely low latency.
- **Technology**: 22 nm FDSOI GF
- **Memory**: SRAM, ~600 kbyte / OxRAM,
- **NN type**: ANN/CNN/MobilNet V1
- **Input throughput** : images 1280 pixels (24 bits RGB pixels), 1280x720 @30 FPS or 1280x360 @60 FPS or 640x480 @90 FPS
- **Inference Latency** : < 10 ms
- **Expected efficiency** : > 10 TOPS/W
- **Expected power consumption** : < 100 mW
- **Status** : Under Fabrication
- **Silicon**: June 26th, 2023
- **Use cases:** 2.1: Autonomous Weeding System, 2.2: Tomate Pest and disease forecast, 3.1: Drones/USV, 3.2 Under water signal classification; 3.3: 3D object detection and classification of road users based on Lidar and camera, 3.4: Robust autonomous landing

NeuroCorgi Architecture

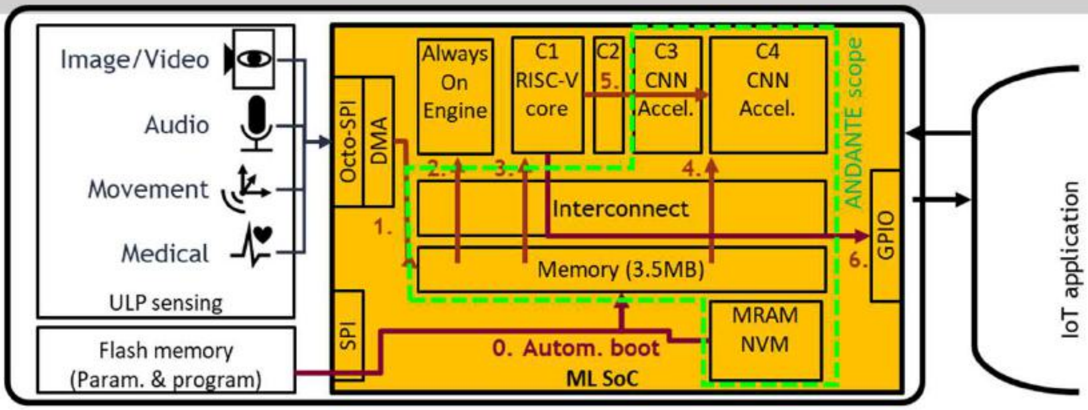


CSEM: Digital CNN

SoC 2.1 Visage 2

- **Target**: Neural Compute Engine (NCE) targeting NN acceleration for smart vision applications in digital life domain
- **Technology**: 22 nm FDSOI GF
- **Memory**: MRAM, 3.5 MB
- **NN type**: ANN/diverse classes
- **Input throughput** : OctoSPI @ 1600 Mbps DCMI @ 500 Mbps
- **Expected efficiency** : 10 TOPS/W
- **Expected power consumption** : 10 uW to 10 mW
- **Status** : Under design, Fab-in September
- **Silicon**: End of December, 2023
- **Use case:** 5.2 vision–based human computer interaction applications

Architecture of End-to-end ML inference SoC with the NCE for ML acceleration

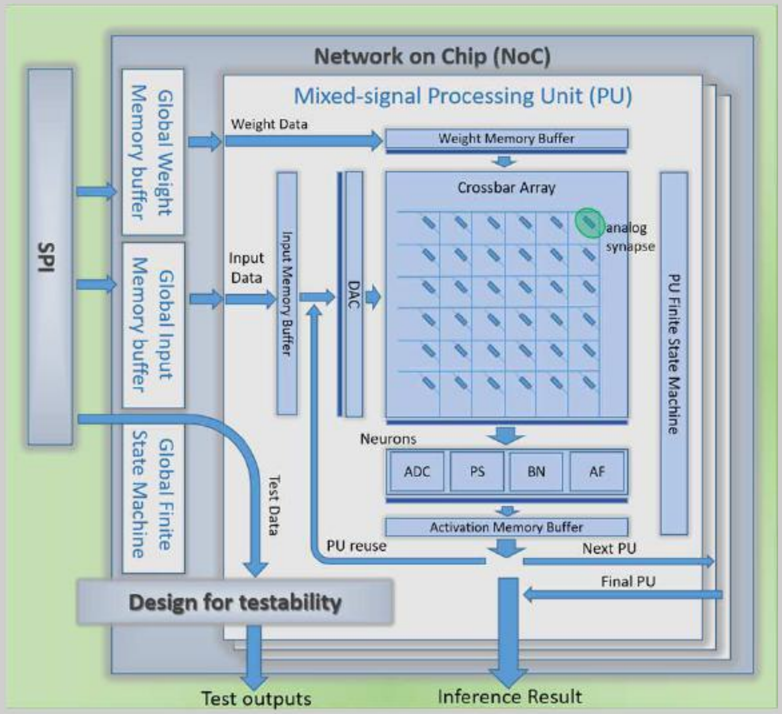


FhG/IIS&EMFT: Mixed Signal ANN

ASIC 3.1 Adelia 22 gen2

- **Target**: Scalable and configurable mixed-signal inference accelerator with a multi-core architecture using analog in-memory computing for voice activity detection (VAD).
- **Technology**: 22 nm FDSOI GF
- **Memory**: SRAM , ~600 kB
- **NN type**: ANN
- **Input throughput** : Audio features up to 64x13x20x 8 bit/s
- **Inference Latency** : < 10 ms
- **Accuracy** : 82% min
- **Expected efficiency** : ~5 TOPS/W (estimated for 8b OP)
- **Expected power dissipation** : 1mW
- **Status** : Silicon under test.
- **Use cases:** 5.1d Voice activity detection (VAD).

Architecture of the ADELIA 22 Gen2 ASIC

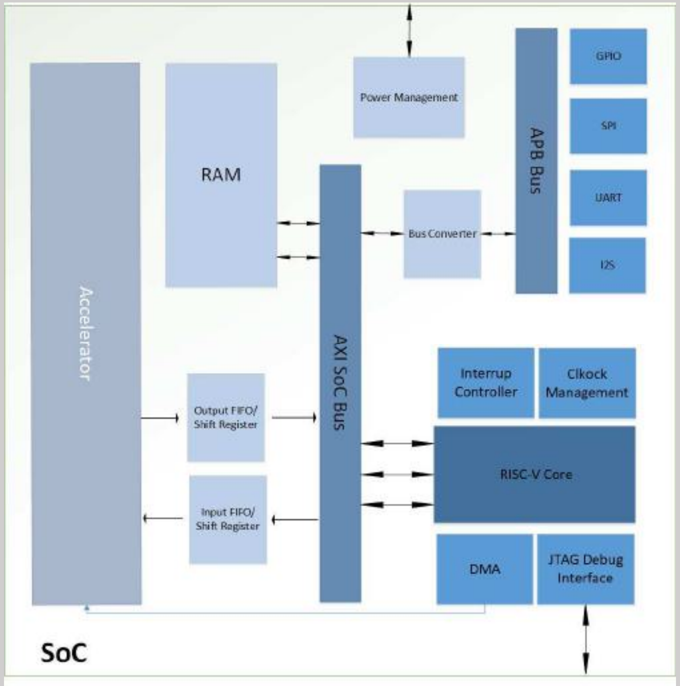


FhG/IPMS: Mixed Signal ANN

ASIC 3.1b IMC

- **Target**: Flexible SoC for convolutional neural networks integrating multiply-accumulate (MAC) accelerators using FeFETs with a RISC-V microcontroller for person detection and classification.
- **Technology**: 22 nm SLPe GF
- **Memory**: FeFET
- **NN type**: ANN/CNN/Yole-V3
- **Throughput**: : 20 inference/s typ
- **Inference latency** : 10 ms
- **Accuracy** : 85% typ
- **Expected efficiency** : 20 TOPS/W
- **Expected power dissipation** : 10 mW
- **Status**: Fab-out July 2023.
- **Use cases:** 1.1 People counting and indoor positioning

Architecture IMC SoC

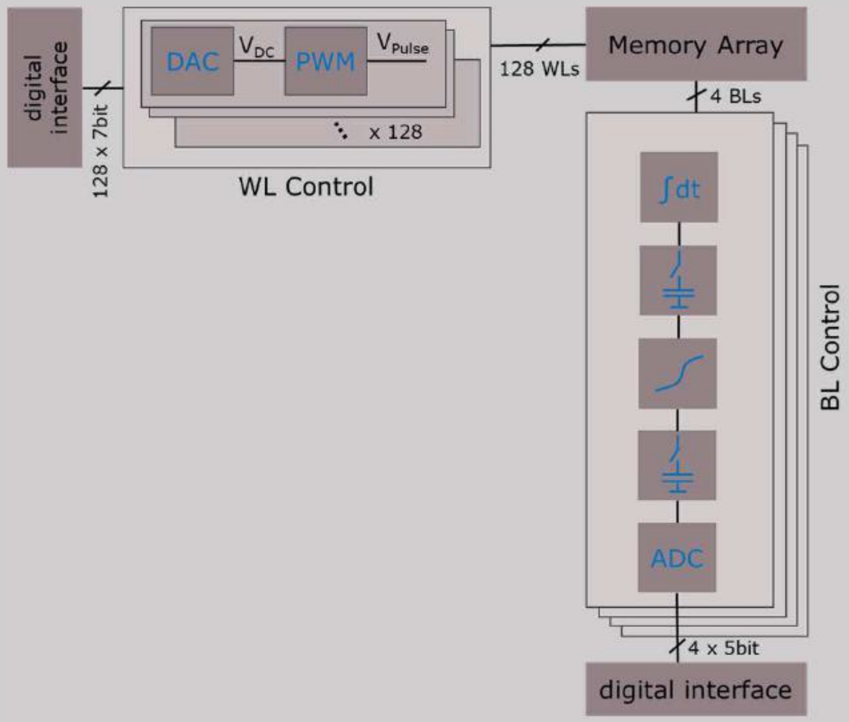


Infineon: analog Neural Network (aNN)

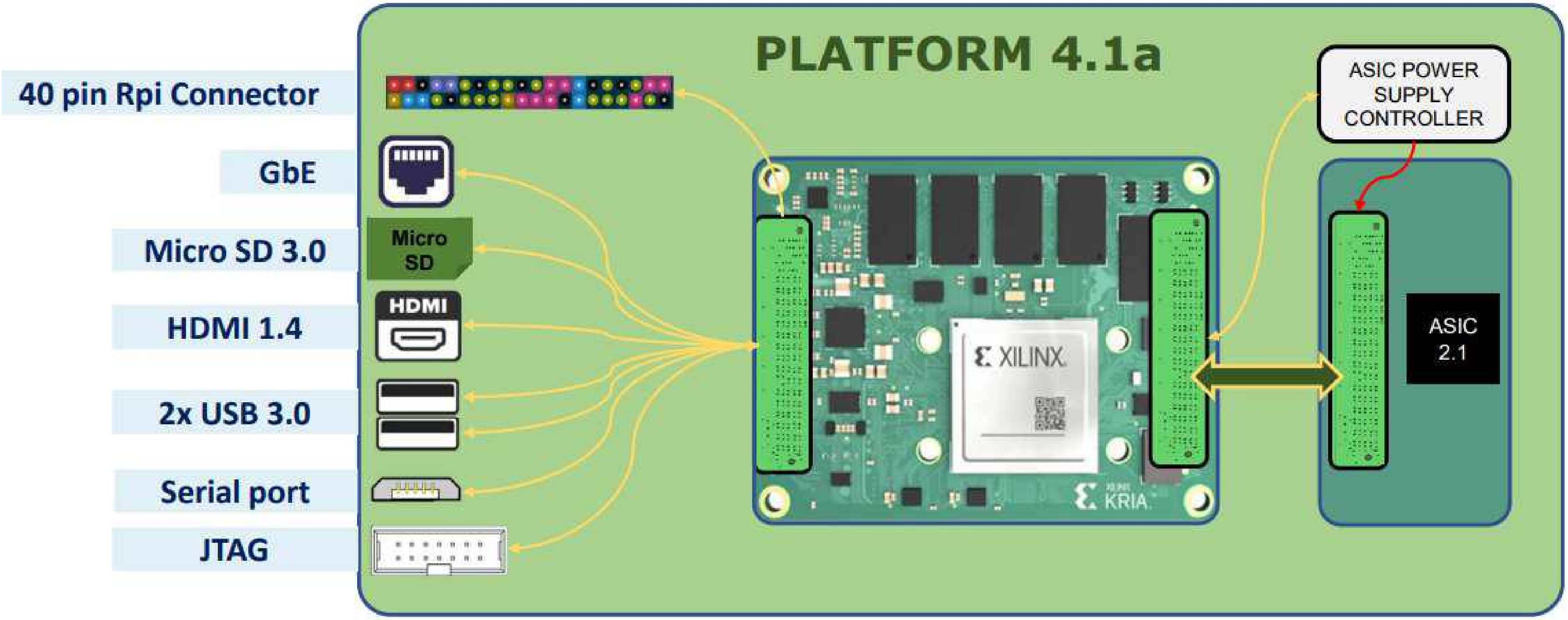
ASIC 3.2 aNN IMC

- **Target**: Analogue neuronal network (aNN) for tinyML applications. To be evaluated in the context color recognition.
- **Technology**: 28 nm HPC+ TSMC
- **Memory**: RRAM , < 20 kbytes
- **NN type**: aNN
- **Input throughput** : 128 x 7 bit
- **Throughput**: 3 inference/s min
- **Inference Latency** : 5 ms max
- **Accuracy** : 85% min
- **Expected efficiency** : < 1 GOPS/W
- **Expected power dissipation** : 1 mW max
- **Status** : Silicon available and validated.
- **Use cases:** UC1.2 color recognition

Block diagram of the Mixed signal aNN



Platform 4.1a : Multi-applications



Take-away

ANDANTE contribute to reach Green Deal Goals

- New **eNVMs** provide very efficient solutions
- Data Analysis at the **Edge** bring the intelligence close to data sources
- **ASICs, SoCs and FPGA HW** architectures (based on SNN, ANN) provide very efficient solutions
- Tools and Methodologies developed simplify the **HW/SW co-design**
- Cost effective and more **intelligent and autonomous CPS and IoT devices**

- Handling efficiently **data Analytics at the Edge**
- **Reduce power consumption, latency, data storage**
- **Increase the intelligence and autonomy of CPS and IoT Systems**

ANDANTE

AI for New Devices And Technologies at the Edge

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"This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement № 876925. The JU receives support from the European Union's Horizon 2020 research and innovation programme and France, Belgium, Germany, Netherlands, Portugal, Spain and Switzerland"

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Thank You