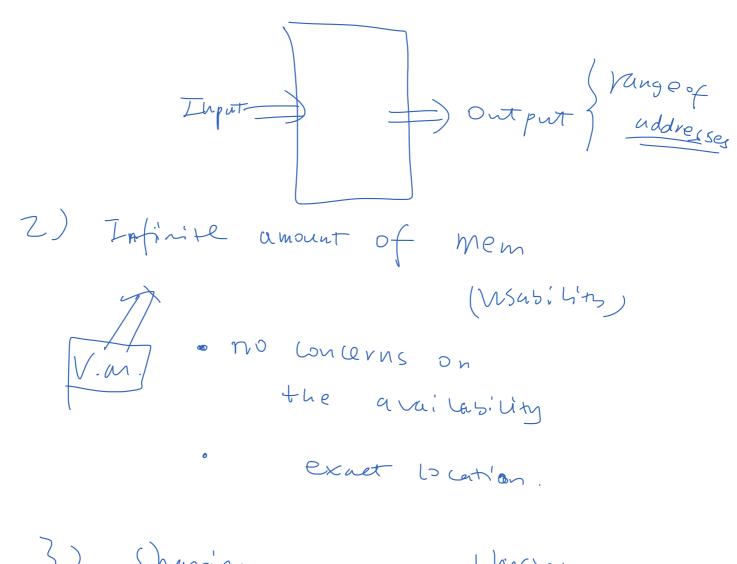
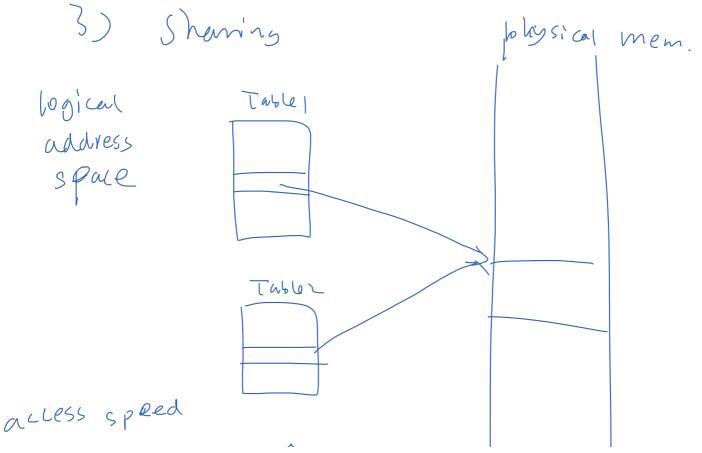
Thursday, November 15, 2018 1:05 PM Architective 4500 05 3640 men on / VM F--5 memory address space Translation map





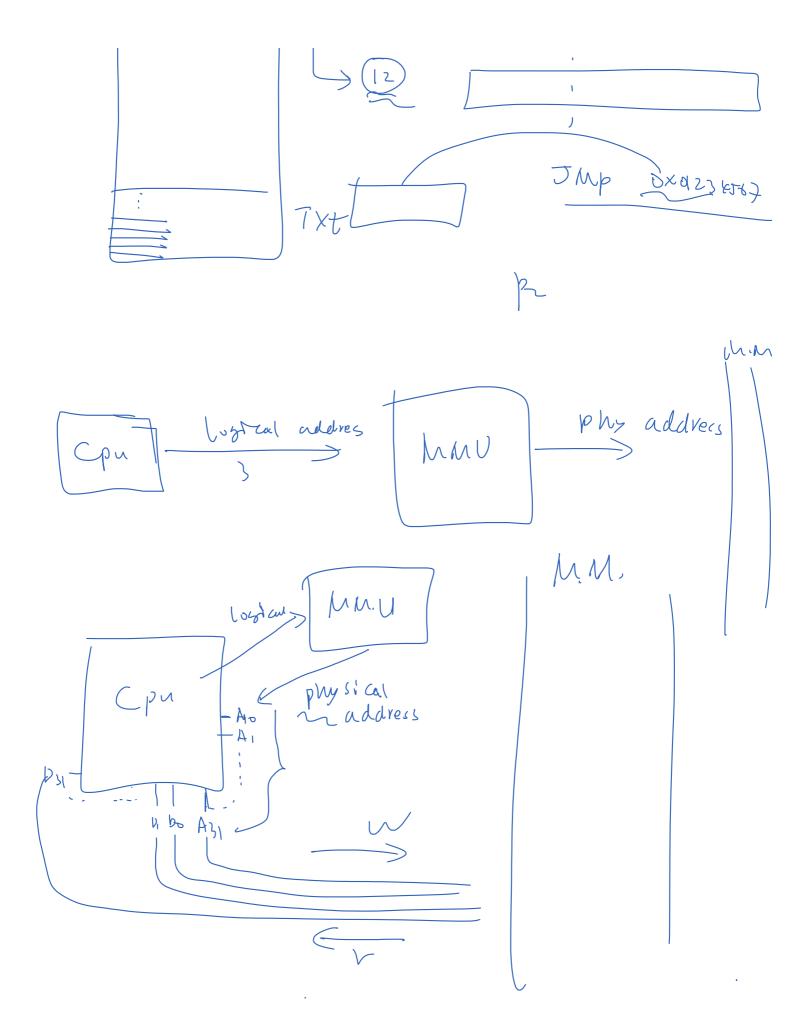
access speed registers CPU direct Cache access mem disk I/o Controller Tape Cupacity pu alless 1) Stored initially on 'disk' in the form of L'Us" groy rams

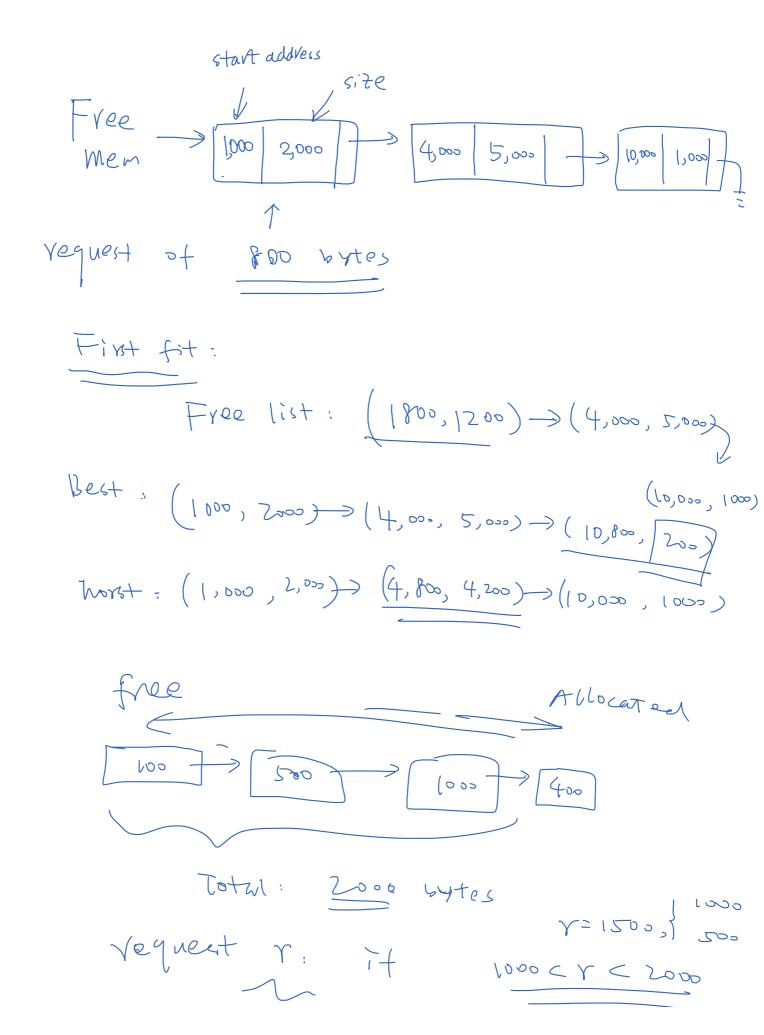
process

Tenstructions 2 derta louded mem address space

 $PC_1$   $P_1$   $PC_2$   $P_2$ 

	ISA	Pi	
	0	PUSH ESP	
	)		
		<b>\$</b>	
Po	210 - ZMARS!	ADD AX, BX	
	12	1	





1+

1000 CY < 2000

Courtiguous allocertion

Varions sites

 $\mathcal{T}$ 

1) remove the

Constrains

2) make sizes "equal"

S = N.P

 $\left[\frac{S}{p}\right] = N$ 

internal fuz weir

P=4KB

tragments on

Compaction

1220 (OSS 2

process 2

32413

h = 8

process 2 terminates

process 1 arrives,

Pi Cern use

the wen when pz just used page site 4KB in logscell address frame w/ equal site (4K15) in phy nem. phy sical Mem 1 GB 14B = 1K.1MB = 256K = 1K.1K.4KB 4kB = 1k. 256. 4. HAS 4KB pager Size 4005 physica mem in total there are K frames.

1115 Page 8

a proless site of 512 KB

then it has  $\frac{512 \text{kB}}{4 \text{kg}} = 128$  |2ages|

Contiguous Allocation

b) Maintains

Where in the phy mem, & From large
is allocated to which process

2) list of free partitions

(Start, Size)

DS will use
pase table

bit map to represent the

TII...

1 bit M O, or I

440 phy men w/ page rite

So we need

256 K bits

32K Bytes

page