RE: [ES-22] VHDL Project Request

Luca Fanucci <luca.fanucci@unipi.it>

gio 17/11/2022 14:48

A:Fabrizio Lanzillo <f.lanzillo@studenti.unipi.it>
Cc:Massimiliano Donati <massimiliano.donati@unipi.it>;Luca Zulberti <luca.zulberti@phd.unipi.it>

1 allegati (170 KB)
Calculation of FO Coefficient.pdf;

Dear Fabrizio,

please find herein attached the design assignment for the exam. If you have a doubt about the assignment and the way to develop the project please let me know

Please remember that BEFORE the exam schedule we have to discuss together the project.

To this aim you should:

1. Send to me by email the project report including the VHDL source code and any other program developed during the design & verification phases (MATLAB, PYTON, C, etc.) possible as a single compressed file (.rar, .zip)
2. Take an appointment with me for the project discussion

In the development of the project please take particular attention to the design verification including a proper test-plan with proper justification.

Very important would be also to synthesize the architecture to a Zync Xilinx FPGA according to the same design flow used in class (i.e. VIVADO tool). Please include in the report the synthesis report, i.e. device utilization (slice, LUT, etc.), maximum frequency and relevant critical path.

Please do not hesitate to contact me for any further clarification.

Good Luck.

Ciao, Luca Fanucci

From: Fabrizio Lanzillo <f.lanzillo@studenti.unipi.it>
Sent: mercoledì 16 novembre 2022 18:38
To: Luca Fanucci <luca.fanucci@unipi.it>
Cc: Massimiliano Donati <massimiliano.donati@unipi.it>; Luca Zulberti <luca.zulberti@phd.unipi.it>
Subject: [ES-22] VHDL Project Request

Name Surname: Fabrizio Lanzillo

Email: f.lanzillo@studenti.unipi.it

Mobile Phone: 3452424475

For one student.

Best Regards,