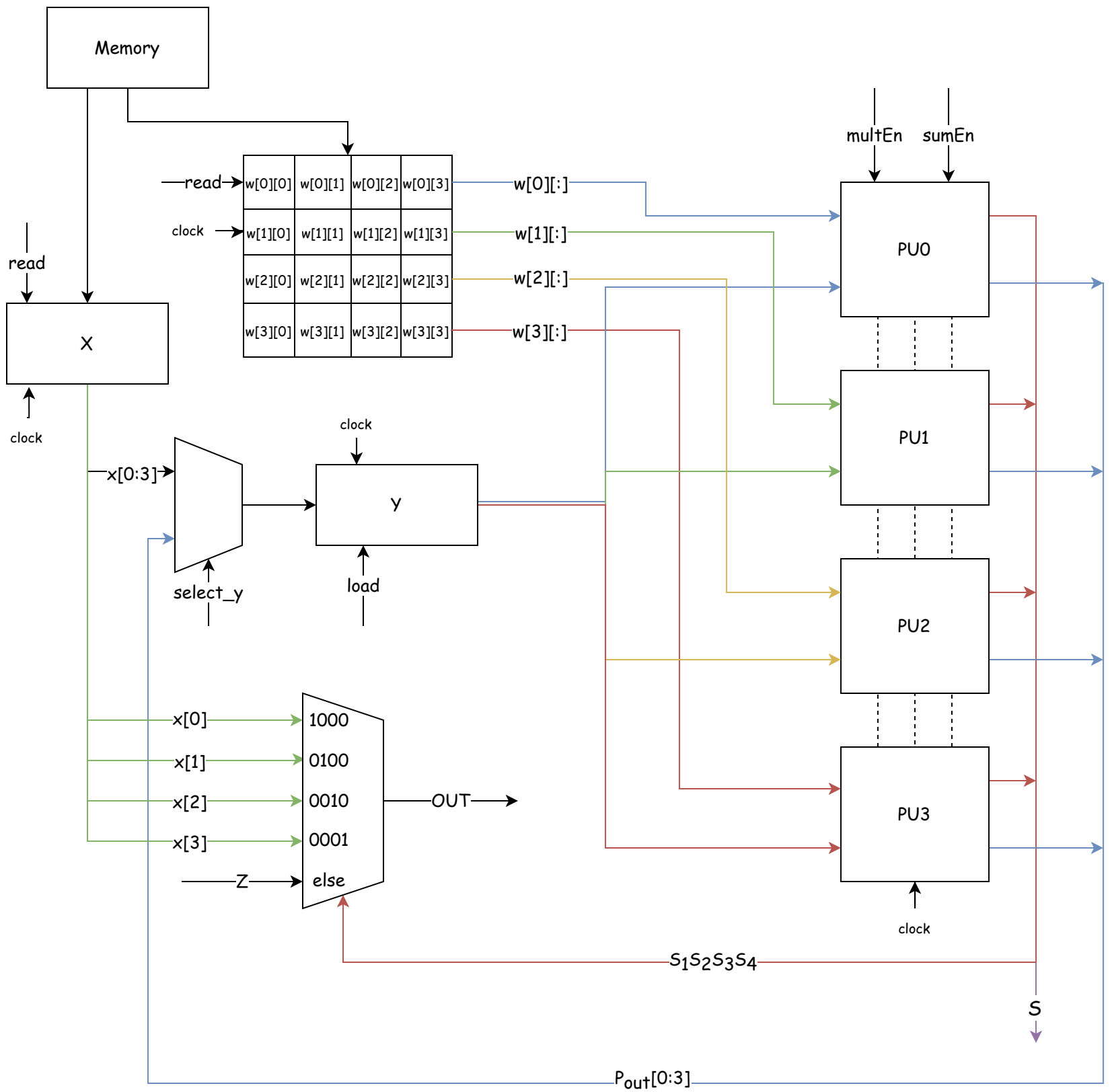- To make sure the output of a PU(process unit) is ready in proper time, we added 2 register and expand PU execution time to three clocks:

  1. Multiplication
  2. Adder tree
  3. Activation + Load

- An X register is added to have original value of neurons for whenever it be needed.

- Arithmetic operations will be performed using the Y register.

- Select of output MUX is a 4 bit one-hot.

- Output is maximum value of neurons.

  The datapath and controller diagrams can be found on the following pages:

Memory

read → w[0][0] | w[0][1] | w[0][2] | w[0][3] — w[0][:]
clock → w[1][0] | w[1][1] | w[1][2] | w[1][3] — w[1][:]
w[2][0] | w[2][1] | w[2][2] | w[2][3] — w[2][:]
w[3][0] | w[3][1] | w[3][2] | w[3][3] — w[3][:]

read

clock

X

x[0:3]

clock

select_y

load

y

multEn sumEn

PU0

PU1

PU2

PU3

clock

x[0] → 1000
x[1] → 0100
x[2] → 0010
x[3] → 0001
Z → else

OUT →

$S_1S_2S_3S_4$

S

$P_{out}[0:3]$

$S = S_1{\sim}S_2{\sim}S_3{\sim}S_4 + {\sim}S_1S_2{\sim}S_3{\sim}S_4 + {\sim}S_1{\sim}S_2S_3{\sim}S_4 + {\sim}S_1{\sim}S_2{\sim}S_3S_4$

PU$_i$

multEn

sumEn

W[0], X[0], W[1], X[1], W[2], X[2], W[3], X[3]

X

+

+

+

RelU

Out$_i$

S$_i$ = ~|Out

clock

clock

read = 1 → Read

load = 1
select_y = 0 → Init

multEn = 1 → Mult

sumEn = 1 → Sum

load = 1
select_y = 1 → Load

done = 1 → Done

s

~s