Experiment 1 – Clock and Periodic Signal Generation

Matin Bazrafshan, 810100093

Mohammad Amin Yousefi, 810100236

***Abstract*— This document is a report for experiment 1 of Digital Design Laboratory at ECE department at University of Tehran. The purpose of this experiment is to provide clocks with different methods.**

***Keywords*— Clock Generation, Ring Oscillator ,LM555, Schmitt Trigger Oscillator, Synchronous Counter, T Flip-Flop**

I. Introduction

In this experiment we will use different ICs to generate clock and periodic signals with different duty cycles.

II. Clock Generation Using ICs And Analog Components

A. Ring Oscillator

We are to measure propagation delay of a inverter, according to the fact which delay of a single inverter is too low to measure, we use 74HCT04 IC and wire up 5 series inverters.

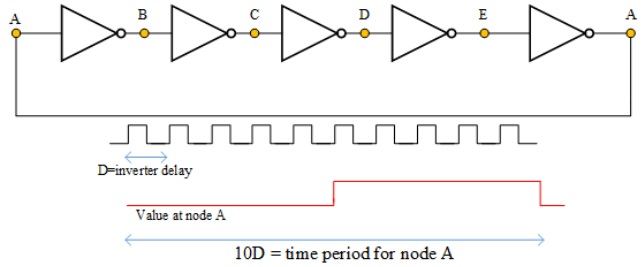

Fig. 1 schematic view of circuit

Every period of measured signal is delay to 0 and to 1 of all counters so it is equal to 2*N*$Delay_{inv}$

Fig. 2 inverter chain frequency

Note that we must use odd numbers of inverters, using even numbers of inverter result in a constant signal.
measured frequency = 11.44 MHz

$$T = \frac{1}{f} = \frac{1}{11.44 \times 10^6} = 87 \times 10^{-9}$$

$$N = 5 \rightarrow 2 \times 5 \times Delay_{inv} = 87 \times 10^{-9} = chain\ delay$$

$$\rightarrow Delay_{inv} = 8.7\ ns$$

B. LM555 timer

We are to generate clock signal using LM555 IC.

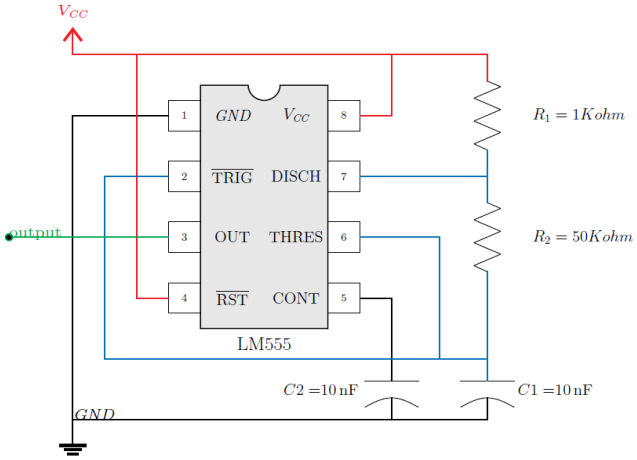

Fig. 3 schematic view of LM555 and wiring of circuit

As we can see, C1 is charged by VCC through R1 and R2 and produces output high, and is discharged by GND which gone through only R_2 and produces output low.

So Charging time $T_1 \propto (R_1 + R_2)$ meanwhile $T_2 \propto R_2$, duty cycle can be calculated by $\frac{R_1+R_2}{R_1+2R_2}$ so to have perfect 50% duty cycle, R_2 should be a high resistance according to the fact that R_1 is constant and equal to $1k\Omega$.

1) $R_2 = 1k\Omega$:
Clock frequency = 37.76 kHz
Measured duty cycle = 63.9%
Calculated duty cycle using equation = $\frac{1k+1k}{1k+2k} \approx 66\%$

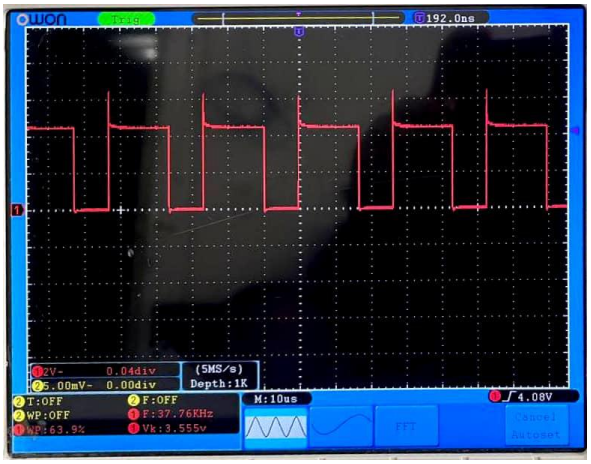

Fig. 4 output signal using $R_2 = 1k\Omega$

2) $R_2 = 10k\Omega$:

Clock frequency = 5.87 kHz
Measured duty cycle = 50.9%

Calculated duty cycle using equation = $\frac{1k+10k}{1k+20k} \approx 52\%$

Fig. 5 output signal using $R_2 = 10k\Omega$

3) $R_2 = 100k\Omega$:

Clock frequency = 625.9 Hz
Measured duty cycle = 50%

Calculated duty cycle using equation = $\frac{1k+100k}{1k+200k} \approx 50\%$

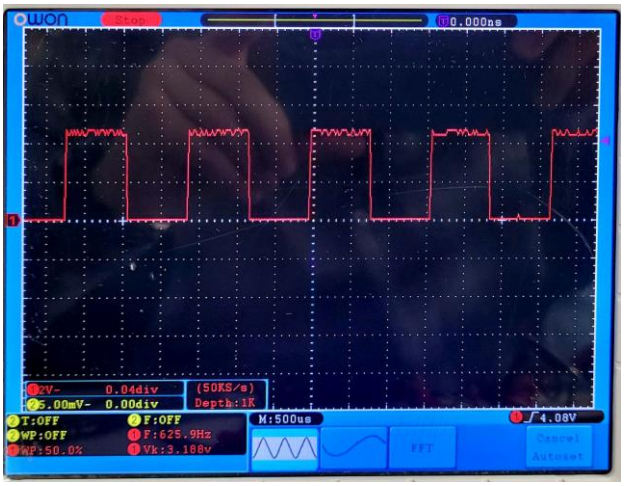

Fig. 6 output signal using $R_2 = 100k\Omega$

C. Schmitt Trigger Oscillator:

Using 74HCT14 IC we wire up a circuit as it is shown in Fig.7

In Schmitt trigger we have $f = \frac{\alpha}{RC}$, α is unknown so we use different resistance to find out α.

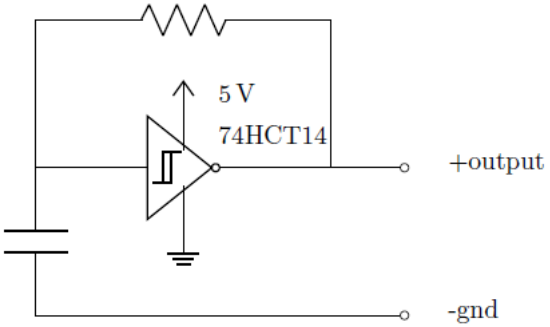

Fig. 7 view of a Schmitt trigger oscillator

Note that capacitance is 10 nF.

1) $R = 470\Omega$:

$f = 146.8\ kHz \rightarrow \alpha = 0.689$

Fig. 8 output signal using $R = 470\Omega$

2) $R = 1000\Omega$:

$f = 69.44\,kHz \rightarrow \alpha = 0.694$

Fig. 9 output signal using $R = 1000\Omega$

3) $R = 2200$:

$f = 27.55kHz \rightarrow \alpha = 0.606$

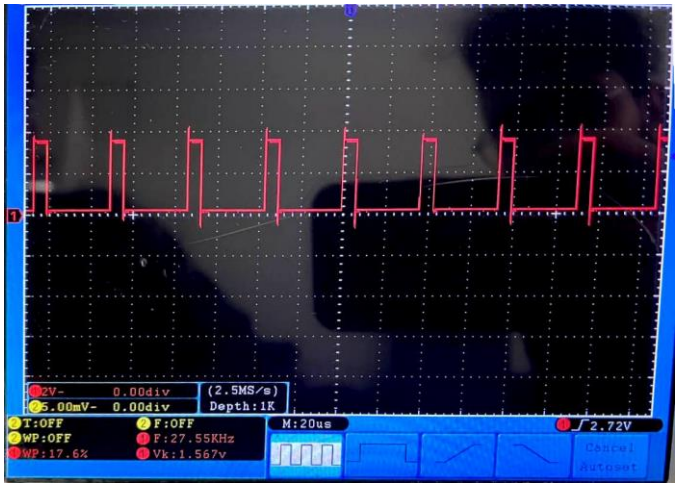

Fig. 10 output signal using $R = 2200\Omega$

D. *Synchronous Counter as a Frequency Divider*

We can generate a low frequency clock but it has a 1-2% timing error which is a great number in low frequencies, instead we can use a higher frequency and use a counter to divide and reduce frequency.

As we shown in Fig. 1, we used ring oscillator to make a high frequency signal.

To divide frequency by 200 we use a 8-bit counter which counts up to 256 and a parallel load 56 so the counter should count 256 – 56 = 200.

The output signal frequency is 58.74 KHz while we know the input signal is 11.53 MHz (Ring Oscillator output signal, measured in second session of Lab)

$\rightarrow 11.53 \times 10^6 \div 200 = 57.65 \times 10^3 = 57.65\,KHz$

So the measured frequency is almost same with calculated one. (minor differences caused by wiring.)

Fig. 11 output signal of counter

E. T Flip-Flop

In previous part we divide a high frequency with a counter but it does not have a 50% duty cycle(98.8%), because we measured carry out of counter which becomes 1 every 200 cycle.

To have a 50% duty cycle signal we can use a T flip-flop which divide signal by 2 and makes it a 50% duty cycle

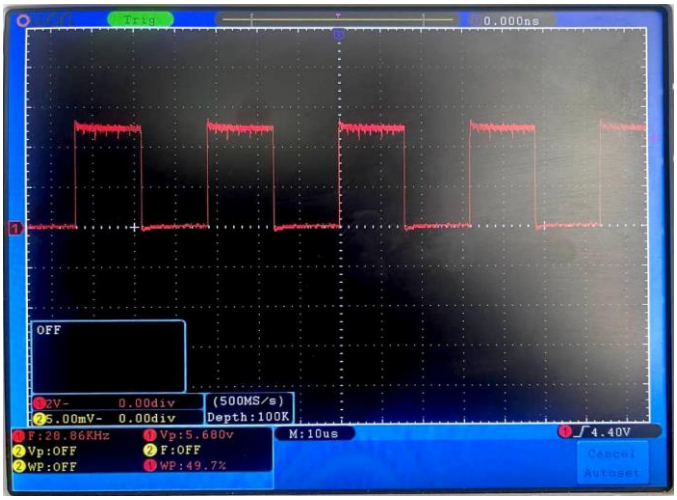

Fig. 12 output signal of T Flip-Flop

Output signal frequency = 28.86 KHz

$\rightarrow 57.65 \div 2 = 28.82\,KHz$ which is same as measured.

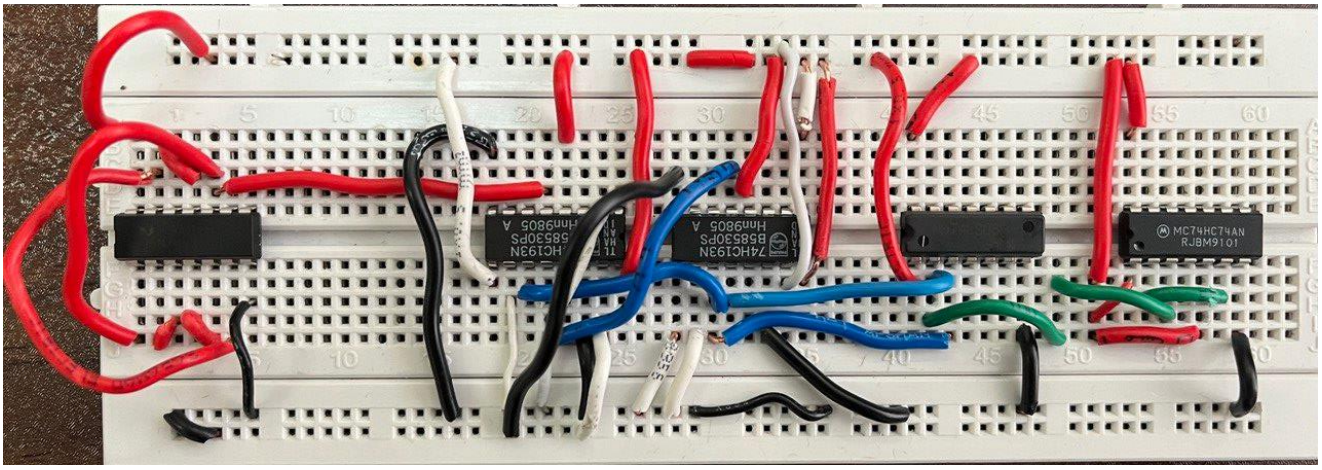

Fig. 13 Final circuit of part E