

وَمَا أُوتِيتُهُ مِنَ الْعِلْمِ إِلَّا قَلِيلٌ

Analog IC Design

Lecture 04 MOSFET Large Signal Model

Dr. Hesham A. Omran

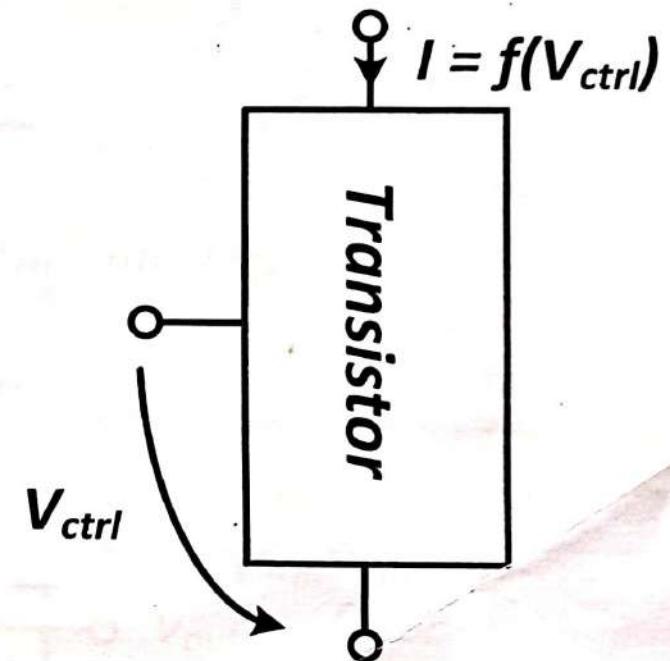
Integrated Circuits Lab (ICL)
Electronics and Communications Eng. Dept.
Faculty of Engineering
Ain Shams University

Outline

- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

Why is the Transistor Different?

- We are used to two-terminal devices
 - Resistors, capacitors, inductors, diodes
- The transistor is a three-terminal device
 - The voltage between two terminals **controls** the current flowing in the third terminal
 - Voltage controlled current source (VCCS)
- This feature enabled a multitude of applications that changed our life!
 - Analog signal amplification and processing
 - Digital logic and memory circuits



VCCS as an Amplifier

- Voltage controlled current source (VCCS): v_{in} controls $i_{out} = ? v_{in}$

★ Conductance as it is $\frac{i}{v}$
 and trans. as it transfer the
 effect from the input Port to the output Port

★ The most important Parameter
 for the transistor.

Transconductance $= \frac{i_{out}}{v_{in}} = G_m$

Current depends on the Volt

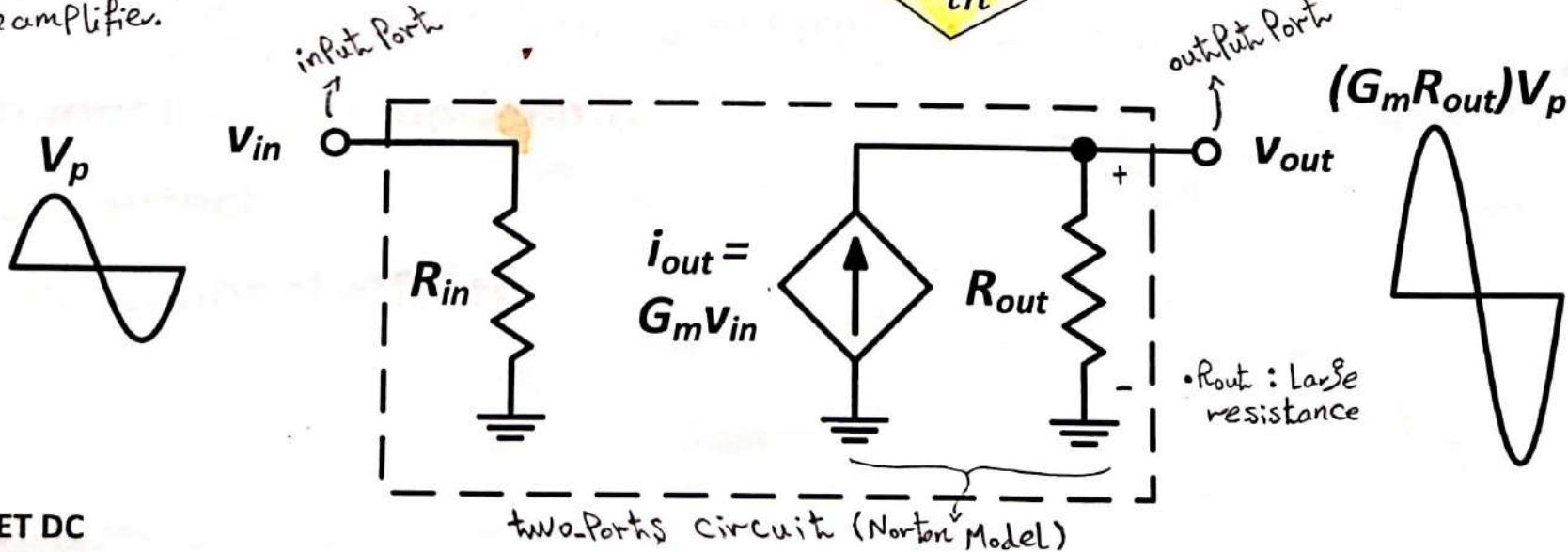
ex: $v_{in} = V_p \sin(\omega t)$

$$v_{out} = G_m v_{in} \times R_{out} = (G_m R_{out}) v_{in} = (G_m R_{out}) V_p \sin(\omega t)$$

★ the new amplitude is:
 $(G_m \cdot R_{out} \cdot V_p)$ instead of
 (V_p) before the amplifier.

Voltage Gain $= A_v = \frac{v_{out}}{v_{in}} = G_m R_{out}$

transconductance * output resistance



Outline

- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

MOSFET

- MOSFET: Metal-oxide-semiconductor field-effect transistor
 - N-channel MOSFET: NMOS → depends on 'N' i.e. electrons
 - P-channel MOSFET: PMOS → depends on 'P' i.e. holes
 - Complementary MOS (CMOS) technology: NMOS + PMOS
- A.k.a. insulated-gate FET or IGFET
- Simply, a VCCS
- The concept of MOSFET was patented in 1925 "Before BJT"
*(But without physical realization
(No implementation))*
- But it was not successfully fabricated till 1960s → in Bell labs (Egyptian + Korean)
Mohamed M. Atalla *Dawon Kahng*
- CMOS technology became the dominant IC fabrication technology by the 1980s
*Due to its ability to implement digital circuits
with very low static power consumption*

N-Channel MOSFET Structure

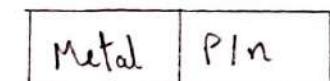
- MOSFET: Metal-oxide-semiconductor field-effect transistor
- Three-terminal device: Gate (G), Source (S), and Drain (D)
- Substrate/Bulk/Body (S/B) can be treated as a fourth terminal

* MOSFET is symmetric device
So what says which terminal is source and which is drain
is the applied voltage.

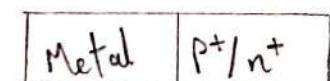
* Extra from digital course



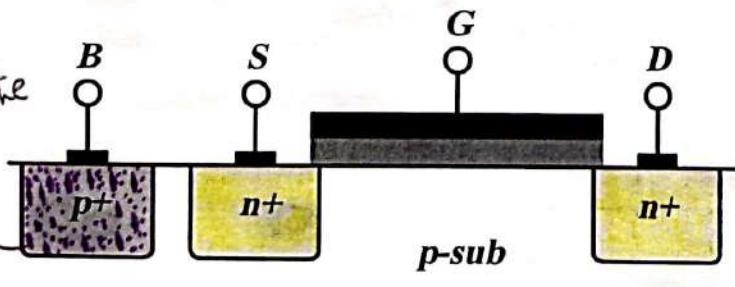
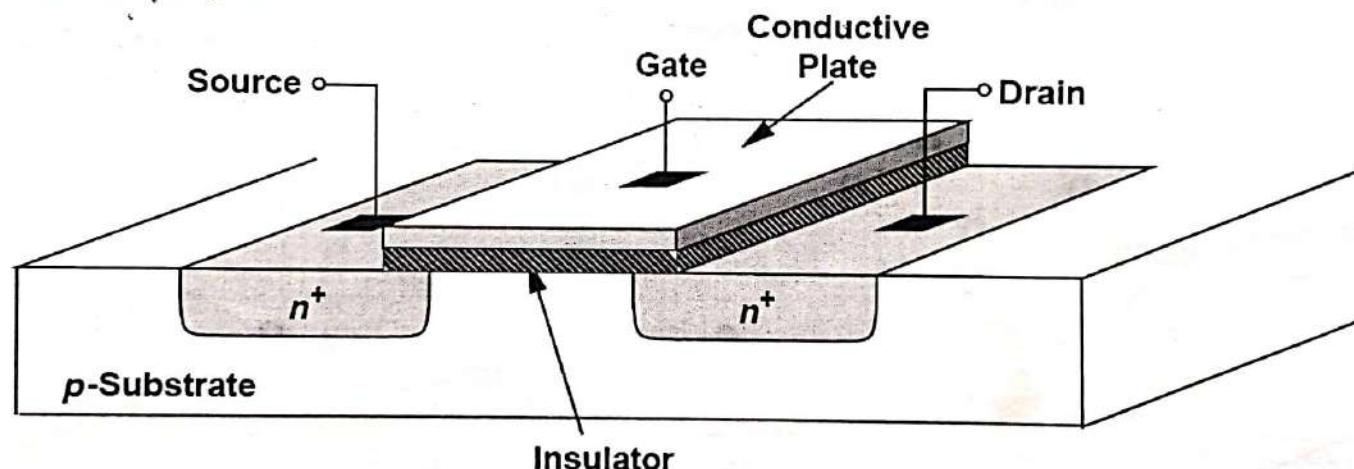
Pn Junction



Schottky Diode



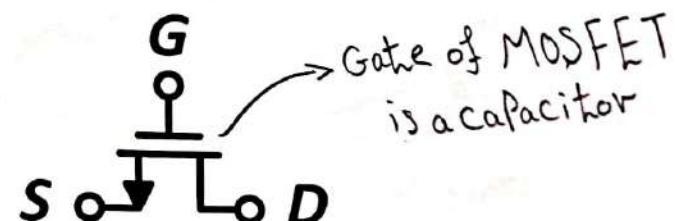
Low resistance ohmic contact.



* When contact substrate it must be P⁺ to be an "Ohmic Contact" otherwise it will be a "Schottky Diode"

04: MOSFET DC

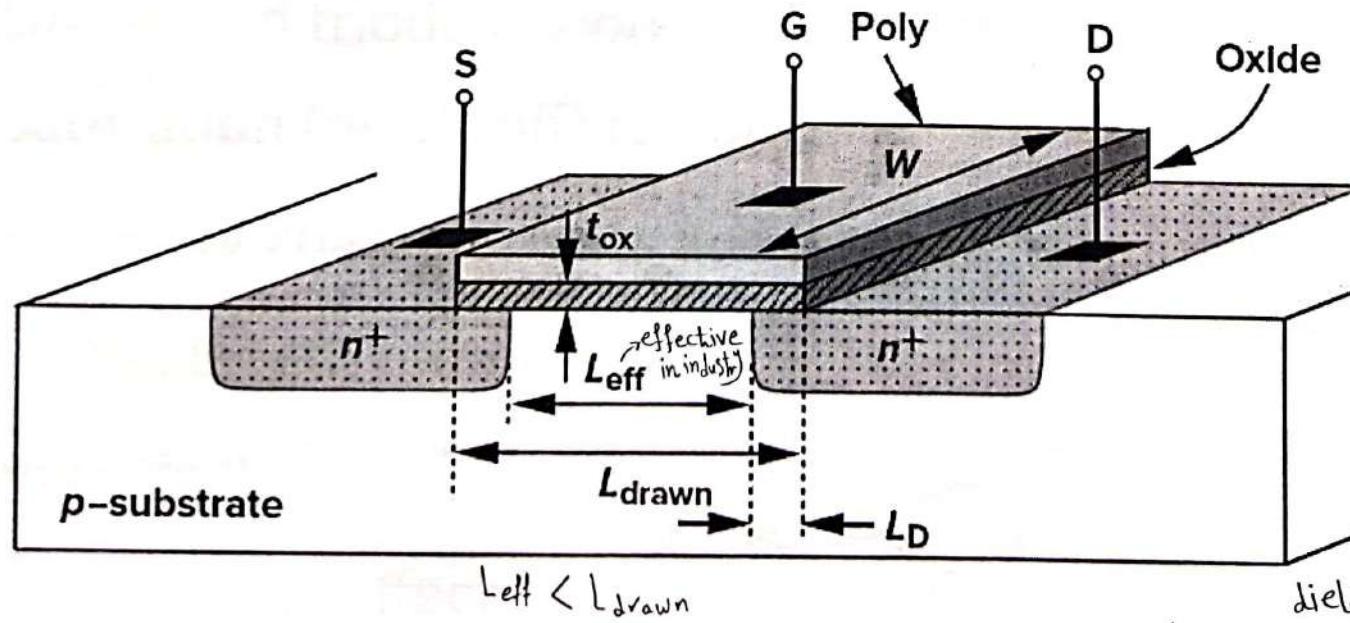
allows current to pass only in one direction which will damage the operation of the MOSFET.



→ leads the Scaling down
and Effects the development
of the field.

MOSFET Dimensions

- Channel length: $L \sim 10\text{nm} - 10\mu\text{m}$
 - The distance between the source & the drain.
 - These are lateral dimensions
 - Designers specify these dimensions
- Channel width: $W \sim 50\text{nm} - 100\mu\text{m}$
- Oxide thickness: $t_{ox} \sim 1\text{nm} - 10\text{nm}$
 - few atoms
 - the smallest dimension in the chip
 - Vertical dimension
 - Process engineers specify these dimensions.
- Gate formed of metal or polysilicon



MOS

* there were
problems in manufacturing
metal with oxide so it then
replaced by "Poly Silicon"

it is a semiconductor so
it is highly doped to
decrease its resistance
and to act as a metal.

* They after this replace
the oxide layer with High-K

dielectric materials then problems occur
between Poly Silicon and High K so, they return back

* High-K materials have high Permittivity
[Razavi, 2017] 9
to Metals.

Outline

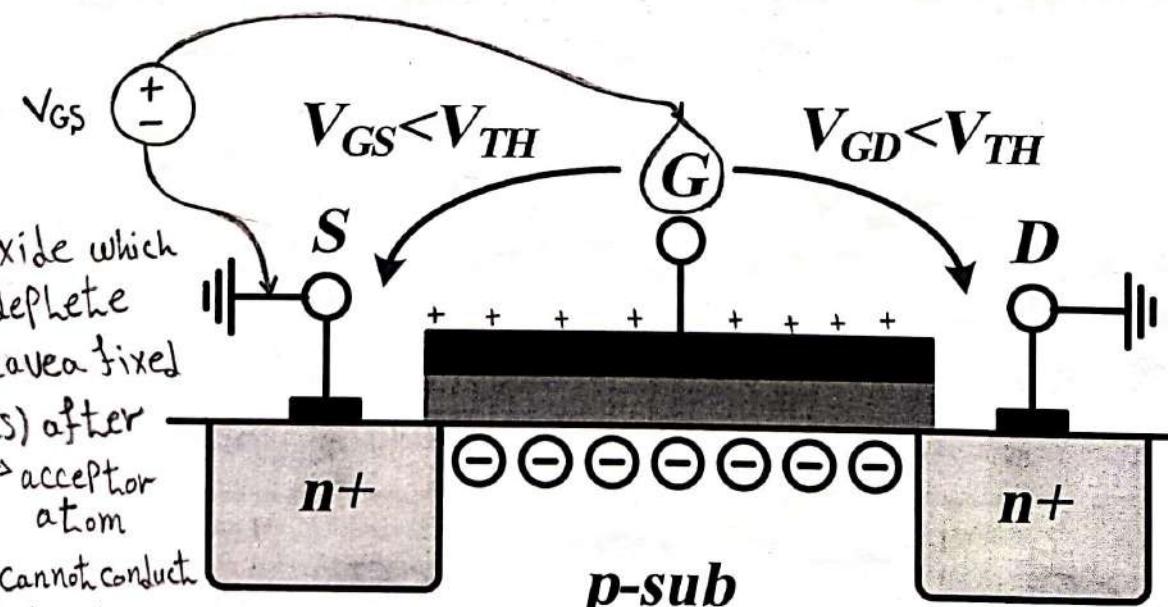
- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

Depletion

- The device acts as a capacitor: positive charge on the gate is mirrored by negative charge in the substrate
- The positive charge on the gate repels the holes in the substrate
 - Fixed negative ions are exposed (uncovered)
 - A depletion region is created

* for a capacitor:
the Positive charges on  on one side should equalize the negative charges on the other plate,

So the area under the oxide which is the substrate will deplete the holes. The holes leave a fixed negative charges (ions) after depletion process.



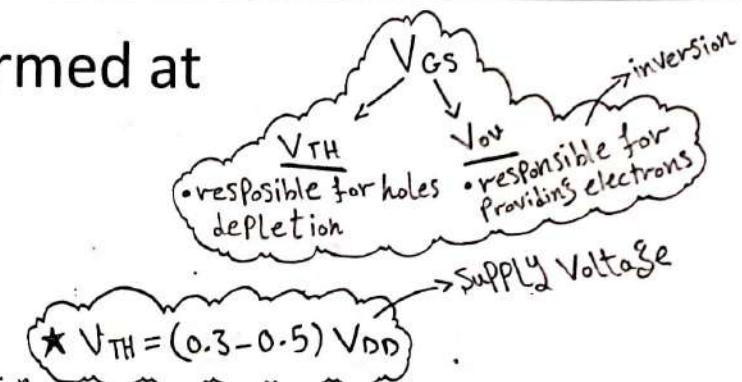
* The fixed negative ions cannot conduct current as they are bonded by a covalent bond with the crystal. So it forms a "Depletion Region" (no current region)

Inversion and Channel Formation

- N-type channel region (inversion layer) formed at

$$V_{GS} > V_{TH}$$

$$V_{GS} = V_{TH} + V_{ov}$$

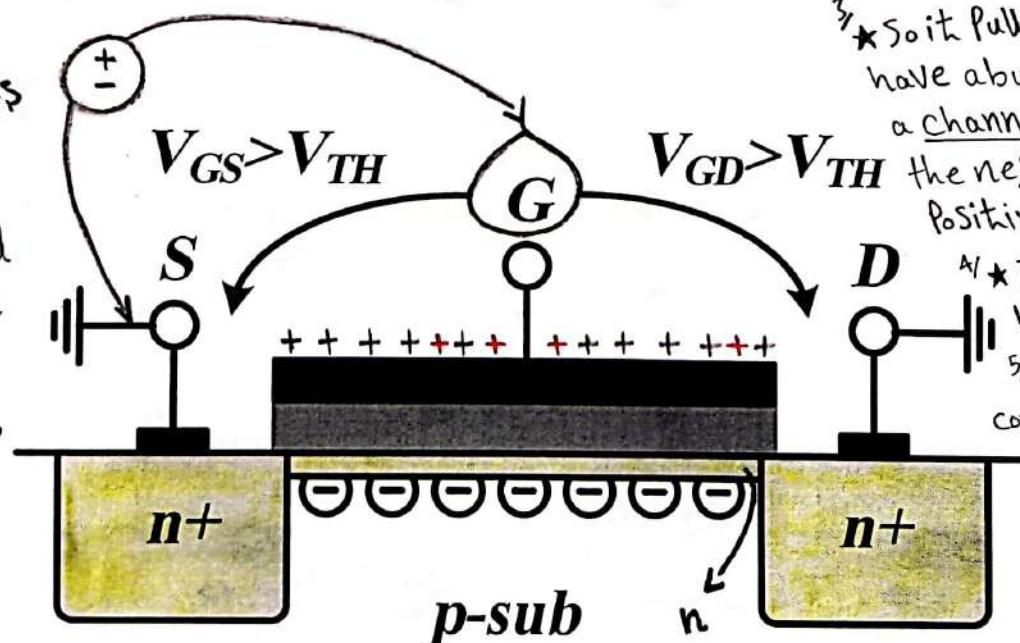


- Threshold voltage: $V_{TH} \sim 0.3V - 1V$
- Overdrive voltage: $V_{ov} \sim 0V - 0.5V$ (for analog circuits)
- Electrons are provided by the n+ source and drain regions

• One of the most important Parameters (Design Parameters) in Analog circuits.

1 ★ By increasing V_{GS} charges on the top plate increase as: $T \uparrow G = C V \uparrow$

2 ★ after depleting (repelling) all the holes in the substrate, the substrate looks for another source for negative charges to balance the increasing positive charges on the metal layer.



3 ★ So it pulls them from the n+ regions which have abundance of electrons, forming a channel or an inversion layer which helps the negative fixed charges to balance the positive charges on top Plate of capacitor

4 ★ Inversion layer: as it inverts the region beneath the oxide from P-type into N-type.

5 ★ Channel formation: as there is n which contains free carriers capable of conducting current between Source & Drain.

Charge in Channel

$$C_{gate} = \frac{\epsilon_{ox} A}{d} = \frac{(\epsilon_{ox})WL}{t_{ox}} = C_{ox}WL$$

↑ Permittivity
↑ relative Permittivity
↑ free Space Permittivity
↑ capacitance Per unit Area.

- For SiO_2

$$\epsilon_{ox} = \epsilon_r \epsilon_0 = 3.9 \times 8.854 \times 10^{-12} \frac{F}{m}$$

- Example: if $t_{ox} = 4nm \rightarrow C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \approx 8.6 \frac{fF}{\mu m^2}$ *if: $WL = 1 \mu m^2$
 $\therefore C_{ox} = 8.6 fF \xrightarrow{10^{-15}}$

$$|Q| = CV = C_{ox}WL \cdot (V_{GS} - V_{TH}) = (C_{ox}WL \cdot V_{ov}) \rightarrow \text{charges responsible for current conduction.}$$

??

$$\star V_{GS} = V_{TH} + V_{ov}$$

↓
Produces fixed charges

effective Voltage "V_{eff}"

- Produces the channel
- Produces the free carriers

Linear Region (Deep Triode)

- Small V_{DS} : We assume the channel is uniform
- MOSFET acts as a voltage controlled resistor (VCR)
 - Vertical field (V_{GS}) controls the channel depth (resistance value)
 - Lateral field (V_{DS}) controls the carrier acceleration (drift current)

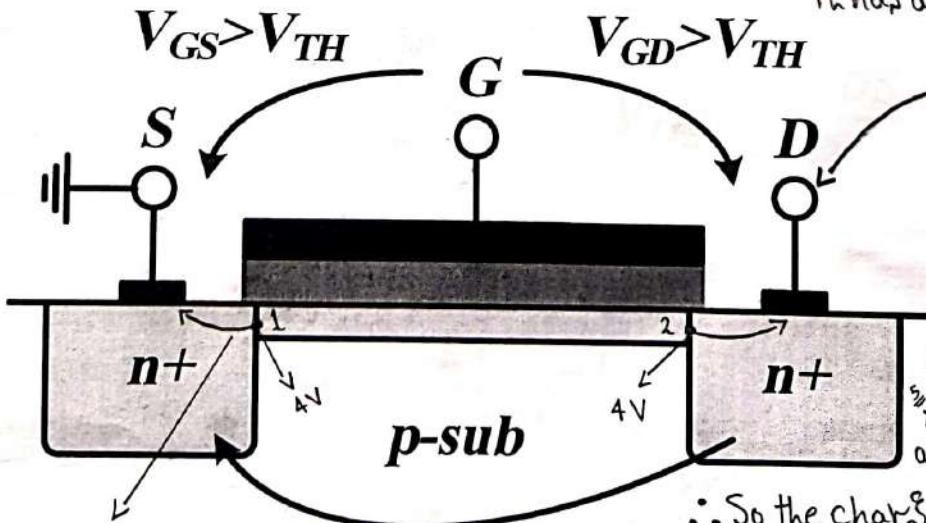
* actually the MOSFET won't be "VCCS"
 → it will be "VCR" instead
 ↳ we can control the resistance of the channel
 By controlling the charges with the gate voltage.
 ↳ so by increasing the gate voltage it provides more charges and decreases the channel R.

$$N_{GS} \propto \frac{1}{R_{DS}}$$

* to produce a current we need:
 1- free carriers
 2- electric field → (voltage difference)

* so we should connect a voltage to the Drain (not the Ground) to produce electric field (lateral).

(25) V_{GS} passes the ball to the channel then V_{DS} shoots the ball to move in the channel.
 * The ball is the free carriers.

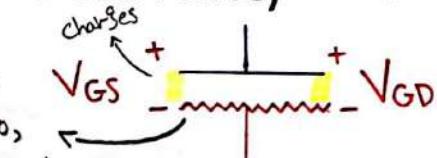


Small V_{DS}

* we can assume a short circuit between the channel and the Source, and the other side also between the channel and the Drain

n^+ : means very high doping so, we can ignore its resistance.

* Bottom Plate is a semiconductor so, it has a resistivity \gg top plate (metal) "conductors"
 ↳ charges + - + - + - + -



* there is a strange thing!
 ↳ the voltage difference on the left side of the capacitor may differ from the voltage difference on the right side of the capacitor, as the left side is "VGS", and the right side is "VGD".

* are V_{GS} and V_{GD} equal? No it isn't a rule as source is not always equal the drain. a must

∴ so the charges beside the source may differ from the charges beside the drain. AS: $Q = CV$

* if for ex: $V_{TH} = 1V$, $V_{GS} = 5V$, so the voltage at point 1 will be 4V
 so if we supply a small volt \approx zero → ∴ the voltage at 2 will also be 4V
 ↳ so the channel will be uniform: the charges at its sides are equal

* the important property of "linear region" 14 quantity

Linear Region (Deep Triode)

* We are concerned with the charges that contributes in current conduction so, we use the overdrive voltage.

$$|Q| = CV = C_{ox}WL \cdot (V_{GS} - V_{TH}) = C_{ox}WL \cdot V_{ov}$$

$$\text{Electric Field} = |E| = \frac{V_{DS}}{L}$$

will cause Drift current
(Drift velocity)

$$E = \frac{\text{Volt}}{\text{distance}}$$

$$\text{Carrier Velocity} = |v| = \mu_n |E| = \mu_n \frac{V_{DS}}{L}$$

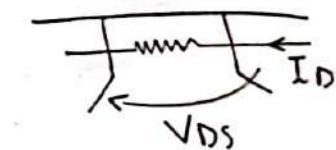
• current is the rate of flow of charges

$$\text{Drain Current} = I_D = \frac{Q}{t} = C_{ox}W \left(\frac{L}{t} \right) \cdot V_{ov} = C_{ox}W \cdot v \cdot V_{ov}$$

$\frac{1}{R_{DS}} = \frac{W}{\mu_n C_{ox} \frac{V_{ov}}{L} \cdot V_{DS}}$

$$I_D = (\mu_n C_{ox} \frac{W}{L} \cdot V_{ov}) \cdot V_{DS} = \frac{V_{DS}}{R_{DS}}$$

Ohm's Law



$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \cdot V_{ov}} = \frac{1}{k'_n \frac{W}{L} V_{ov}} = \frac{1}{k_n V_{ov}} = \frac{1}{\beta_n V_{ov}}$$

$$\therefore R_{DS} \propto \frac{1}{V_{ov}}$$

$$\therefore R_{DS} \propto \frac{1}{V_{GS}}$$

∴ VCR

04: MOSFET DC

* Some references

$$\cdot \frac{W}{L} = k'_n$$

$$\cdot \mu_n C_{ox} \frac{W}{L} = k_n = \beta_n$$

$$\text{Aspect Ratio} = \frac{W}{L}$$

ex. $\frac{4}{0.5} = 8$

it is deliberately to know "L" as it is an important parameter affects the behavior of the MOSFET, so, Don't Simplify

Linear Region (Deep Triode)

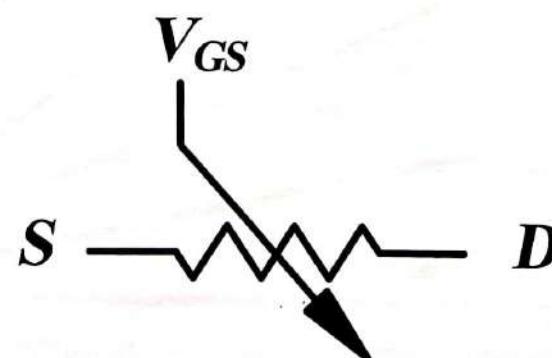
* Linear: as the current is proportional to V_{DS} (linearly).

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot V_{ov} \cdot V_{DS} = \frac{V_{DS}}{R_{DS}}$$

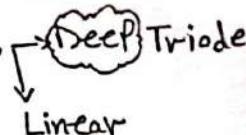
$$I_D \propto V_{DS}, \text{slope} = \mu_n C_{ox} \frac{W}{L} V_{ov}$$

$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \cdot V_{ov}} = \frac{1}{k'_n \frac{W}{L} V_{ov}} = \frac{1}{k_n V_{ov}} = \frac{1}{\beta_n V_{ov}}$$

$$\text{Aspect Ratio} = \frac{W}{L}$$



Linear Region (Deep Triode)

Small V_{DS} 
Deep Triode
Linear

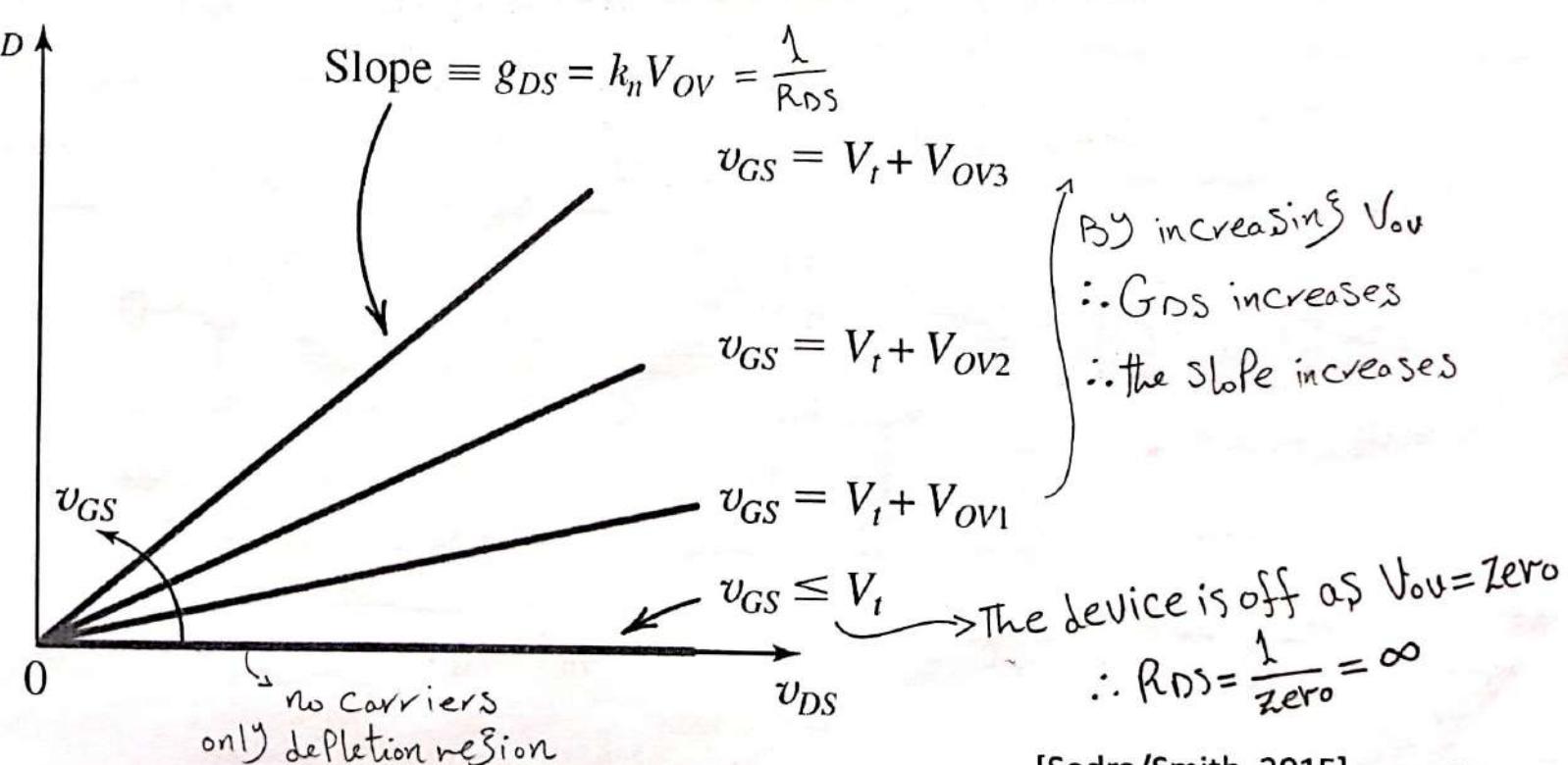
- MOSFET acts as a voltage controlled resistor (VCR)

$$R_{DS} = \frac{1}{G_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \cdot V_{ov}} = \frac{1}{k'_n \frac{W}{L} V_{ov}} = \frac{1}{k_n V_{ov}} = \frac{1}{\beta_n V_{ov}}$$

- Linear characteristics

* all this is based on the assumption that ' V_{DS} ' is small so, the MOSFET is in the "Deep triode/Linear" region. What if we increase the V_{DS} ?

- The MOSFET will enter the "Triode region"



Triode Region

□ V_{DS} increases: The channel becomes tapered

□ Voltage at source side: $V_{GS} - 0 = V_{GS} = V_{TH} + V_{ov}$

- If $V_{GS} > V_{TH}$ or $V_{ov} > 0$: The channel exists at source

□ Voltage at drain side: $V_{GS} - V_{DS} = V_{GD} = V_{TH} + (V_{ov} - V_{DS})$

- If $V_{GD} > V_{TH}$ or $V_{DS} < V_{ov}$: The channel exists at drain

• Assume:

$$\rightarrow V_{th} = 1V$$

$$\rightarrow V_{GS} = 5V$$

$$\therefore V_{ov} = 4V$$

$$\rightarrow V_{DS} = 1V$$

$$\therefore V_{GD} = 4V$$

$$V_G - V_D$$

$$\stackrel{5-1}{\therefore} V_{GS} > V_{TH}$$

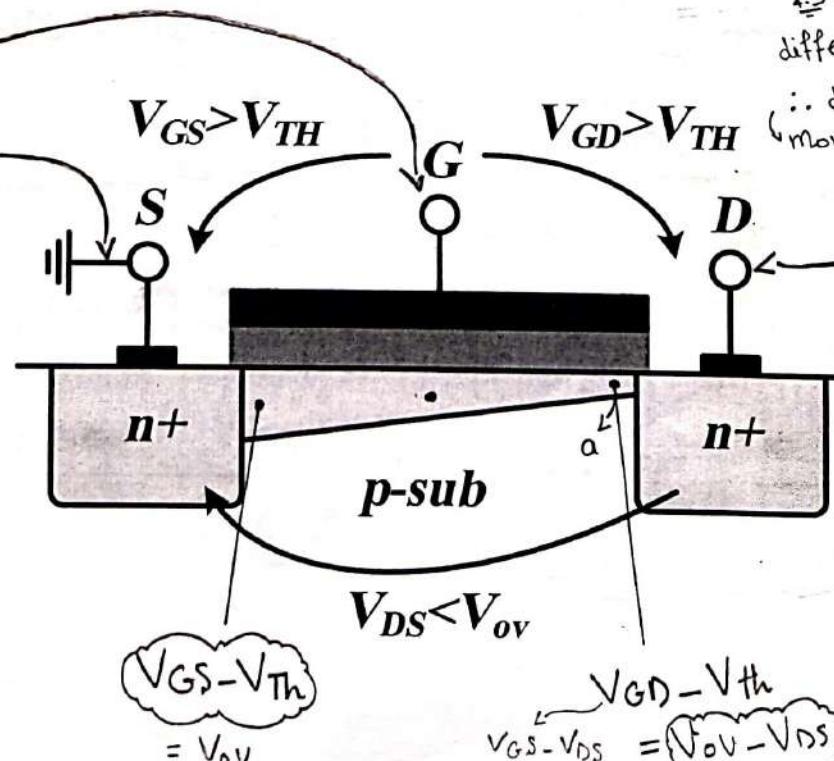
triode condition

$$\because V_{GD} > V_{th}$$

$$\therefore V_{GS} - V_{DS} > V_{th}$$

$$\therefore V_{DS} < V_{GS} - V_{th}$$

triode condition



\therefore different voltage differences @ each side

\therefore different 'Q' at each side.

(more 'Q' @ source as more voltage) $\therefore Q = CV$

\therefore BY increasing the Drain Voltage

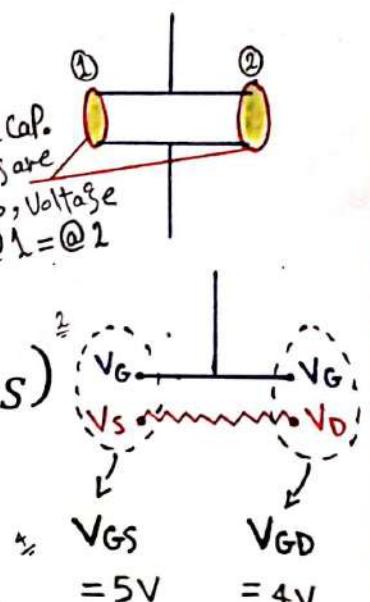
\therefore the depth @ Point 'a' decreases.

\therefore the channel will take a "tapered" shape

\therefore the region is triode

\therefore There is a channel @ the drain only if: $V_{GD} > V_{TH}$

$$\therefore V_{GS} - V_{DS} > V_{TH}$$



Triode Region

- V_{DS} increases: The channel becomes tapered
- Voltage at source side: $V_{GS} - 0 = V_{GS} = V_{TH} + V_{ov}$
 - If $V_{GS} > V_{TH}$ or $V_{ov} > 0$: The channel exists at source
- Voltage at drain side: $V_{GS} - V_{DS} = V_{GD} = V_{TH} + (V_{ov} - V_{DS})$
 - If $V_{GD} > V_{TH}$ or $V_{DS} < V_{ov}$: The channel exists at drain

* The channel is not uniform so, we cannot calculate the charge from the overdrive voltage
 we should calculate the average charge to find the current so, we will take the average overdrive voltages @ the channel.

★ Average overdrive voltage:

²
 • Average: of the channel isn't uniform "triode: tapered shape"

$$(V_{ov})_{average} = \frac{V_{ov} + (V_{ov} - V_{DS})}{2} = V_{ov} - \frac{V_{DS}}{2}$$

- Replace V_{ov} with $(V_{ov})_{average}$ → in the previous current equation (derived in Linear region)

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \underbrace{\left(V_{ov} - \frac{V_{DS}}{2} \right)}_{\text{Average overdrive Voltage}} \cdot V_{DS} = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

3. $V_{DS} (V_{ov} - \frac{V_{DS}}{2})$ ^{quadratic "not linear"} _{or V_{DS} was very small.}

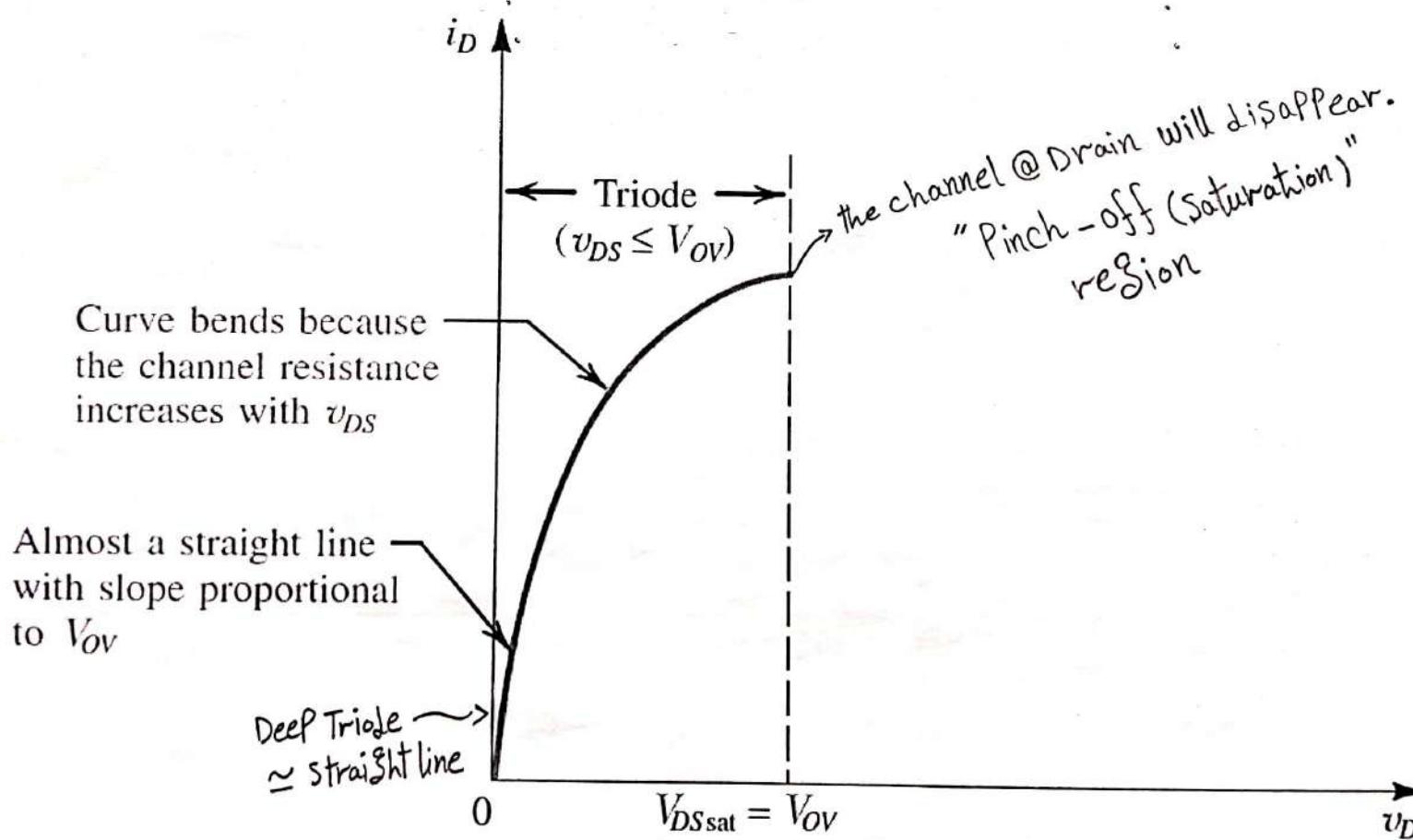
* We neglect $\frac{V_{DS}}{2}$ as: $\rightarrow V_{ov} \gg \frac{V_{DS}}{2}$ in Depletion

Triode Region

□ Inverted parabola

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

inverted Parabola $\sim -x^2/2$



Pinch-Off (Saturation)

*Most important region:
as here the MOSFET is VCCS.

- $V_{GD} = V_{GS} - V_{DS} \leq V_{TH} \rightarrow V_{DS} \geq V_{GS} - V_{TH} = V_{ov}$
- No channel at drain side
- V_{DS} has no more control on the shape and charge of the channel

$\frac{5.25}{\text{square}} \quad \text{Average overdrive voltage: } (V_{ov})_{\text{average}} = \frac{V_{ov} + 0}{2} = \frac{V_{ov}}{2} \neq f(V_{DS})$

- $\frac{5.3}{\text{square}}$ $\quad \text{Voltage across channel is constant} = V_{GS} - V_{TH} = V_{ov} \neq f(V_{DS})$
- Extra V_{DS} falls on the small region between channel and drain

Phenomenon occurs when $V_{GD} = V_{TH}$

"The current will saturate i.e. will be const."

ex. $V_{GS} = 5V, V_{TH} = 1V \rightarrow$ when increase V_{DS} until

$4V \rightarrow V_{GD} = 5 - 4 = 1 = V_{TH}$ (Pinch off)

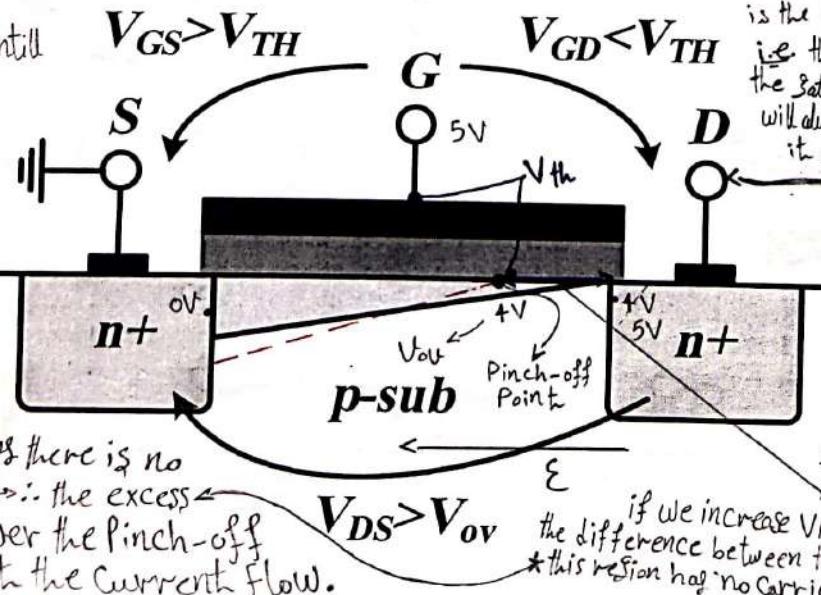
if we increase V_{DS} to 5V (exceed the Pinch off)

$\frac{5.4}{\text{square}}$ $V_{GD} < V_{TH}$

*The voltage across the channel will always be const.
 $\rightarrow I_D$ will be constant. (VCCS) $= V_{ov}$

$\frac{5.5}{\text{square}}$ By increasing the voltage over the Pinch-off Volt the Pinch-off Point will be shifted towards the Source.

04: MOSFET DC



$\frac{5.5}{\text{square}}$ Pinch-off Point by definition is the point @ which the channel disappears i.e. the voltage difference between the Gate and the Pinch-off Point will always be V_{TH} wherever it will be.

$\frac{5.6}{\text{square}}$ So, there is a channel @ Source. $V_{GS} > V_{TH}$

$\frac{5.7}{\text{square}}$ By increasing V_{DS} the channel @ the Drain decreases until it disappears @: Pinch-off Point

$V_{GD} = V_{TH}$ #

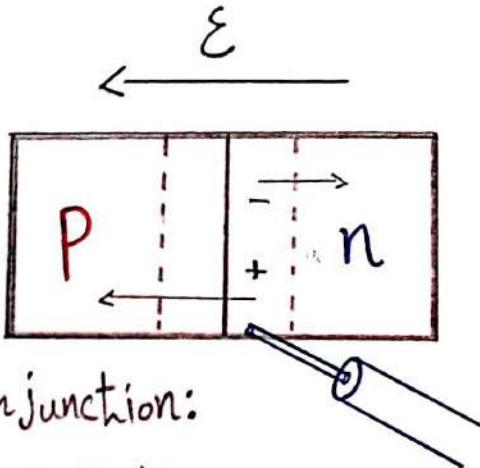
$V_{DS} = V_{ov}$ #

$\frac{5.8}{\text{square}}$ if we increase V_{DS} more than V_{GS} as: by definition the difference between the Gate & Pinch-off Point = V_{TH}
*this region has no carriers.

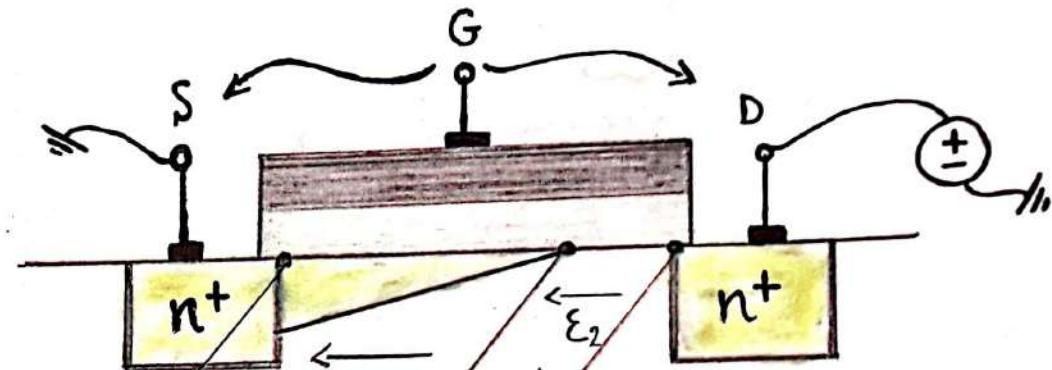
$\frac{5.9}{\text{square}}$ carriers as there is no Voltage over the Pinch-off
will not affect the current flow.

* If there are no carriers between the drain & Pinch-off Point, How could the current flow?!

∴

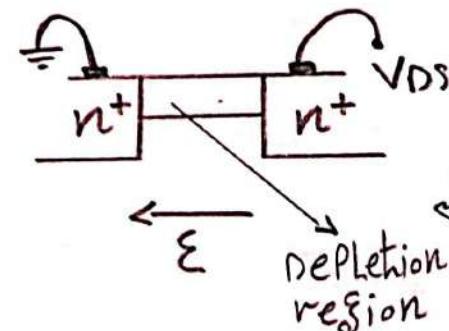


- * In the P-n junction:
 - there is a depletion region, where there is no current.
 - ↳ There is no current as there is an electric field but no carriers.
 - * Drift Current
 - electric field
 - carriers
 - If by some how, we inject carriers in the depletion region
∴ Current will flow



- ∴
* The Volt of the source is zero and the Pinch-off Point is 4V
∴ There is a Voltage difference on the channel.
∴ But from where?

∴ an electric field is created, "E₁" → The channel!
which make the electrons move from the source towards the Pinch-off point, after the electrons reach the depletion region the second electric field "E₂" will move them.



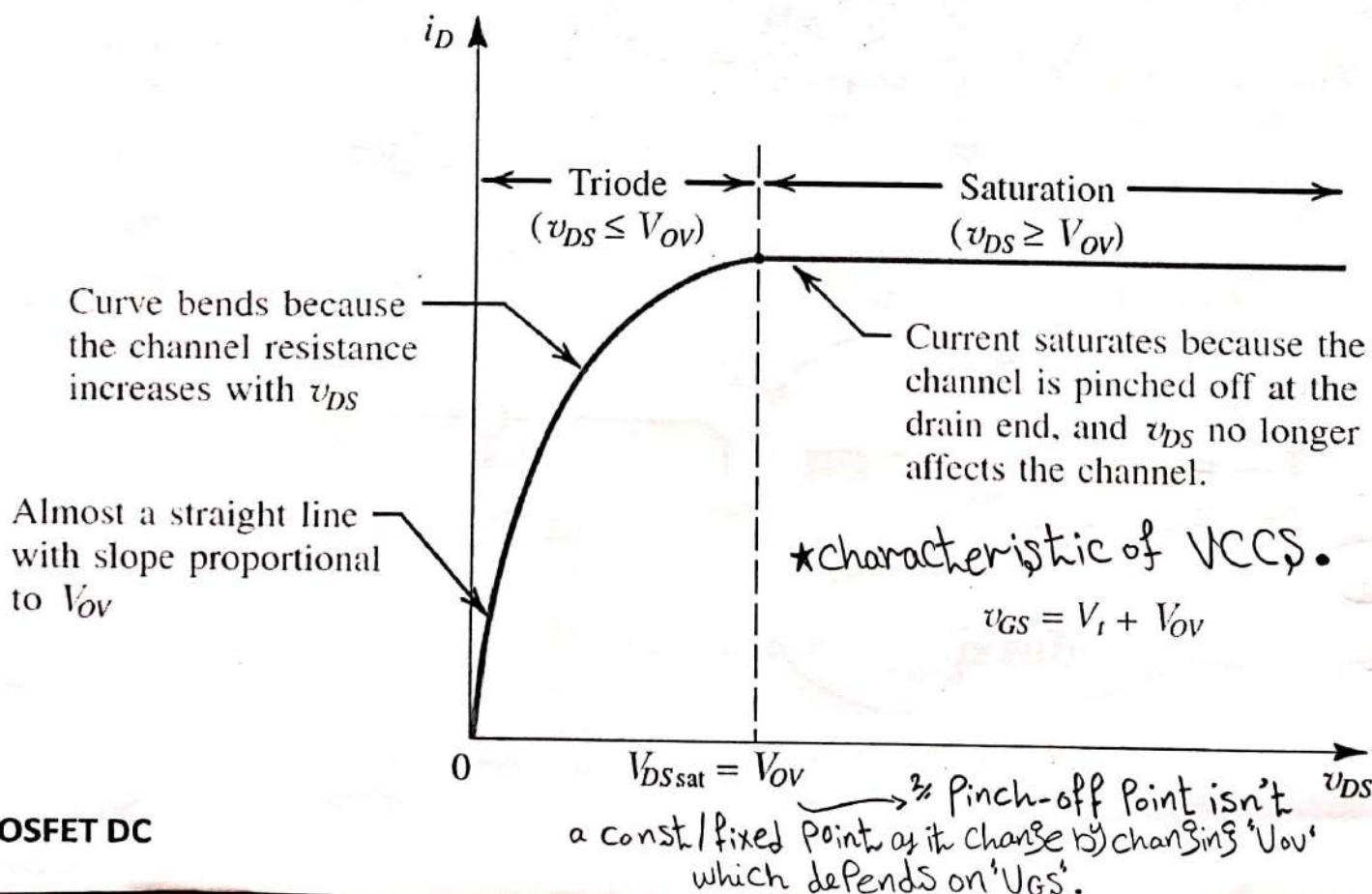
- ∴ here there is also an electric field and a depletion region is created.
↳ There is no carriers (injection) as there is no channel to bring carriers from it.

Pinch-Off (Saturation)

- Replace V_{ov} with $(V_{ov})_{average}$ and V_{DS} with V_{ov}

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \frac{V_{ov}}{2} \cdot V_{ov} = \frac{\mu_n C_{ox} W}{2} \cdot V_{ov}^2 \neq f(V_{DS})$$

- Current remains constant (saturates) \rightarrow vccs



$V_{ov} > V_{DS}$
 $V_{GD} < V_{th}$

Pinch-Off (Saturation)

- The channel is pinched off if the difference between the gate and drain voltages is not sufficient to create an inversion layer

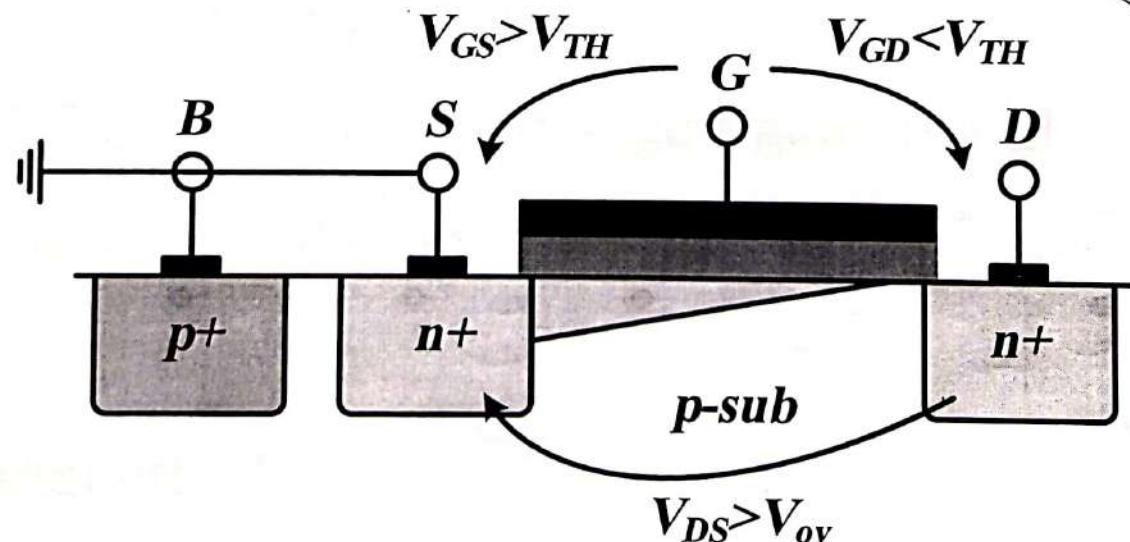
$$V_{GD} \leq V_{TH} \text{ OR } V_{DS} \geq V_{ov}$$

- Square-law (long channel MOS)

↳ $I_D \propto V_{ov}^2$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2$$

The Most Popular
equation (formula) in the analog
circuit Design



→ Valid for long channel
MOSFET.
i.e. "L" is a very large

→ Long channel
Model

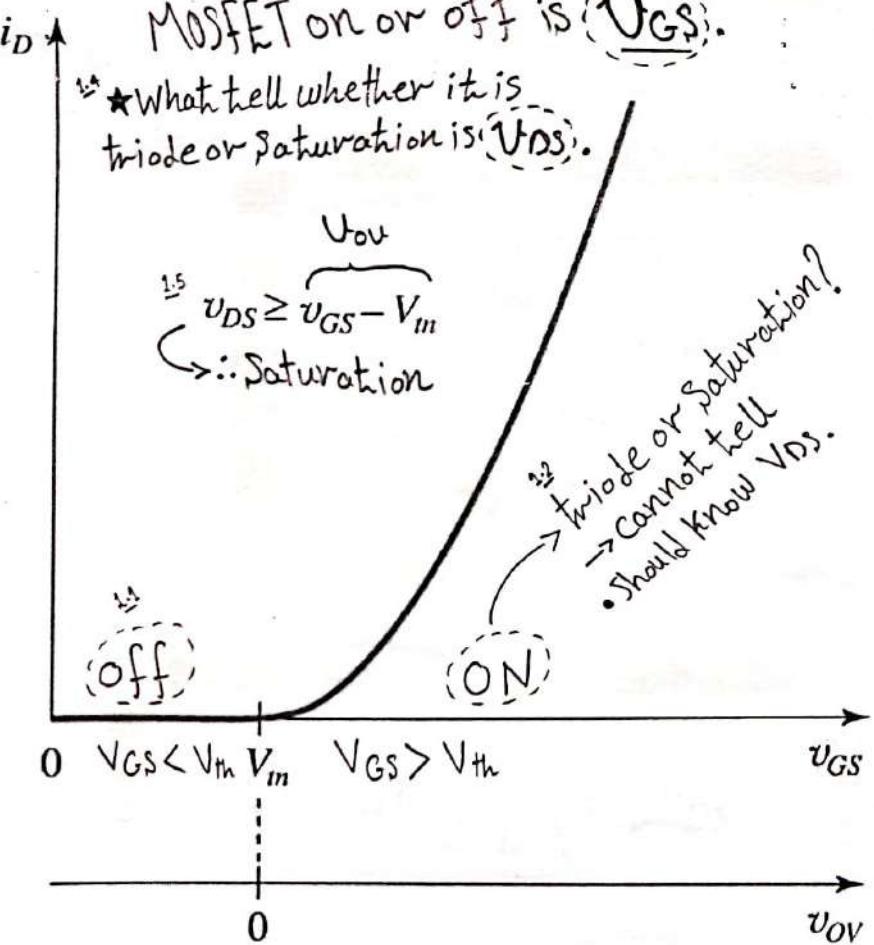
Outline

- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

IV Characteristics

^{2.3} ★ Saturation is the region of interest for the analog designer as the MOSFET in it is V_{CCS} which we will use to build amplifiers.

Parabola equation

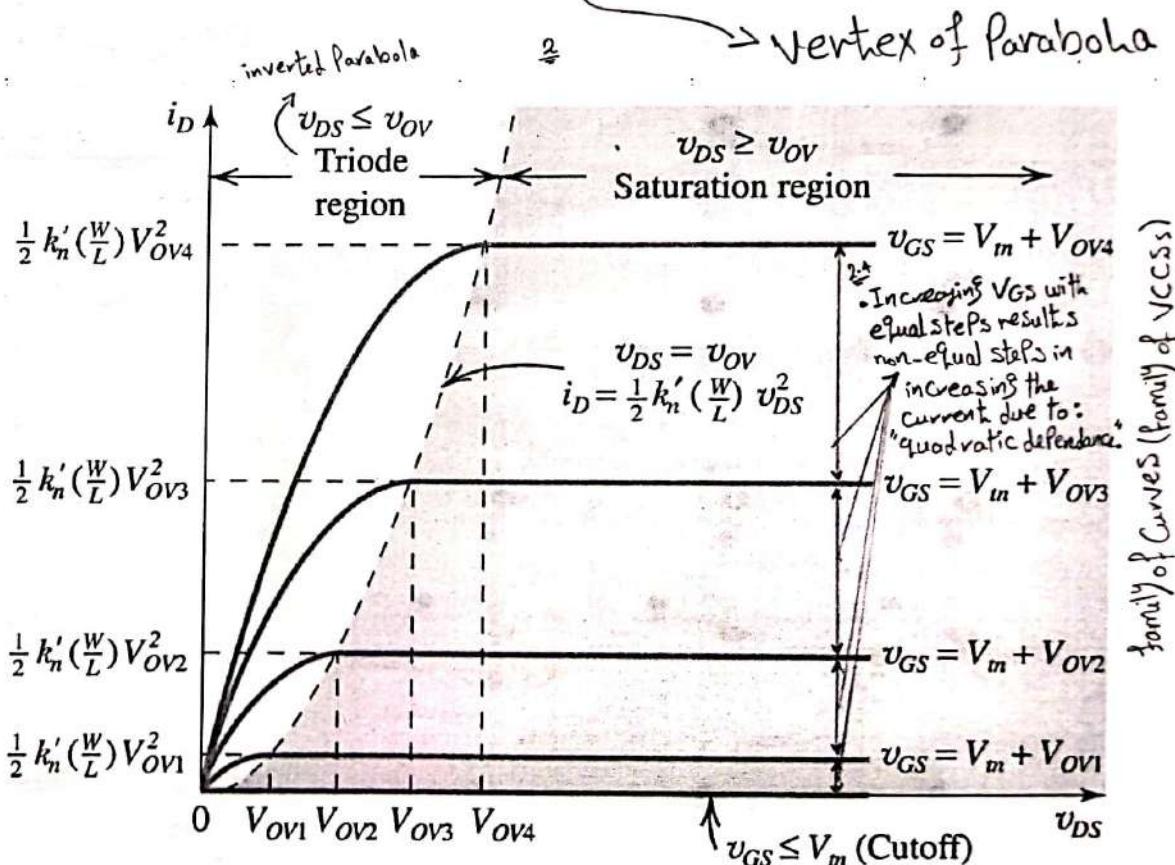


$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot (V_{GS} - V_{TH})^2$$

^{2.5} Square law

^{2.5} ★ What determines whether the MOSFET on or off is (V_{GS}).

^{2.5} ★ What tells whether it is triode or saturation is (V_{DS}).



Regions of Operation Summary

will
be discussed
later

OFF
(Subthreshold)

$$V_{GS} < V_{TH}$$

ON

$$V_{GS} > V_{TH}$$

Triode

$$V_{DS} < V_{ov}$$

Or

$$V_{GD} > V_{TH}$$

Pinch-Off (Saturation)

$$V_{DS} \geq V_{ov}$$

Or

$$V_{GD} \leq V_{TH}$$

$$I_D = \mu C_{ox} \frac{W}{L} \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

- Depends on Both: V_{DS} & V_{ov}
- If $\frac{V_{DS}}{2}$ is very small we can neglect it and work in Deep triode (linear) region of a 'VCR'.

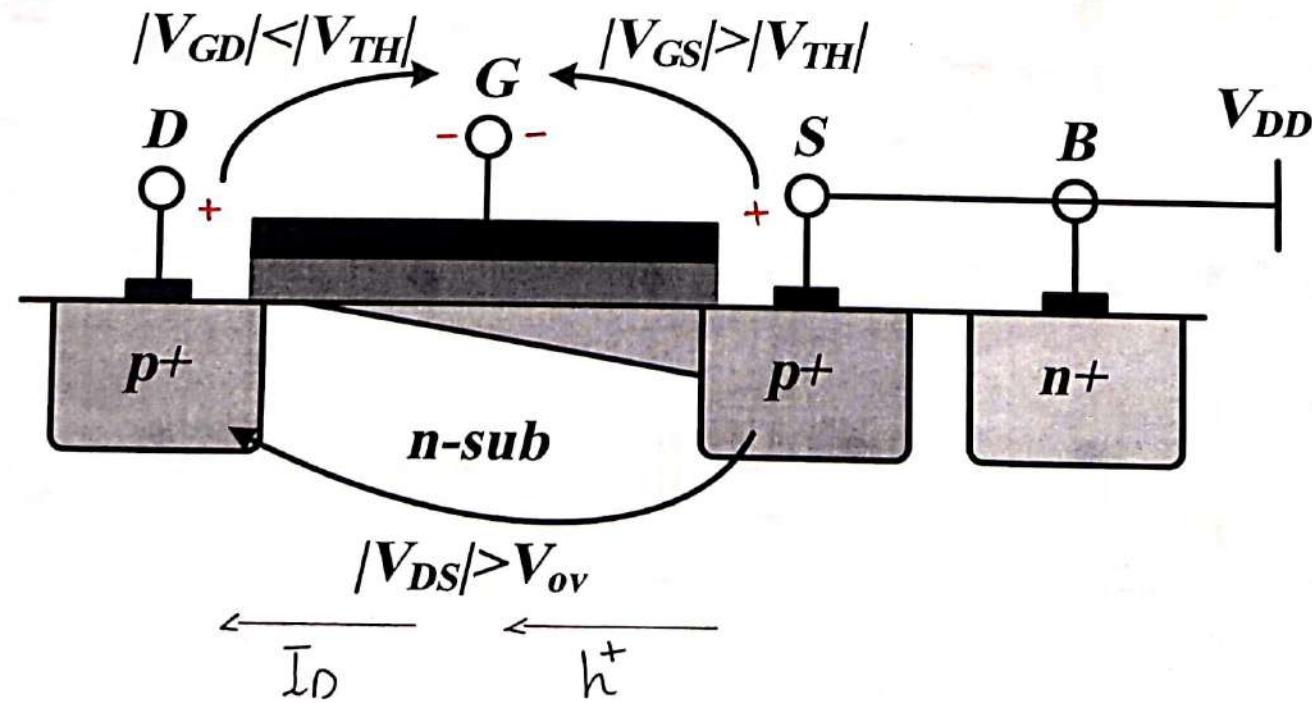
$$I_D = \frac{\mu C_{ox} W}{2} V_{ov}^2$$

$I_D \neq f(V_{DS}) \rightarrow \text{"vccs"}$

P-Channel MOSFET (PMOS)

- Electrons have higher mobility than holes (2 – 4 times) Depending on technology
 $\therefore I_{PMOS} < I_{NMOS}$
- For same W/L and V_{ov} , NMOS current is 2 – 4 times higher than PMOS

* $I_D \propto M C_{ox} \frac{W}{L}$ *Should be increased to 2-4 times, so as to oppose the decrease caused by the low mobility of holes.*



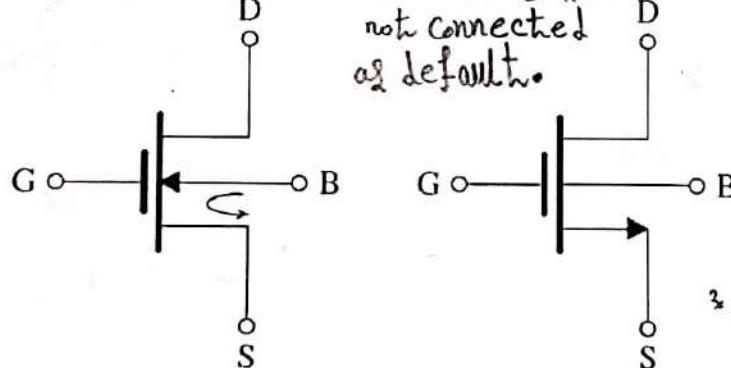
MOSFET Symbols

- S/D junction diodes must be reverse-biased under all conditions
 - NMOS bulk connected to most negative potential (ground)
 - PMOS bulk connected to most positive potential (VDD)

Default Bulk Connection
NMOS: Ground
PMOS: VDD

* arrow is always drawn @ Source

NMOS

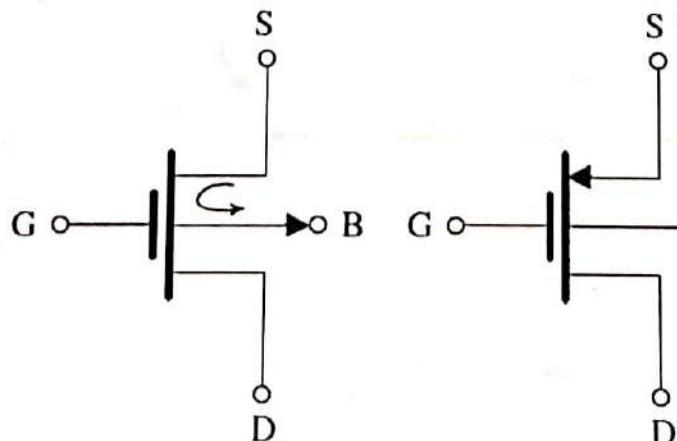


* This symbol is used when the Bulk is not connected as default.

* The most popular symbol.

Digital symbol.

PMOS

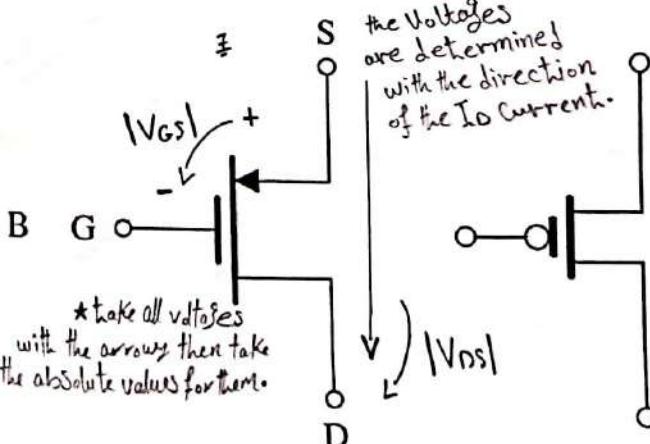
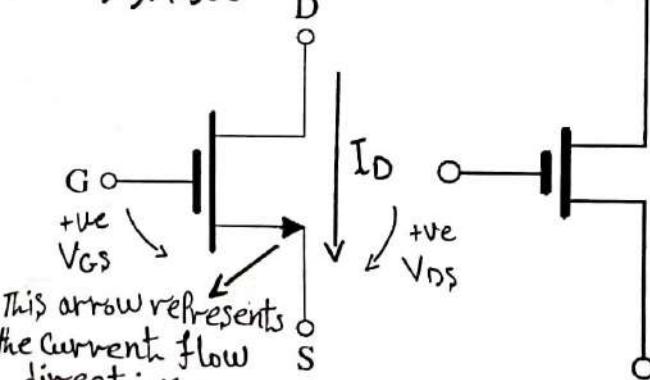


* take all voltages with the arrows then take the absolute values for them.

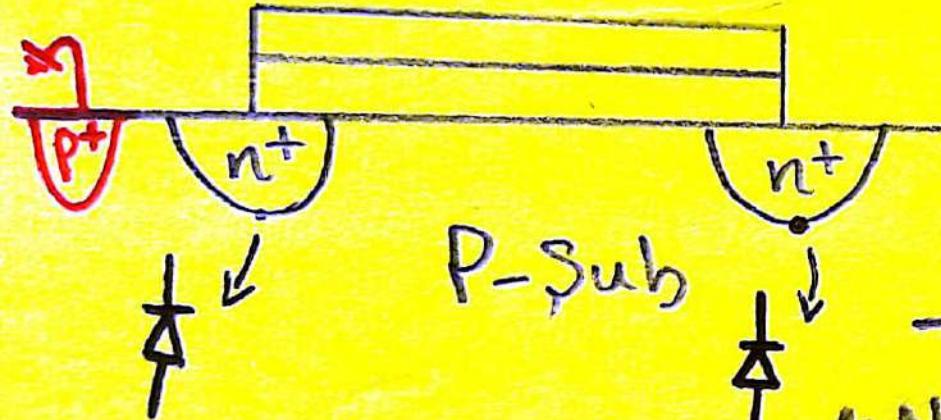
| V_{GS} |

| V_{DS} |

* The convention way to draw current (DC) from up to down.



* Why Body Connection is So important?



* There are two PN junctions exist in the MOSFET, one @ the source and the other @ the drain.

→ Do we want these junctions?

* No, We don't want these junctions to affect the operation of the MOSFET so, we have to maintain these junctions reverse-biased, and this will be done by connecting the anode - which is the bulk - to the most negative potential in the circuit, which is the ground in the single supply circuit. As for PMOS the bulk is connected to the most positive potential which is the VDD.

Large Signal Model in Saturation

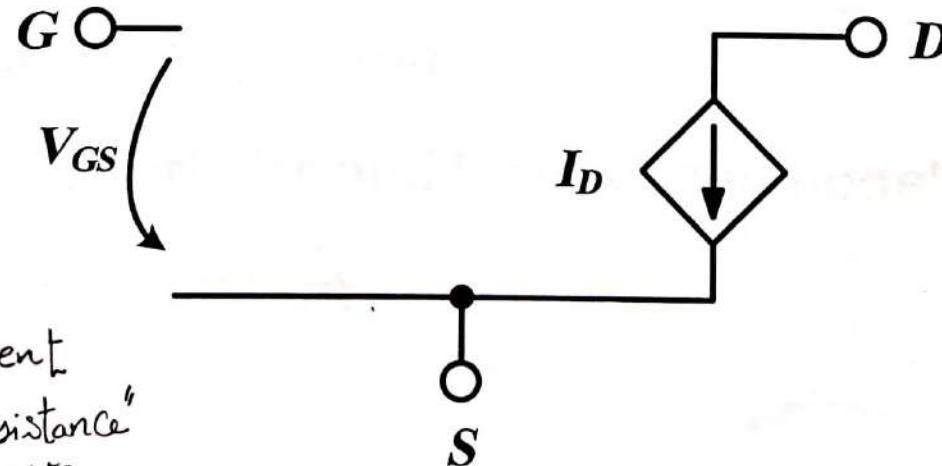
- Ideal VCCS: no dependence on V_{DS}

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2 = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot (V_{GS} - V_{TH})^2$$

1. • the current @ the Drain " I_D " depends on the Gate Voltage " V_{GS} ".

2. • the Gate is open circuit.

3. • the Previous illustration is the ideal case, we know from our previous study to thevenin and Norton model that there is no "ideal current source" or "ideal voltage source" any current source should have "parallel resistance" and any voltage source should have "series resistance"

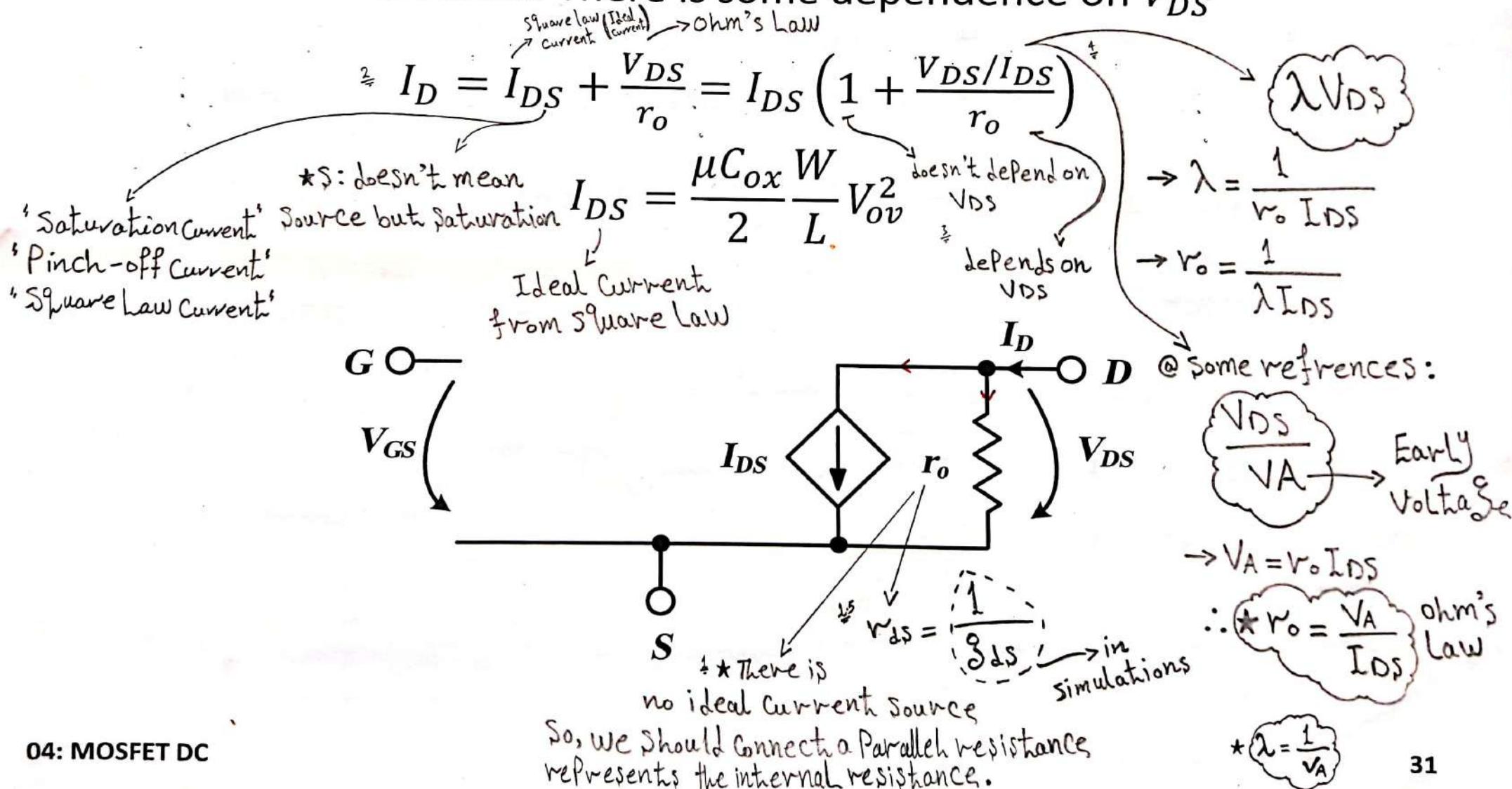


Outline

- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

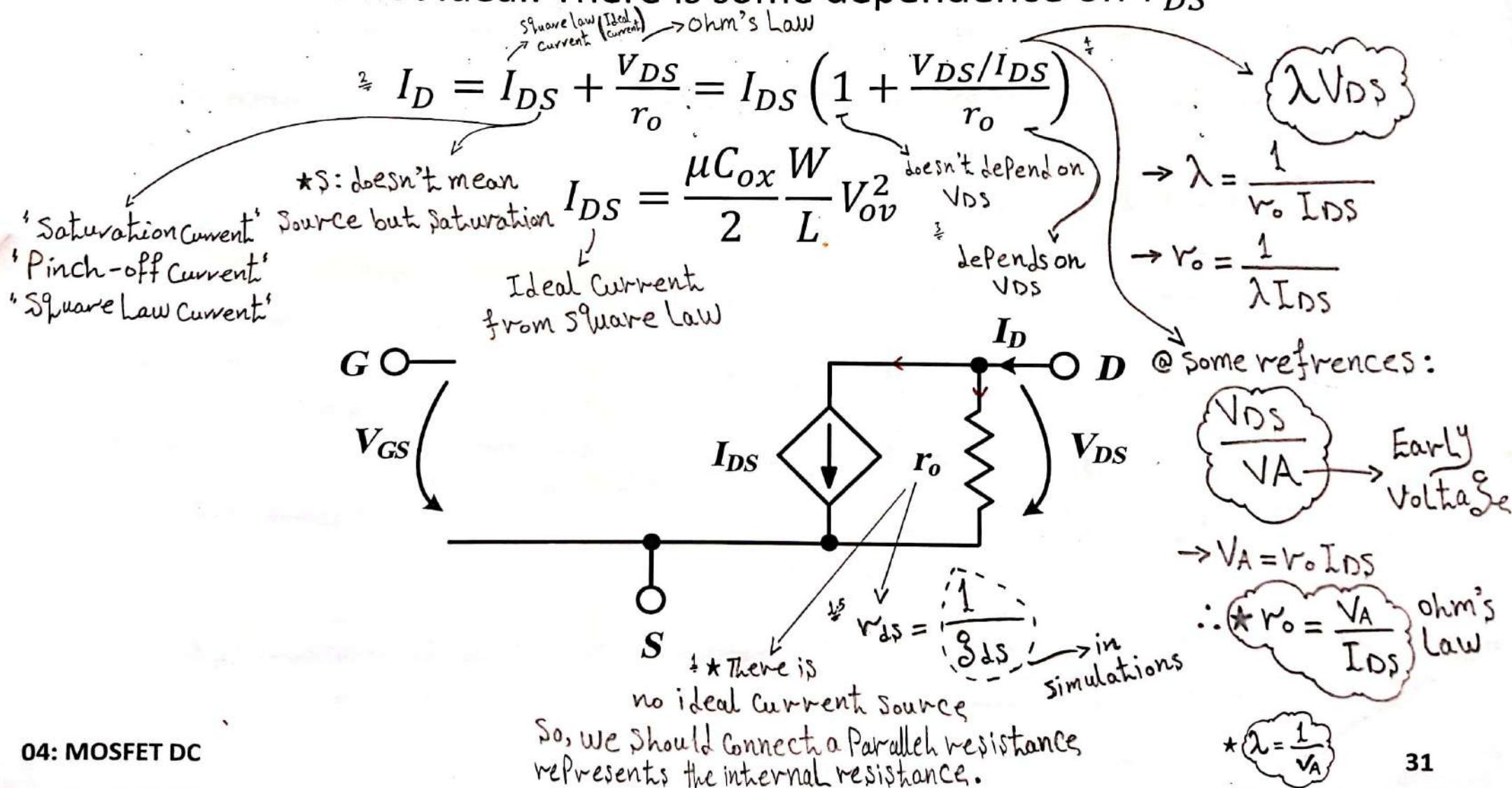
Large Signal Model with Finite Output Res

- The transistor is a VCCS
- The VCCS is not ideal: There is some dependence on V_{DS}



Large Signal Model with Finite Output Res

- The transistor is a VCCS
- The VCCS is not ideal: There is some dependence on V_{DS}



Channel Length Modulation (CLM)

- The VCCS is not ideal: There is some dependence on V_{DS}

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{g_{ds}} = \frac{V_A}{I_{DS}} = \frac{1}{\lambda I_{DS}}$$

$\dagger V_A$: Early voltage ($V_A \propto L$) $\leftrightarrow \lambda$: Channel length modulation coefficient ($\lambda \propto 1/L$)

$$I_D = I_{DS} + \frac{V_{DS}}{r_o} = I_{DS} \left(1 + \frac{V_{DS}/I_{DS}}{r_o} \right) = \frac{\mu C_{ox} W}{2 L} V_{ov}^2 (1 + \lambda V_{DS})$$

* Some people think: If I am dealing with: 90nm technology then all the transistors must be 90nm that is not true (X)

length

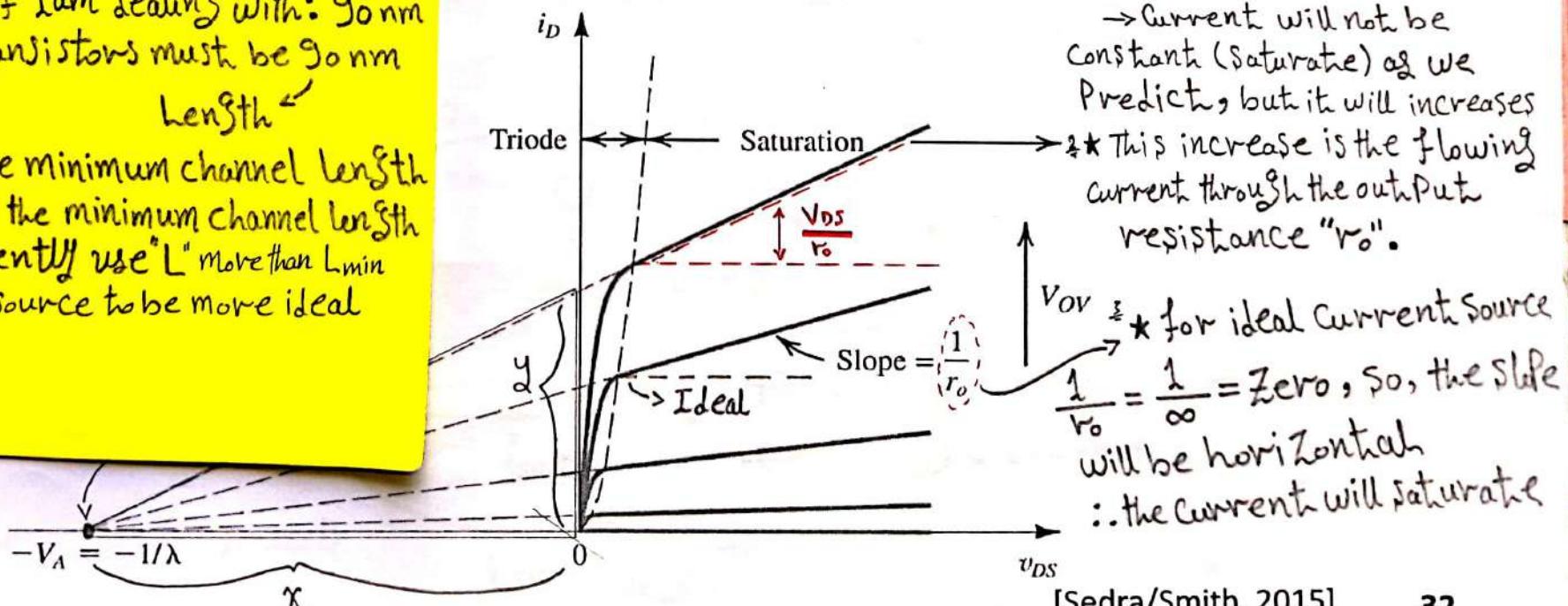
→ actually: 90 nm is the minimum channel length

* In Digital: use only the minimum channel length

* In Analog: We frequently use "L" more than L_{min} as we want our current source to be more ideal

$\therefore L \propto r_o, L \propto V_A$

$$\therefore r_o = \frac{V_A}{I_{DS}} \#$$



Channel Length Modulation (CLM)

★ Physical reason
"explanation"
for: r_o

The VCCS is not ideal: There is some dependence on V_{DS}

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{g_{ds}} = \frac{V_A}{I_{DS}} = \frac{1}{\lambda I_{DS}}$$

• Channel length modulation coefficient ($\lambda \propto 1/L$)

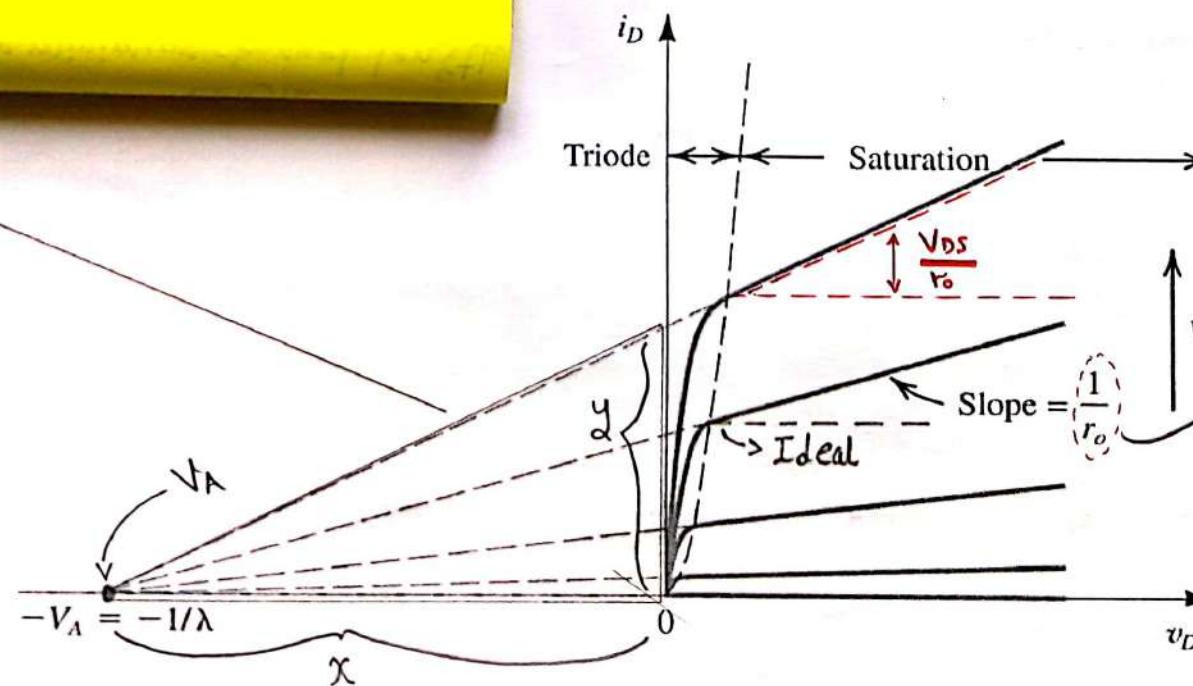
$$+ \frac{V_{DS}/I_{DS}}{r_o} = \frac{\mu C_{ox} W}{2 L} V_{ov}^2 (1 + \lambda V_{DS})$$

• Slope:

$$\frac{y}{x} = \frac{I_{DS}}{V_A}$$

$$= \frac{1}{r_o}$$

$$\therefore r_o = \frac{V_A}{I_{DS}} \quad \#$$



↓ ★ By increasing V_{DS} :
→ Current will not be constant (saturate) as we predict, but it will increase.
★ This increase is the flowing current through the output resistance "r_o".

* for ideal current source
 $\frac{1}{r_o} = \frac{1}{\infty} = 0$, so, the slope will be horizontal
∴ the current will saturate

* Some People thinks: If I am dealing with: 90 nm technology then all the transistors must be 90 nm that is not true (X) length ↴

→ actually: 90 nm is the minimum channel length

* In Digital: use only the minimum channel length

* In Analog: We frequently use "L" more than L_{min} as we want our current source to be more ideal

$$\therefore L \propto V_o, L \propto V_A$$

Channel Length Modulation (CLM)

- L_{eff} decreases with $V_{DS} \rightarrow$ Shorter L gives more current
- V_A : Early voltage ($V_A \propto L$)
- λ : Channel length modulation coefficient ($\lambda \propto 1/L$)

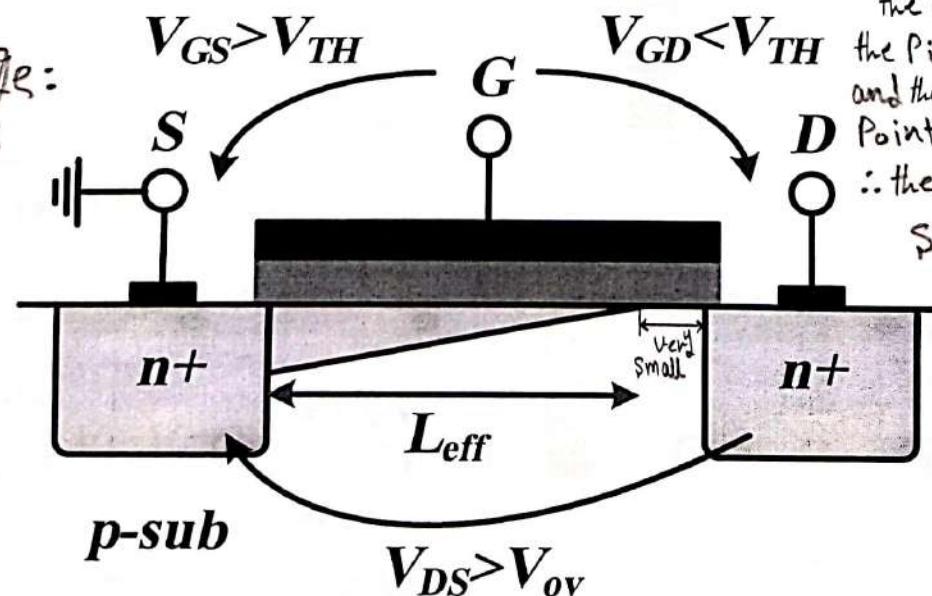
$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS})$$

$$r_o = \frac{V_A}{I_{DS}} = \frac{1}{\lambda I_{DS}}$$

- V_A increases with V_{DS} : higher r_o as we go deeper into saturation

* By increasing the drain voltage:
 ↳ The Pinch-off Point will be shifted towards the source so, the length of the channel "L" decreases to be " L_{eff} "

* $\uparrow I_D \propto \frac{W}{L} \downarrow$
 • So, I_D will slightly increase



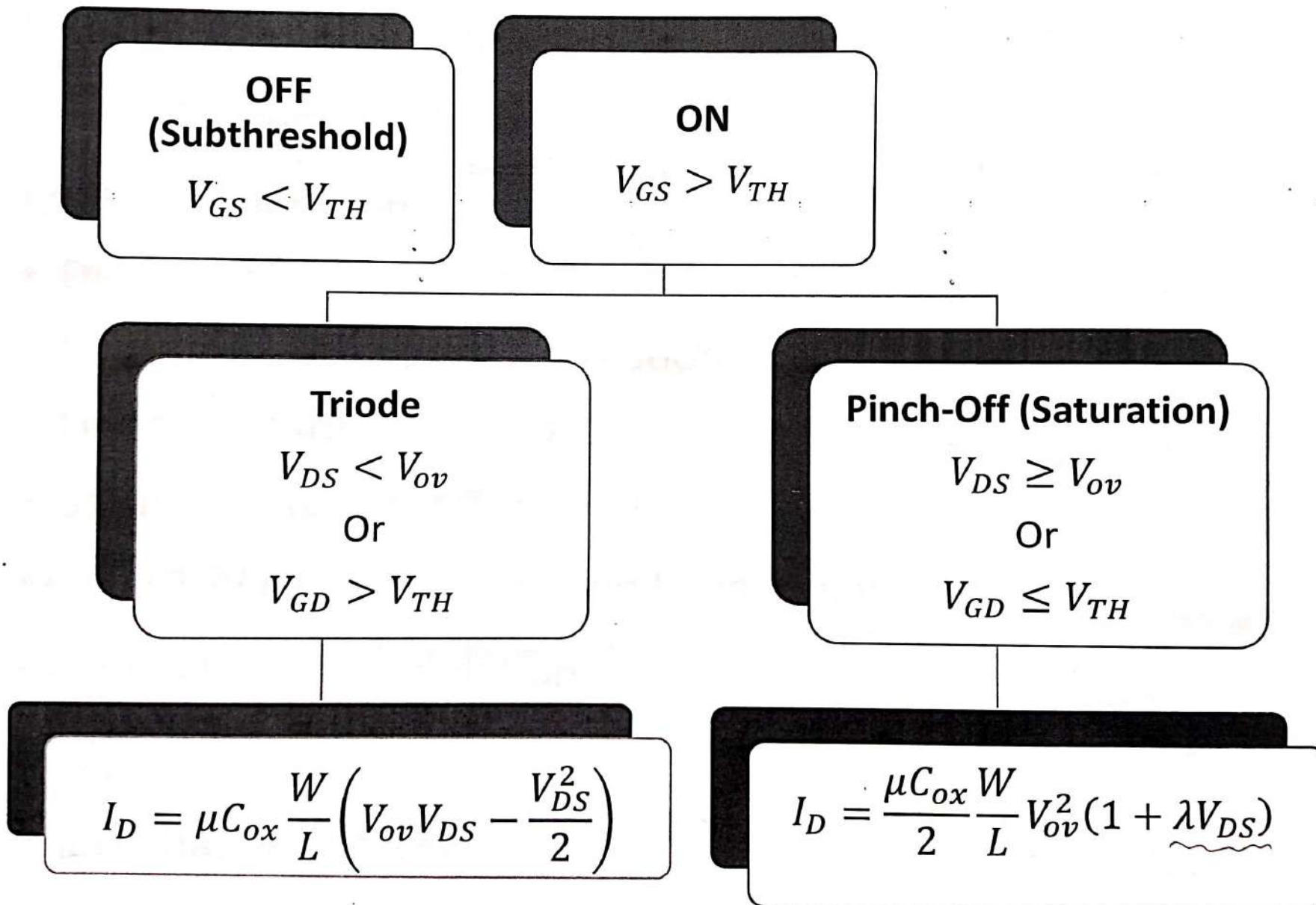
★ V_A is not constant as it depends on:
 the channel length, we say before that
 the Pinch-off Point is shifted towards the source
 and the region between the drain and the Pinch-off
 Point is very very small so, if L is large
 ∴ the effect of this region is negligible
 So, $L \uparrow \therefore r_o \uparrow \therefore V_A \uparrow \therefore \lambda \downarrow$

channel length modulation is weak.

* for ideal case:

$$\begin{matrix} r_o & \downarrow \\ \infty & \end{matrix} \quad \begin{matrix} V_A & \downarrow \\ \infty & \end{matrix} \quad \begin{matrix} \lambda & \downarrow \\ 0 & \end{matrix}$$

Regions of Operation Summary



Outline

- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

Body Effect

- V_{SB} affects the charge required to invert the channel

- Increasing V_S or decreasing V_B increases V_{TH}

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|} \right)$$

- Φ_F = surface potential at threshold *always +ve as the body is the most +ve Potential*

- Depends on doping level and intrinsic carrier concentration n_i

- γ = body effect coefficient

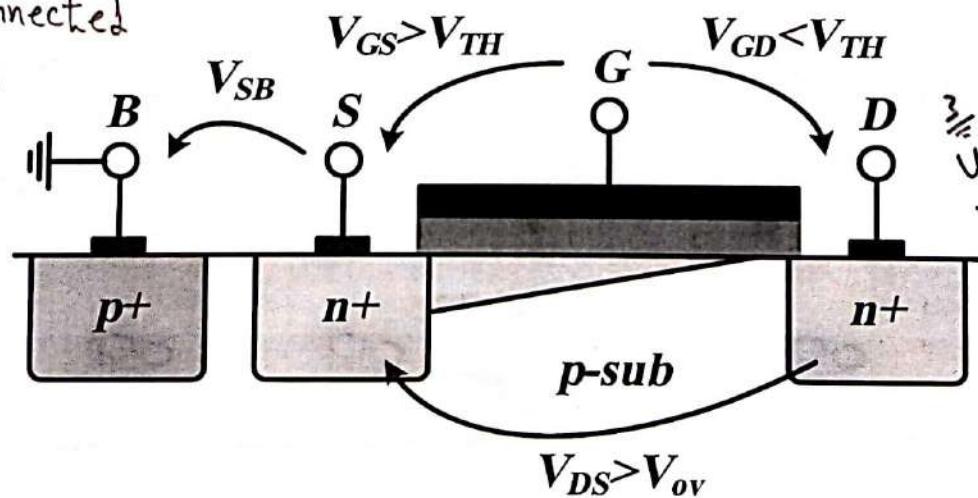
- Depends on C_{ox} and doping

Gamma

\therefore Before: We assume that:
The source & the body are both connected
to the ground, but if this case
is not valid \therefore there will be
a potential difference between
the source & the body V_{SB}

The source of this Mos
is floating and not
connected to the ground

04: MOSFET DC



\therefore if $V_{SB} = 0$

$$\therefore V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|} \right)$$

$$\therefore V_{TH} = V_{TH0} \rightarrow \text{Threshold Voltage}$$

@ zero-Bias

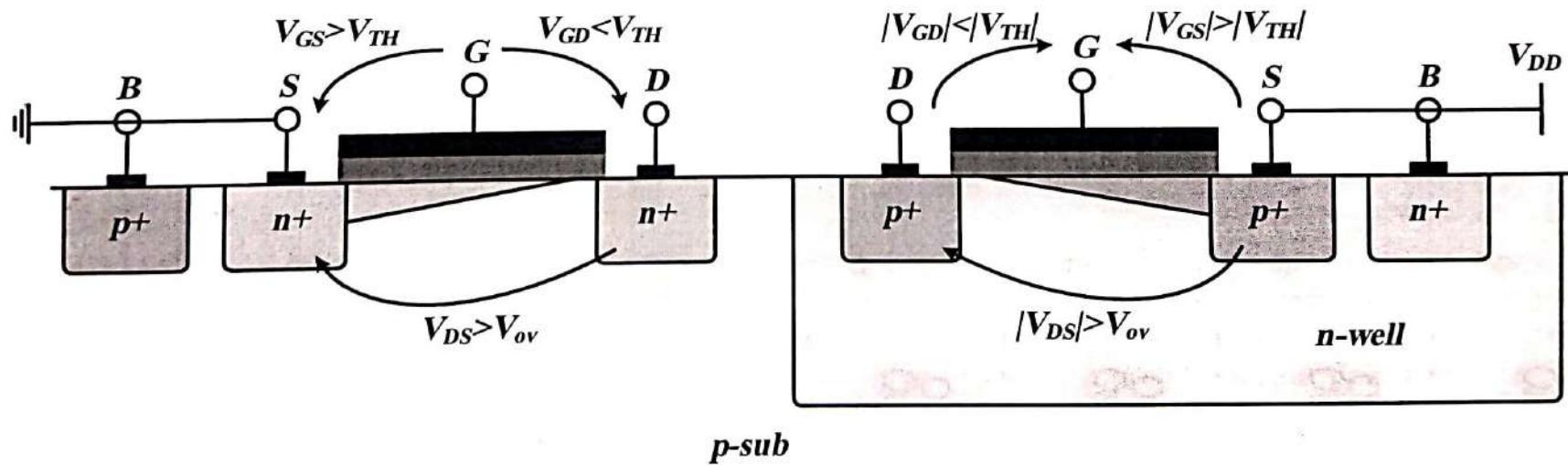
\therefore Conclusion: By increasing V_{SB} V_{TH} will increase which will makes I_D decreases (in case of const. V_{GS})

$\because V_{SB} \uparrow \therefore V_{TH} \uparrow$
 $\therefore I_D \downarrow$

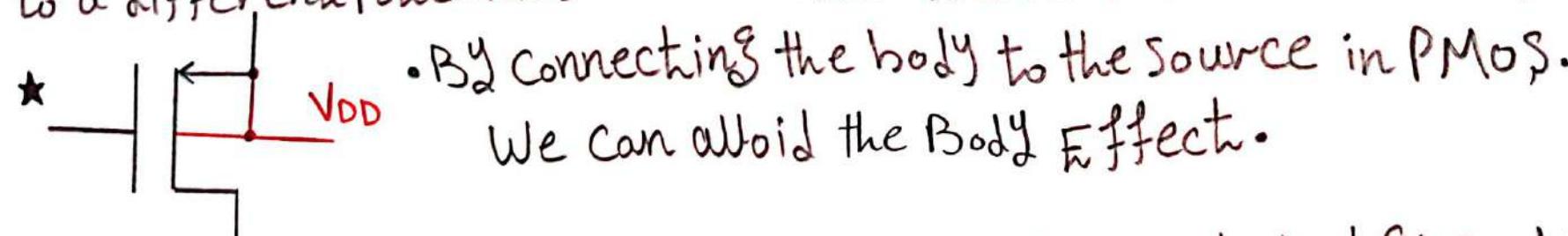
as: $I_D \propto (V_{GS} - V_{th})$

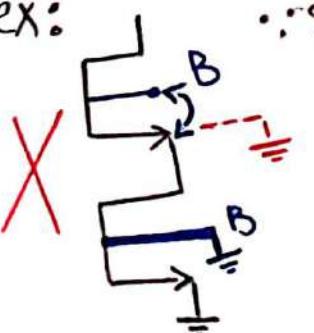
CMOS

- CMOS = NMOS + PMOS on the same substrate
- S/D junction diodes must remain reverse-biased
 - NMOS bulk connected to most negative potential (ground)
 - PMOS bulk connected to most positive potential (VDD)



- NMOS requires P-substrate while PMOS requires n-substrate
 So, How can we able to combine them on the same substrate in the CMOS?
- We begin with P-sub making a normal "NMOS", then inside the P-Sub we make a doping region of n-type called "n-well", inside the n-well we can make PMOS.
 - It's very important to know that the "P-sub" is common for all NMOS in the circuit. So, they all have the same body. So, We have to connect this body to the ground.
 - for PMOS: We can make more than one "n-well" so, we can connect every well to a different potential - we don't have to connect all n-wells to the same potential -.

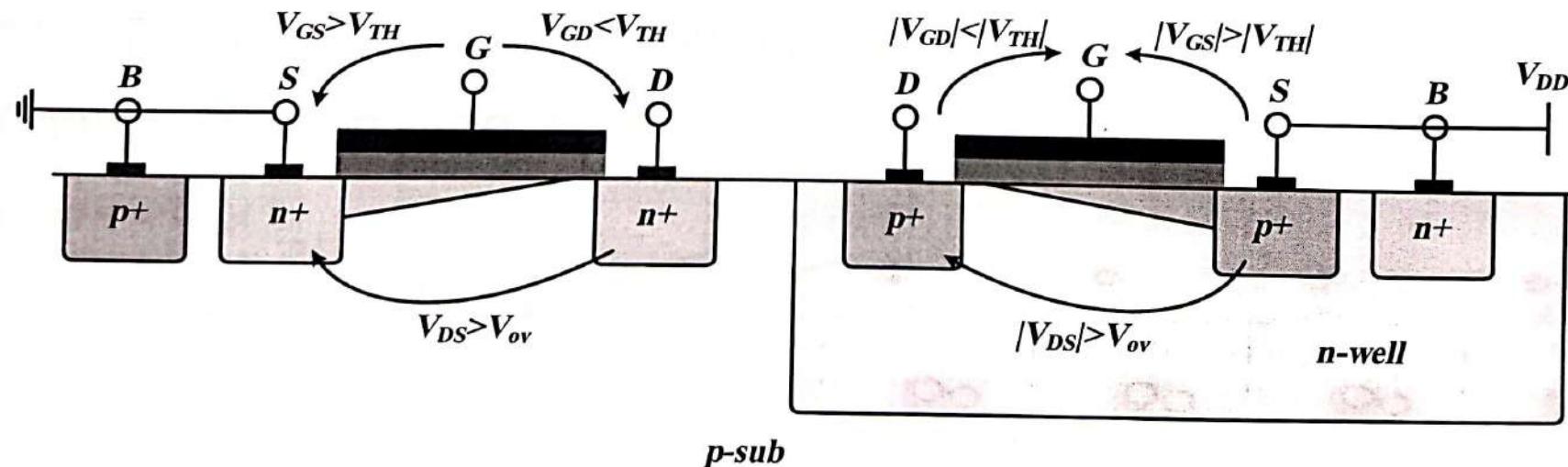


- This connection is not valid for NMOS except for some technologies which allow to make "triple well" (well inside a well inside a well)
- ex:
- ~~X~~ 
- ∴ Same Body
 ∴ We connect the source of the upper NMOS to the Ground
 ∴ I cancel the lower NMOS and run the circuit
- * N-well: NMOS formed by n+ on substrate. PMOS formed by P+ on n-well, which sits on the substrate.
- * Double well: N-MOS formed by n+ on p-well, which sits on the sub. PMOS formed by P+ on n-well, which sits on the substrate.
- * Triple well: NMOS formed by n+ on P-well, which sits inside an n-well, which further sits on the substrate.
- PMOS formed by P+ on n-well which sits on the substrate.

CMOS

- CMOS = NMOS + PMOS on the same substrate
- All NFETs share the same substrate
 - If source is floating then will have body effect
- Each PFET can have an independent n-well
 - Connect body to floating source to avoid body effect
- NFET can be placed in a “private” well in twin/triple-well technologies

→ CONS.: the well consumes large area so increases the area of the device.
i.e. overhead

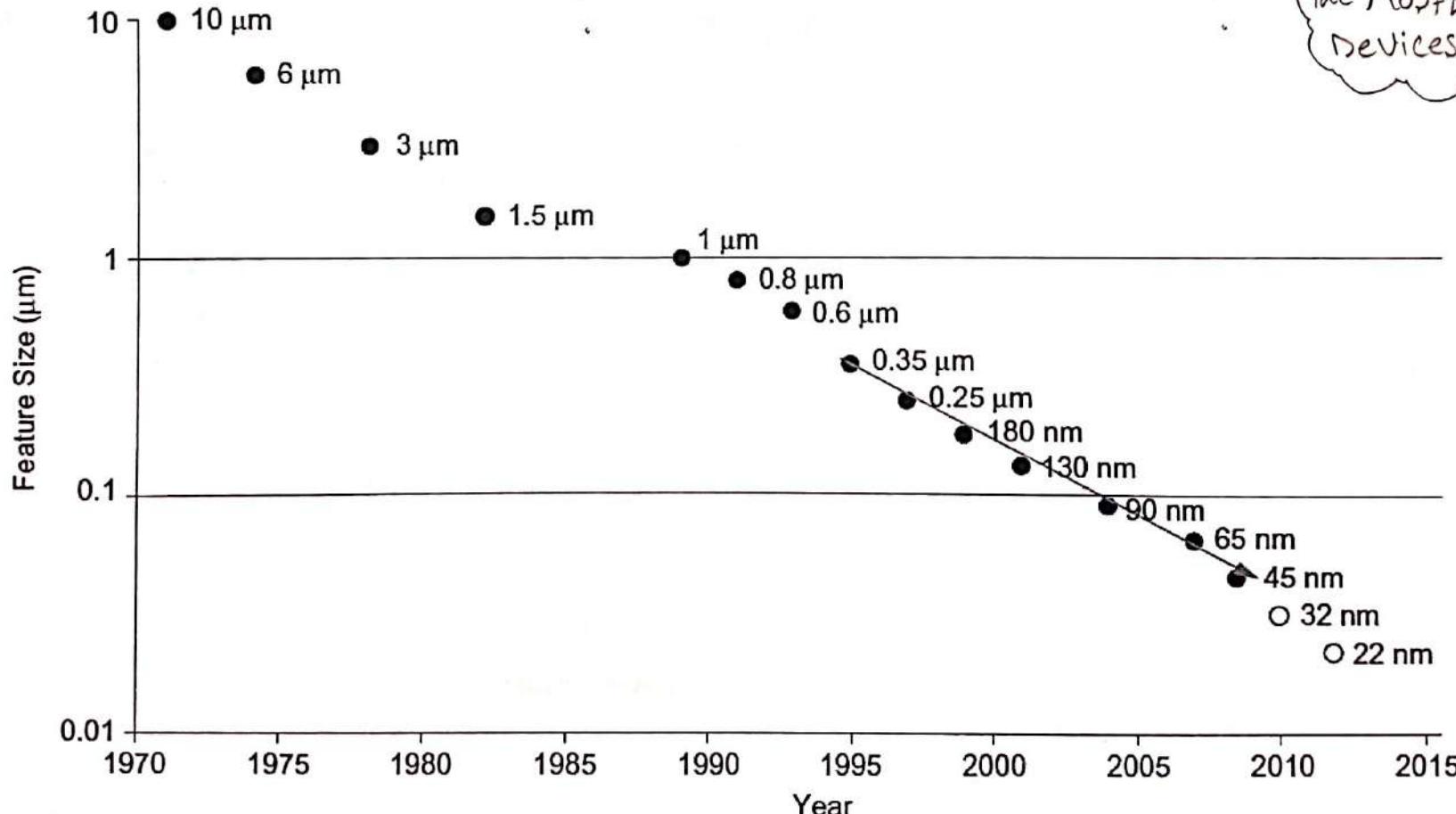


Outline

- Why is the transistor different?
- MOSFET structure
- MOSFET operation
 - Depletion
 - Inversion and channel formation
 - Linear and triode region
 - Saturation (pinch-off) region
- MOSFET IV characteristics and large signal model
- Channel length modulation
- Body effect
- Short channel effects

CMOS Technology Scaling: Moore's Law

- Min feature size (L_{min}) shrinking 30% ($\approx 1/\sqrt{2}$) every 2-3 years
 - Transistor area (and cost) are reduced by a factor of 2
- Device scaling brings new challenges in circuit design



* Mainly You can study the effects of scaling down on the MOSFET in the Devices courses

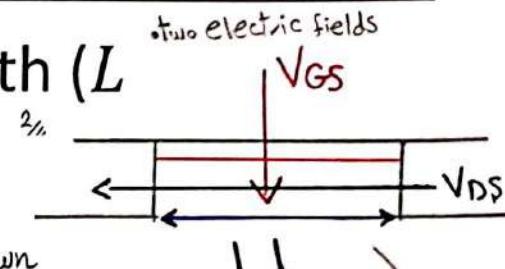
Short Channel Effects: Velocity Saturation

- For deep-submicron MOSFET with short channel length ($L < 0.25\mu m$) the lateral electric field is very high

* While decreasing (scaling down) L , the electric field increases. Why we don't scale down V_{DS} ?
 → actually we tries to scale down V_{DS} and we success to scale it down from 5V to sub 1V

$$E = \frac{V_{DS}}{L}$$

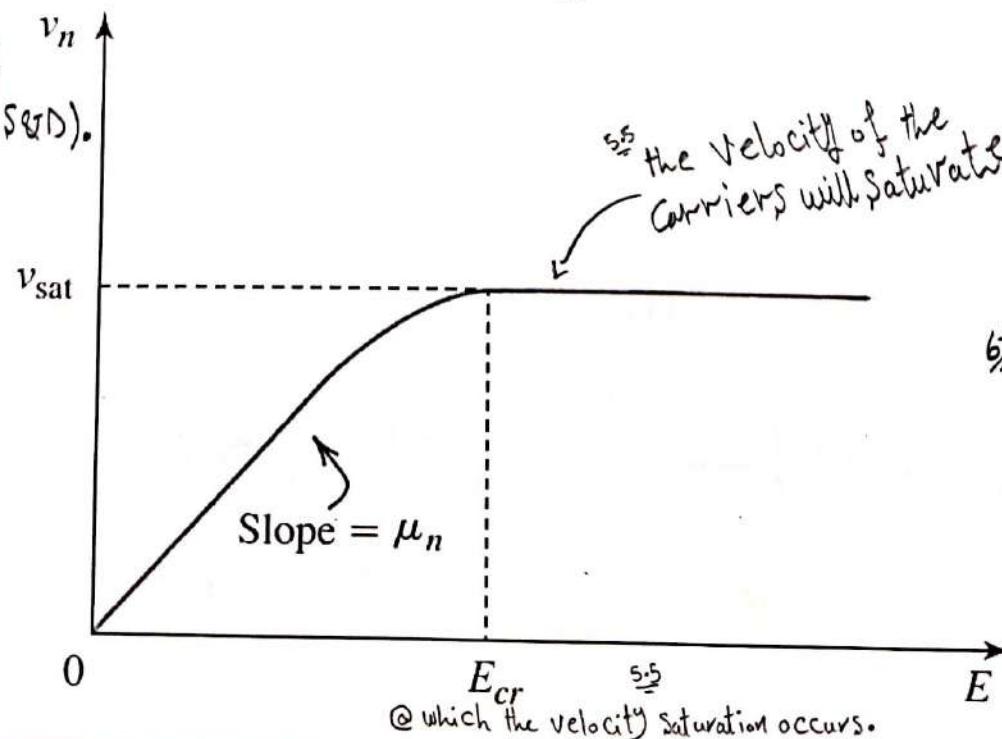
But we cannot keep up with the speed of scaling down of the channel length.
 ↳ 3 orders of magnitude
 $V_{DS} \rightarrow$ less than 1 order.



- @ $E = E_{cr}$ ($V_{DS} = V_{DSSat}$) the velocity of the carriers saturates

* Why it's called:
 "short channel effects"
 ↳ As the most important parameter in scaling down process is the channel length: (distance between S & D).

$$v_{sat} = \mu E_{cr} = \mu \frac{V_{DSSat}}{L} \approx 10^7 \text{ cm/s}$$



* By increasing the lateral electric field
 ↳ The velocity of the carriers increases

$$V \propto E$$

$$V = \mu E$$

6.5

$$E_{cr} = \frac{V_{DSSat}}{L}$$

Velocity Saturation: IV Characteristics

- Long channel: Triode region

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

- Velocity sat happens before pinch-off if $V_{DSSat} < V_{ov}$

- Replace V_{DS} with V_{DSSat} and $v = \mu_n \frac{V_{DS}}{L}$ with $v_{sat} = \mu_n \frac{V_{DSSat}}{L}$

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left(V_{ov} - \frac{V_{DSSat}}{2} \right) \cdot V_{DSSat} = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSSat}}{2} \right)$$

- Including channel length modulation effect (the physical reason is different, but the effect on I_D is the same)

$$I_D = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSSat}}{2} \right) (1 + \lambda V_{DS})$$

★ Two important new properties ★

1. Current independent of L + linear dependence on V_{ov}

∴ $I_D \propto L$
∴ scaling down won't affect current anymore.
• L is inside "v_{sat}" which is constant

★ The Velocity Saturation will affects only if : $V_{DS, \text{sat}} < V_{OU}$

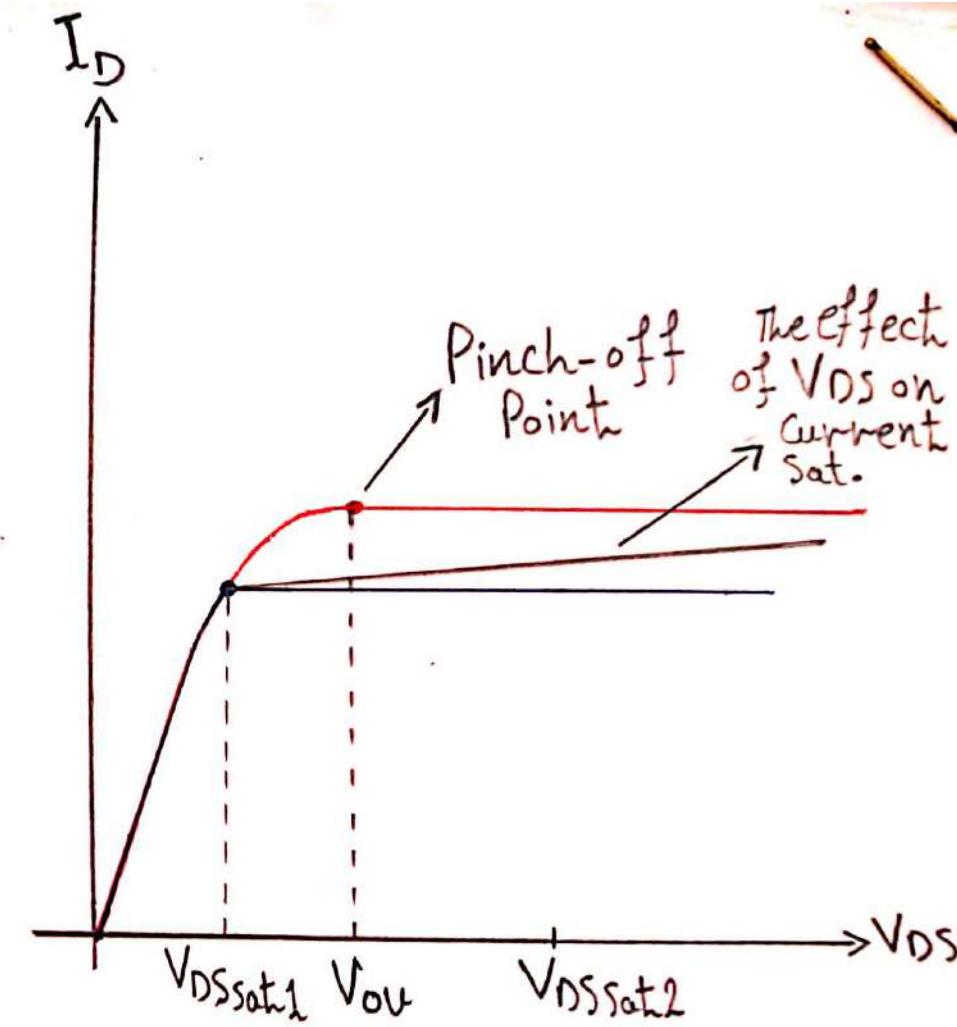
i.e. it happens before the Pinch-off

↳ after sub. by $V_{DS, \text{sat}}$:

$$★ I_D = C_{ox} W V_{sat} \cdot \left(V_{OU} - \frac{V_{DS, \text{sat}}}{2} \right)$$

→ including the channel length Modulation.

$$★ I_D = C_{ox} W V_{sat} \cdot \left(V_{OU} - \frac{V_{DS, \text{sat}}}{2} \right) \cdot (1 + \lambda V_{DS})$$



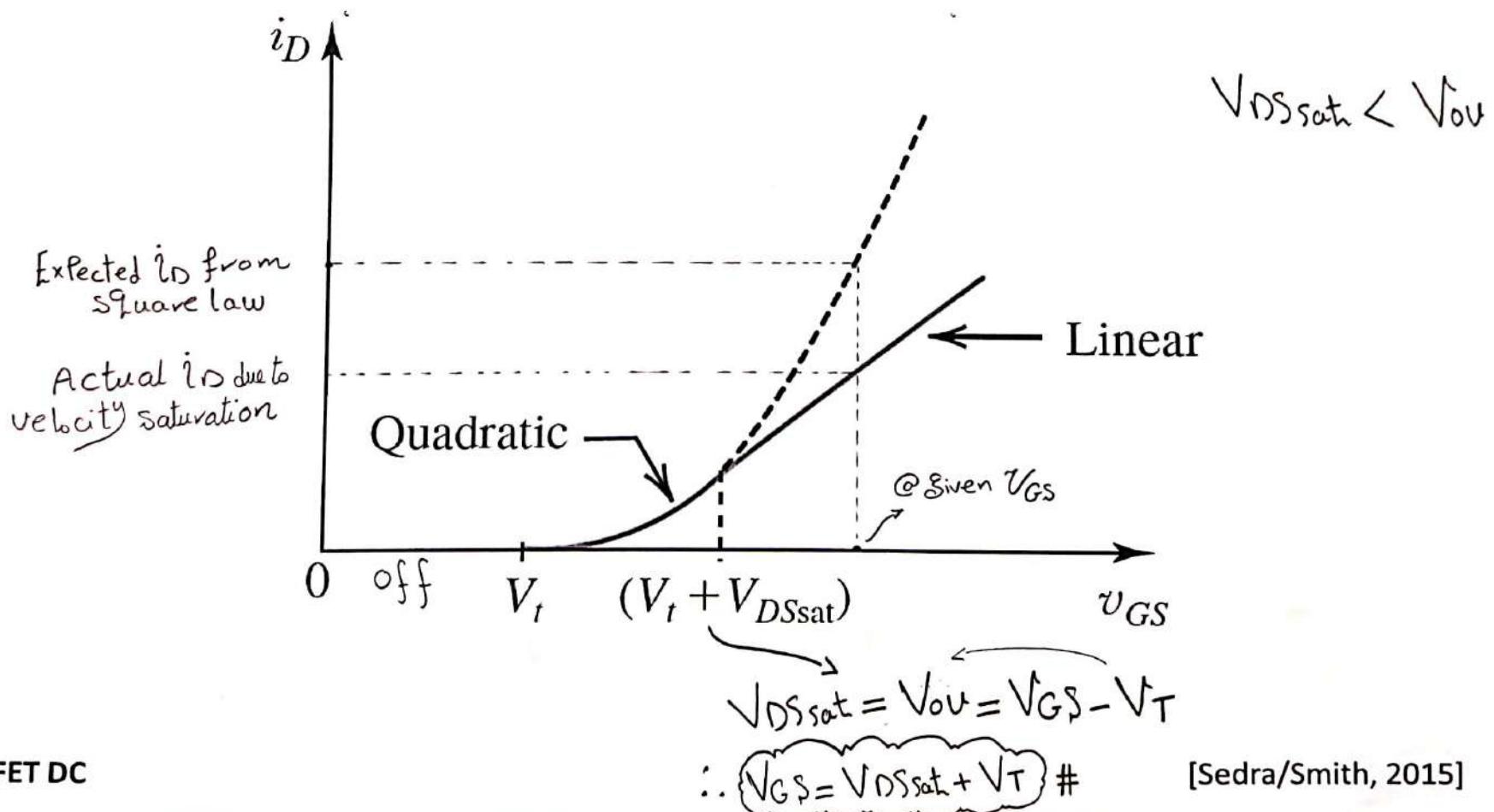
★ How Can We Put into Consideration channel length modulation without Pinch-off?

↳ Actually The channel length Modulation is a very simple explanation. In General we say that always the Drain Voltage have an effect on the current, i.e. the current won't Saturate in an ideal way, There will be a slope despite the Physical reason behind this effect (channel Length modulation - Drain induced barrier lowering - etc.)

Velocity Saturation: IV Characteristics

- Velocity sat happens before pinch-off if $V_{DSSsat} < V_{ov}$

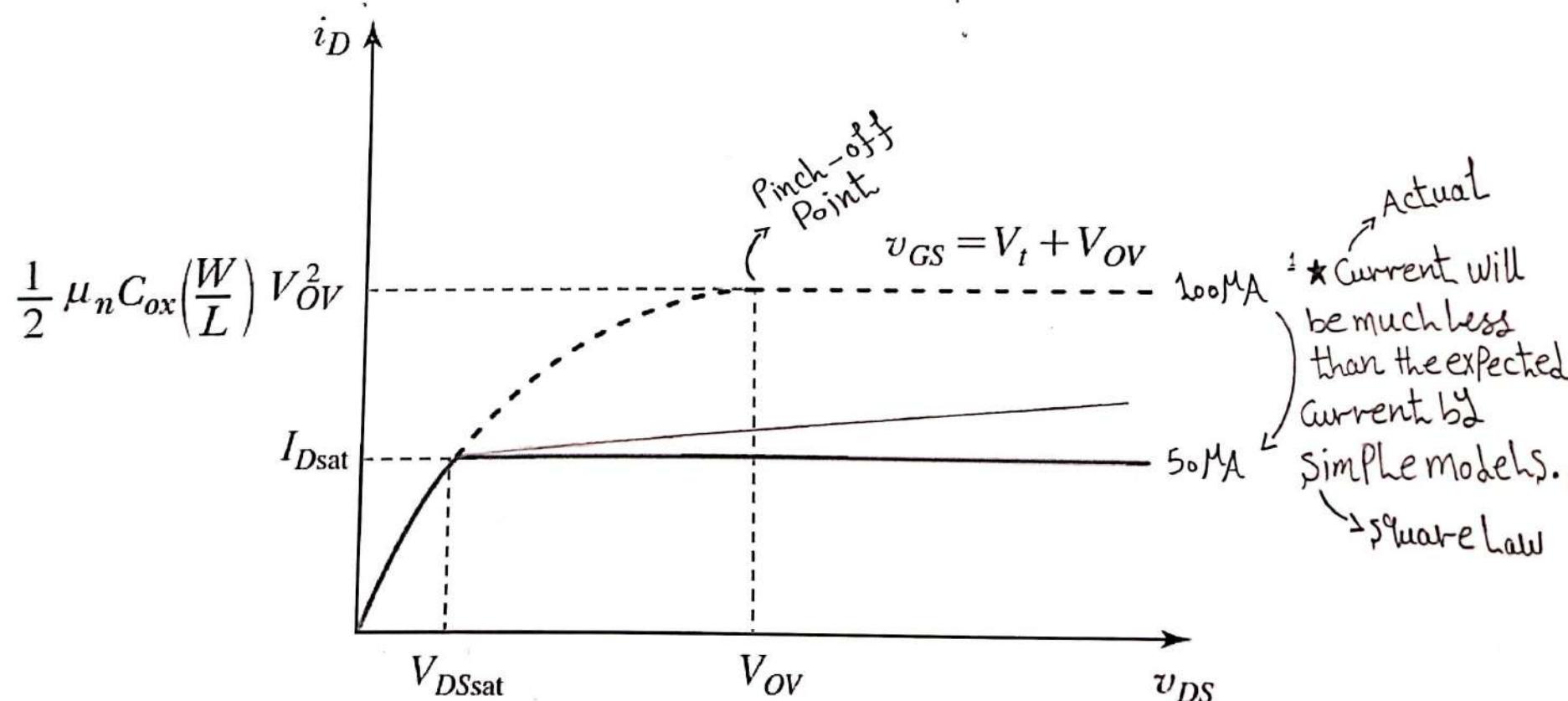
$$I_D = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSSsat}}{2} \right) (1 + \lambda V_{DS})$$



Velocity Saturation: IV Characteristics

- Velocity sat happens before pinch-off if $V_{DSSat} < V_{ov}$

$$I_D = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSSat}}{2} \right) (1 + \lambda V_{DS})$$



* Analog Designers are less concerned with Velocity Saturation than Digital Designers. Why?

* Digital

→ for device to be ON:

$$V_{GS} = V_{DD} \quad (0, 1)$$

$$V_{ov} = V_{DD} - V_T$$

* The greatest possible overdrive voltage → as V_{DD} is the greatest V_{GS} .

$$\therefore V_{DSSat} < V_{ov}$$

* Analog

→ They use a small overdrive voltage (relatively)

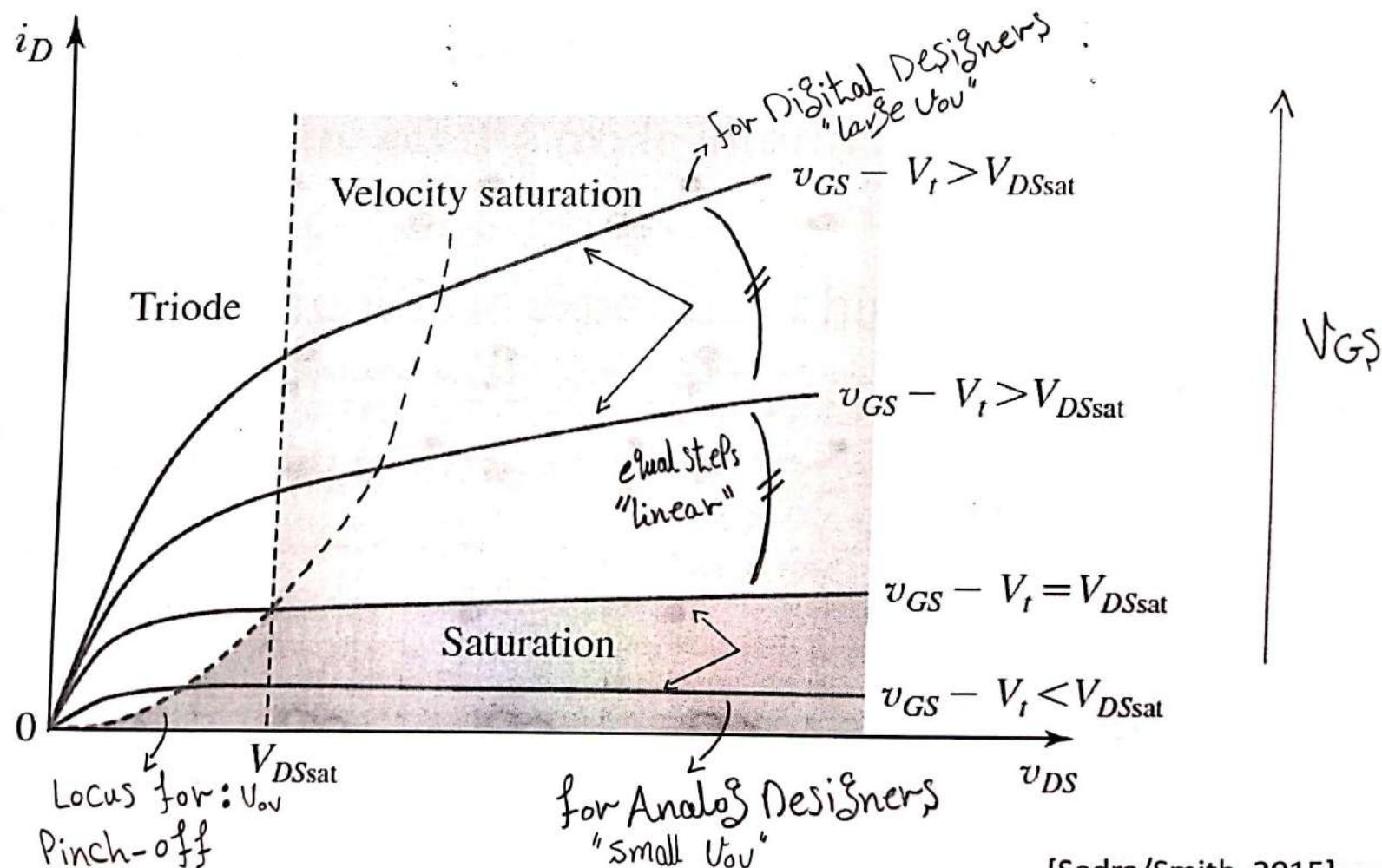
$$V_{ov} \sim 0.1 - 0.3 \text{ V}$$

$$\therefore V_{ov} < V_{DSSat}$$

Velocity Saturation: IV Characteristics

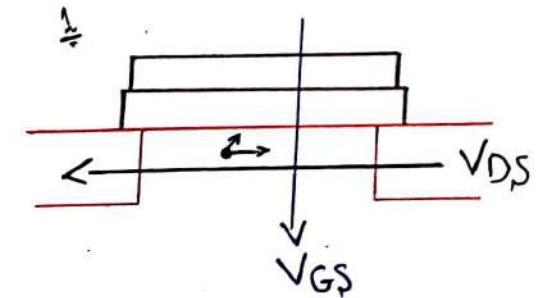
- Velocity sat happens before pinch-off if $V_{DSSsat} < V_{ov}$

$$I_D = C_{ox} W v_{sat} \cdot \left(V_{ov} - \frac{V_{DSSsat}}{2} \right) (1 + \lambda V_{DS})$$



Short Channel Effects: Mobility Degradation

- Vertical electric field: $E_{vert} = V_{GS}/t_{ox}$ ↑ scaling down ↓
 - Attracts carriers into channel
 - Long channel: $Q_{channel} \propto E_{vert}$
- At high vertical field strengths (V_{GS}/t_{ox})
 - The carriers scatter off the oxide interface more often
 - Scattering slows carrier progress (decreases the average velocity)
 - Leads to less current than expected at high V_{GS}
- Mobility degradation can be modeled by replacing μ with a smaller μ_{eff} that is a function of V_{GS}
 - ↳ decreases



↳ By scaling down t_{ox} : The vertical electric field increases ($E_{vert} \propto 1/t_{ox}$)

* By increasing E_{vert} it pulls the electrons (which are moving towards the drain) towards the interface between the silicon and the oxide increasing the scattering which decreases the average velocity of the carriers (as if μ decreases)

$$\mu_{eff}$$

$$V_{GS} \propto \frac{1}{\mu_{eff}}$$

↳ two opposite factors

1- increasing V_{GS} gives larger μ_{eff} which increases the current.
2- the previous factor will decrease as a result of mobility degradation.

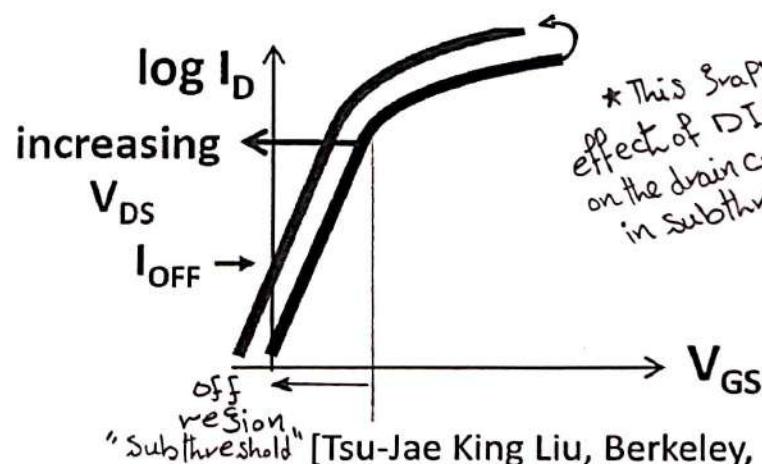
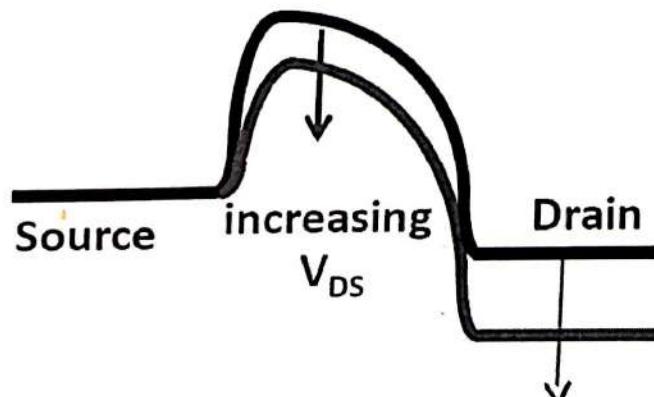
Short Channel Effects: DIBL

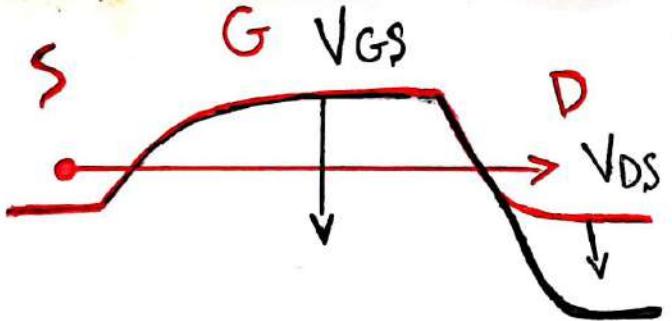
- DIBL: Drain-Induced Barrier Lowering
- Electric field from drain affects threshold voltage
 - More pronounced in short channel devices

$$V'_{TH} = V_{TH} - \eta V_{DS}$$

- η : DIBL coefficient $\sim 100mV/V$
- High drain voltage causes current to increase (similar to channel length modulation)
- Gate is losing control over the channel

The main function of the transistor depends on the control of the gate, unless it will be a resistor not a transistor.





(Energy Band Diagram)
Long channel

* for an electron @ Source wants to move to the drain it should pass across the gate barrier, the function of the Voltage on the Gate is to lower this barrier and let the electron pass.

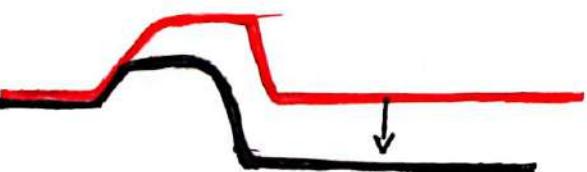
→ The Voltage @ drain (V_{DS}) lowers the drain

* for long channel device: The drain Voltage only affects the drain energy (Potential).

* for short channel: lowering the drain (increasing Voltage @ Drain) affects also the gate barrier height (which is the threshold voltage) $V_{th} \downarrow \therefore I_D \uparrow$

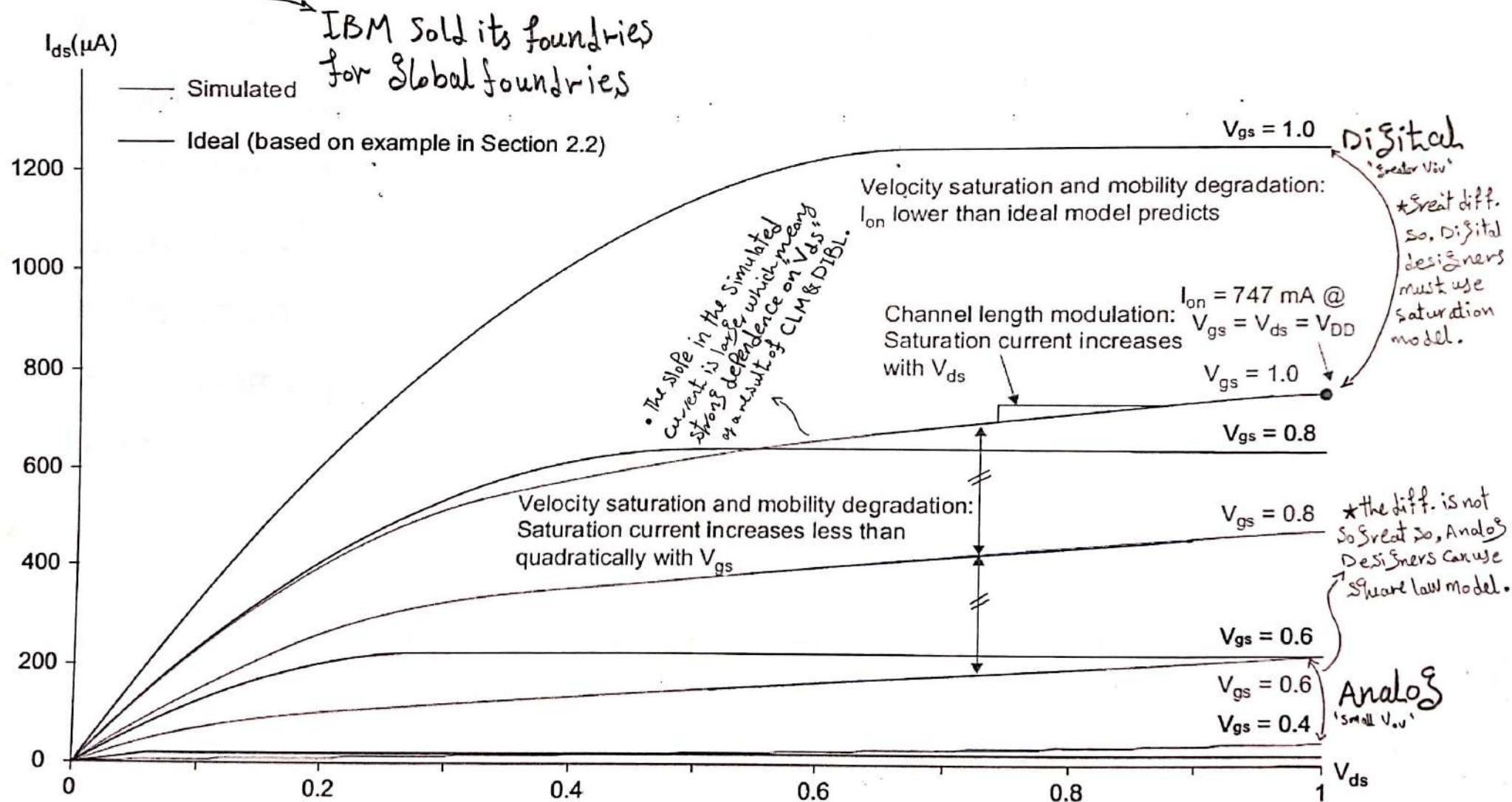
$$I_D = I_{DS} (1 + \lambda V_{DS}) \rightarrow \text{Same as channel length modulation}$$

$$\therefore \lambda = CLM + DIBL + \begin{matrix} \text{any other factor which} \\ \text{makes } V_{DS} \text{ affects} \\ \text{the current.} \end{matrix}$$



Short-Channel MOSFET I-V Ccs

- 65 nm IBM process, $V_{DD} = 1.0$ V



Why Do We Still Learn Square-Law?

- For digital and RF, use min L
 - ① ■ You care most about speed and power
- For analog, we use relatively long L
 - We care about matching, gain, and low-frequency noise
- For digital V_{ov} is large = $V_{DD} - V_{TH}$
- ② ■ Short channel effects (e.g., velocity sat.) are more pronounced
- For analog V_{ov} is relatively low
 - Short channel effects (e.g., velocity sat.) are less pronounced
- ③ □ Simple model provides a great deal of intuition that is necessary in analog design

* ■ We must simulate the circuit to get more accurate results

→ simple models guide us what parameter to increase and which one to decrease → Trends
but we take more accurate results from the simulation. ↗ which device

* Without this intuition you'll make random sweeps and random iterations (unguided random iterations)

& You won't reach the optimum design point.

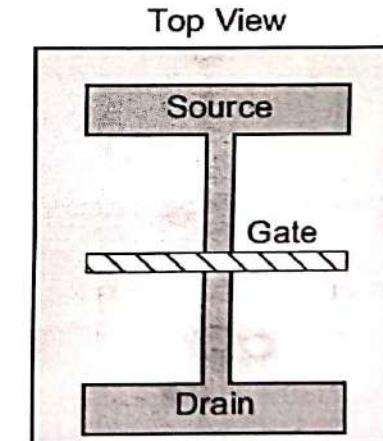
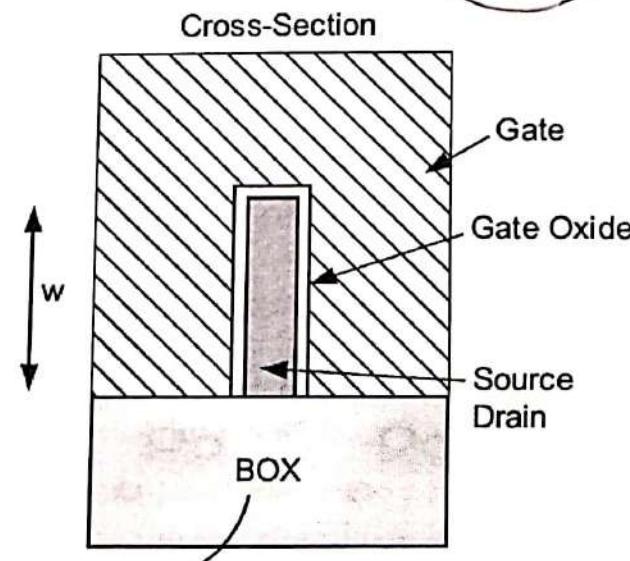
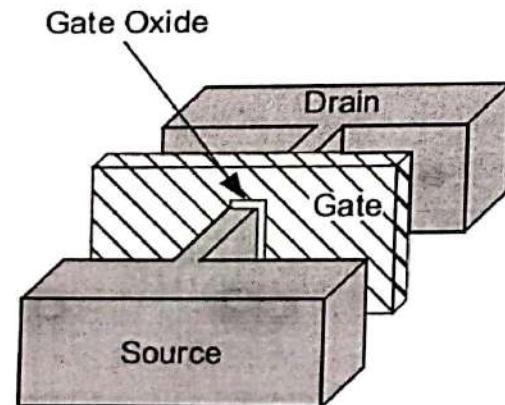
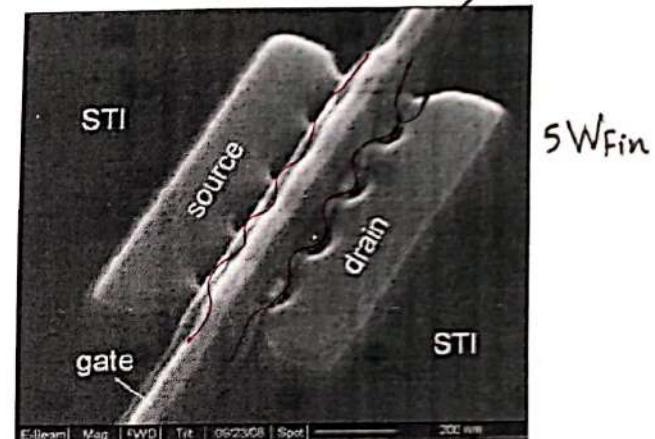
Is the Square-Law Still Valid?

- Valid “relatively” if
 - 1 ■ Relatively long channel length (not minimum length)
 - 2 ■ Strong inversion, but not too strong (e.g., $V_{ov} \approx 100 - 300mV$)
 - For small and negative V_{ov} : moderate and weak inversion (subthreshold operation)
 - ID-VGS relation gradually becomes exponential
 - For large V_{ov} : velocity saturation happens before pinch-off
 - ID-VGS relation becomes linear
- If the above conditions are not valid (If I need to use minimum L or larger or smaller V_{ov} than the above range)
 - Use design charts or look-up tables, e.g., gm/ID design methodology (to be explained later) * As there is no simple equation to model the modern mosfet devices.
- Actually, better to use gm/ID methodology even if the above conditions are valid!
 - much more effective and productive designer.

FinFET

- Planar CMOS cannot be scaled below 20nm due to excess leakage current and severe short channel effects
- FinFET: gate has better control on the channel
 - Intel's version is called trigate FET
 - Generally: multigate transistor
- In the future: Gate-all-around

*% More Complex as this is constant width which is: $W_{Fin} * 5$*



Buried Oxide (Better): increases Performance [Weste & Harris, 2010] 51

* More control for the Gate, and enables us to do vertical stacking
↓
i.e. Boosting No. of Mos. on chip.

References

- A. Sedra and K. Smith, "Microelectronic Circuits," Oxford University Press, 7th ed., 2015
- B. Razavi, "Fundamentals of Microelectronics," Wiley, 2nd ed., 2014
- B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2nd ed., 2017
- N. Weste and D. Harris, "CMOS VLSI Design," Pearson, 4th ed., 2010

Thank you!

Dr. Hesham Omran (Lecture)

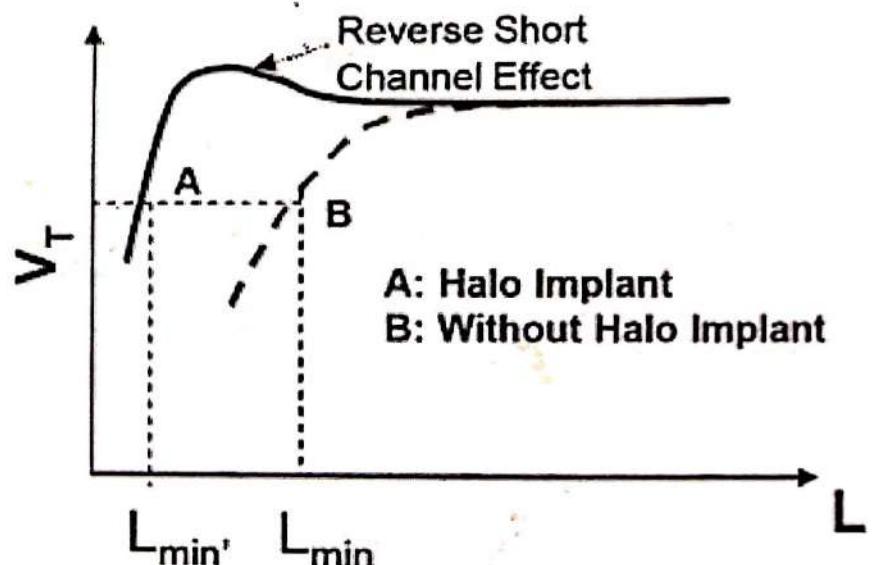
Fady Sabry Negm (Slides)

Short Channel Effect (V_t roll-off)

- In short channel devices, S/D depletion regions extend into the channel

- Impacts the amount of charge required to invert the channel
- And thus makes V_{TH} a function of channel length
- Somewhat similar to DIBL

- Short channel effect (SCE):
 - V_{TH} decreases with smaller L
- Reverse short channel effect (RSCE):
 - Halo doping is used to fix DIBL
 - V_{TH} increases then decreases with smaller L



★ Slide (5): unlike BJT, MOSFETs (Generally FETs) are 'Unipolar' which means that they have only one charge carrier e^- or h^+ while BJT (Bipolar Junction transistor) is 'Bipolar' as there are both e^- & h^+ as the base is different type than Emitter & Collector.

★ Slide (6): $V_{GS} = V_{th}$ \rightarrow ∴ Inversion has occurred (the channel is formed)
Before V_{th} (Subthreshold) there is accumulation but the ~~whole~~ whole channel is not yet formed.

- $V_{th} = 0$ isn't good as if you make any swing it can go to -ve. but it can be used in some applications (Power amplifier).

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

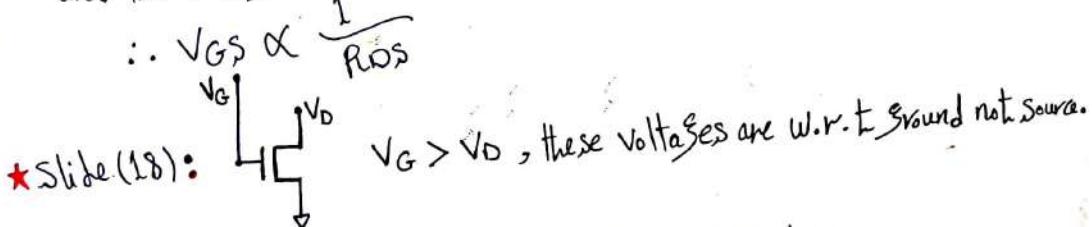
actually: Mathematically if $V_{th} = 0$, I_D has a value
But you can't neglect the physical behavior of the device.

★ Slide (15): We find from these relations that there is a linear relation between the current & the electric field, current & the voltage which is the characteristics of a resistive element.

∴ VCR

- There is an inverse relation between the resistance of the channel and the voltage, this voltage is V_{GS} as it is the "control voltage"

$$\therefore V_{GS} \propto \frac{1}{R_{DS}}$$



★ Slide (21): Why there is no charge @ Pinch-off point?

$$Q = C \Delta V = C (V_{ov} - V_{DS}), @ \text{Pinch-off Point } V_{DS} = V_{ov}$$

$$\therefore Q = \text{Zero.}$$

وَمَا أُوتِيتُهُ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Allah almighty said in the Qur'an :
“and you 'O humanity' have been given but little knowledge.”

لَوْزَنَ النَّاسُ كُلُّهُمْ وَسْتَصْبِغُوا ذُمِرًا ترکوهْ مَا قَامَ لِلنَّاسِ وَنِيَا وَلَوْزَنِ

The Muslim Caliph Umar ibn Abdulaziz, May Allah have mercy on him, Said:
“If every time people found something difficult, they abandoned it, then neither worldly affairs nor religion would have ever been established for people.”

- All Credits for these lectures go to **Dr. Hesham Omran**, Associate Professor at Ain Shams University and CTO at Master Micro, May Allah bless Dr. Hesham for these Lectures.

<https://www.master-micro.com/professional-courses/analog-ic-design>



- These Notes were made by: **Fady Sabry Negm** and any success or guidance is from Allah, and any mistake or lapse is from me and Satan.