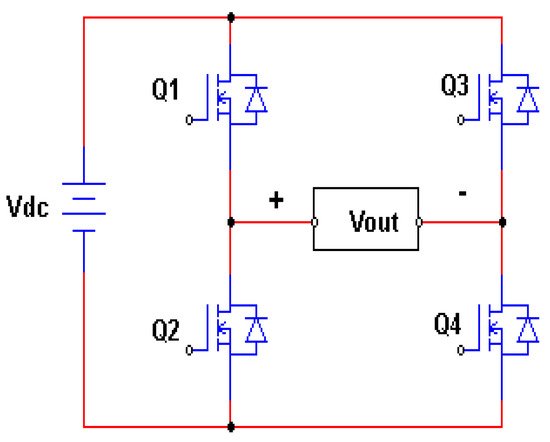
ENGR 4500 – H Bridge Design

An H Bridge Design consists of 4 Power MOSFET, where 2 of them turns on and the other 2 turns off, and a gate driver IC for each of the MOSFET. Here is an example schematic



* Q1 and Q4 to turn on and Q2 and Q3 to turn off on 1 cycle
* And then Q1 and Q4 to turn off and Q2 and Q3 to turn on
* Avoid Q1 and Q2 (and Q3 and Q4) to simultaneously be on

Task to build an H Bridge

1. Build a PWM generator
2. Use a Half-Bridge Gate Driver IC to control the left-hand side of H Bridge
3. Repeat for control of the right-hand side of H-Bridge

PWM Generator

1. **TLC555/NE555**
2. **SN74HC04N**/CD74HC4049/74HC4049N (Hex Inverter)

Gate Driver

1. **IR2113**
2. **LM5100**
3. LMG1205
4. LT7061

Power MOSFET

1. **IRLZ44N**
2. **IPA029N06N**

[PWM Generator Design 3](#_Toc117059988)

[1st Design TLC555 Variant (GreatScott) 3](#_Toc117059989)

[2nd Design NE555 (Astable Mode) 8](#_Toc117059990)

[2nd Design TLC555 Variant (Astable Mode) 14](#_Toc117059991)

[3rd Design ICM5555 21](#_Toc117059992)

[H Bridge Gate Driver Design 23](#_Toc117059993)

[Design 1: LM5101/IPA032N06N3 23](#_Toc117059994)

[Design 2: LM5106/IPA032N06N3 27](#_Toc117059995)

[Design 3: IRLZ44N/IR2113 36](#_Toc117059996)

# PWM Generator Design

## 1st Design TLC555 Variant (GreatScott)



Diagram

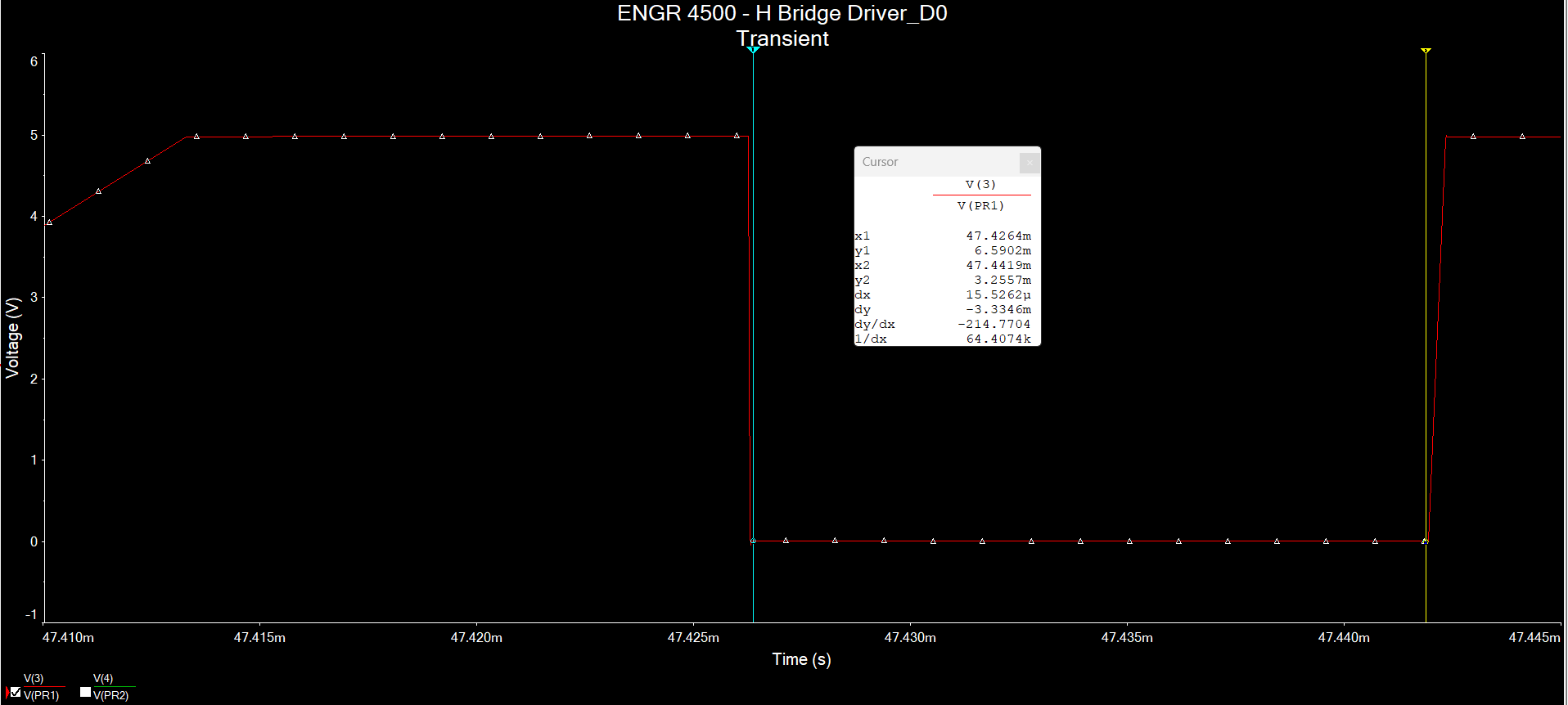
Description automatically generated

Ton: 47.4262m - 47.4133m = 0.0129m

A screenshot of a computer

Description automatically generated with medium confidence

Toff: 47.4419 - 47.4264m = 0.01555m



Period = 1/(Toff + Ton) = 1/(0.0129m+0.0155m) = 3.5211\*10^4 Hz = 35.211kHz

Using cursors as measurement: 35.0383 kHz

A picture containing text, computer, computer, indoor

Description automatically generated

Still first design but switch out the 10nF electrolytic and 2.2nF with regular capacitors

Diagram

Description automatically generated

Ton: 41.4492m-41.4363m = 0.0129m



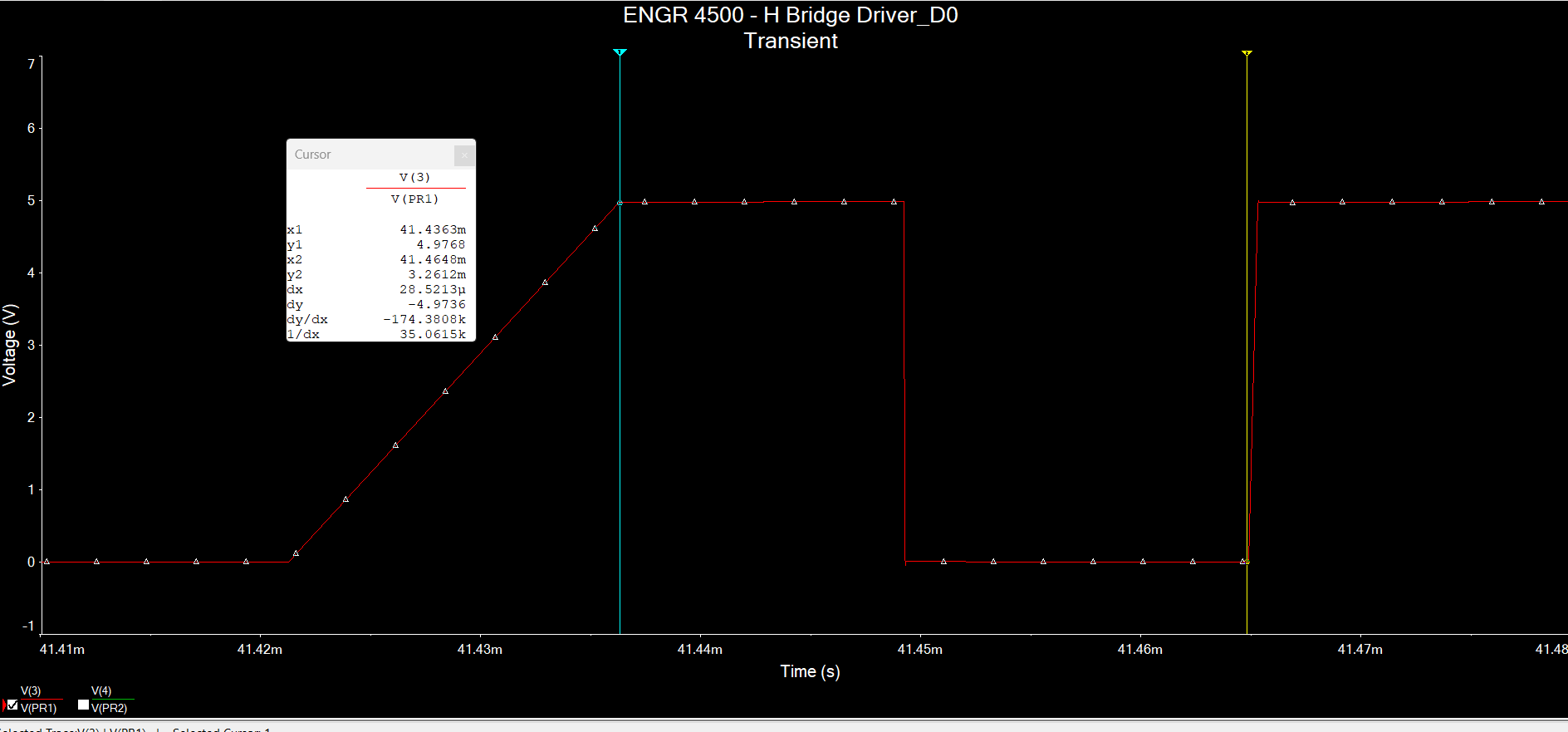
Toff: 41.4648m – 41.4493m = 0.0155m

A screenshot of a computer screen

Description automatically generated with medium confidence

Period: 1/(0.0129m+0.0155m) = 3.5211\*10^4 Hz = 35.211kHz

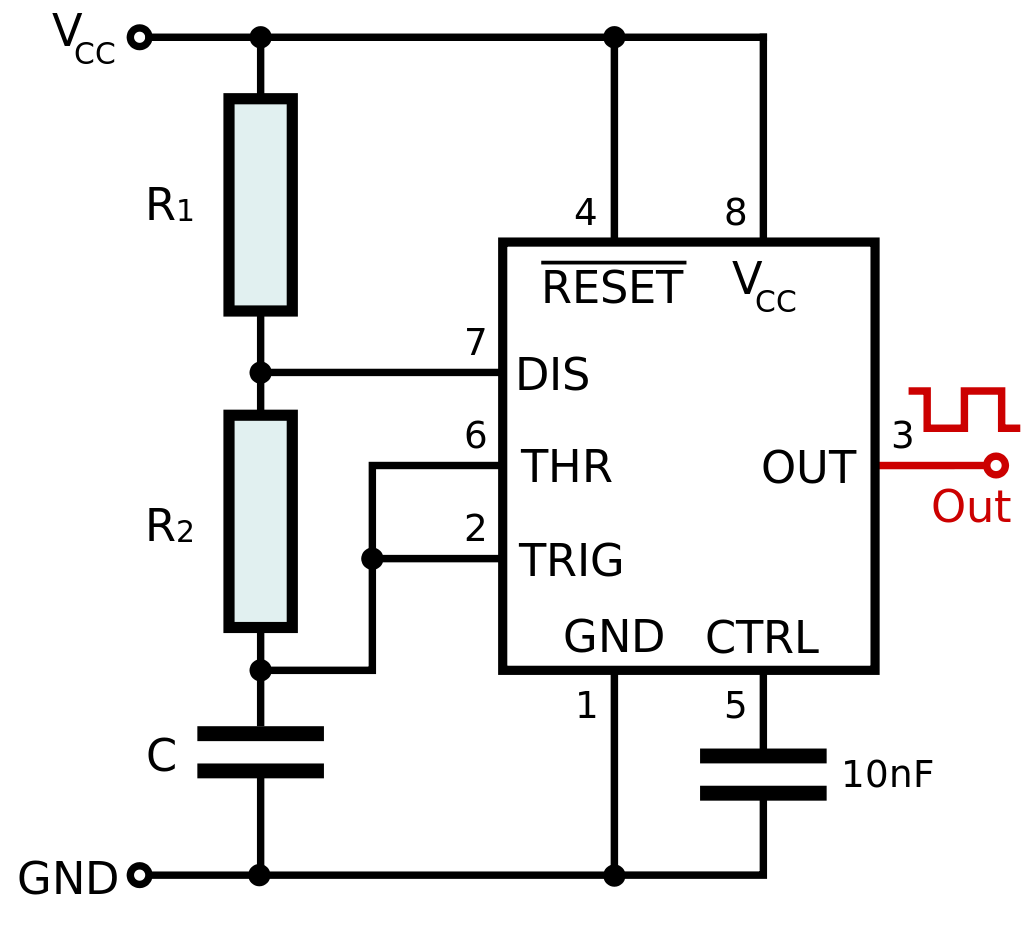
Cursor measurement: 35.0615kHz



## 2nd Design NE555 (Astable Mode)

We can use the NE555 in astable mode using this schematic.

*Note: This circuit below only allows for 50% or higher Duty Cycle*



The frequency is defined as

The duty cycle is defined as

The output high interval is defined as

The output low interval is defined as

We want a 100kHz PWM signal with a duty cycle of 50-55% to feed into the Gate Driver. Let us say and . Determine C

The capacitor value is not standard plus the Duty cycle is not ~52%. Let us redo our calculations but first determine the duty cycle

Let

Still not standard but we are close to 100pF or 150pF standard values

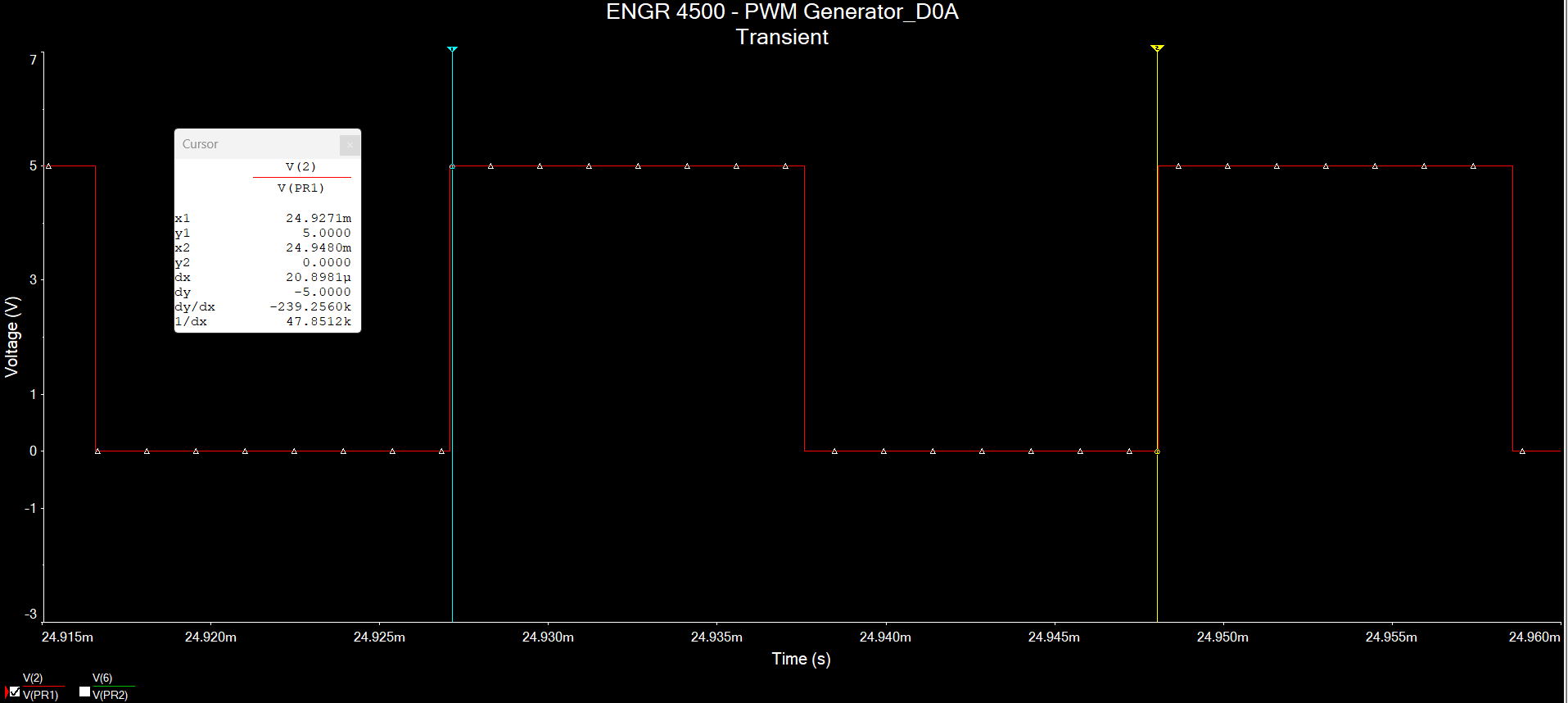
From the Wikipedia page on 555 timer astable mode, there is actually a list of standard component values:

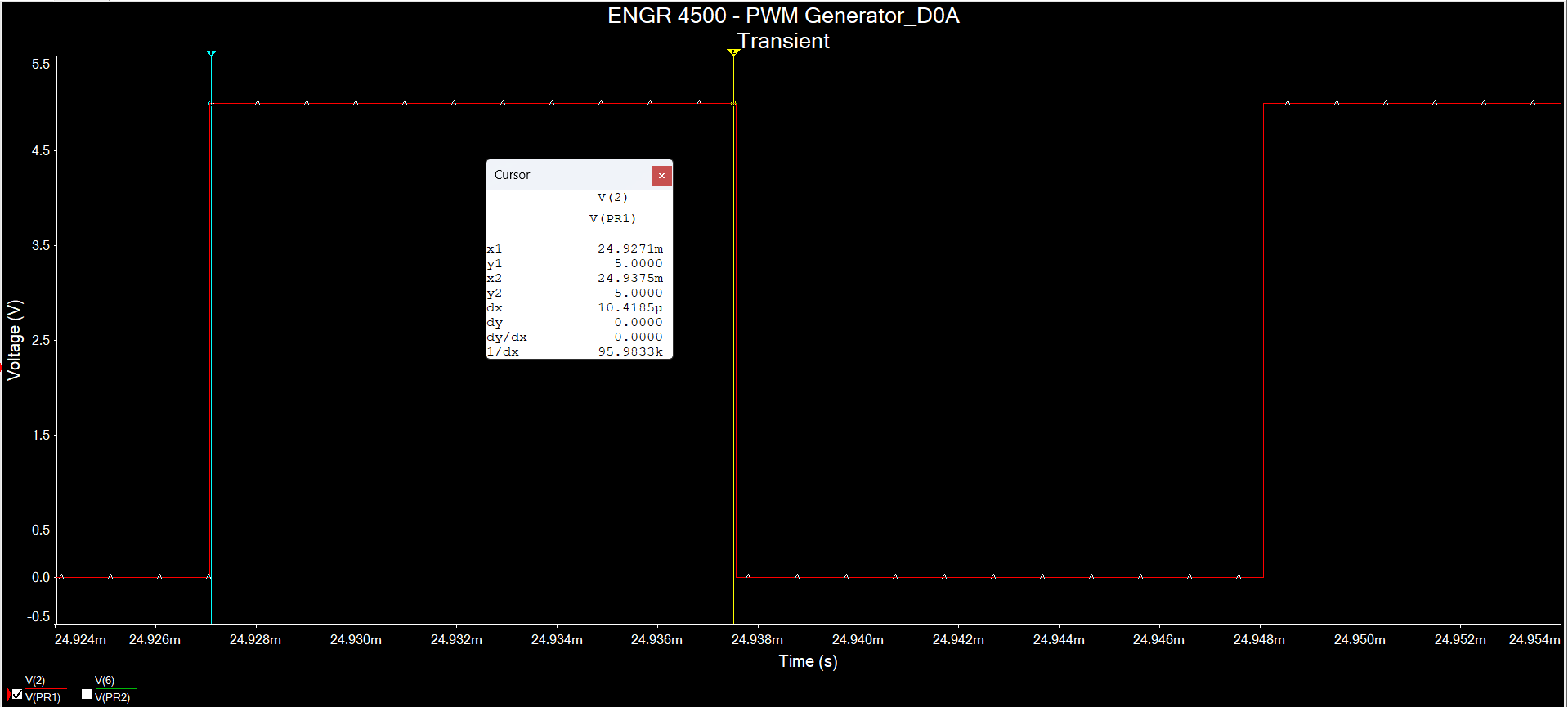
Table

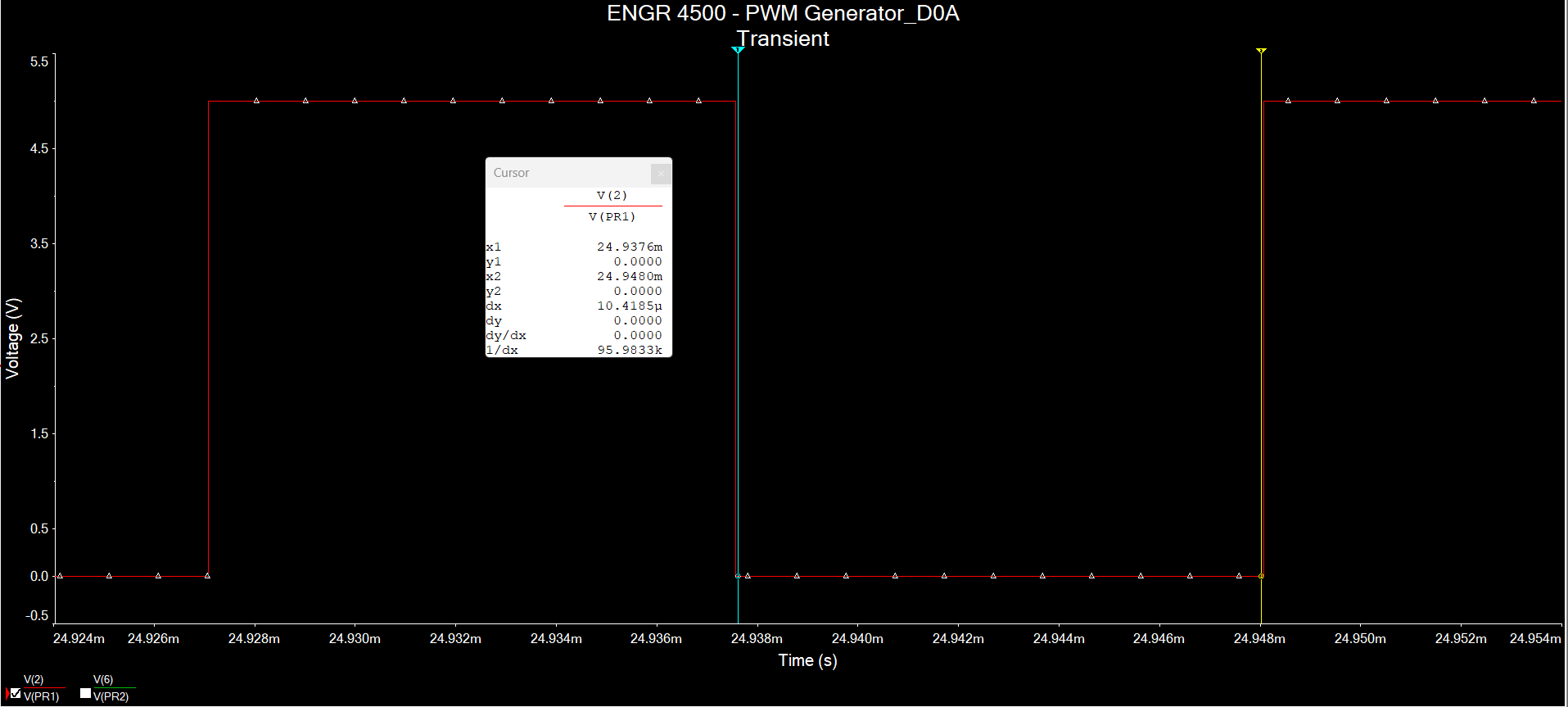
Description automatically generated

We can see that if we use R1 = 8.2k, R2 = 68k, and C = 100pF results in 52.8% duty cycle for a 100kHz signal

Simulation Results:







But the interactive mode shows that the frequency is 89.4kHz

Diagram, schematic

Description automatically generated

But changing R1 to 3.3k and R2 to 56k and keeping C1 results in a calculated frequency

Simulation results shows it is 108kHz

Diagram, schematic

Description automatically generated

But with R1 = 7.5k and R2 = 68k and keeping C1 results in a calculated frequency of 100.536kHz

Simulation result shows it is 89.4kHz

Diagram, schematic

Description automatically generated

R1 = 7.5k and R2 = 56k. Keep C1 results in a calculated frequency of 120.727kHz

Simulated results shows 101kHz

Diagram, schematic

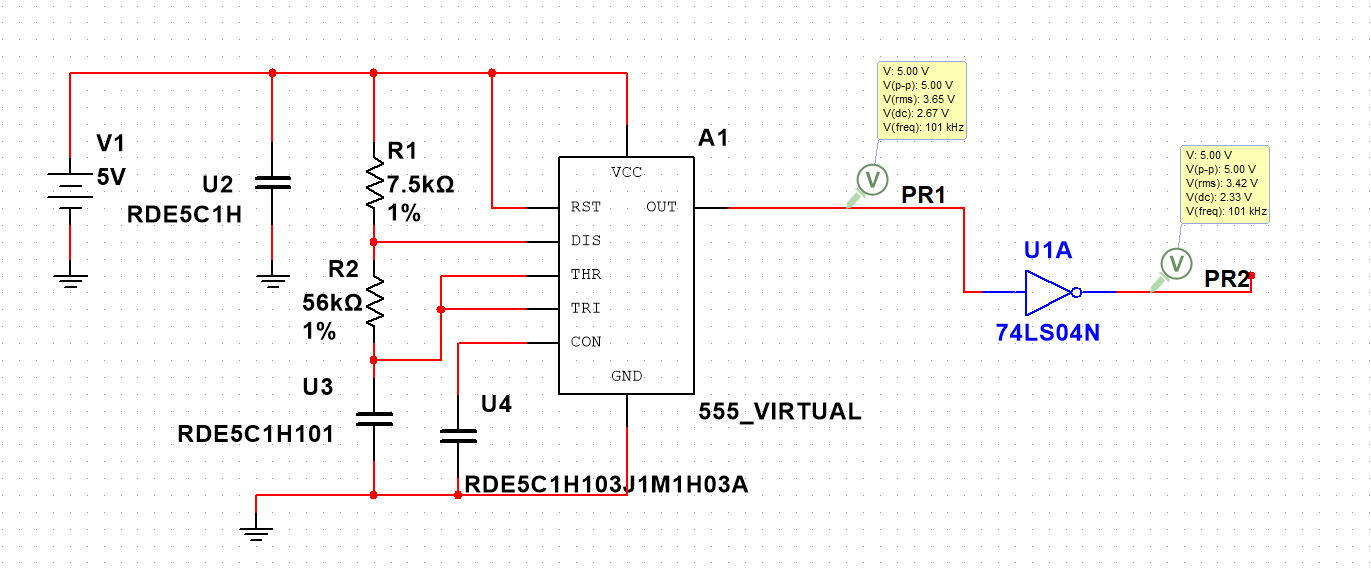
Description automatically generated

We should proceed with this rather than the 2nd or 3rd design for now

Part: [**RDE5C1H104J2K1H03B**](https://www.digikey.com/en/products/detail/murata-electronics/RDE5C1H104J2K1H03B/10691753) (0.1uF ceramic capacitor)

[**RDE5C1H101J0M1H03A**](https://www.digikey.com/en/products/detail/murata-electronics/RDE5C1H101J0M1H03A/4771115) (100pF ceramic capacitor)

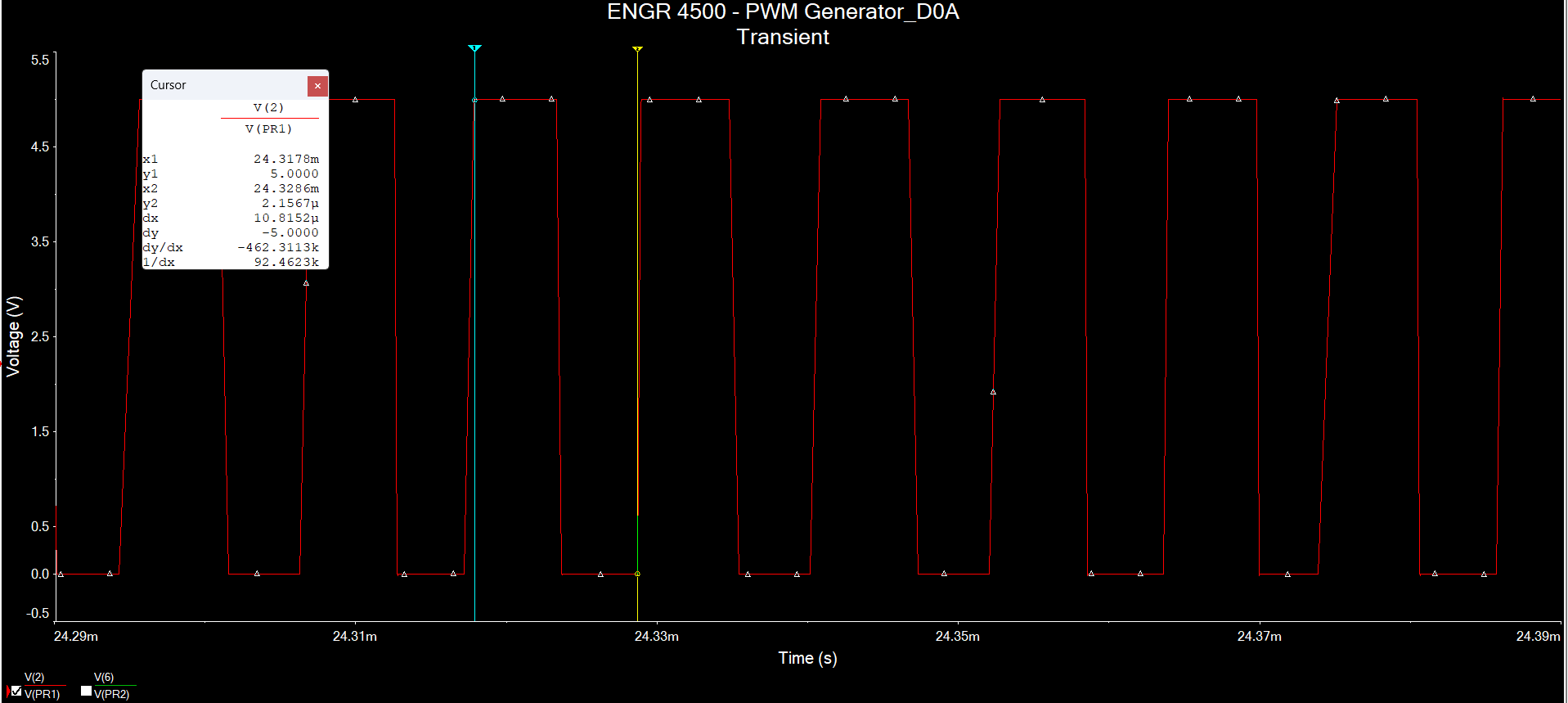
[RDE5C1H103J1M1H03A](https://www.murata.com/en-us/products/productdetail?partno=RDE5C1H103J1M1H03A) (10nF ceramic capacitor)



## 2nd Design TLC555 Variant (Astable Mode)

I attempted to use the TLC555 with the schematic meant for the NE555. These were the poor results

Noninverted Signal (f = 92.4623k)



A picture containing graphical user interface

Description automatically generated

Graphical user interface

Description automatically generated

Inverted Signal Frequency (f = 92kHz)

A screenshot of a computer

Description automatically generated with medium confidence  
Graphical user interface

Description automatically generated

Graphical user interface

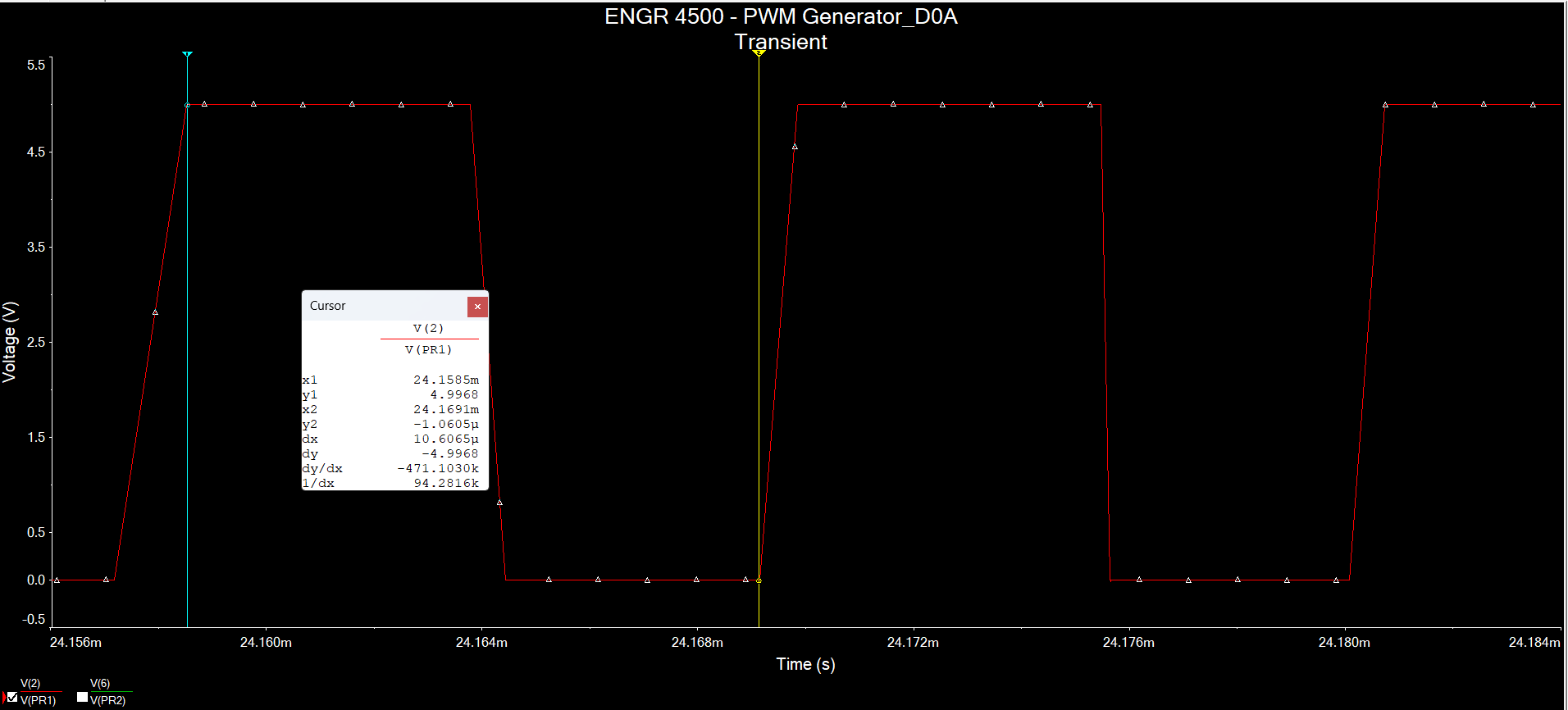
Description automatically generated

Added a 0.1uF ceramic and 1uF electrolytic capacitors in parallel to the TLC555 (power supply requirement according to datasheet)

Diagram, schematic

Description automatically generated

Noninverted Signal (f = 94.2816k)



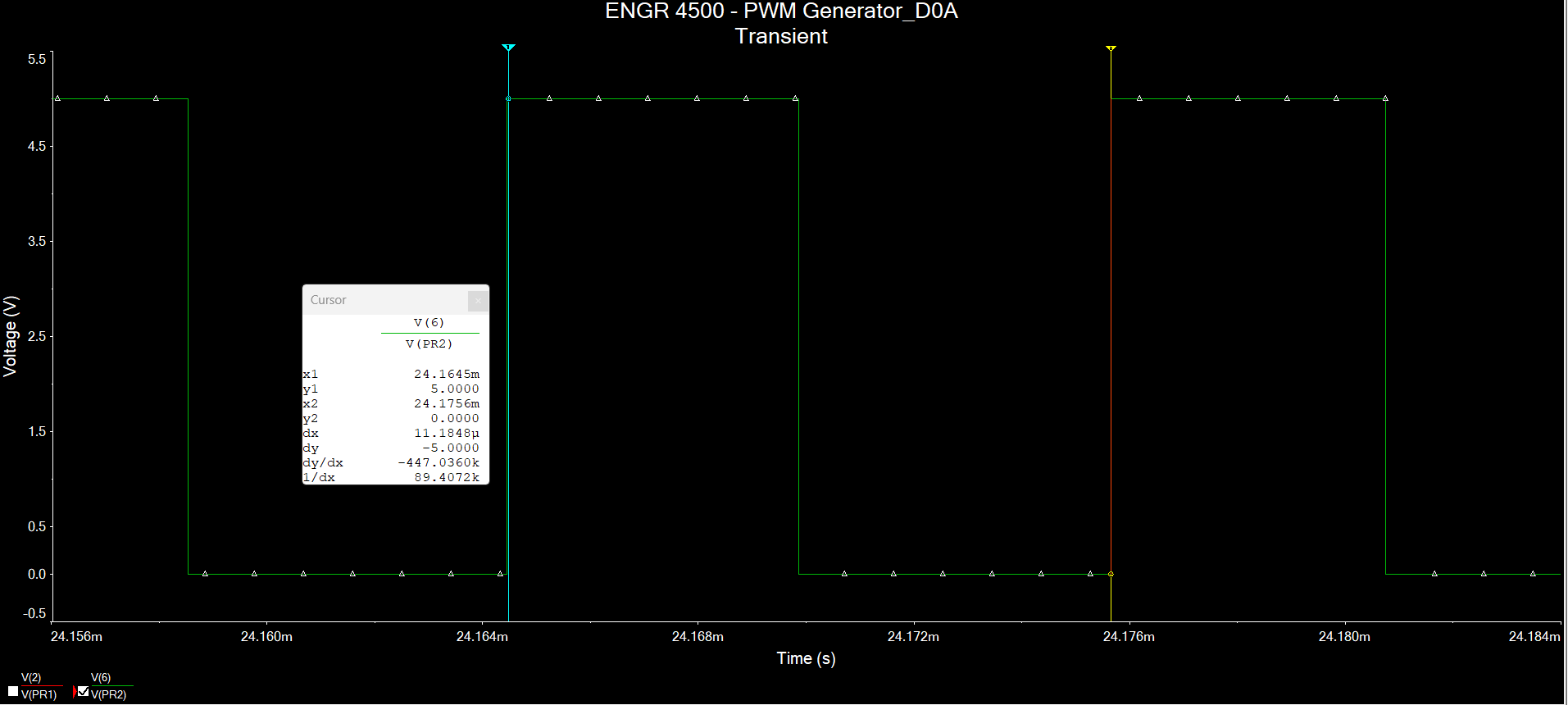
Graphical user interface

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

Inverted Signal (f = 89kHz)



Graphical user interface

Description automatically generated

Instead, using this [source](https://e2e.ti.com/support/clock-timing-group/clock-and-timing/f/clock-timing-forum/879112/faq-how-do-i-design-a-stable-timer-oscillator-circuits-using-lmc555-tlc555-lm555-na555-ne555-sa555-or-se555) and the given equation to find the oscillation frequency

Diagram, schematic

Description automatically generated

Rearranging the equation to find a suitable

We know we want a 100kHz signal. We can also set C = 100uF

Diagram, schematic

Description automatically generated

Simulation does not work

A picture containing chart

Description automatically generated

## 3rd Design ICM5555

General layout. We use (a) for 50% Duty Cycle

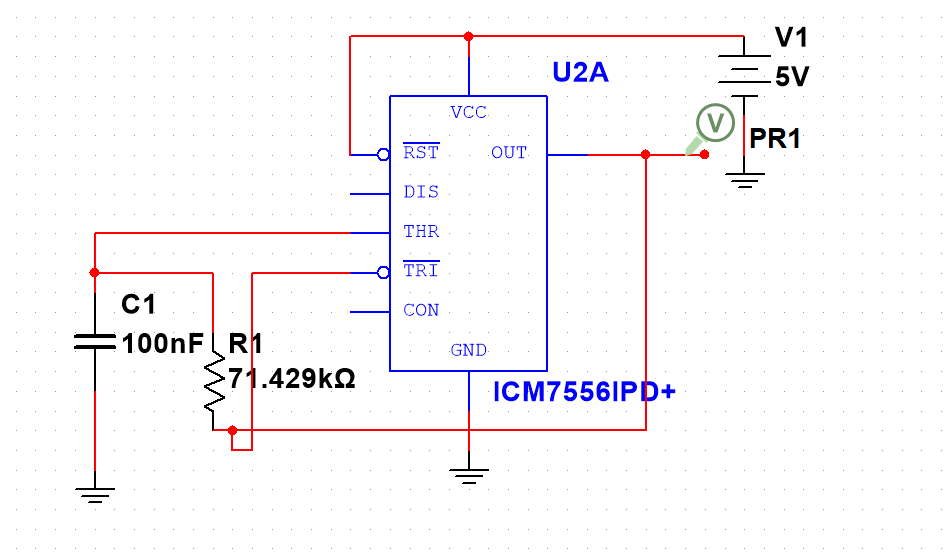
Diagram, schematic

Description automatically generated

For a 50% duty cycle,

Let us generate a 100kHz PWM. Say

We can check if this works in Multisim



The simulation produce no waveform

Graphical user interface, text, application

Description automatically generated

# H Bridge Gate Driver Design

## Design 1: LM5101/IPA032N06N3

Diagram, schematic

Description automatically generated

|  |  |
| --- | --- |
| Parameters | Value |
| Gate Driver | LM5101A |
| VDD | 10V |
| Qgmax | 52nC (datasheet of power mosfets) |
| fsw | 100kHz |
| Dmax | 60% |
| Vdh | 0.98V (datasheet of fast recovery diode) |
| Vhbr | 7.1V (datasheet of LM5101A) |
| Vhbh | 0.4V (datasheet of LM5101A) |

Select Bootstrap and VDD capacitor

* Bootstrap capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit in any circumstances during normal operation

The quiescent current of the bootstrap circuit must be 10uA max (from the datasheet of LM5101)

In practice, the bootstrap capacitor should be greater than the calculated value above to account for the power stage skipping a pulse due to load transients

The local VDD bypass capacitor should be 10x the above value

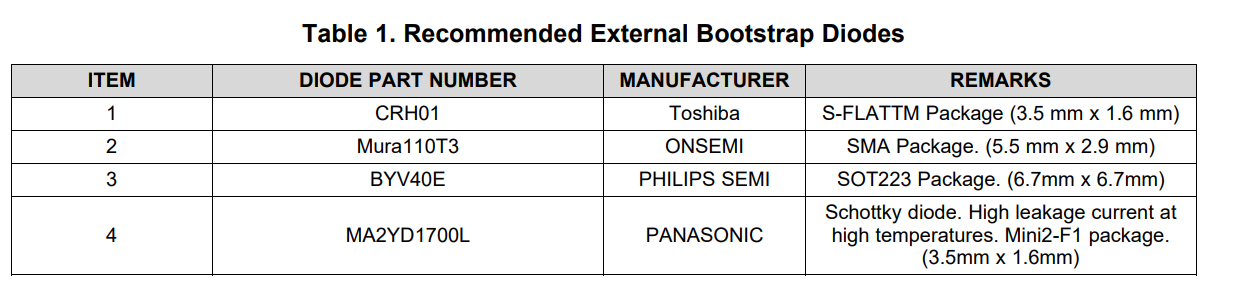
Note: Bootstrap and Bias Capacitors should be ceramic types with X7R dielectric

* Voltage rating must be 2x maximum VDD to account for loss over capacitance
  + In this case, 2x10V = 20V

Select External Bootstrap Diode and Resistor

* Bootstrap capacitor is charged by the VDD through the internal bootstrap diode every cycle when LS MOSFET turns on
  + Charging the capacitor involves high peak currents and the power dissipation in the internal bootstrap diode may be significant
  + For high frequency and high capacitive loads, it may be necessary to consider an external bootstrap diode in parallel with internal bootstrap diode to reduce power dissipation
* Examine Application Note  [SNVA083.](https://www.ti.com/lit/an/snva083b/snva083b.pdf?ts=1665259176240)

The power dissipation through the gates



All of these are not available at Mouser. Only CRH01 and BYV40E is available at digikey. CRH01 has a pspice file

We will use the external bootstrap diode once we have the full transmitter network

* The Bootstrap resistor is selected to reduce the inrush current in Dboot. Recommended bootstrap resistor size is between 2 ohms and 10 ohms. Let us select 2.2 ohms

Select Gate Driver Resistor

* Gate Driver Resistor is sized to reduce ringing caused by parasitic inductances and capacitances and limit the current coming out of the gate driver.
* Use 4.7-ohm resistors. VOH is 0.45V and VOL is 0.25V (from datasheet)

Estimate the driver power losses

Allowable IC power loss (where Tj is junction temperature, Ta is ambient temperature, and Rja is the junction to ambient thermal resistance)

Therefore our component list is

|  |  |  |
| --- | --- | --- |
| Part | Component Value | Manufacturer |
| Bootstrap Capacitor (Ceramic X7R) | 100nF (0.1uF) | RDER71H104K0M1H03A  Murata |
| Bypass Capacitor (Ceramic X7R) | 1uF | RDER71H105K2M1H03A  Murata |
| External Fast Recovery Diode |  |  |
| Bootstrap Resistor | 2.2 ohm (10W) | 40J2R2E by Ohmite |
| Gate Driver Resistor | 4.7 ohm (10W) | 30J4R7E by Ohmite |

Schematic:

Diagram

Description automatically generated

Simulation Result: N/A (Subckt error on the LM5101A model itself)

## Design 2: LM5106/IPA032N06N3

Diagram, schematic

Description automatically generated

|  |  |
| --- | --- |
| Parameters | Values |
| Gate Driver IC | LM5106 |
| VDD | 10V |
| Qgmax | 53nC |
| fsw | 100kHz |
| Dmax | 60% |
| Ihbo | 10uA |
| VDh | 0.98V |
| VHBR | 7.3V |
| VHBH | 0.4V |

*Select Bootstrap and VDD capacitor*

Just like for LM5101 the bootstrap capacitor should be greater than calculated values to account for transients

And just like LM5101 the bypass capacitor should be 10x greater than the bootstrap capacitor

And just like LM5101, the bootstrap and bypass capacitor should be ceramic X7R type with voltage rating twice the allowed VDD

*Selecting Resistor Values for Deadtime*

* Use Figure 19 from Datasheet

Chart, line chart

Description automatically generated

Let us set a deadtime of 500ns. We may need to adjust this later in the simulation

*Select Gate Resistor*

* Not in the LM5106 datasheet but we can use the procedure from LM5101
* Let us use a 4.7-ohm resistor. Voh is 0.85V and Vol is 0.4V

*Power Dissipation Considerations*

*Select External Diode*

* Does not have information from LM5106 Datasheet. But we can use the LM5101 datasheet as a guideline. Let us use the CRH01 for LM5106

Parts List

|  |  |  |
| --- | --- | --- |
| Part | Value | Manufacturer |
| Bootstrap Capacitor (Ceramic X7R) | 100nF (0.1uF) | RDER71H104K0M1H03A  Murata |
| Bypass Capacitor (Ceramic X7R) | 1uF | RDER71H105K2M1H03A  Murata |
| External Fast Switch Diode | 200V 1A 34ns reverse time | CRH01 by Toshiba |
| Deadtime Resistor | 90kOhms 1% 0.5W | CMF5590K000BHEB by Vishay |
| Gate Resistor | 4.7 ohm (10W) | 30J4R7E by Ohmite |
| MOSFET Filter Capacitor | 100uF | KCM55WC71E107MH13 by Murata |

Schematic:

Diagram, schematic

Description automatically generated

Simulation (of LHS):

Chart

Description automatically generated

A picture containing night

Description automatically generated

Simulate with Complimentary PWM signal (RHS)

Diagram, schematic

Description automatically generated

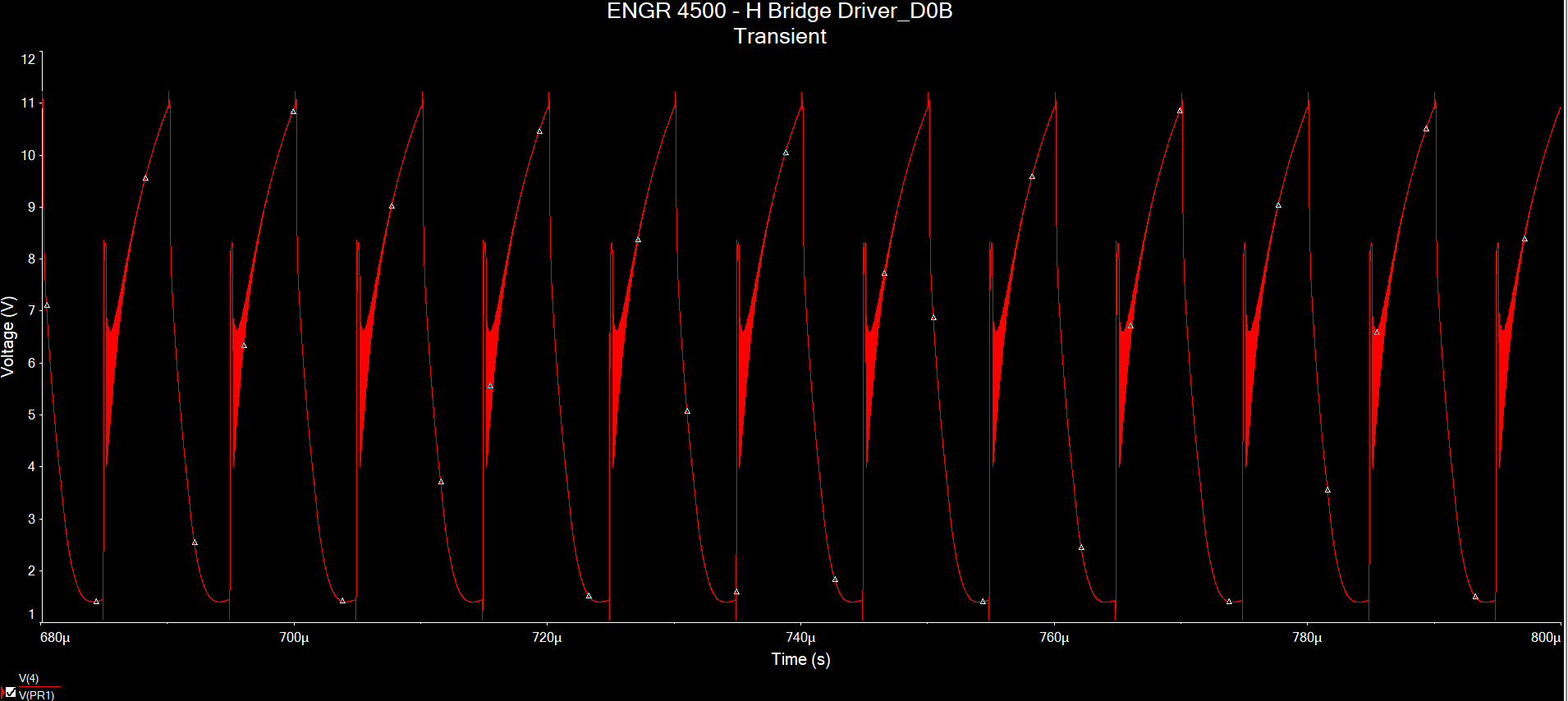
Chart

Description automatically generated

A picture containing light, different

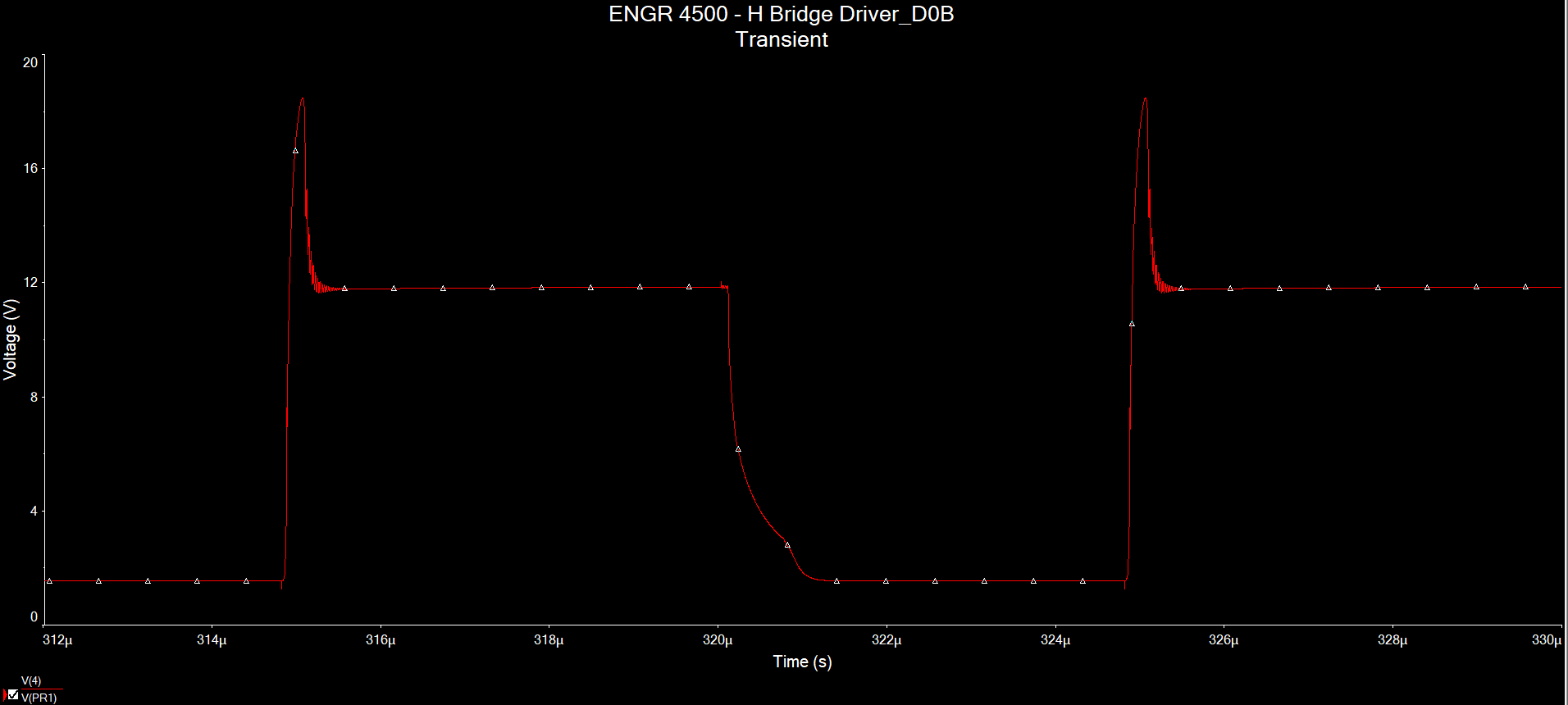
Description automatically generated

Now add in HHSD630ELL101MJC5S for the 100uF capacitor and see how it behaves

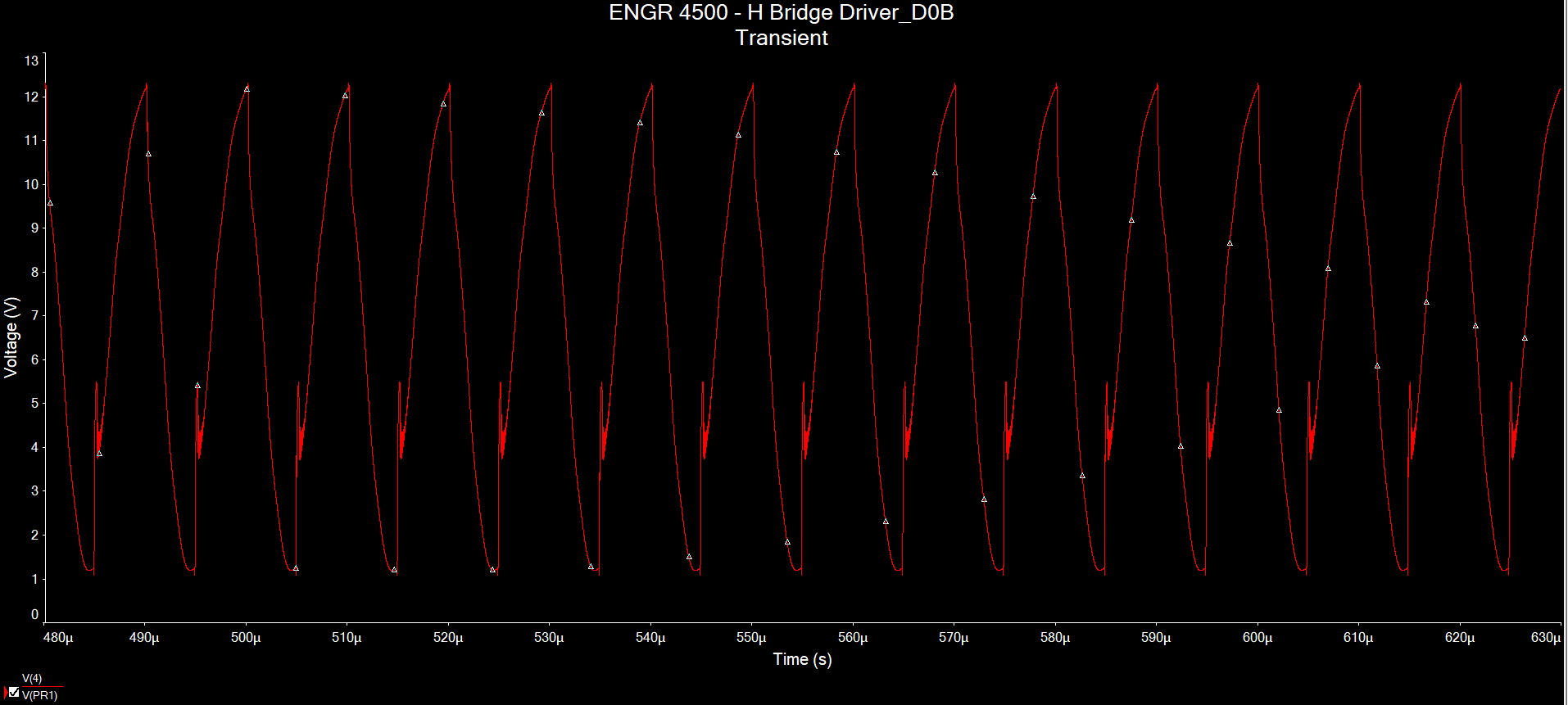


This aluminum organic hybrid capacitor is no good. Try a different one

Try EMZR350ARA101MF61G an aluminum electrolytic capacitor



Not good either. Try a ceramic capacitor KCM55WC71E107MH13 from Murata



Imperfect Sinusoidal Wave – looks better than the aluminum electrolytic capacitors

Now combine LHS and RHS into one Full Bridge Inverter

Diagram, schematic

Description automatically generated

Simulation Results

Background pattern

Description automatically generated

## Design 3: IRLZ44N/IR2113

Using GreatScott H-Bridge Inverter design from his DIY Wireless Power Transfer video

Diagram, schematic

Description automatically generated

We can replace the LM7805 with a 5V DC source for simulation purposes only. Also replace the TLC555 and 74HC4049N (constitutes the PWM generator) with PWM\_Complementary component from Multisim. As a result, this is the simulation circuit schematic:

Diagram, schematic

Description automatically generated

The part in this simulation are RDER71H104K0M1H05A (100nF ceramic capacitor), RCEC71H106K3A2H03B (10uF ceramic capacitor), and UF4007 (fast recovery diode)

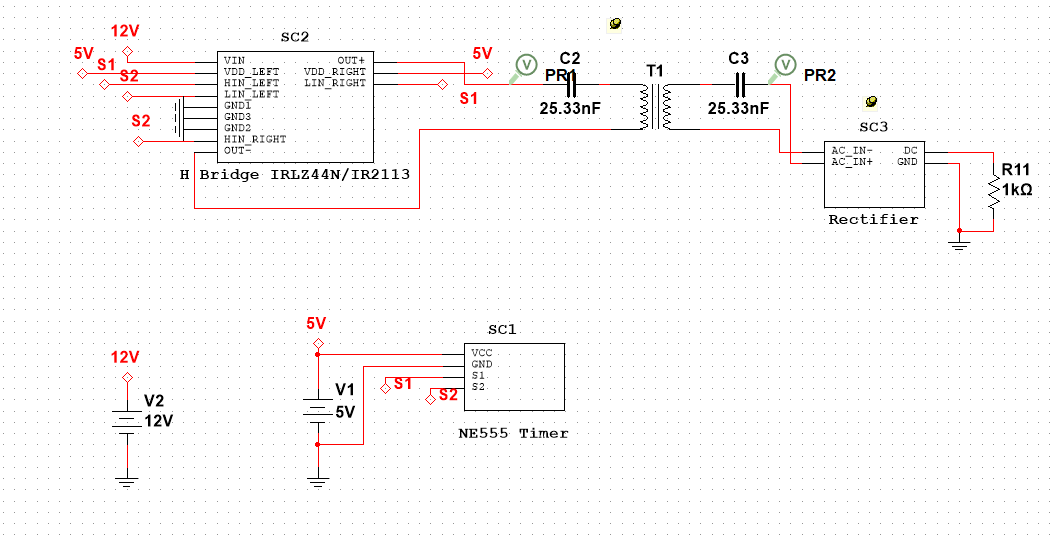
Chart, histogram

Description automatically generated

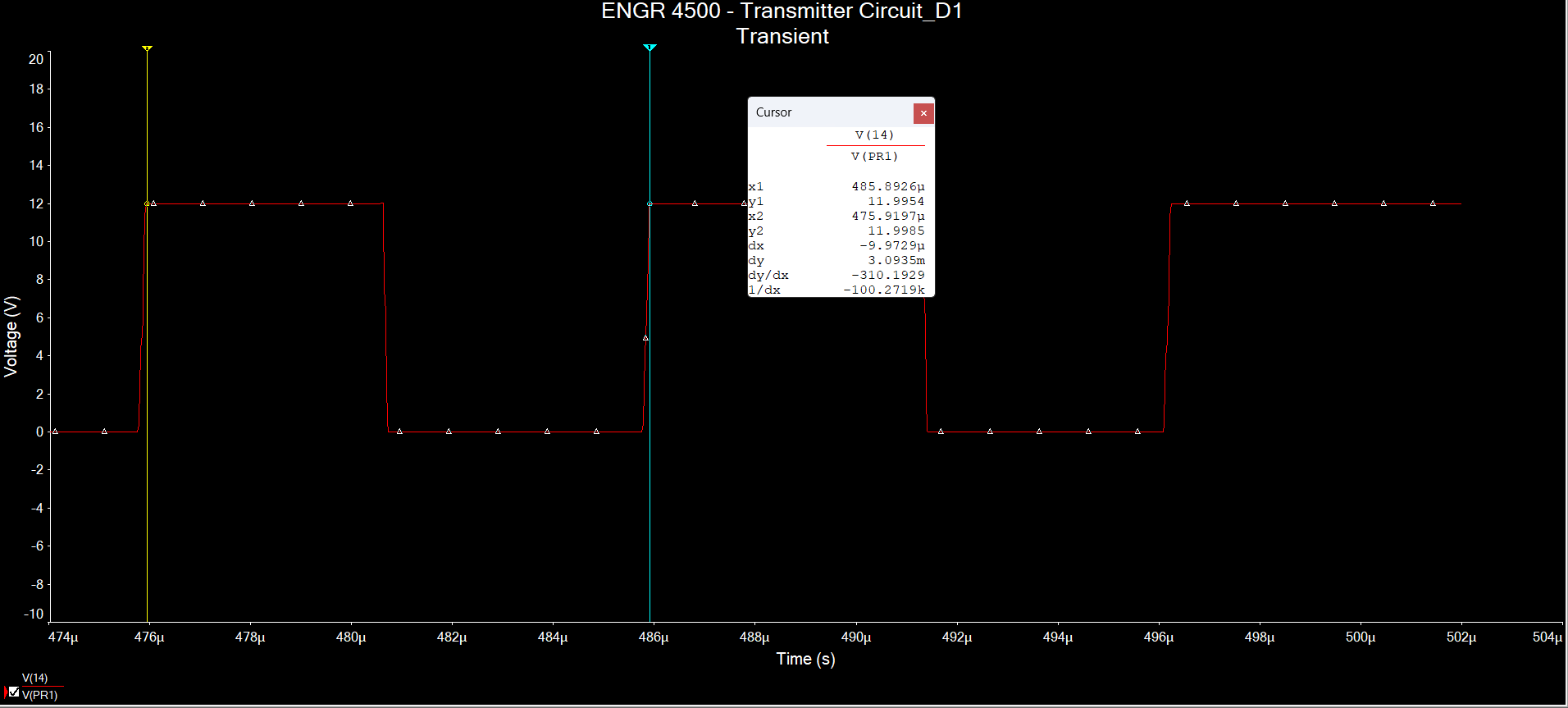
# Integration

## Design 3: IRLZ44N/IR2113

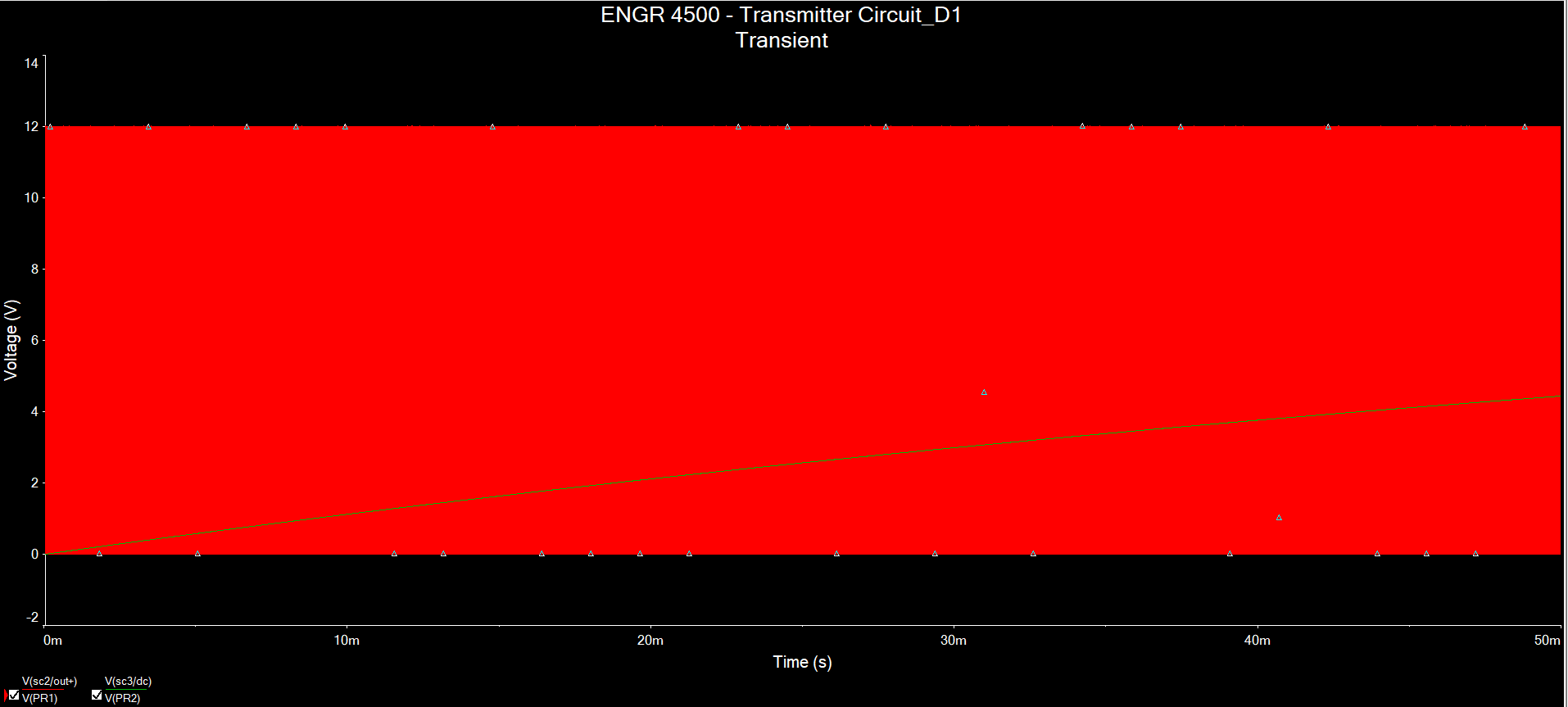
This is the schematic



Try to probe the voltage before the transmitter capacitor shows that it is a PWM wave with 100kHz (this is good!)



But the voltage on the load is rising which means the full power is not reaching it (not good!)

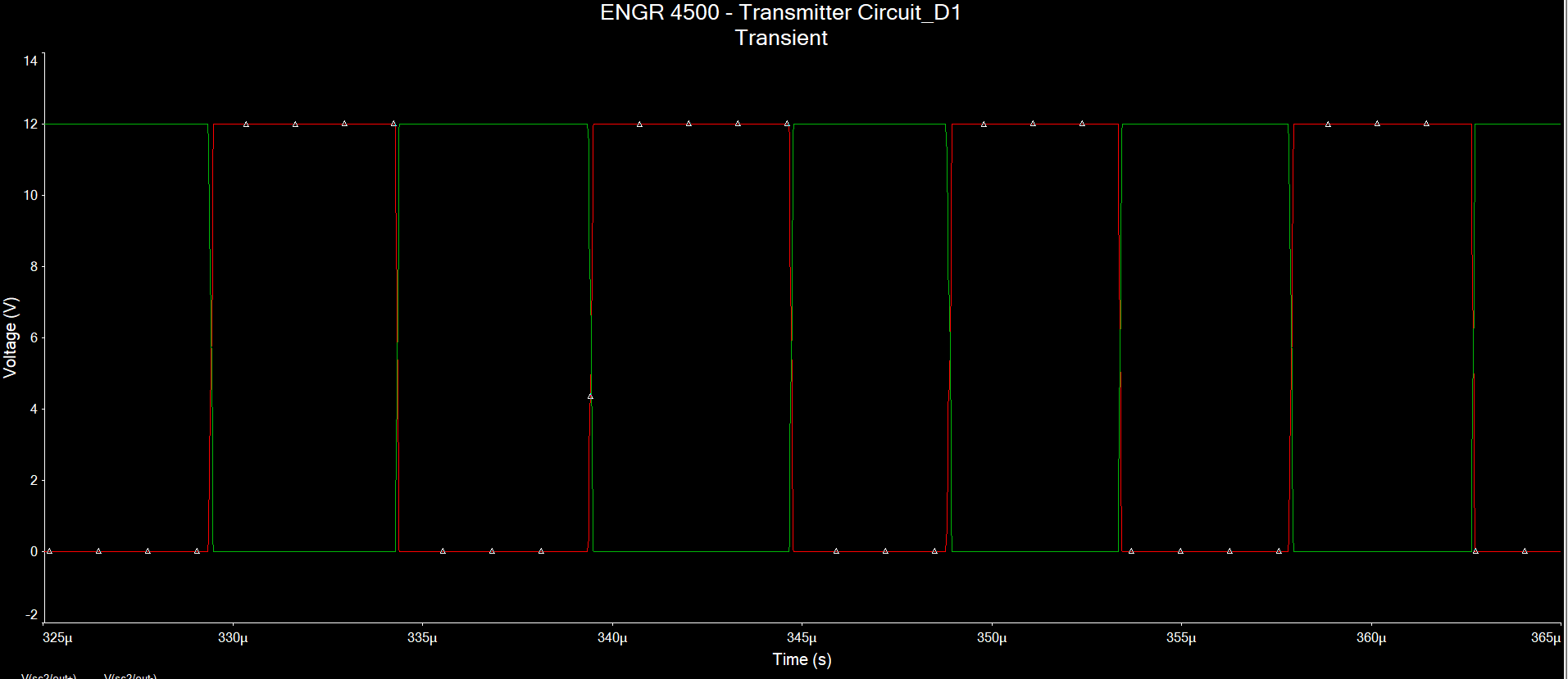


Probing the transformer results in a somewhat sinusoidal pattern but there is this charge/discharge ripple (not good!)

Chart

Description automatically generated

Inspecting the waveform of the output of the H bridge (Out+ and Out-) shows PWM in complementary fashion (really good!)



This is probing the before Tx cap and after Rx cap which produce a almost sinusoidal curve but there is this ringing at the peak which comes from the inductor (not good!)

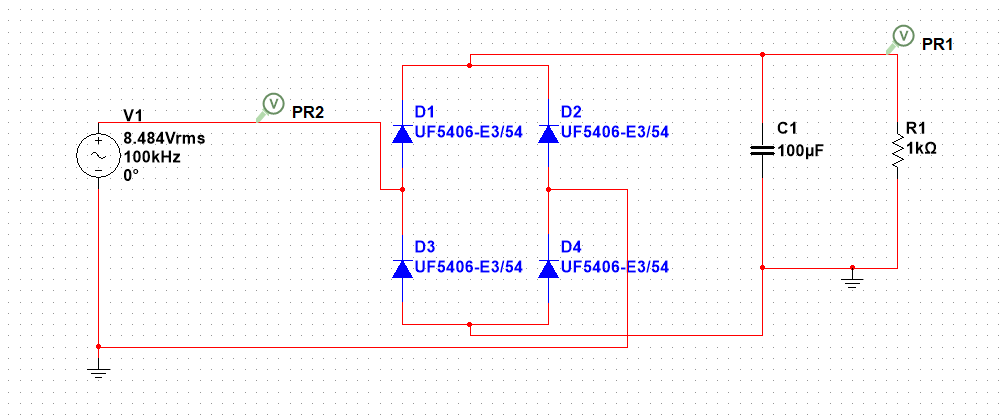
A picture containing background pattern

Description automatically generated

# Testing

## Checking the Rectifier Circuit

Schematic (Vrms = 0.707Vpk = 0.707(12) = 8.484Vrms)



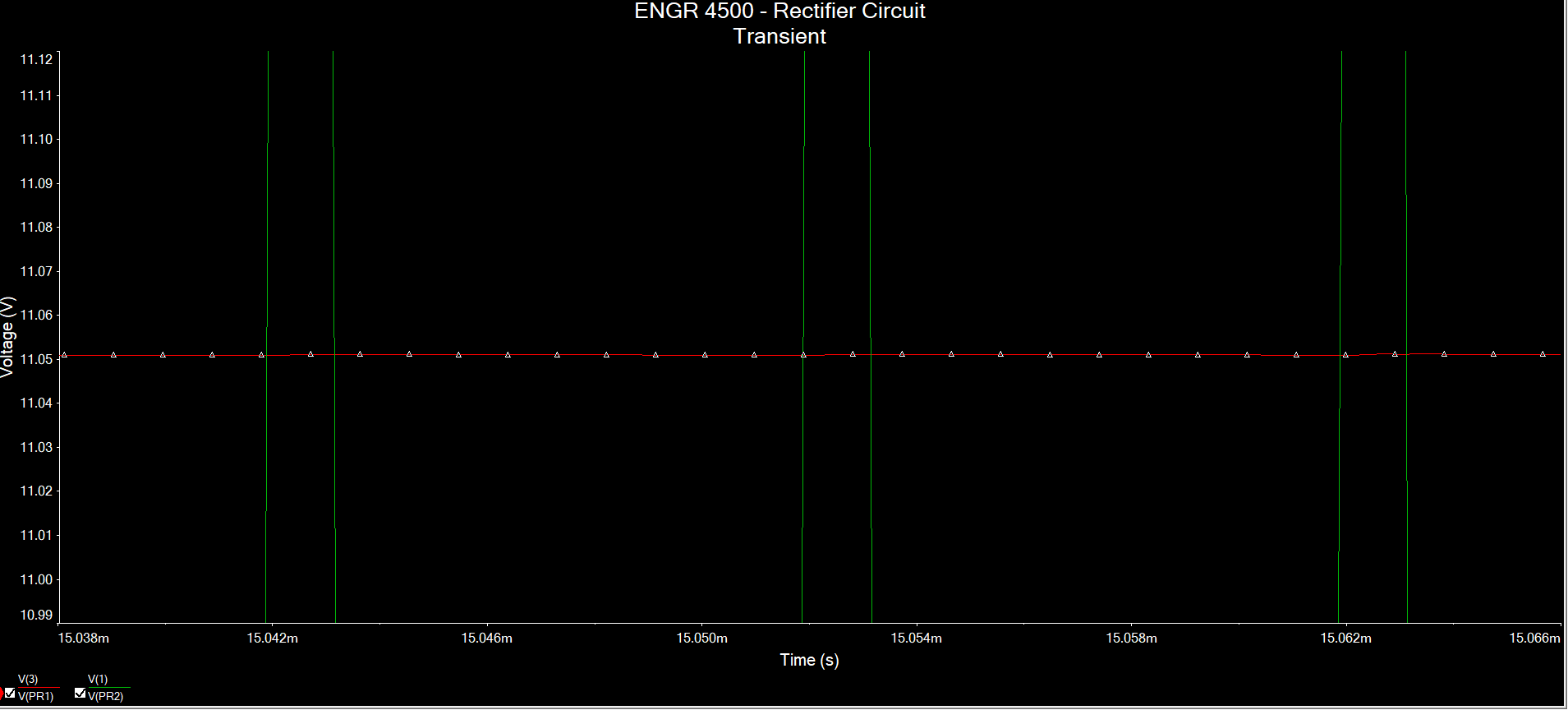
Simulation Result (rectified the voltage to 10.65V)



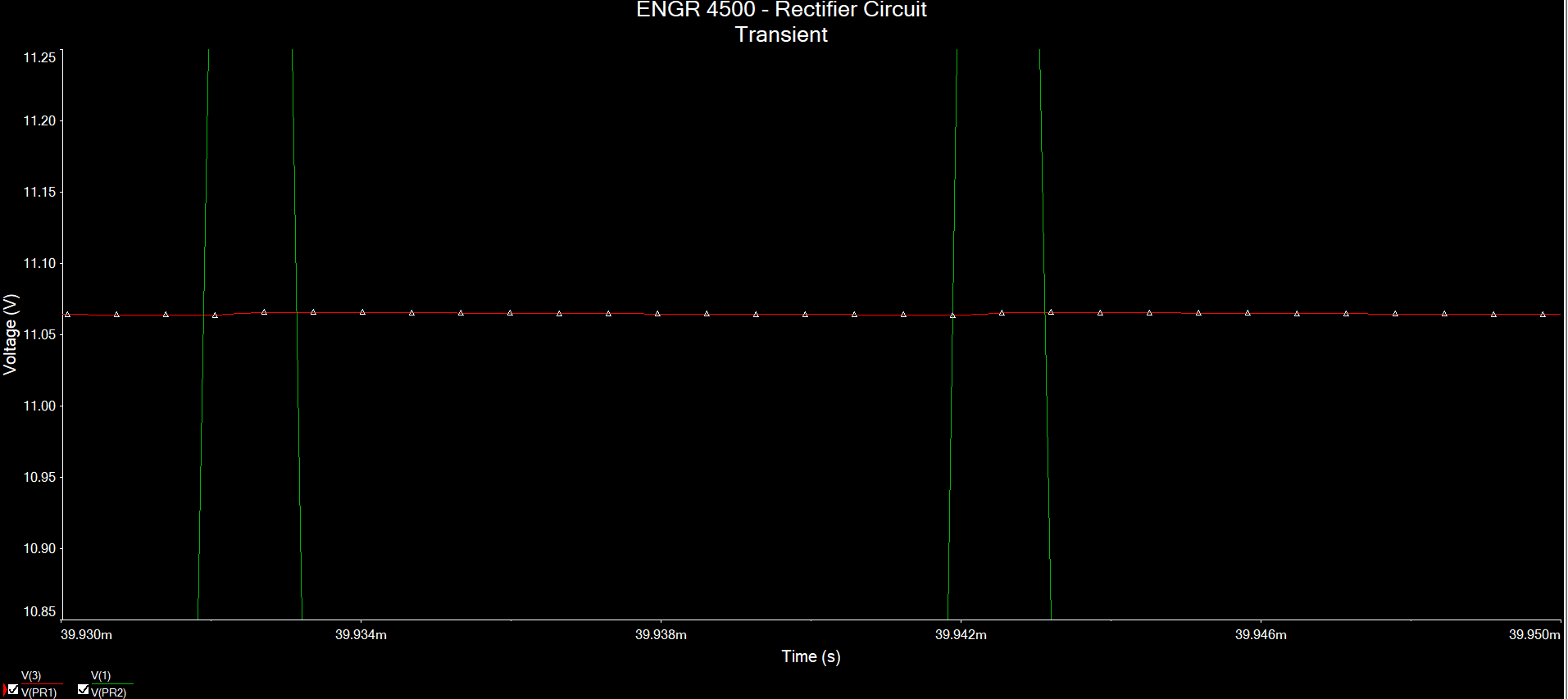
A picture containing text, night, light

Description automatically generated

Changing the capacitance from 100uF to 500uF results in 11.05VDC



Changing the capacitance from 100uF to 50uF results in 11.06VDC

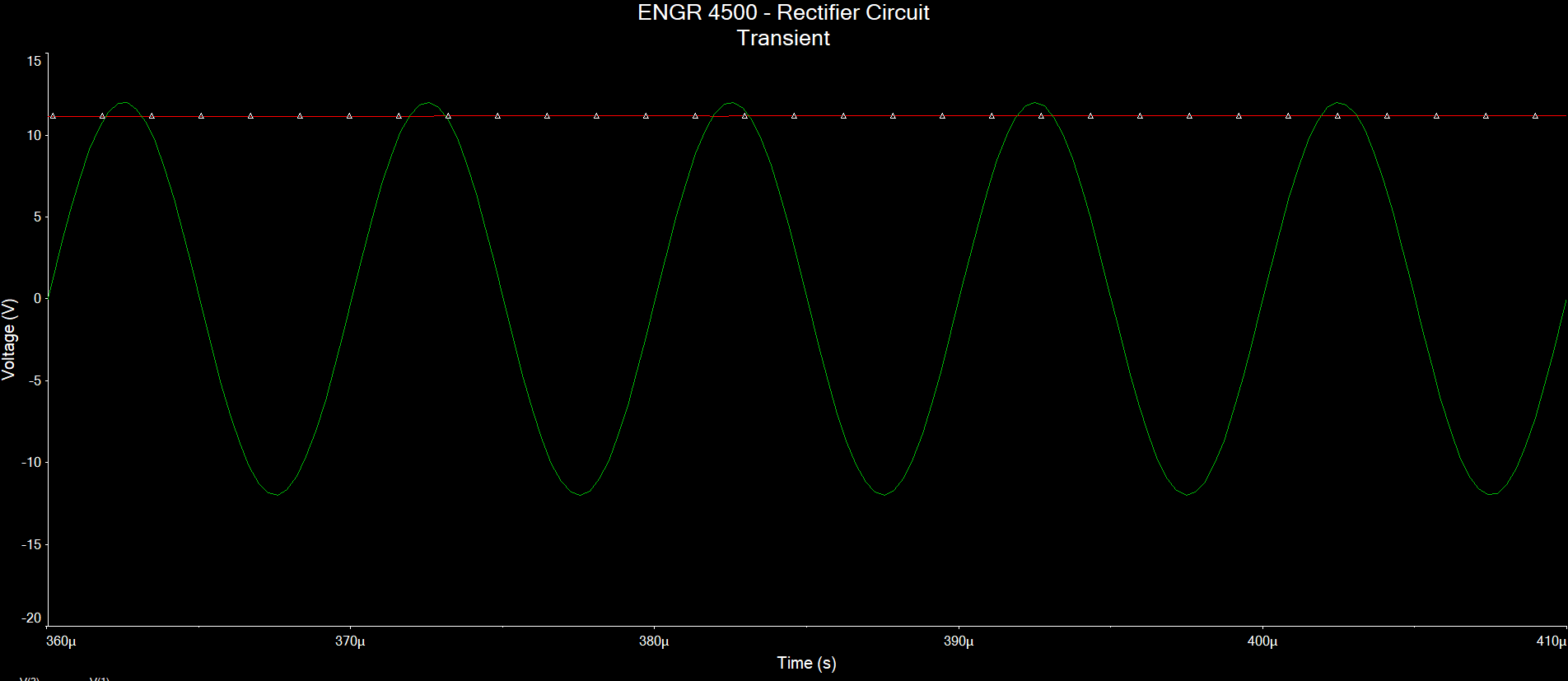


Changing the diode to 1N5402G (200V 3A Standard Rectifier Diode)

Diagram, schematic

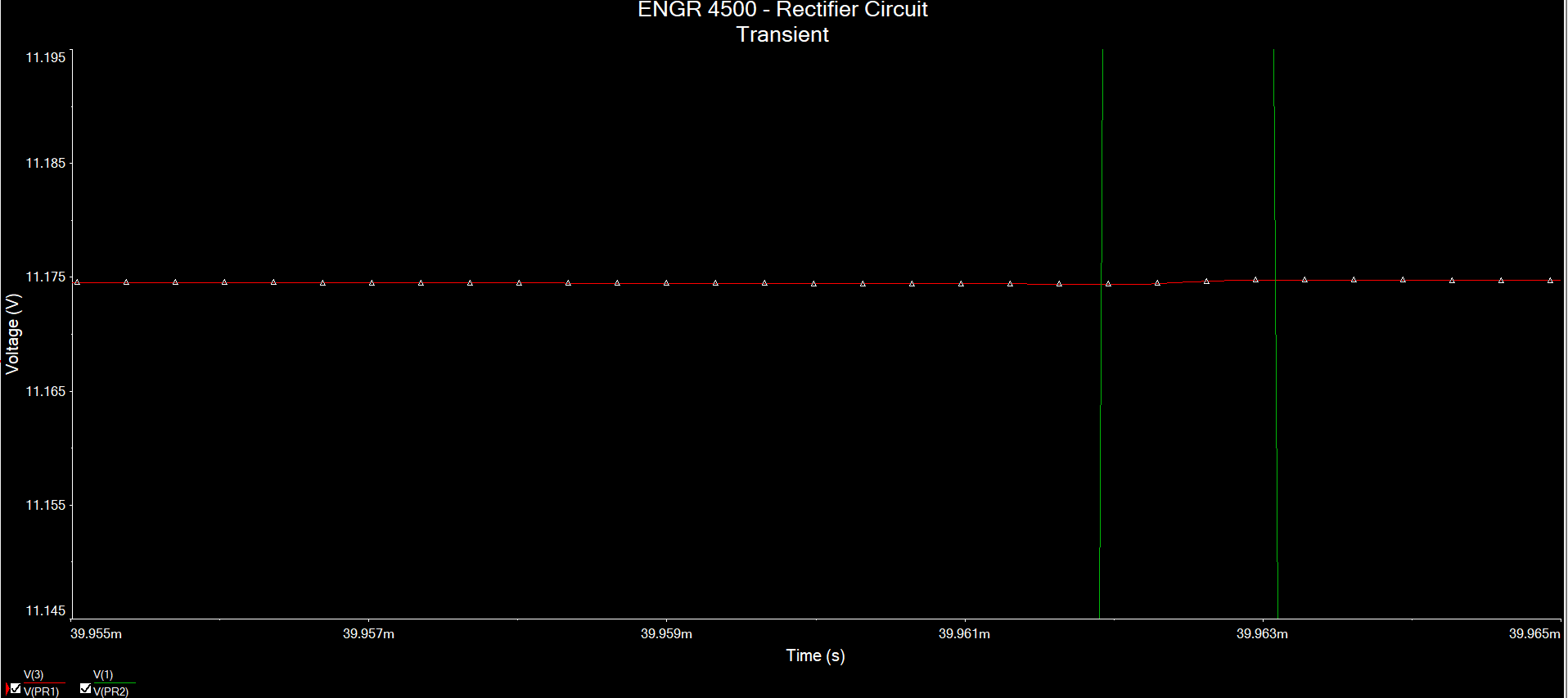
Description automatically generated

This result in a DC voltage of 11.18V for a 100uF capacitor

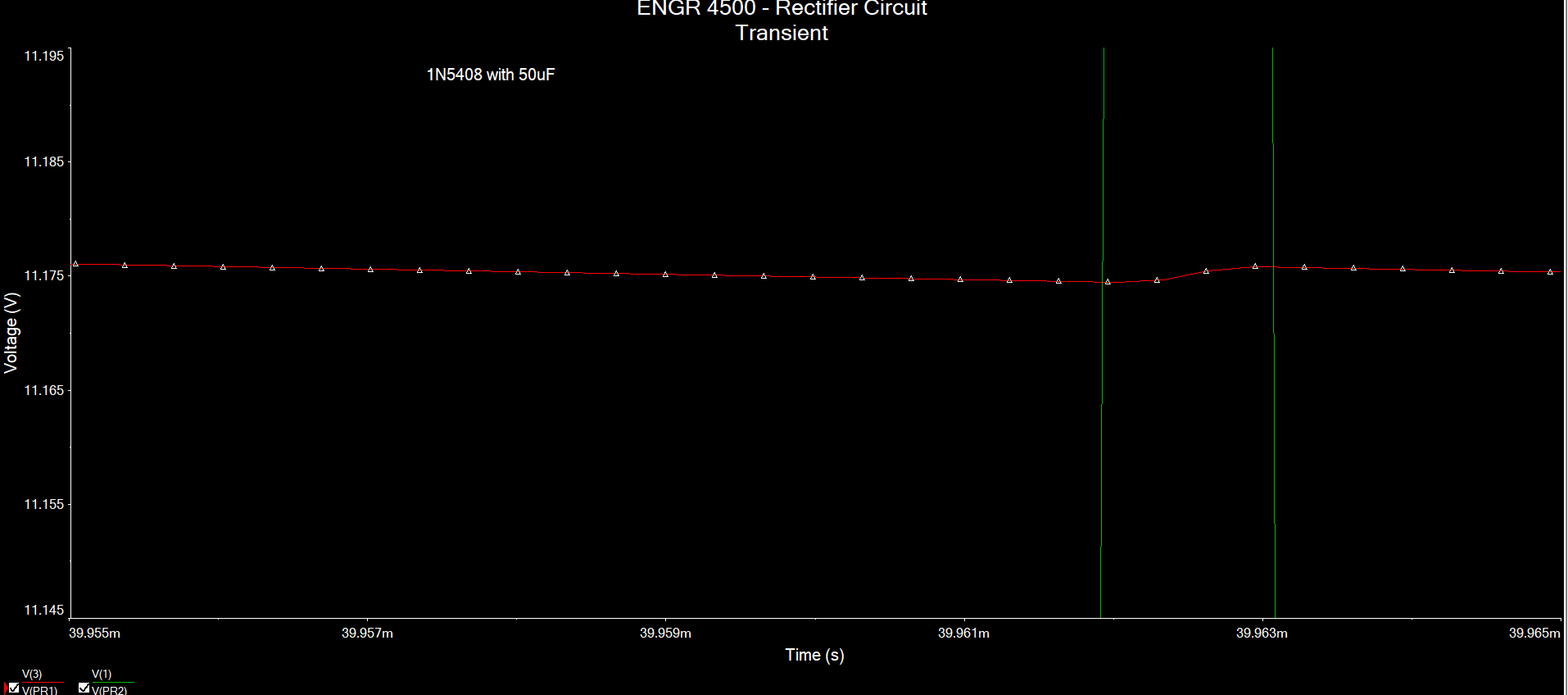


Chart, histogram

Description automatically generatedChanging the capacitance to 500uF results in 11.175VDC



Changing the capacitance to 50uFresults in 11.175V



## Changing the Capacitance

Change the capacitance to 50nF from 25.33nF  


Changing the capacitance to 100nF from 25.33nF

Chart

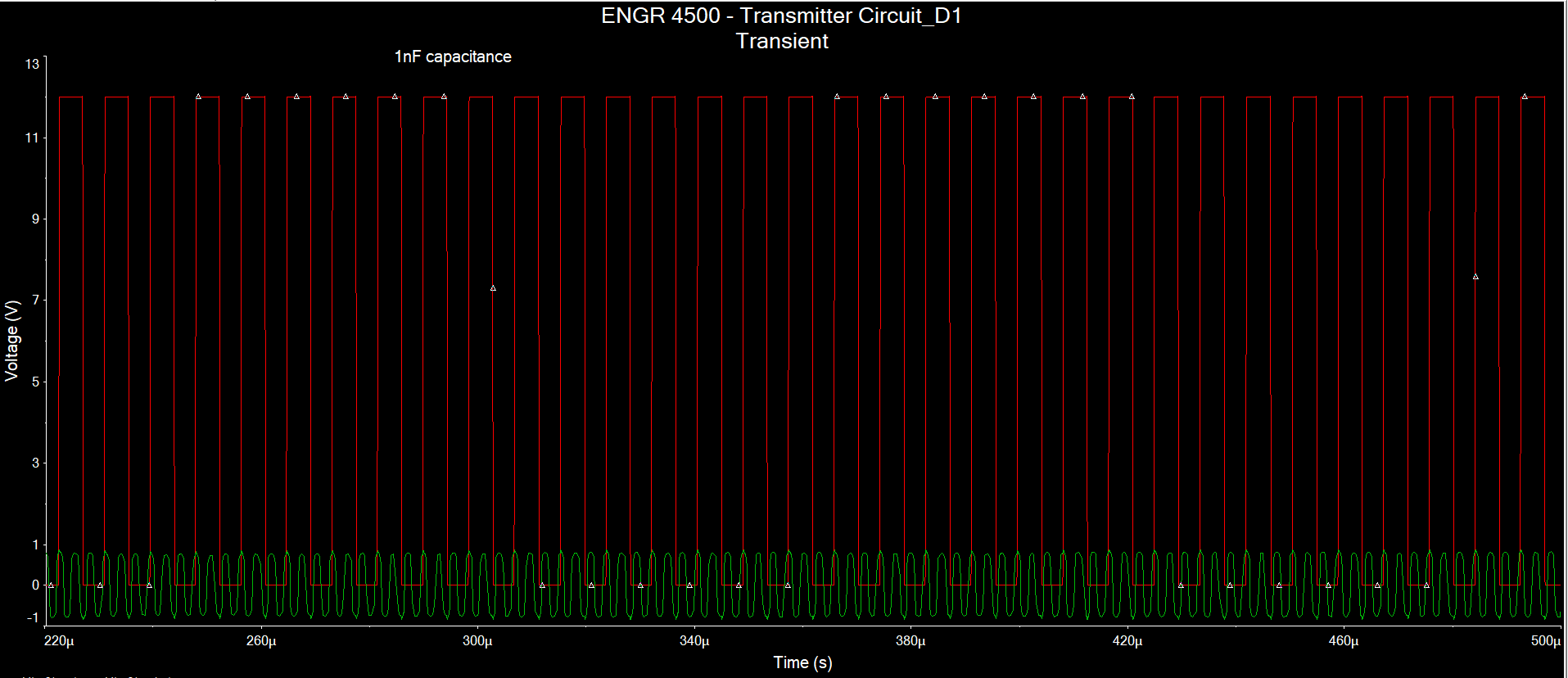
Description automatically generated

Changing the capacitance to 10nF from 25.33nF

Chart, histogram

Description automatically generated

Changing the capacitance to 1nF from 25.33nF



The limit seems to be 0.1nF for a 100uH system

Chart, histogram

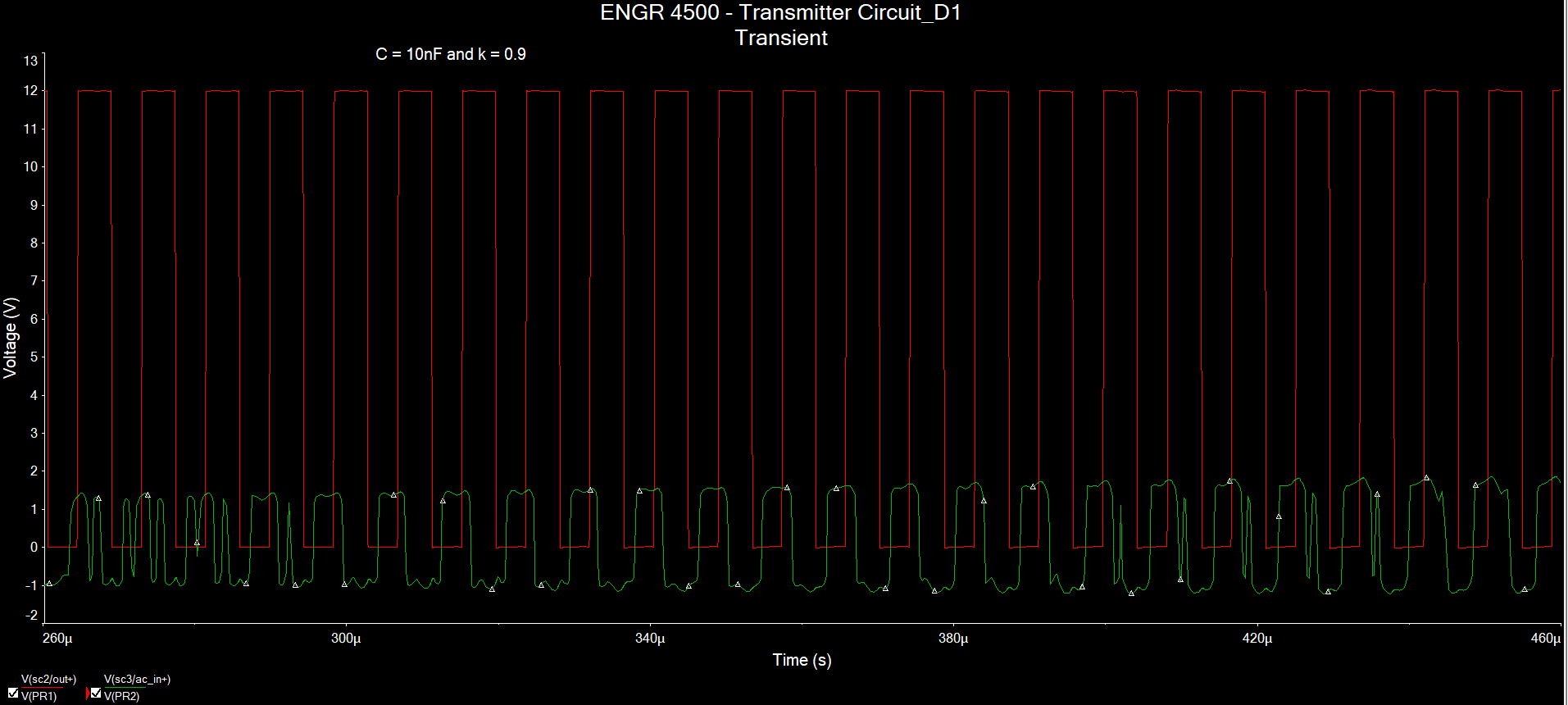
Description automatically generated

25.33nF and k = 0.9

Chart, histogram

Description automatically generated

10nF and k=0.9



50nF and k=0.9

A picture containing histogram

Description automatically generated

100nF and k=0.9

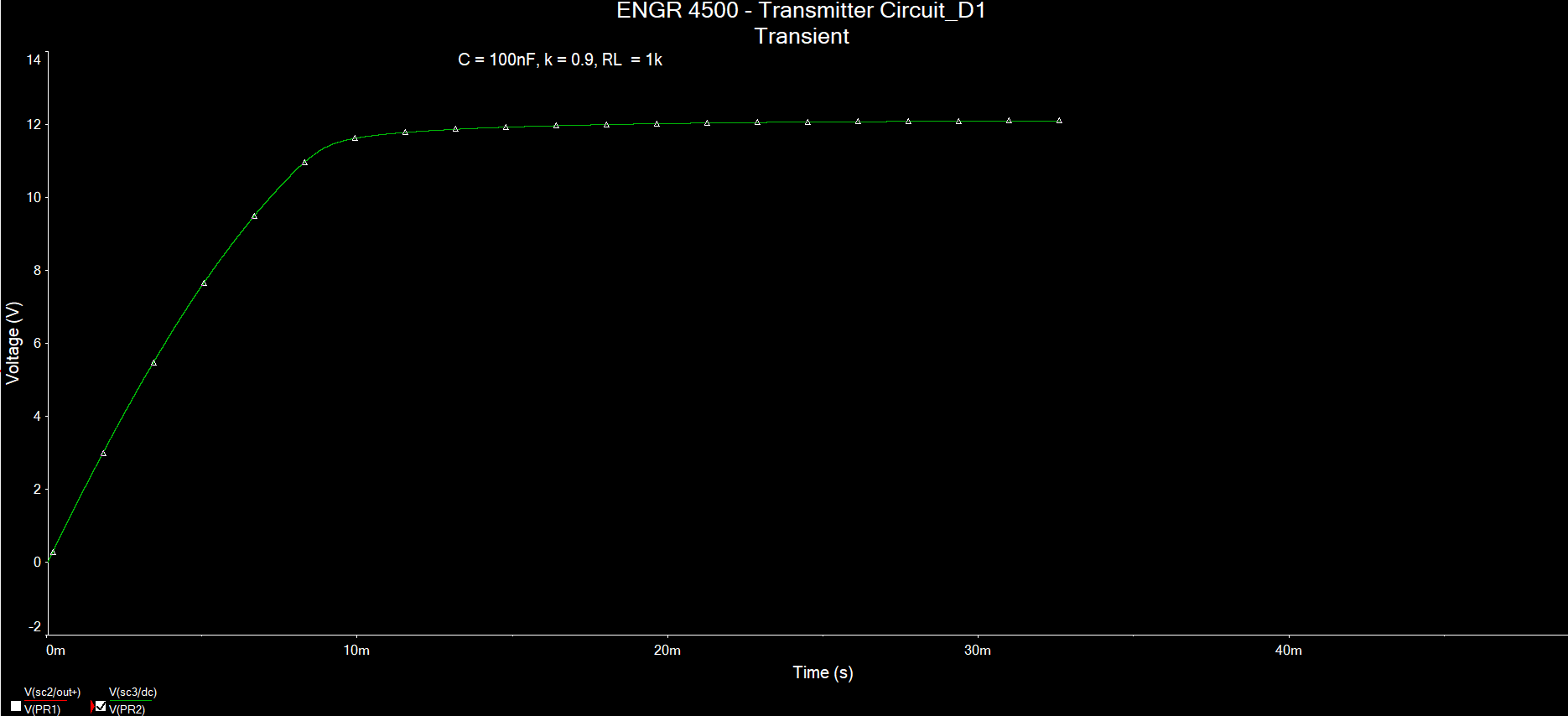
Chart, histogram

Description automatically generated

Chart, histogram

Description automatically generated

Looking at the load shows that the DC voltage does reach 12.1V at steady state

Try it with 25.33nF, k = 0.9 does not reach the same result

A picture containing graphical user interface

Description automatically generated

Even with k = 0.5

A picture containing graphical user interface

Description automatically generated

## Changing the Inductance

Changing the inductance to 24uF (by Wurth Elektronik)

If L = 24uH

L = 24uH, C = 105nF at k = 0.9

Chart

Description automatically generated

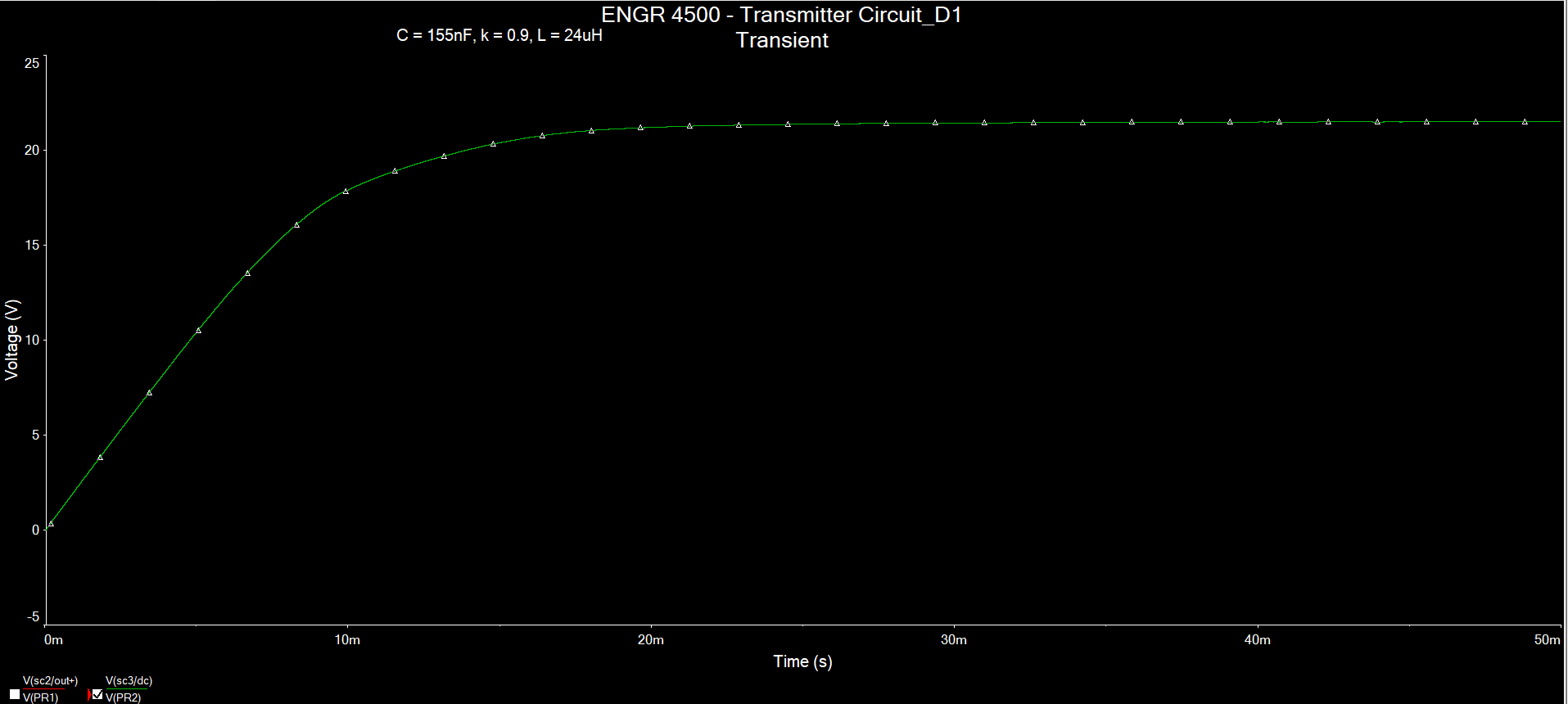
A picture containing graphical user interface

Description automatically generated

C = 155nF, k = 0.9, L = 24uH

Chart, histogram

Description automatically generated



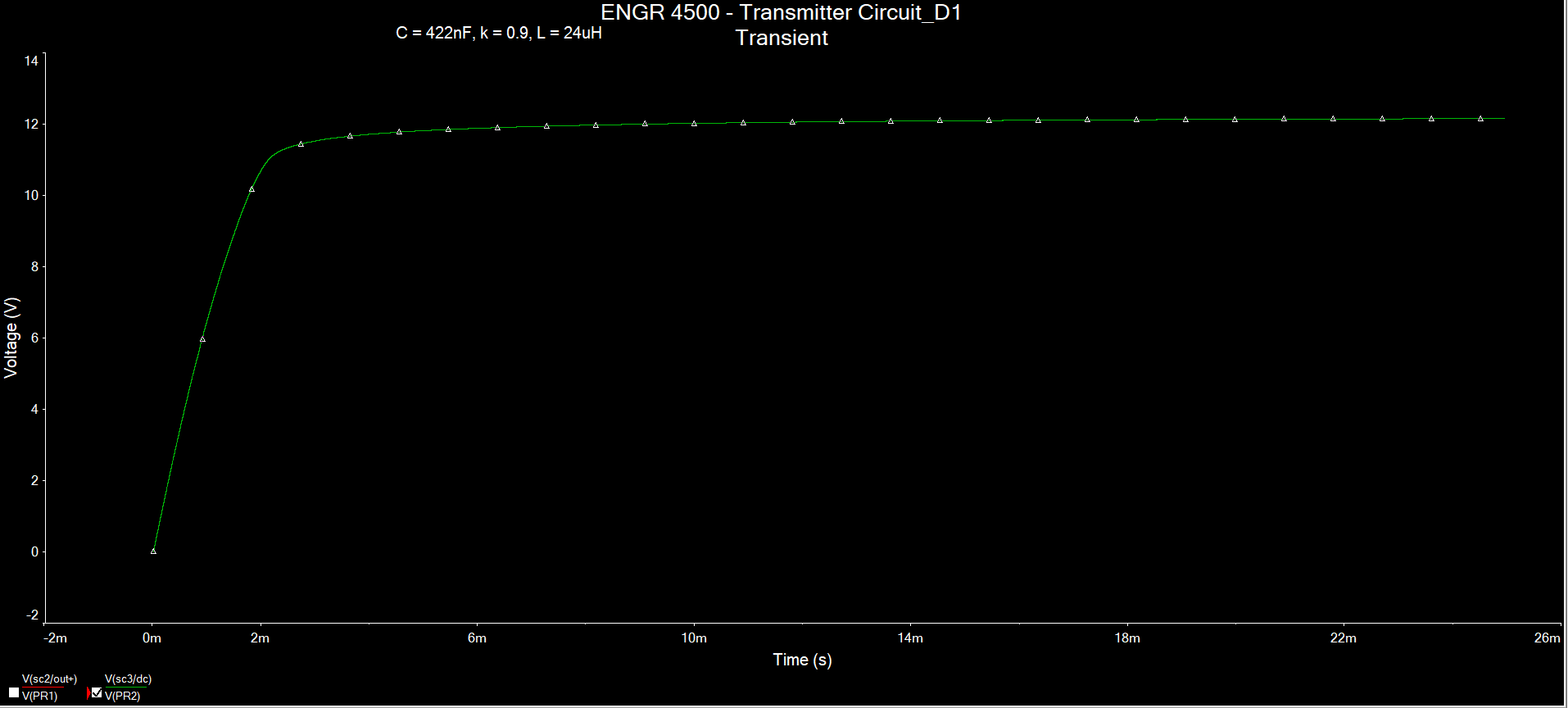
C = 422nF, k = 0.9, L =24uH

Chart

Description automatically generated

Chart

Description automatically generated



C = 55nF, L = 24uH, k = 0.9

Chart, histogram

Description automatically generated

A picture containing line chart

Description automatically generated

So we need to check the H bridge with ideal components

## Checking the H Bridge Design with Ideal Components

C = 25.33nF, L = 100uH , k = 0.9

Chart

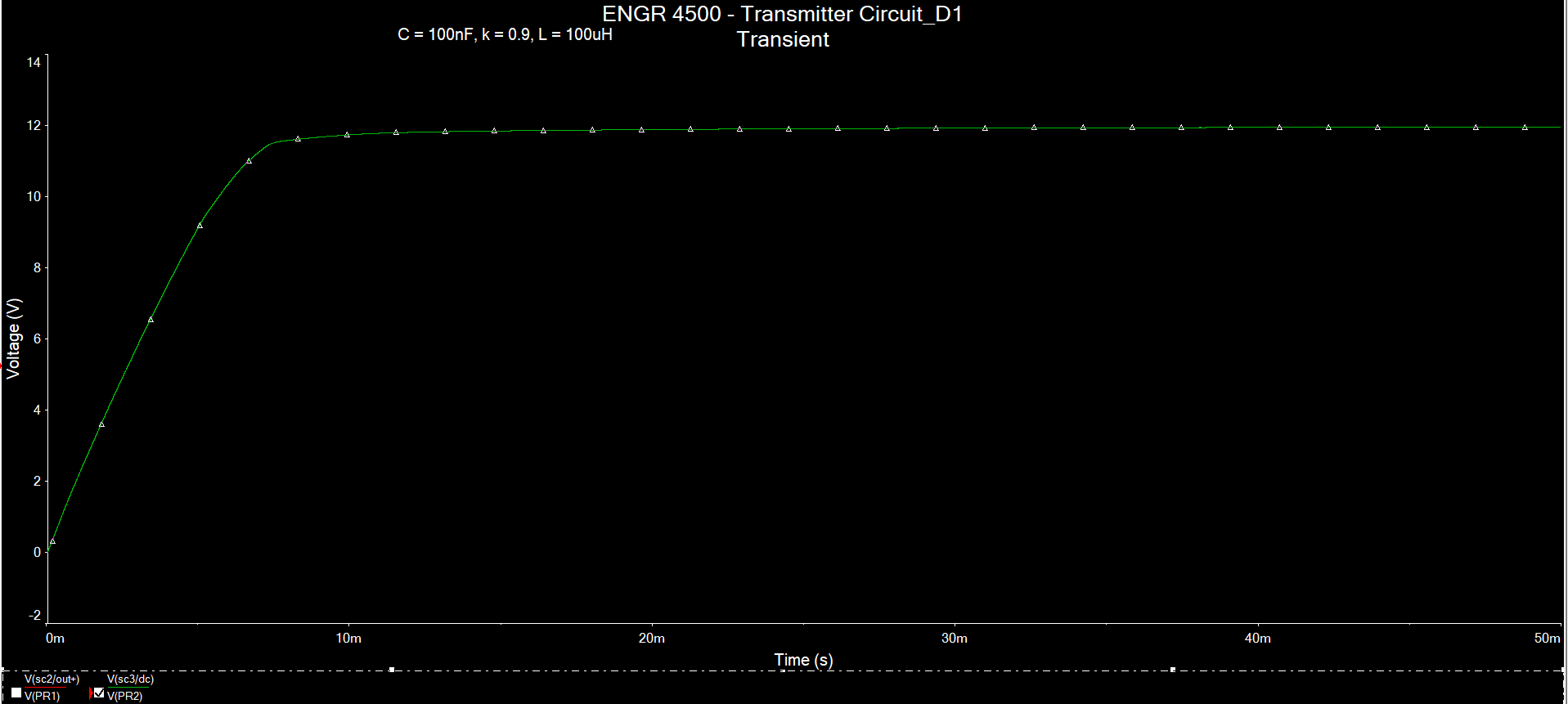
Description automatically generated  
A picture containing text, indoor, screenshot, dark

Description automatically generated

C = 100nF, L = 100uH, k = 0.9

Chart, histogram

Description automatically generated



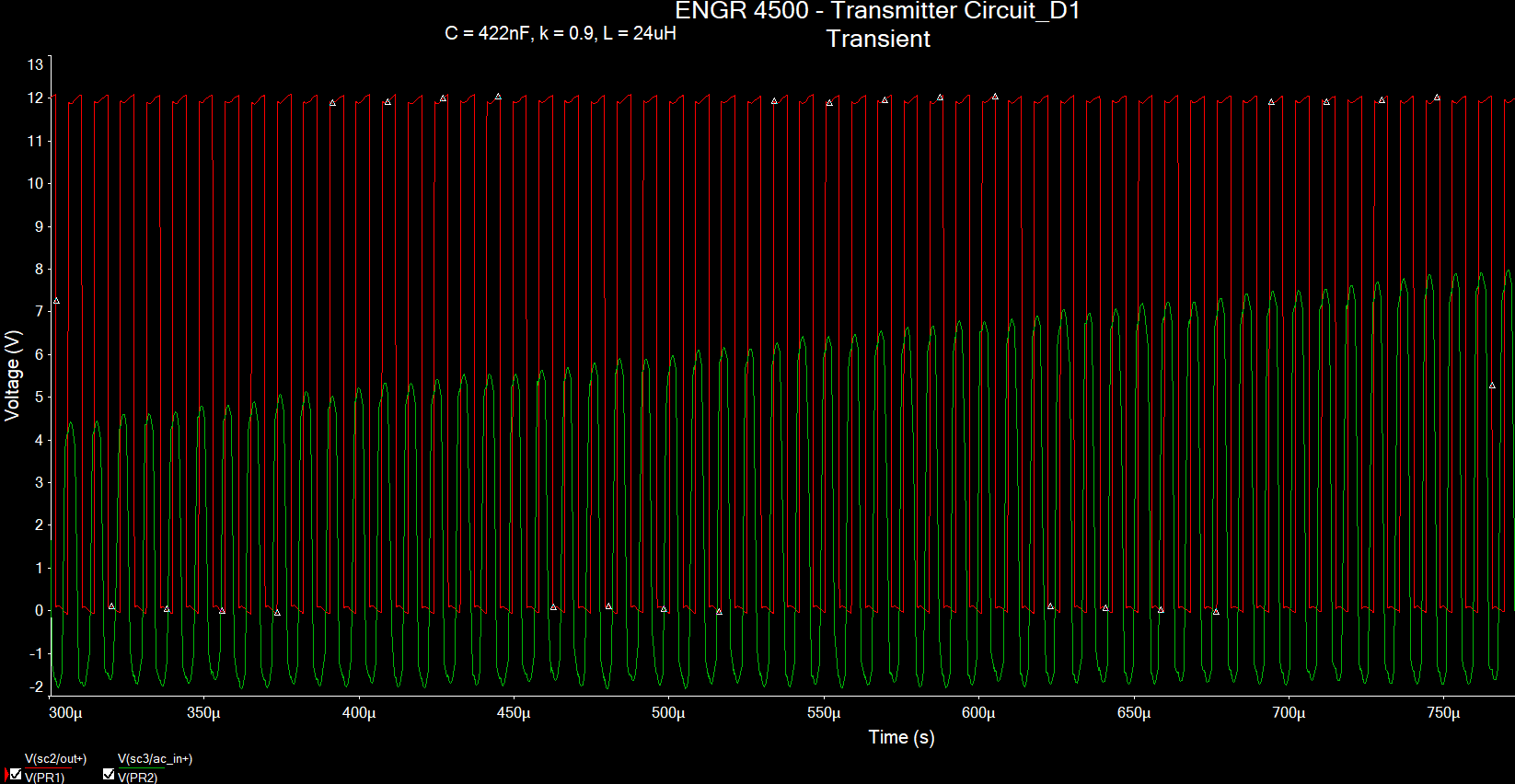
C = 105nF, L = 24uH, k = 0.9

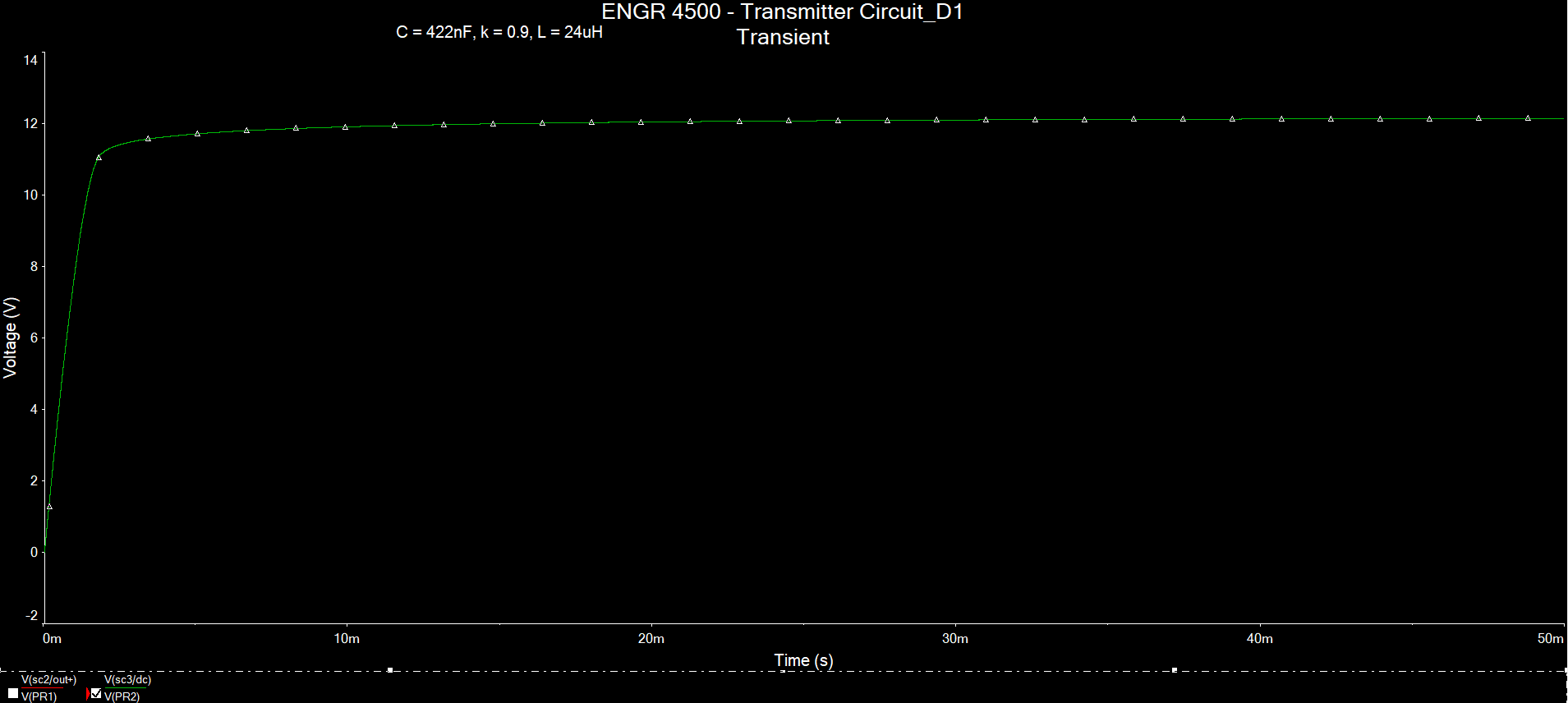
Chart

Description automatically generated



C = 422nF, L = 24uH, k = 0.9





## Changing the PWM Generator with an Ideal Component

### Ideal 555 Timer

Diagram, schematic

Description automatically generated

C = 25.33n, L = 100u, k = 0.9, Cr = 500u

Chart, histogram

Description automatically generated

A picture containing chart

Description automatically generated

C = 100n, L =100u, k = 0.9, Cr = 500uChart

Description automatically generated with medium confidence

A picture containing graphical user interface

Description automatically generated

### Multisim PWM Generator

Diagram, schematic

Description automatically generated

For C = 25.33nF, L = 100u, k = 0.9, Cr = 500u

Chart, histogram

Description automatically generated

A picture containing text, indoor

Description automatically generatedC = 100nF, L = 100u, k = 0.9, Cr = 500u

A screenshot of a computer screen

Description automatically generated with medium confidence

C = 200nF, L = 100u, k = 0.9, Cr = 500u

A picture containing graphical user interface

Description automatically generated

C = 150nF, L = 100u, k = 0.9, Cr = 500u

A screenshot of a computer

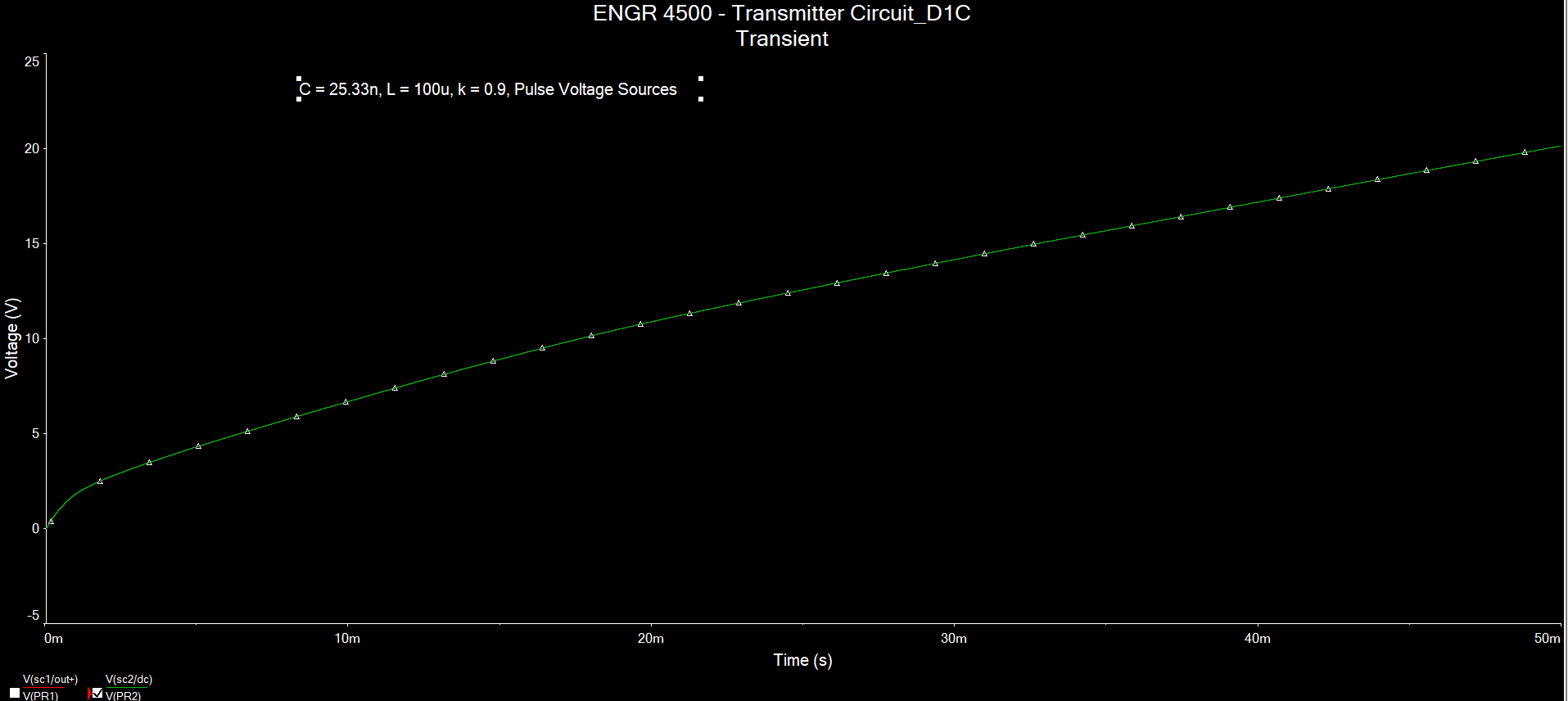
Description automatically generated with medium confidence

### Multisim Pulse Source

C = 25.33n, L = 100u, k = 0.9

Chart

Description automatically generated



C = 100n, L = 100u, k = 0.9

Chart, histogram

Description automatically generated

A picture containing indoor, way, dark

Description automatically generated

C = 150n, L = 100u, k = 0.9

A picture containing text

Description automatically generated

Graphical user interface

Description automatically generated