Introduction to the **Design Verification Unit** **COMS30026**

(COMS30066 with coursework)

Kerstin Eder

Trustworthy Systems Lab

University of BRISTOL

Department of COMPUTER SCIENCE

Welcome to Design Verification

- Lecturer and Unit Director
  - Kerstin EDER
  - Department of Computer Science
- Lecture slides, exercises and additional material are available at uobdv.github.io/Design-Verification/
- Recordings of the lectures will be made available via Blackboard
  - Topics for each week can be found on github
- Comments and feedback are always welcome
  - Blackboard discussion forum

Design Verification Unit Details

- Lectures during weeks 1-5, 7-8 and week 12
  - Wednesday 10:00 (50 min) online synchronous session (Lecture)
    - Microsoft Teams:

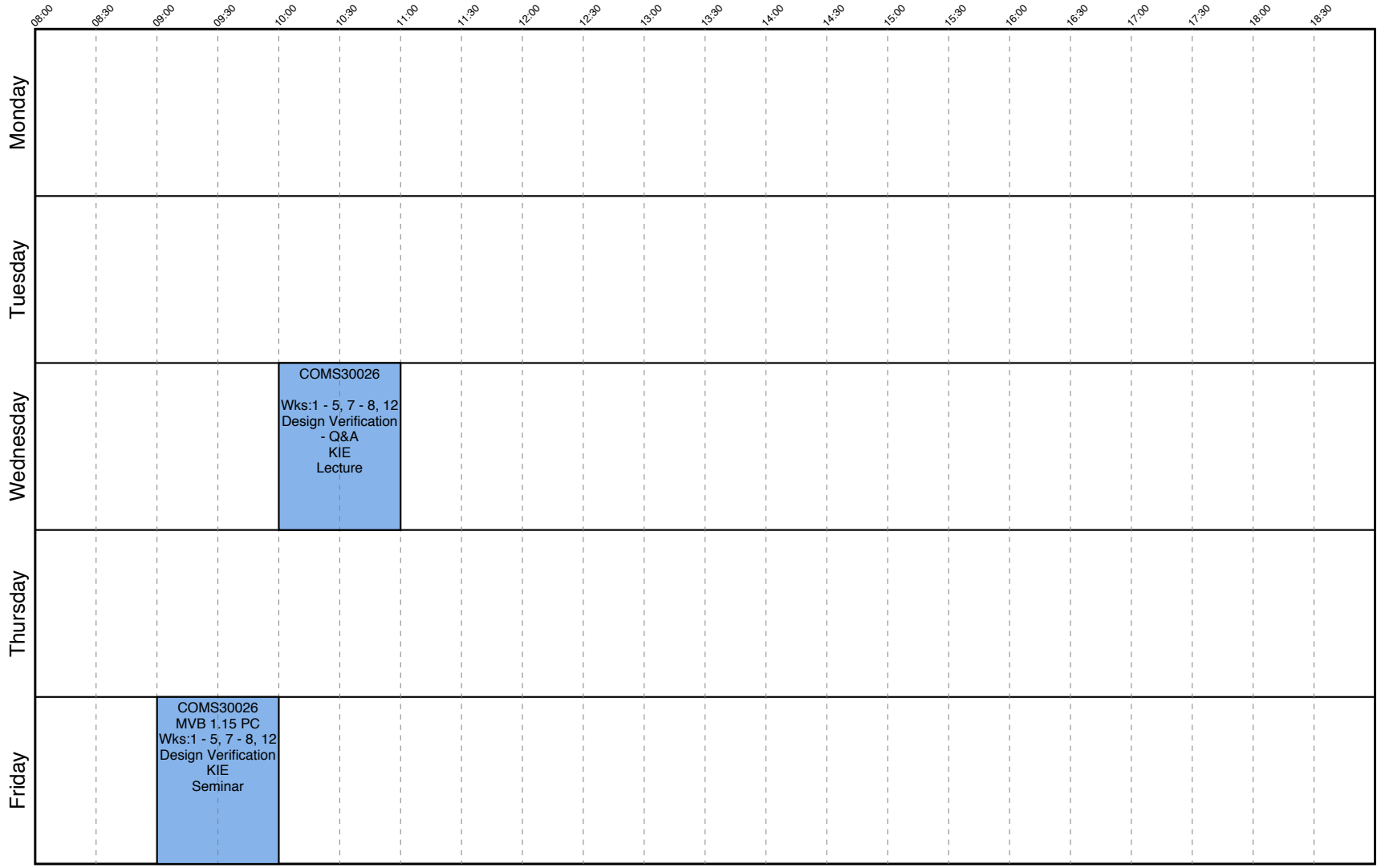
      COMS30026: Design Verification (Teaching Unit) 2021/22 (TB-1, A)

Please check your timetable regularly in case of any changes.

- Practical Work during weeks 1-5, 7-8 and week 12
  - Friday 9:00 (50 min) lab session
    - MVB 1.15 PC lab and/or
    - online support via Teams
  - Teaching Assistant: Xuan Zheng

Timetable

University of BRISTOL Timetable of activities - Teaching Block 1 (weeks 1 - 12)



Design Verification Assessment

- Assessment
  - **COMS30024** (exam only)
    - will be assessed in the January exam period
    - viva-based exam most likely online
  - **COMS30066** (by coursework)
    - will be assessed by coursework (only)
    - focus on coursework during weeks 9-11
    - viva-based interview on coursework

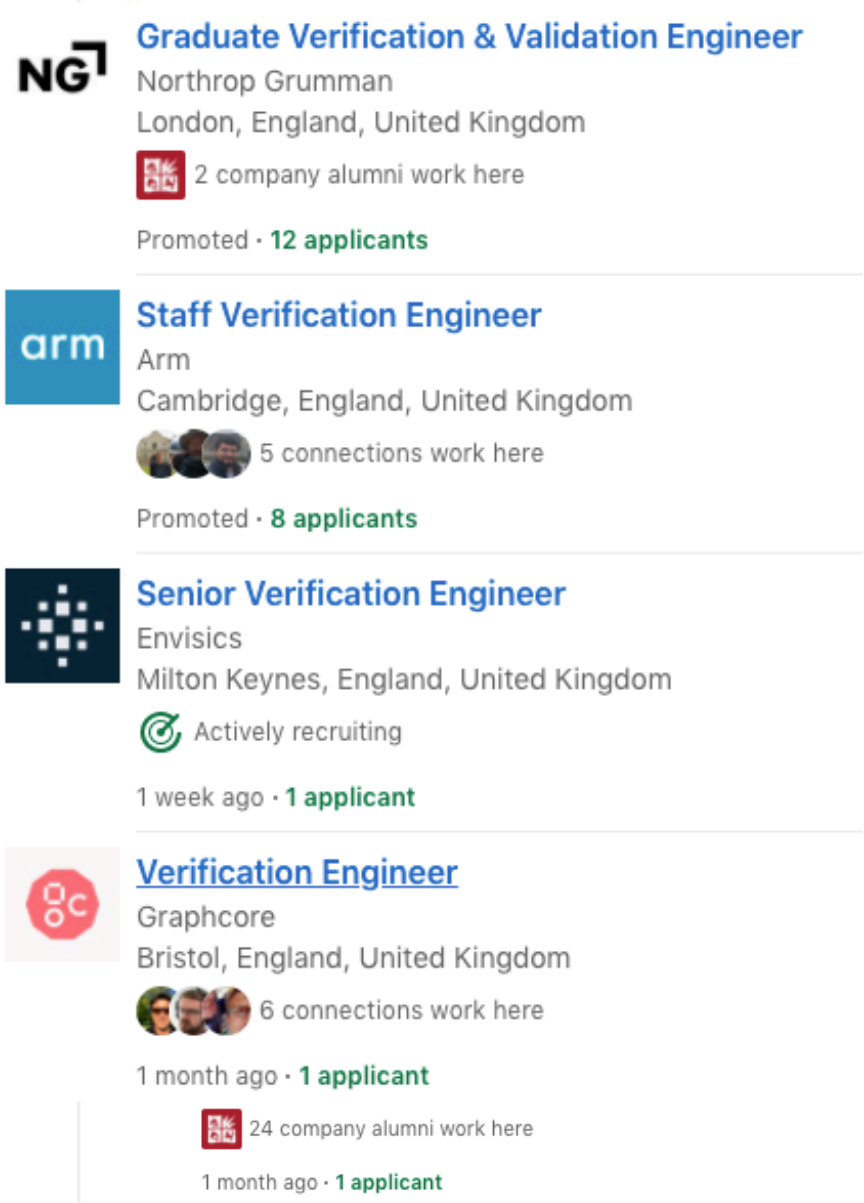
Literature and Study Resources

- **Writing Testbenches: Functional Verification of HDL Models** by Janick Bergeron. Second Edition, Kluwer, 2003.
- **Comprehensive Functional Verification** by Bruce Wile, John Goss and Wolfgang Roesner. Elsevier, 2005.
- verificationacademy.com
- **In addition:**
  - Lecture slides and on-line tutorials on github unit web page
  - On-line documentation of ModelSim/Questa Simulator and SpecMan Elite
  - Watch the unit web page on github for further supplementary literature.

[**Credits:** Parts of the lecture notes contain material from the book “Comprehensive Functional Verification” by Bruce Wile etal, the book ”Writing Testbenches: Functional Verification of HDL Models” by Janick Bergeron, the book ”The Verilog Hardware Description Language” by Donald Thomas and from lecture slides developed at IBM (by Avi Ziv and Jaron Wolfstal), the University of Pittsburgh, Penn State University, North Carolina State University and Ohio State University. The HDL for the assignments has been developed at IBM.]

What is this unit about?

Aim: To familiarise you with the state of the art in Design Verification, and to give you the **technical background** plus some of the **practical skills** expected from a professional Design Verification Engineer.



What is this unit about?

Aim: To familiarise you with the state of the art in Design Verification, and to give you the **technical background** plus some of the **practical skills** expected from a professional Design Verification Engineer.

- **Pre-/Co-requisites:** programming experience and a basic understanding of computer architecture

On successful completion of this unit, you will be able to:

- understand the complexities and limits of verification;
- carry out functional verification and determine its effectiveness;
- set appropriate verification goals, select suitable verification methods and assess the associated risks;
- compile a verification plan that fits into the flow of a design project.

Unit Outline

Lecture Topics

- Introduction: What is Verification? What is a Testbench?
- Verification hierarchy, basics and tools including basic Verilog HDL
- Verification cycle, methodology and plan
- Simulation-based Verification: stimuli generation, checking, coverage
- Advanced Testbench Design Methodology with SpecMan Elite
- Assertion-based Verification (ABV)
- (Functional Formal Verification and Property Checking)

Practical work

- Exercise 1: Evita Verilog interactive tutorial (do @ home asap)
- Exercise 2: Introduction to the ModelSim/Questa Simulator
- Practical 1, weeks 2-4: Verification of calculator design with ModelSim
- Exercise 3: How to collect Code Coverage with ModelSim/Questa
- Exercise 4: Introduction to SpecMan Elite
- Practical 2, weeks 5, 7 and 12: Advanced testbench design with SpecMan Elite and formal verification with JasperGold

What is Design Verification?

What is Design Verification?

"Design Verification is the process used to gain confidence in the correctness of a design w.r.t. the requirements and specification."

Types of verification:

- Functional verification
- Timing verification
- ...
- What about performance?

Verification vs Validation

- Verification:
  - Confirms that a system has a given input / output behaviour, sometimes called the **transfer function** of a system.
- Validation:
  - Confirms that the system's transfer function results in the intended system behaviour when the system is employed in its target environment, e.g. as a component of an embedded system.
- Validation is sometimes used when verification is meant.

Annex A
(informative)

The Role of Testing in Verification and Validation

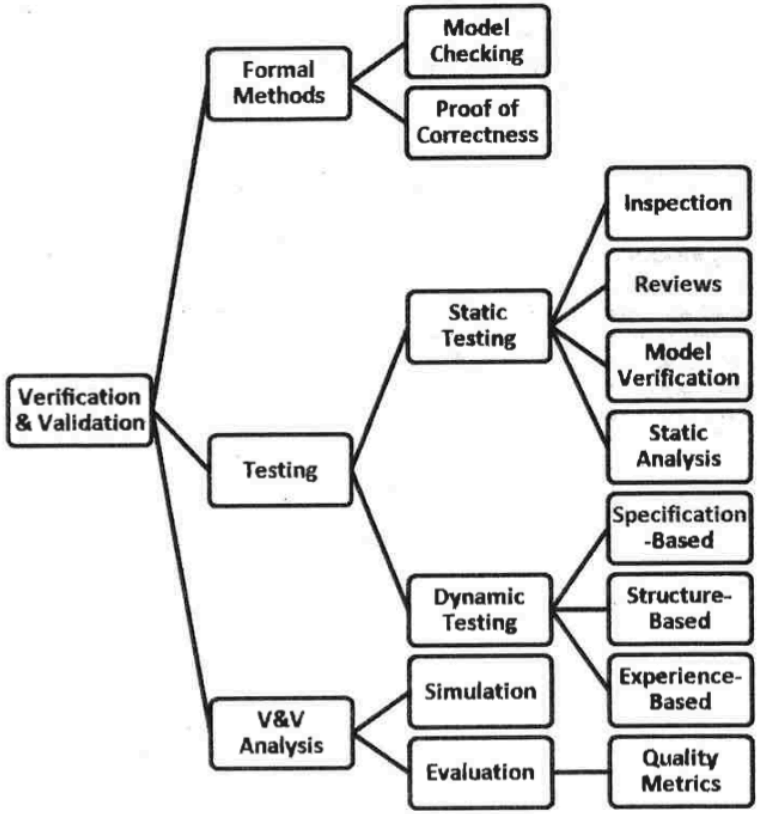


Figure 11 — Hierarchy of Verification and Validation activities

Figure 11 defines the complete nature of verification and validation (V&V) activities. V&V can be done on system, hardware, and software products. These activities and planning are defined and refined in IEEE 1012 and ISO/IEC 12207. Much of V&V is accomplished by testing. The ISO/IEC 29119 standard addresses the Dynamic and Static software testing (directly or via reference), thus covering parts of this verification and validation model. ISO/IEC 29119 is not intended to address all the elements of the V&V model, but it is important for a tester to understand where they fit within this model.

DRAFT INTERNATIONAL STANDARD ISO/IEC DIS 29119-1

ISO/IEC JTC 1 Secretariat: **ANSI**

Voting begins on **2012-10-09** Voting terminates on **2013-01-09**

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Software and systems engineering — Software testing —

Part 1:
Concepts and definitions

Ingénierie du logiciel et des systèmes — Essais du logiciel —
Partie 1: Concepts et définitions

ICS 35.080

To expedite distribution, this document is circulated as received from the committee secretariat. ISO Central Secretariat work of editing and text composition will be undertaken at publication stage.

Pour accélérer la distribution, le présent document est distribué tel qu'il est parvenu du secrétariat du comité. Le travail de rédaction et de composition de texte sera effectué au Secrétariat central de l'ISO au stade de publication.

Next

- Recordings of lectures (about 2h - 3h per week)

  Week 1:

  - ✓ Introduction to Design Verification
  - ✓ Verification Hierarchy
  - ✓ Driving & Checking

  – uobdv.github.io/Design-Verification/
  shows a **weekly schedule of topics** to watch BEFORE the next online session, ideally

  – Recordings are available from Blackboard unit page

- Tasks for you this week:

  – **Attend the lab session** with Xuan on Friday to set up remote access to the EDA tools

  – **Paper review "*The limits of correctness*"**

Paper review

Brian Cantwell Smith. 1985. The limits of correctness.
SIGCAS Comput. Soc. 14,15, 1,2,3,4 (Jan 1 1985), 18–26.
DOI: https://doi.org/10.1145/379486.379512

THE LIMITS OF CORRECTNESS†

Brian Cantwell Smith*

- *Identify the main lines of argument*
- *Why does the author question the notion of "correctness"?*
- *What are the two or three key take-away messages for you?*

Over the last ten years, the Defense Department has spent many millions of dollars on a new computer technology called "program verification" - a branch of computer science whose business, in its own terms, is to "prove programs correct". Pro-

And my answer, to give away the punch-line , is no. For fundamental reasons - reasons that anyone can understand - there are inherent limitations to what can be proven about computers and computer programs. Although program verification is an important new technology, useful, like so many

TABLE 1: Generic Marking Criteria mapped against the three marking scales

Grade	0-20 point scale	0-100 point scale	Criteria to be satisfied
A	20 19 18	100 94 89	➢ Work would be worthy of dissemination under appropriate conditions. ➢ Mastery of advanced methods and techniques at a level beyond that explicitly taught. ➢ Ability to synthesise and employ in an original way ideas from across the subject. ➢ In group work, there is evidence of an outstanding individual contribution. ➢ Excellent presentation. ➢ Outstanding command of critical analysis and judgement.
	17 16 15	83 78 72	➢ Excellent range and depth of attainment of intended learning outcomes. ➢ Mastery of a wide range of methods and techniques. ➢ Evidence of study and originality clearly beyond the bounds of what has been taught. ➢ In group work, there is evidence of an excellent individual contribution. ➢ Excellent presentation. ➢ Able to display a command of critical analysis and judgement.
B	14 13 12	68 65 62	➢ Attained all the intended learning outcomes for a unit. ➢ Able to use well a range of methods and techniques to come to conclusions. ➢ Evidence of study, comprehension, and synthesis beyond the bounds of what has been explicitly taught. ➢ Very good presentation of material. ➢ Able to employ critical analysis and judgement. ➢ Where group work is involved there is evidence of a productive individual contribution.
C	11 10 9	58 55 52	➢ Some limitations in attainment of learning objectives but has managed to grasp most of them. ➢ Able to use most of the methods and techniques taught. ➢ Evidence of study and comprehension of what has been taught ➢ Adequate presentation of material. ➢ Some grasp of issues and concepts underlying the techniques and material taught. ➢ Where group work is involved there is evidence of a positive individual contribution.
D	8 7	48 45	➢ Limited attainment of intended learning outcomes. ➢ Able to use a proportion of the basic methods and techniques taught. ➢ Evidence of study and comprehension of what has been taught, but grasp insecure. ➢ Poorly presented. ➢ Some grasp of the issues and concepts underlying the techniques and material taught, but weak and incomplete.
E	6	42	
	5	35	➢ Attainment of only a minority of the learning outcomes. ➢ Able to demonstrate a clear but limited use of some of the basic methods and techniques taught. ➢ Weak and incomplete grasp of what has been taught. ➢ Deficient understanding of the issues and concepts underlying the techniques and material taught.
	1 - 4	7 - 29	➢ Attainment of nearly all the intended learning outcomes deficient. ➢ Lack of ability to use at all or the right methods and techniques taught. ➢ Inadequately and incoherently presented. ➢ Wholly deficient grasp of what has been taught. ➢ Lack of understanding of the issues and concepts underlying the techniques and material taught.
0	0	0	➢ No significant assessable material, absent, or assessment missing a "must pass" component.

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Questions

https://www.bristol.ac.uk/tsl