Introduction to
Design Verification
COMS31700

Kerstin Eder

Design Automation and Verification

University of BRISTOL

Department of COMPUTER SCIENCE

Welcome to COMS31700

- Lecturer
  - Kerstin EDER
  - Department of Computer Science
  - Room 3.25 MVB
  - Kerstin.Eder@bristol.ac.uk
  - Office hours:
    - Tu before our lectures but not 10:30-12:00
    - Alternatively, just come to my office.
    - Email may not get you a timely response.
- Lecture notes, exercises and assignments are/will be online at:
  http://www.cs.bris.ac.uk/Teaching/Resources/COMS31700/
- Comments and feedback are always welcome

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COMS31700 Unit Details

- Lectures (weeks 1 – 12)
  - Please check your timetable, at the moment:
  - Monday (1h) 14:00 – 14:50 in MVB 1.11
    - except for wk1, wk8, wk12 in QB 1.18
  - Tuesday (2h) 14:00 – 15:50 in MVB 1.11
    - except for wk4 PHYS B16/17 ENDERBY and wk8 QB 1.8
- Practical Work (weeks 1 – 12)
  - You are expected to invest 2h per week into practical work.
  - DV Help Desk on demand
  - Teaching Assistant: Kris Nikov and George Field
- Assessment   Deadlines will soon be on COMS31700 web page!
  - 2 assignments (25% due in week 5/6, 25% due in week 10/11/12)
  - individual feedback session and assignment review seminars
    - Option to obtain "feed forward"
  - 1 exam (50% in January)

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Literature and Study Resources

- **Janick Bergeron**
  Writing Testbenches: Functional Verification of HDL Models.
  First Edition, Kluwer, 2000, ISBN: 0-7923-7766-4
  Second Edition, Kluwer, 2003, ISBN: 1-4020-7401-8
- verificationacademy.com
- In addition:
  - Lecture slides and on-line tutorials on COMS31700 web page
  - On-line documentation of ModelSim/Questa Simulator and SpecMan Elite
  - Watch the unit web page for further supplementary literature.

[**Credits:** Parts of the lecture notes contain material from the book "Comprehensive Functional Verification" by Bruce Wile etal, the book "Writing Testbenches: Functional Verification of HDL Models" by Janick Bergeron, the book "The Verilog Hardware Description Language" by Donald Thomas and from lecture slides developed at IBM (by Avi Ziv and Jaron Wolfstal), the University of Pittsburgh, Penn State University, North Carolina State University and Ohio State University. The HDL for the assignments has been developed at IBM.]

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What is this unit about?

Aim:
To familiarise you with the state of the art in Design Verification, and to give you the **technical background** plus some of the **practical skills** expected from a professional Design Verification Engineer.

- Pre-/Co-requisites: programming experience

On successful completion of this unit, you will be able to:
- understand the complexities and limits of verification;
- carry out functional verification and determine its effectiveness;
- set appropriate verification goals, select suitable verification methods and assess the associated risks;
- compile a verification plan that fits into the flow of a design project;
- organise a verification team.

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Unit Outline

Lecture Topics
- Introduction: What is Verification? What is a Testbench?
- Verification Flow and Tools including basic Verilog HDL coding
- Verification cycle, methodology and plan including coverage
- Simulation-based Verification: Stimulus Generation and Checking
- Assertion-based Verification (ABV)
- Advanced Testbench Design Methodology with SpecMan Elite
- (Functional Formal Verification and Property Checking)

Labs
- Exercise 1: Evita Verilog interactive tutorial (do @ home asap)
- Exercise 2: Introduction to the ModelSim/Questa Simulator
- A1, weeks 2-6: Verification of calculator design with ModelSim/Questa
- Exercise 3: How to collect Code Coverage with ModelSim/Questa
- Exercise 4: Introduction to SpecMan Elite
- A2, weeks 7-11: Advanced testbench design with SpecMan Elite

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What is Design Verification?

What is Design Verification?

"Design Verification is the process used to gain confidence in the correctness of a design w.r.t. the requirements and specification."

Types of verification:
- Functional verification
- Timing verification
- ...
- What about performance?

Verification vs Validation

- Verification:
  - Confirms that a system has a given input / output behaviour, sometimes called the **transfer function** of a system.
- Validation:
  - Confirms that the system's transfer functions results in the intended system behaviour when the system is employed in its target environment, e.g. as a component of an embedded system.
- Validation is sometimes used when verification is meant.

Why is Verification important?

- Verification is the single biggest lever to effect the triple constraints:

Quality
- A high quality track record preserves revenue and reputation.
- Ideally a team can establish a "right-first-time" track record.

Cost
- Fewer revs through the development/fabrication process means lower costs.
- Respinning a chip costs hundreds of thousands of £/$/€
  + the associated lost opportunity costs.

Timing/Schedule
- Fewer revs through the development/fabrication process means faster time-to-market.
- Respinning a chip costs 6-8 weeks at least
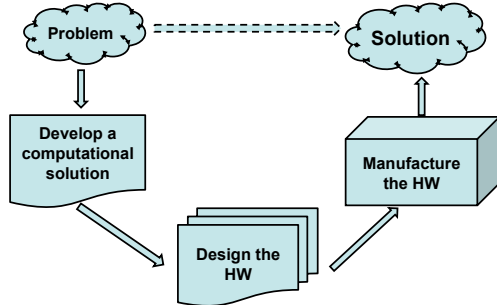 + the associated "lost opportunity" costs.

All about Bugs

Types of bugs
How are bugs introduced?
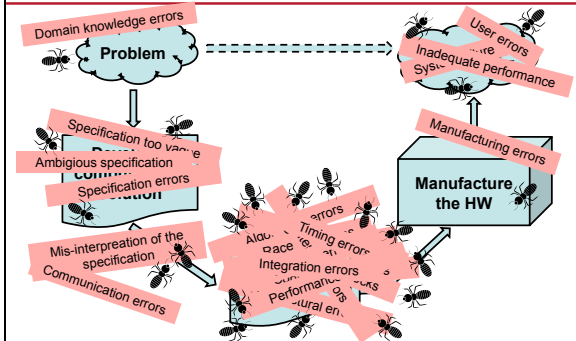How can bugs be found?

Why do Designs have Bugs?
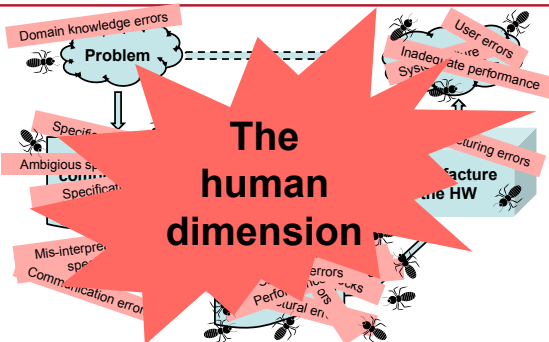
Why do Designs have Bugs?

Problem → Solution
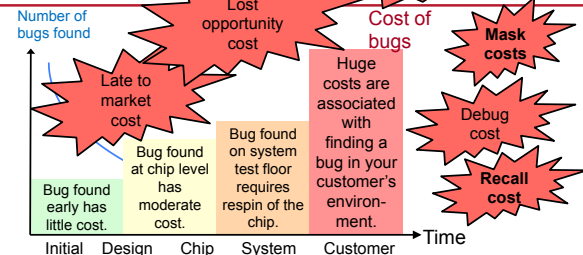
Develop a computational solution

Design the HW

Manufacture the HW

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Why do Designs have Bugs?

Domain knowledge errors
Problem
User errors
Inadequate performance
System
Specification too vague
Ambigious specification
Specification errors
Manufacturing errors
Manufacture the HW
Mis-interpreation of the specification
Communication errors
Timing errors
Race
Integration errors
Performance
Architectural errors

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Why do Designs have Bugs?

Domain knowledge errors
Problem
User errors
Inadequate performance
System

The human dimension

Specification
Ambigious s
Specification
Mis-interpre
Communication error
Manufacturing errors
Manufacture the HW
Performance
Architectural en

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Cost of Bugs over

Number of bugs found

Loss of Reputation

Lost opportunity cost

Cost of bugs

Mask costs

Late to market cost

Bug found early has little cost.

Bug found at chip level has moderate cost.

Bug found on system test floor requires respin of the chip.

Huge costs are associated with finding a bug in your customer's environment.

Debug cost

Recall cost

Initial | Design | Chip | System | Customer → Time

The longer a bug goes undetected, the more expensive it is!

Remember the Intel FDIV bug!
ttp://en.wikipedia.org/wiki/Pentium_FDIV_bug

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Mask costs (Electronics Weekly, 10 October 2007)

EDA AND IP
Why design a custom integrated circuit?

Mask costs versus line width

Process (μm)	Vdd	Metal	Gates/sq mm	Mask set cost ($)
0.065	1.0	9	400k	3,000,000
0.09	1.0	9	200k	1,500,000
0.13	1.2	7	100k	750,000
0.18	1.8	6	40k	250,000
0.25	2.5	5	24k	150,000
0.35	3.3	3	12k	40,000
0.5	3.3	3	5k	20,000
0.6	5.0	2	4k	18,000

A CLASS ACT IS TOUGH TO FOLLOW

SCHURTER

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Increasing Design Complexity vs tight TTM Constraints

ITRS Edition 2009, Design Chapter (http://www.itrs.net)
– Hardware and Software Design Gaps versus Time

log

LoC SW/Chip
Gates/Chip
Gates/Day
LoC/Day

Additional SW required for HW
2x/10 months

Technology capabilities
2x/36 months

HW including SW design gap

HW design gap

Moore's Law

HW design productivity
Filing with IP and memory

HW design productivity

SW productivity
2x/5 years

1981 1985 1989 1993 1997 2001 2005 2009 2013 2017 2021 2025 time
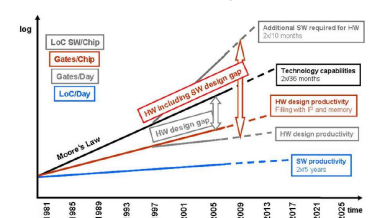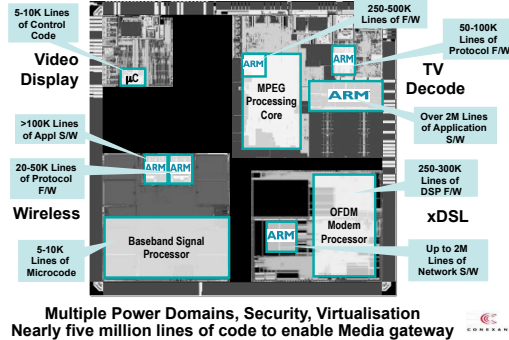
Getting it right (first time) is more and more difficult:
– rapidly increasing design complexity
– tight "time-to-market" constraints
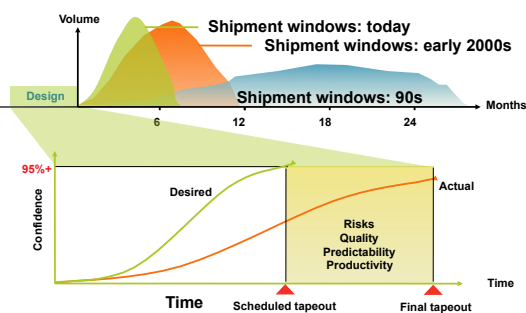
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Increasing Design Complexity

5-10K Lines of Control Code

Video Display

μC

250-500K Lines of F/W

MPEG Processing Core

ARM

50-100K Lines of Protocol F/W

TV Decode

>100K Lines of Appl S/W

20-50K Lines of Protocol F/W

ARM ARM

Wireless

Over 2M Lines of Application S/W

250-300K Lines of DSP F/W

5-10K Lines of Microcode

Baseband Signal Processor

ARM

OFDM Modem Processor

xDSL

Up to 2M Lines of Network S/W

**Multiple Power Domains, Security, Virtualisation
Nearly five million lines of code to enable Media gateway**

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Increasing Design Complexity

- From mobile phone to smart phone

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Shorter Time-To-Market Windows

Volume

Shipment windows: today
Shipment windows: early 2000s

Design

Shipment windows: 90s

6   12   18   24   Months

95%+

Confidence

Desired

Actual

Risks
Quality
Predictability
Productivity

Time

Scheduled tapeout   Final tapeout

Time

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Increasing Verification Productivity

Need to minimise verification time e.g. by using:

- **Parallelism:** Add more resources
- **Abstraction:**
  - Higher level of abstraction (i.e. C vs Assembly)
  - This often means a reduction of control!
- **Automation:**
  - Tools to automate standard processes
  - Requires standard processes/methodology.
  - Usually a variety of functions, interfaces, protocols, and transformations must be verified.
  - Not all (verification) processes can be automated.

Productivity improvements drive early problem discovery!

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Increasing Verification Productivity

**Productivity improvements drive
early problem discovery**

Total Number of Bugs found

Test

Verification

Time
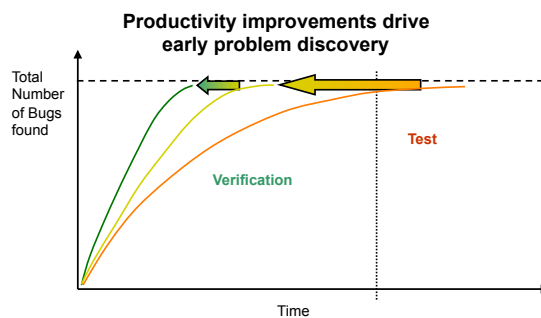
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## Cost of Bugs to IP companies

- IP business model means ARM is not impacted by immediate re-spin costs
- BUT.....
  - The ARM partners are shipping >6B units per year (2011)
  - The potential impact to business partners and is MASSIVE!
    - Support burden, debug and maintenance overhead
    - Cost of lost opportunity for client and for ARM
    - Potential for loss of credibility and reputation
      - Credibility impact translates to opportunity impact
    - Erosion of product integrity due to limitations of metal fixes
  - Critical bugs may quickly escalate to Exec level between ARM and ARM's partners
  - Remember the Intel FDIV bug!
    http://en.wikipedia.org/wiki/Pentium_FDIV_bug
    - Bugs are a reality – perfect verification is a myth.
    - What matters is the ARM response.
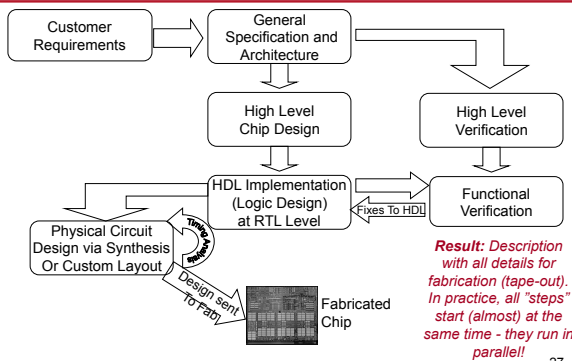
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Verification in the IC Design Process

The IC Design Process
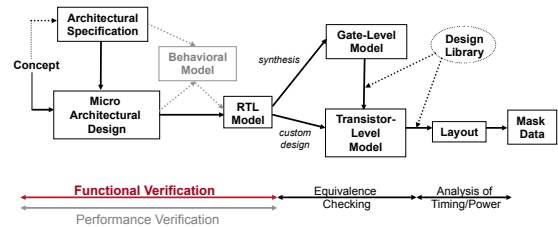
Functional verification aims to demonstrate that the functional intent of a design is preserved in its implementation.

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Chip Design Process

Result: *Description with all details for fabrication (tape-out). In practice, all "steps" start (almost) at the same time - they run in parallel!*
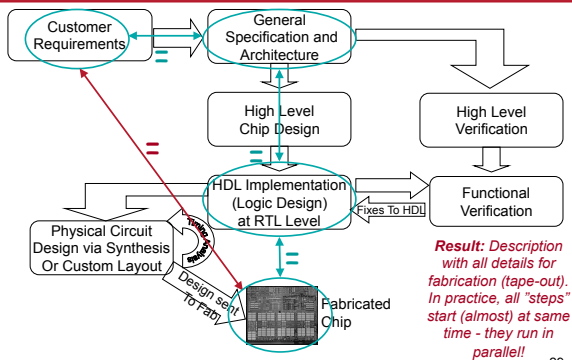
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Role of Verification in IC Design

IC design process is complex:
- **Engineers need to balance conflict of interest:**
  - Tight time-to-market constraints vs. increasing design complexity
- **Aim:** "Right-first-time" design, "correct-by-construction"
- More and more time-consuming to obtain acceptable level of confidence in correctness of design!
- **design time << verification time**
  - Remember: Verification does not create value!
    - But it preserves revenue and reputation!
  - Up to 70% of design effort can go into verification.
  - 80% of all written code is in the verification environment.
  - Properly staffed design teams have dedicated verification engineers.
  - In some cases verification engineers outnumber designers 2:1.
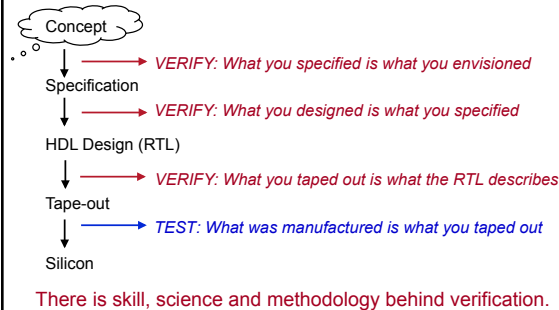
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Chip Design Process

Result: *Description with all details for fabrication (tape-out). In practice, all "steps" start (almost) at same time - they run in parallel!*

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What are you going to verify?

How do Designers know whether a circuit is correct?

Concept

→ *VERIFY: What you specified is what you envisioned*

Specification

→ *VERIFY: What you designed is what you specified*

HDL Design (RTL)

→ *VERIFY: What you taped out is what the RTL describes*

Tape-out

→ *TEST: What was manufactured is what you taped out*

Silicon

There is skill, science and methodology behind verification.

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Reconvergence Models [Bergeron]

Conceptual representation of the verification process
- Most important question:

What are you verifying?

**Transformation**

Verification

- Purpose of verification is to ensure that the result of some transformation is as intended or as expected.

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Verification vs. Test

- **Often confused!**
  - Purpose of test is to show design was **manufactured** properly.
  - Verification is done to ensure that **design meets its functional intent prior to manufacture!**

Specification — HW Design — Netlist — Fabrication — Silicon Chip
Verification — Test
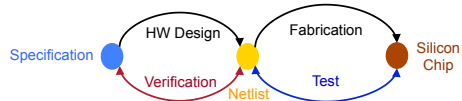
- One test method is scanning: **"Design for Test"** methodology
  - Link all internal registers together into a chain.
  - Chain accessible from chip pins.
  - Allows control/observation of internal state.
  - Impacts area of design, but keeps testing cost down.
- Why not **"Design for Verification"?** [Hot topic of research!]
- @DT, consider: What is design supposed to do? How will it be verified?

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Formal: Equivalence Checking

Compares two models to check for equivalence.
- Proves mathematically that both are *logically equivalent*.
  - Commonly used on **lower levels** of design process.
- Example: RTL to Gates (Post Synthesis)

RTL — Synthesis — Gates
Equivalence Check
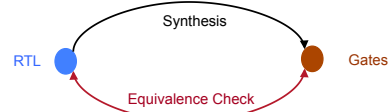
Why do equivalence checking when EDA tools exist for synthesis?

- See "*HDL Chip Design - A Practical Guide for Designing, Synthesising, and Simulating ASICs and FPGAs using VHDL or Verilog*" book by Douglas Smith page 136 and compare MUX spec with what they claim will be synthesised!

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Equivalence Checking

F

G

Inputs — Outputs
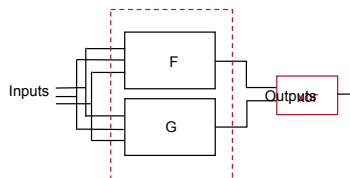
- Conceptually, is there an input vector such that the output of the XOR gate can be "1"?

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Cost of Verification

Necessary Evil
- Always takes too long and costs too much.
- As number of bugs found decreases, cost and time of finding remaining ones increases.

So when is verification done?   (Will investigate this later!)
  - Remember: Verification does not generate revenue!

Yet indispensable
- To create revenue, design must be functionally correct and provide benefits to customer.
- Proper functional verification demonstrates **trustworthiness** of the design.
- Right-first-time designs demonstrate **professionalism** and "increase" reputation of design team.

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Slide 37

Verification is similar to statistical hypothesis testing

Hypothesis "under test" is: **The design is functionally correct.**

	Good Design (no bugs in design)	Bad Design (buggy design)
Bugs found		
No Bugs found		

Slide 38

Verification is similar to statistical hypothesis testing

Hypothesis "under test" is: **The design is functionally correct.**

	Good Design (no bugs in design)	Bad Design (buggy design)
Bugs found	Type I: False Positive	
No Bugs found		

Type I mistakes ("convicting the innocent", a "false alarm"):
- Easy to identify - found error where none exists.

Slide 39

Verification is similar to statistical hypothesis testing

Hypothesis "under test" is: **The design is functionally correct.**

	Good Design (no bugs in design)	Bad Design (buggy design)
Bugs found	Type I: False Positive	
No Bugs found		Type II: False Negative

Type I mistakes ("convicting the innocent", a "false alarm"):
- Easy to identify - found error where none exists.

Type II mistakes ("letting the criminal walk free", a "miss"):
- Most serious - verification failed to identify an error!
- Can result in a bad design being shipped unknowingly!

Slide 40

Summary

- **What is Design Verification?**
  - Why do we care?
  - Verification vs validation
- **Bugs**
  - Sources of bugs
  - Cost of bugs
  - Importance of Design Verification
- **Impact of increasing design complexity**
  - ITRS
  - Shrinking time to market windows
  - Increasing Productivity
- **The chip design process**
  - Where does Verification "fit"?
- **Reconvergence Models**
  - Help us identify what is being verified