

Design Verification

COMS30026

(COMS30066 with coursework)

WEEKLY LIVE SESSION – W7

Kerstin Eder

Trustworthy Systems Lab

Topics W5

- ✓ High-level Verification: sn and e – Part 1
- ✓ High-level Verification: sn and e – Part 2
- ✓ **Cadence e language training course**

Topics W5

- ✓ High-level Verification: sn and e – Part 1
- ✓ High-level Verification: sn and e – Part 2
- ✓ **Cadence e language training course**
- **Lab from Week 6:**
 - Practical 2 (Weeks 6-11)**
 - calc1 DUV provided as **white box design**
 - Specification clarification
 - Refinement of your **Verification Plan**
 - Debug calculator design using Specman and “e”
 - Basic “e” testbench on Blackboard

DESIGN VERIFICATION Practical 2: Debugging a Calculator Design (Weeks 6-11)

The aim of this practical is for you to explore advanced verification methodologies and to experience the power of automation in simulation-based verification with state-of-the-art industrial verification tools.

This practical requires you to find bugs in the same calculator design as used for Practical 1, but this time you should explore the use of the e language and the Specman Elite verification environment to perform the verification. In particular, this practical offers you the opportunity to practice and develop skills in using an advanced verification methodology including constrained pseudo-random test generation, automatic checking and different forms of coverage.

For this practical, the calc1 calculator design source code is provided. An example .e testbench has been demonstrated during a live session. This testbench implements basic constrained pseudo-random test generation, a simple check for the ADD command and shows how coverage can be collected. The .e code of this testbench is provided to give you a starting point.

Calculator Specification - [same functionality as for Practical 1]

Input/Output Specification

The calculator has 4 commands: add, subtract, shift left and shift right. It can handle (but not process) 4 requests in parallel. All 4 requestors use separate input signals. All requestors have equal priority. Figure 1 shows the input output ports of the calculator.

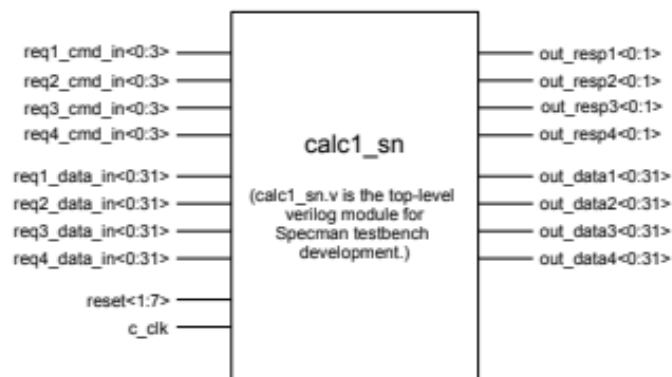


Figure 1: Top-level of Calculator Design for Specman Testbench Development

Topics W7

- ✓ Assertion-based Verification – Part I
 - ✓ Introduction and OVL
- Assertion-based Verification – Part II
 - Property formalisation and SVA
- Functional Formal Verification

Revision: Use of Assertions

- Properties describe facts about a design.
- Properties can be used to write
 - Statements about the expected behaviour of the design and its interfaces
 - Combinatorial and sequential
 - (Can be used for simulation-based or for formal verification.)
 - Checkers that are active during simulation
 - e.g. protocol checkers
 - Constraints that define legal stimulus for simulation
 - Assumptions made for formal verification
 - Functional coverage points
- Remember to re-use existing assertions, property libraries or checks embedded in VIP.

Topics W7

- ✓ Assertion-based Verification – Part I
 - ✓ Introduction and OVL
- Assertion-based Verification – Part II
 - Property formalisation and SVA
- Functional Formal Verification
- **Lab Week 7:**
 - Practical 2 (Weeks 6-11)**
 - **SN Demo** in the lab this week
 - **Cadence e language training course**
 - *All .e and .v files and the lab sheet are on BB, please download in preparation for the demo.*

Next

- Recordings of lectures for **Week 7**:
 - ✓ Assertion-based Verification – Part I and Part II
 - ✓ Functional Formal Verification (by end of week)
 - uobdv.github.io/Design-Verification/
shows a **weekly schedule of topics** to watch, ideally BEFORE the next online session
 - Recordings are available from Blackboard unit page
- Tasks for you this week:
 - Ensure you've watched the e language lectures and you have familiarized yourself with **Practical 2**
 - **Complete the e language training course** (if you've signed up)
 - **Attend the lab session** for a demo of the basic e language testbench modules to be used for **Practical 2**

Apple Guest Lecture 2021

Pete Vigil on *Design Verification for GPUs - Practice and Challenges*

Wednesday, 15 December 2021, 10am GMT

This talk covers the broad range of verification tools, techniques and processes, introduces aspects of GPU architecture, and explores the unique challenges of verification for GPU designs.

Speaker Bio: Pete Vigil is the site lead and design verification manager for the GPU group at Apple's St. Albans site. He has worked in verification for over 30 years, from start-ups to large companies, and on many types of designs including CPUs, GPUs, and other IP. Pete holds a BSCSE from Santa Clara University, has co-founded two verification start-ups. and is co-author on a number of design patents.

Design vs Verification

Salaries


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Experience	Graduate	3 years	5 years	10 years	12+ years
Digital IC Design	<i>Perm (p.a)</i> £34,000	£42,000	£52,000	£65,000	£75,000+
	<i>Cont (p.h)</i> -	£42	£48	£50	£52+
Digital IC Verification	£34,000	£42,000	£55,000	£65,000	£80,000+
	-	£42	£48	£52	£55+
Physical Design	£34,000	£42,000	£52,000	£65,000	£75,000+
	-	£40	£46	£50	£52+
FPGA Design	£31,000	£40,000	£47,000	£60,000	£70,000+
	-	£40	£48	£50	£52+
Analog/Mixed Signal IC Design	£34,000	£42,000	£52,000	£65,000	£75,000+
	-	£42	£48	£52	£55+
RF IC Design	£37,000	£45,000	£57,000	£70,000	£85,000+
	-	£42	£48	£52	£55+
Analog / RF Layout	£30,000	£38,000	£41,000	£52,000	£60,000+
	-	£40	£45	£50	£50+
IC Test	£32,000	£38,000	£40,000	£45,000	£60,000+
	-	£45	£50	£55	£60+
IC Process	£32,000	£38,000	£40,000	£45,000	£60,000
	-	-	-	-	-

Opportunities – Week 7



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Austin, TX 78758
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info@dvclub.org

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Welcome to DVClub!

Our charter is to provide local education and networking events for the semiconductor verification and design community in North America. Founded by Eric Hennenhoefer in 2005, and now managed by Paradigm Works Engineers - Michael Hoyt, Jim Crocker, and Kelly Larson (Tesla). DVClub regularly holds events across North America including - San Jose, Austin, Boston, Portland, Toronto, RTP, and Fort Collins. If you are new to DVClub, please [join DVClub](#) or [register for a specific event](#) and follow us on [Twitter](#) for updates on upcoming events in your area!

[Register For An Event](#)[Join DVClub](#)

DVClub Conference Schedule 2021 (Online)

May 5	Silicon Valley/LA/Portland	September 15	Austin/Ft Collins/MN
June 9	Austin/Ft. Collins/MN	October 20	North America
July 21	Toronto/Boston/RTP	November 17	Silicon Valley/LA/Portland
August 11	Silicon Valley/LA/Portland	December 8	Austin/Ft Collins/MN

[Upcoming Events](#)

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<https://dvclub.org/>

Opportunities – Week 7

DVClub

The Design and Verification Club (Europe and India)

The principal goal of each DVCLUB conference is the sharing of technical expertise amongst professionals while helping build the verification community through regular educational and networking events. DVClub membership is free and is open to all non-service provider semiconductor professionals.

DVClub currently has chapters in Austin, Bangalore, Boston, Bristol, Cambridge, Dallas, Delhi, Eindhoven, Grenoble, RTP, Shanghai, Silicon Valley, Sophia Antipolis and Toronto. T&VS organise events in Europe and India.



DVClub Europe

Forthcoming Events

DVClub Europe: Diary Dates

Using ML and AI in EDA Tools	Nov 23, 2021
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Previous Events

Formal Verification Adoption Made Easy	Sep 07, 2021
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Using Python in Verification	Apr 20, 2021
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Accelerating your SoC Verification	Feb 23, 2021
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DVClub India

Forthcoming and Previous Events

Safety Driven Verification	Sep, 2018
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Unique Challenges in Verifying Automotive SoCs	Nov, 2017
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Verification IPs – Build vs Buy	Apr, 2017
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IP Verification Challenges	May, 2016
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[See all previous Events](#)



DVClub China

[See previous Events](#)

<https://www.testandverification.com/conferences/dvclub>

Opportunities – Week 7

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NOV 23



DVclub Europe: Using ML and AI in EDA Tools

by Tessolve Semiconductor Ltd

34 followers [Follow](#)

Free

[Register](#)

Do not miss the opportunity to join us for interesting talks on industry specific topics

About this event

Using ML and AI in EDA Tools

- Four verification experts will spend 20 minutes each outlining tools and methodologies aimed at Using ML and AI in EDA Tools

Agenda (GMT)

Date and time


Tue, 23 November 2021
12:00 – 13:30 GMT
[Add to calendar](#)

Location


Almondsbury Interchange Hotel
Gloucester Road
Almondsbury
Bristol
BS32 4AA
[View Map](#)


<https://www.testandverification.com/conferences/dvclub/europe/using-ml-and-ai-in-eda-tools>


Opportunities – Week 7


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NMI Meet and Greet Event

 24th November

 09:00 – 15:00

 Holiday Inn, Newport





NOV 24



NMI Meet & Greet Event

by Angela Tansey

175 followers [Follow](#)

Free

[Register](#)

Bring R&D, Universities, Manufacturing and Suppliers together to discuss how emerging R&D capabilities bring new opportunities.

About this event

The purpose of the NMI Meet & Greet events is to bring R&D, Universities, Manufacturing and Suppliers together to discuss how emerging R&D capabilities bring new opportunities for collaboration in the future with the wider Semiconductor supply chain.

NMI existing members have the equipment, knowledge and expertise that supports both mass production and some of the smaller specialised FABS that are often located within the universities facilities.

Date and time

Wed, 24 November 2021
09:00 – 15:00 GMT
[Add to calendar](#)

Location

Holiday Inn Newport, an IHG Hotel
The Coldra
Newport
NP18 2YG
[View Map](#)

<https://www.eventbrite.co.uk/e/nmi-meet-greet-event-tickets-192182562217>

Questions



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<https://www.bristol.ac.uk/tsl>