Incisive Enterprise Simulator

IUS 8.2 — November 2008

This is a quick reference for the Incisive simulators. It lists only common options (type `-help` for all options). For more information, see *NC-Verilog Simulator Help* or *NC-VHDL Simulator Help*.

Setup Files

`cds.lib` defines design libraries and associates logical lib names with physical locations; specifies `tmp` area for design libaries, and includes other `cds.lib`. CDS.LIB statements:

DEFINE *lib_name path*
UNDEFINE *lib_name*
INCLUDE *filename*
SOFTFINCLUDE *filename*
ASSIGN *lib* **TMP** *path*
UNASSIGN *lib* **TMP**

`hdl.var` defines tool and utility variables. Variables include:

`LIB_MAP, NCELABOPTS, NCPROTECTOPTS, NCSIMRC, NCSIMOPTS, NCSDFCOPTS, NCUPDATEOPTS, NCVHDLOPTS, NCVERILOGOPTS, NCVLOGOPTS, WORK, VERILOG_SUFFIX, VHDL_SUFFIX, VIEW, VIEW_MAP`

`setup.loc` specifies the search order that tools use while searching for `cds.lib` and `hdl.var` files

`ncsimrc` command file when *ncsim* is invoked; contains commands used with every simulation run

Environment and License (UNIX)

License

Copy license file (`license.dat`) to license server. Run *`install_dir`*`/tools/bin/lmgrd -c` *`path_of_license`*`.dat`

Environment

Add *`install_dir`*`/tools/bin` to `PATH` variable. Set `CDS_LIC_FILE` variable to *`port-name@lic-server`*. Set `LD_LIBRARY_PATH` (Solaris and Linux) or `LIBPATH` (AIX) to *`install_dir`*`/tools/lib`

Options Common to all IUS Binaries

`-64BIT`
Invoke 64-bit executable

`-APPEND_LOG`
Append messages to an existing log file

`-CDSLIB` *`cdslib_filename`*
Specify the `cds.lib` file to load

`-ERRORMAX` *`integer`*
Specify the maximum number of errors processed

`-FILE` *`filename`*
Load command-line arguments from file

`-HDLVAR` *`hdlvar_filename`*
Specify the `hdl.var` file to load

`-HELP`
Print all available options

`-LOGFILE` *`filename`*
Specify the file to contain log information

`-MESSAGES`
Enable printing of messages

`-NCERROR` *`warning_code`*
Increase a message's severity from warning to error

`-NCFATAL` *`warning_error_code`*
Increase message's severity from warning/error to fatal

`-NEVERWARN`
Disable printing of all warning messages

`-NOSTDOUT`
Turn off output to the screen

`-NOWARN` *`warning_code`*
Disable printing of the specified warning message

`-STATUS`
Print the run-time status at the end of processing

`-UPDATE`
Verify and update, if necessary

`-VERSION`
Print the version number

NCVHDL Options

`-AMS`
Enable AMS parsing

`-ASSERT`
Enable PSL language parsing

`-INITZERO`
Initialize integer and time objects to zero

`-LINEDEBUG`
Enable source line number debugging

`-NOVITALCHECK`
Suppress VITAL compliance checking

`-PROPFILE` *`filename`*
Load PSL verification code from a file

`-RELAX`
Enable relaxed interpretation of VHDL constructs

`-SMARTORDER`
Order-independent compilation (OIC)

`-SMARTSCRIPT` *`filename`*
Specify OIC compilation script output file

`-V93`
Enable VHDL-93 features

`-WORK` *`library`*
Specify the work library

NCVLOG Options

`-AMS`
Enable AMS parsing

`-ASSERT`
Enable PSL language parsing

`-CHECKTASKS`
Check all `$tasks` are predefined system tasks

`-DEFINE` *`identifier`*`[=`*`value`*`]`
Define a macro

`-IEEE1364`
Report errors according to IEEE 1364 standard

`-INCDIR` *`directory`*
Specify an `include` directory

`-LIBCELL`
Mark cells with `` `celldefine ``

`-LIBMAP`
Specify the Verilog library mapping file

`-LINEDEBUG`
Enable source line number debugging

`-PROPFILE` *`filename`*
Load PSL verification code from a file

`-SV`
Enable SystemVerilog features

`-V1995 | -V95`
Turn off new Verilog-2001 keywords

`-VIEW` *`view_name`*
Specify the view name

`-WORK` *`library`*
Specify the work library

NCELAB Options

`-ACCESS` *`access_specification`*
Set default access visibility
+rwc turn on read/write/connectivity

`-AFILE` *`filename`*
Specify an access file

`-COVERAGE` *`coverage_type`*
Enable coverage type

`-DEFPARAM` *`param=value`*
Associate values with Verilog parameters

`-GENAFILE` *`filename`*
Generate an access file

`-GENERIC` *`generic=>value`*
Set values of VHDL generics

`-LIBMAP` *`filename`*
Specify the Verilog library mapping file

`-LIBNAME` *`library=name`*
Specify the name of a library to search

`-NOSPECIFY`
Disable timing checks, path delays, or SDF annotation

`-NOTIMINGCHECKS`
Disable timing checks

-SDF_CMD_FILE *sdf_command_file*
Specify file of SDF annotation commands
-SDF_FILE *sdf_file*
Specify SDF file to use
-SDF_NO_WARNINGS
Do not report SDF warnings
-SDF_PRECISION *precision*
Specify precision for SDF data
-SNAPSHOT *snapshot_name*
Specify the name of the simulation snapshot
-TFILE *filename*
Specify a timing file
-TIMESCALE *'time_unit/time_precision'*
Set default timescale on Verilog modules
-VHDL_TIME_PRECISION *time_precision*
Set default time precision for VHDL
-WORK *library*
Specify the WORK library

NCSIM Options

-GUI
Start SimVision before running simulation
-INPUT *filename*
Run a Tcl script at startup
-LICQUEUE
Use license queue mechanism
-LOADVPI *shared_libname:bootstrap_fncname*
Dynamically load in VPI <*arg*> = lib:boot_fn(s)
-PLINOWARN
Do not print PLI warning and error messages
-PPE
Enter post-processing mode (PPE) mode in GUI
-PPDB *database_name*
Enter PPE mode with the specified database open
-PROFILE
Generate a run-time profile of the design
-SDF_NO_WARNINGS
Do not report SDF warnings
-SIMVISARGS <*arg*>
Specify string of SimVision arguments to run at startup.
-TCL
Enter interactive mode before running simulation

Low-Power Options

-LPS_CPF *cpf_filename*
Specify name of the CPF file
-LPS_SIMCTRL_ON
Enable simulation-time control over the simulation
-LPS_STIME *start_time*
Specify low-power simulation start time
-LPS_VERBOSE {1 | 2 | 3}
Enable reporting of power information
-LPS_ISO_VERBOSE
Enable reporting of isolation information
-LPS_LOGFILE *filename*
Specify the log file name
-LPS_VERIFY
Generate assertions to verify power control signals
-LPS_RTN_OFF
Turn off implicit state retention behavior
-LPS_ISO_OFF
Turn off implicit isolation behavior
-LPS_STL_OFF
Turn off implicit state loss behavior

irun

Use *irun* to simulate in single-step mode. Include all source files and options on the irun command line. For example:

```
irun -v93 -access +r -gui \
file.v file.vhd file.e file.c
```

You can include all arguments in an arguments file.

```
irun -f irun.args
```

NC Utilities

ncdc: Decompile a Verilog, VHDL or mixed design
ncexport: Copy the source code for an entire compiled or elaborated VHDL design hierarchy into a directory and generate a compilation script
ncgentb: Read an EVCD file and generate a testbench
nchelp: Get help on messages generated by nc binaries
nclaunch: GUI for easy launching of simulation tools
ncls: List compiled objects stored in the library systems, display attributes and information about those objects
ncpack: Change properties of a packed library database
ncprotect: Protect proprietary model information
ncrelocate: Relocate VHDL design library for general use
ncrm: Delete library contents, design units, snapshots, etc.
ncsdfc: Compile and decompile SDF files
ncshell: Generate shells to facilitate model import
ncsuffix: Display the machine architecture and revision number of the library system
ncupdate: Recompile out-of-date units and re-elaborate
simvisdbutil: Command-line database translation utility

Predefined Tcl Variables

display_unit
Time unit used to display time values
vlog_format
Format for output of Verilog values
vhdl_format
Format for output of VHDL values
intovf_severity_level
Simulator stop level upon integer overflow at run time
assert_report_level
Minimum severity level for which VHDL assertion report messages should be output
assert_stop_level
Minimum severity level for which VHDL assertions should cause simulation to stop
pack_assert_off
Package names from which asserts are switched off
help *-variables* for a complete list of variables
echo $*var_name* for the value of a specific variable

ncsim Tcl Debugging Commands

assertion
Assertion-based verification feature
coverage
Set up or perform coverage
database
Control an SHM, VCD, or EVCD database
deposit
Set the value of an object
describe
Display information about a simulation object
drivers
Display all contributors to the value of object
force
Force a specified object to a given value
release
Release an object from a force command
probe
Specify objects for database (SHM, VCD, EVCD)
reset
Reset loaded snapshot to its original state at time zero
run
Advance the simulation time
save
Create a snapshot of the current simulation state
restart
Restart simulation with a saved snapshot
scope
Set the current debug scope
stop
Create or operate on breakpoints
value
Display the current value of specified object(s)