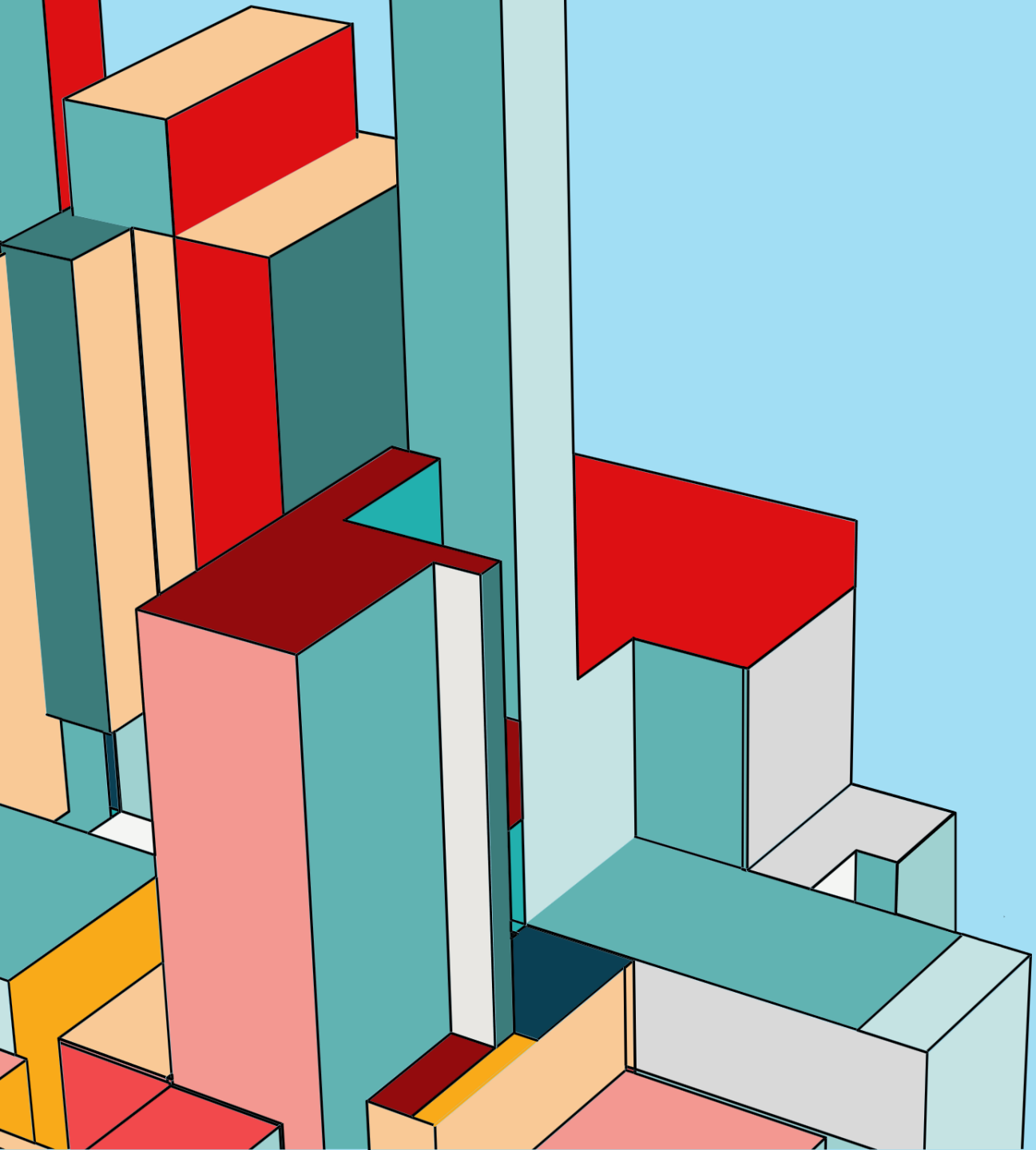
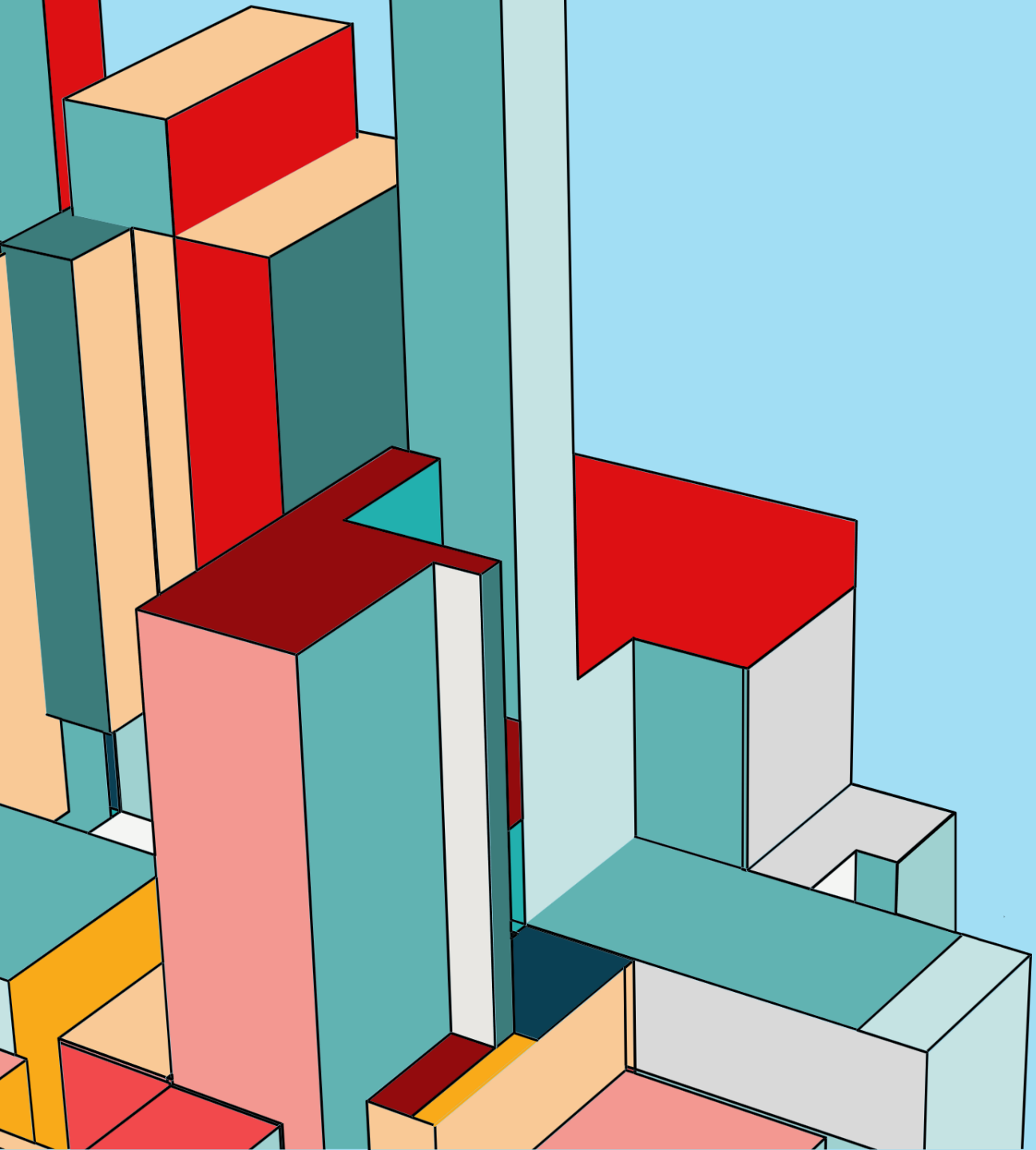


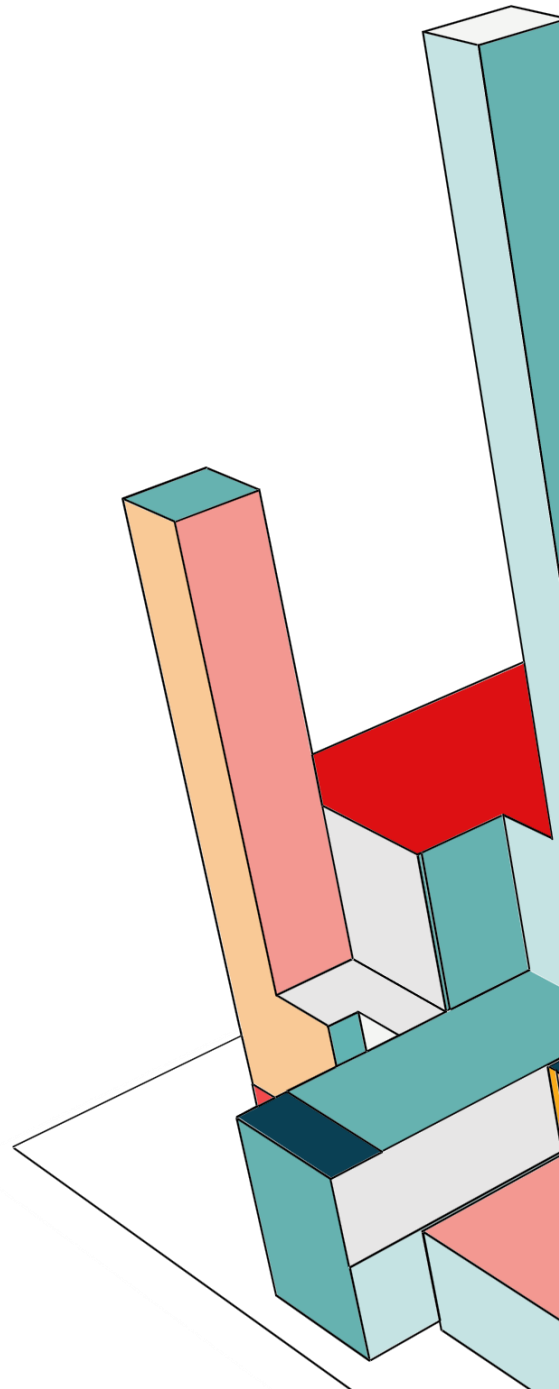
CSE231/EEE211/ETE 211: DIGITAL LOGIC DESIGN

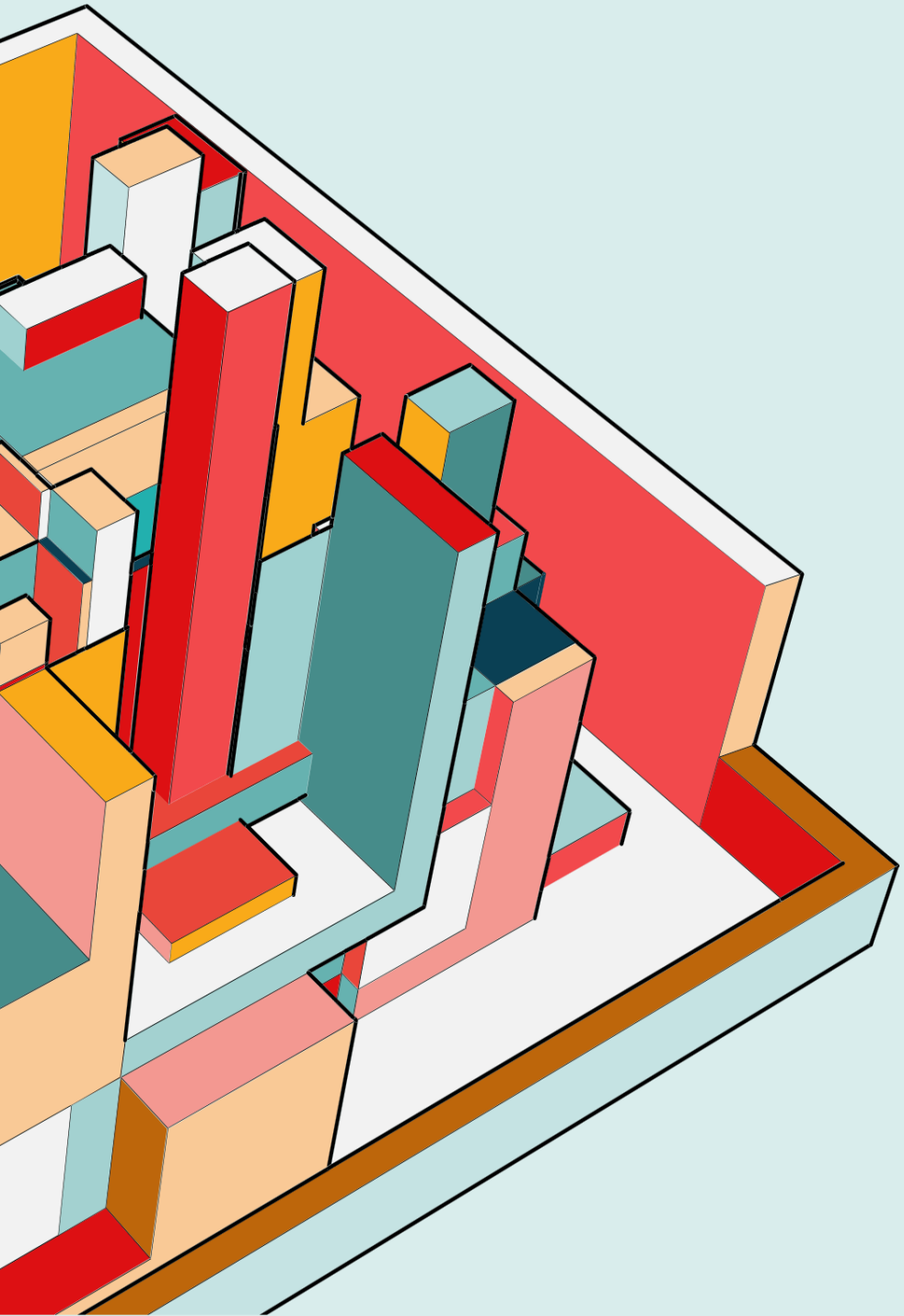


CHAPTER 6: REGISTERS & COUNTERS

AGENDA

- Register
    - 4 bit register
    - Shift/Serial register
    - Serial Adder
    - Universal Shift Register
- Counter
    - Ripple counter
    - Synchronous counters
    - Four-bit synchronous binary counter
    - Four-bit up–down binary count
    - Johnson Counter & Ring Counter



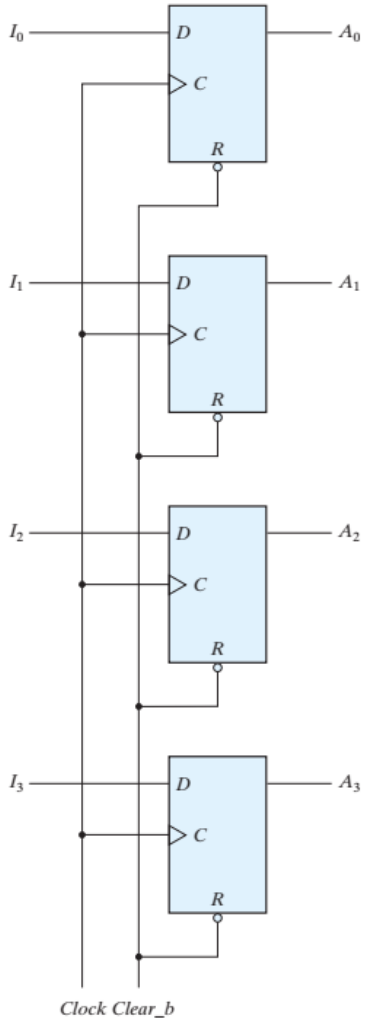


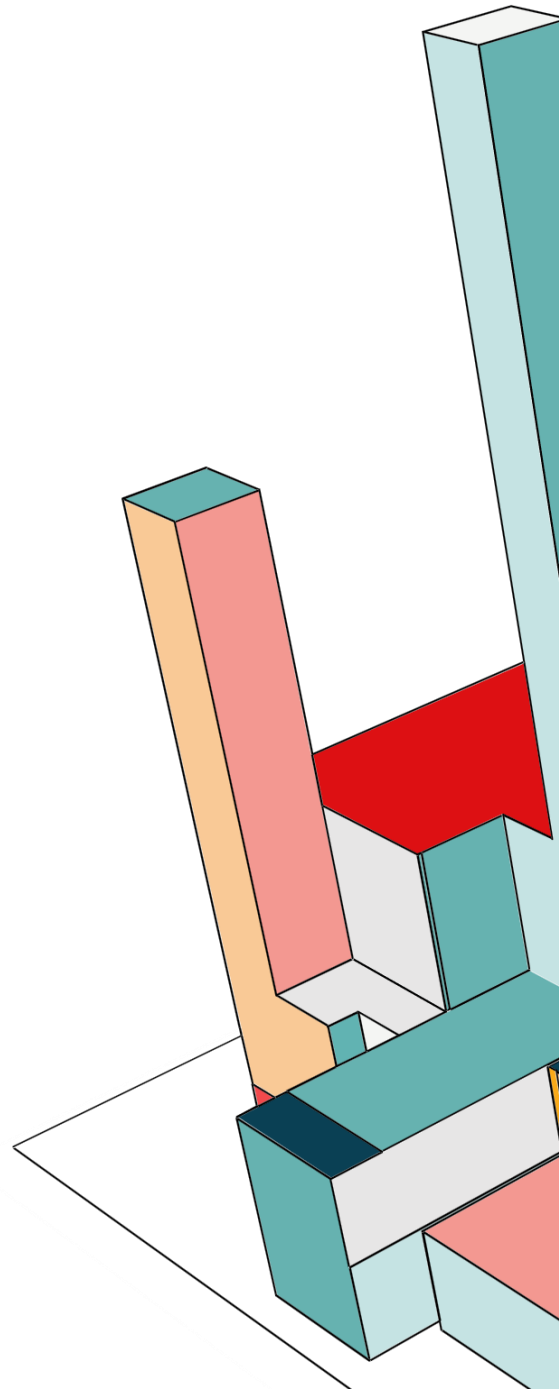
REGISTER

REGISTER

- A register is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information.
- An n-bit register consists of a group of n flip-flops capable of storing n bits of binary information.

❖A 4 bit register





REGISTER WITH PARALLEL LOAD

- Registers with parallel load are a fundamental building block in digital systems.
- Synchronous digital systems have a master clock generator that supplies a continuous train of clock pulses. The pulses are applied to all flip-flops and registers in the system.
- The master clock acts like a drum that supplies a constant beat to all parts of the system. A separate control signal must be used to decide which register operation will execute at each clock pulse.
- The transfer of new information into a register is referred to as *loading* or *updating* the register. If all the bits of the register are loaded simultaneously with a common clock pulse, we say that the loading is done *in parallel*.

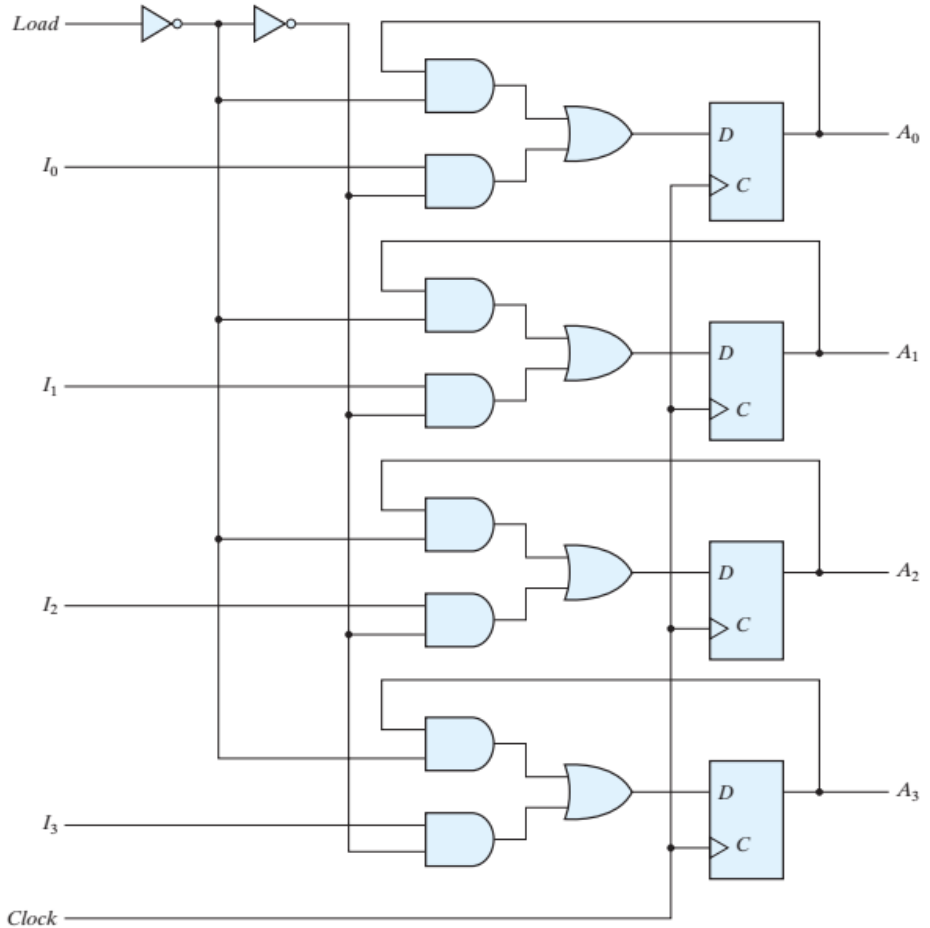
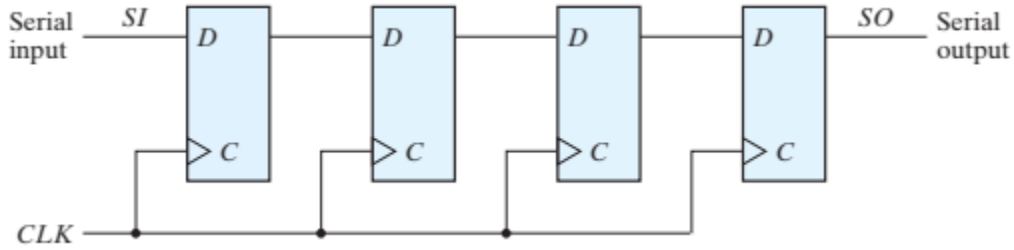
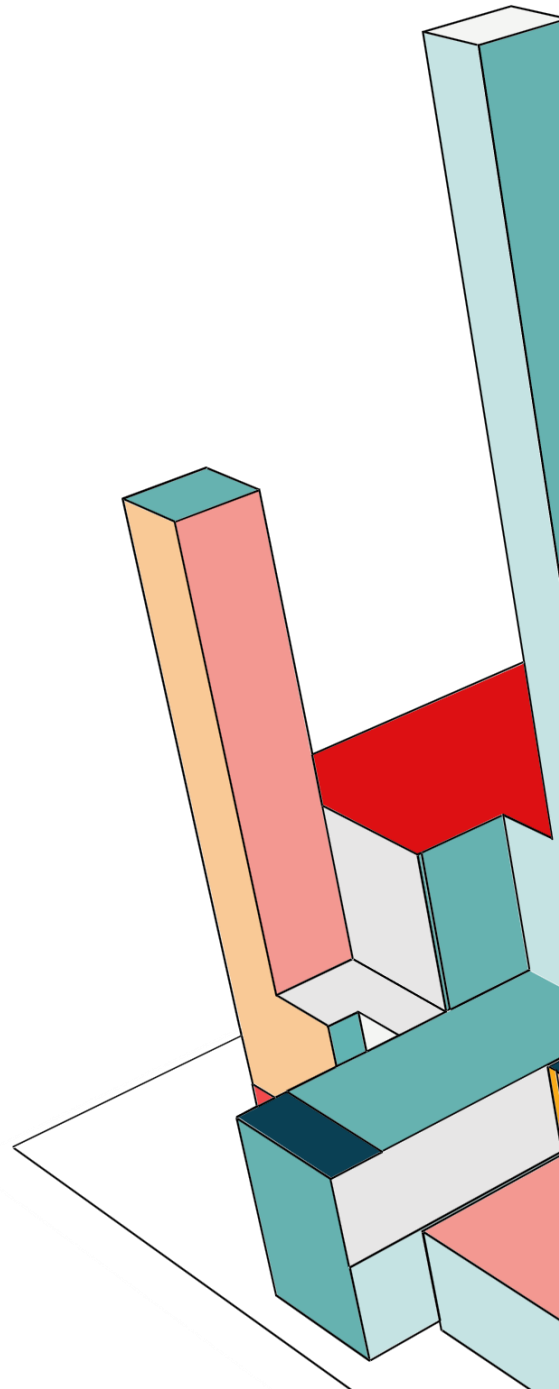


FIGURE 6.2
Four-bit register with parallel load

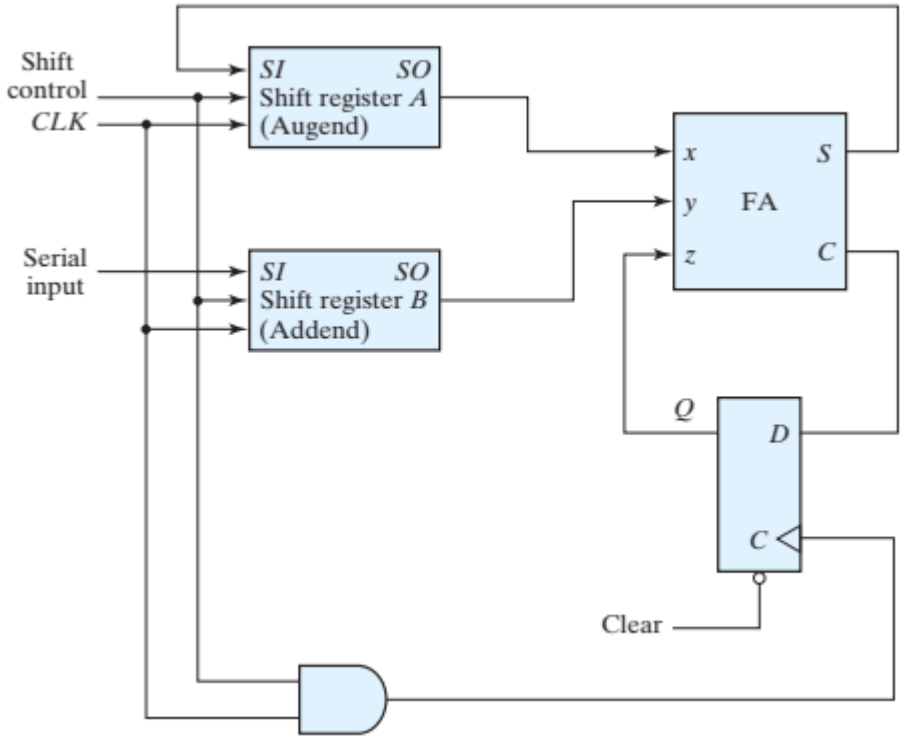
SHIFT/SERIAL REGISTER

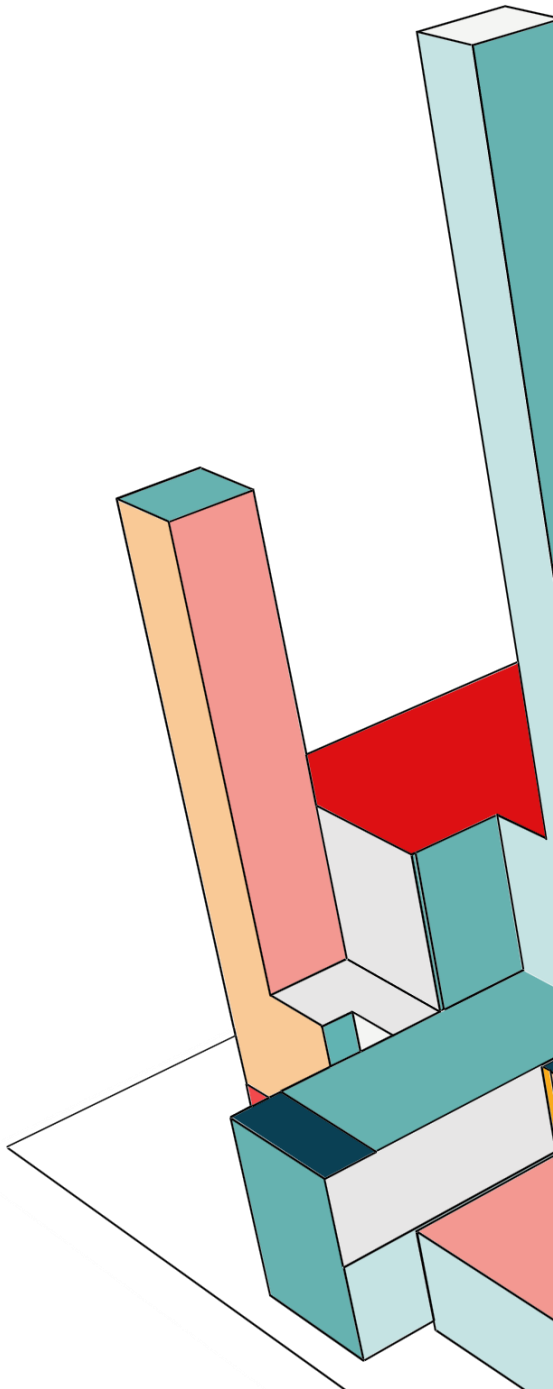
- A register capable of shifting the binary information held in each cell to its neighboring cell, in a selected direction, is called a *shift register.*
- The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop.
- All flip-flops receive common clock pulses, which activate the shift of data from one stage to the next.





SERIAL ADDER





UNIVERSAL SHIFT REGISTER

- A register capable of shifting in one direction only is a *unidirectional* shift register. One that can shift in both directions is a *bidirectional* shift register. If the register has both shifts and parallel-load capabilities, it is referred to as a *universal shift register.*

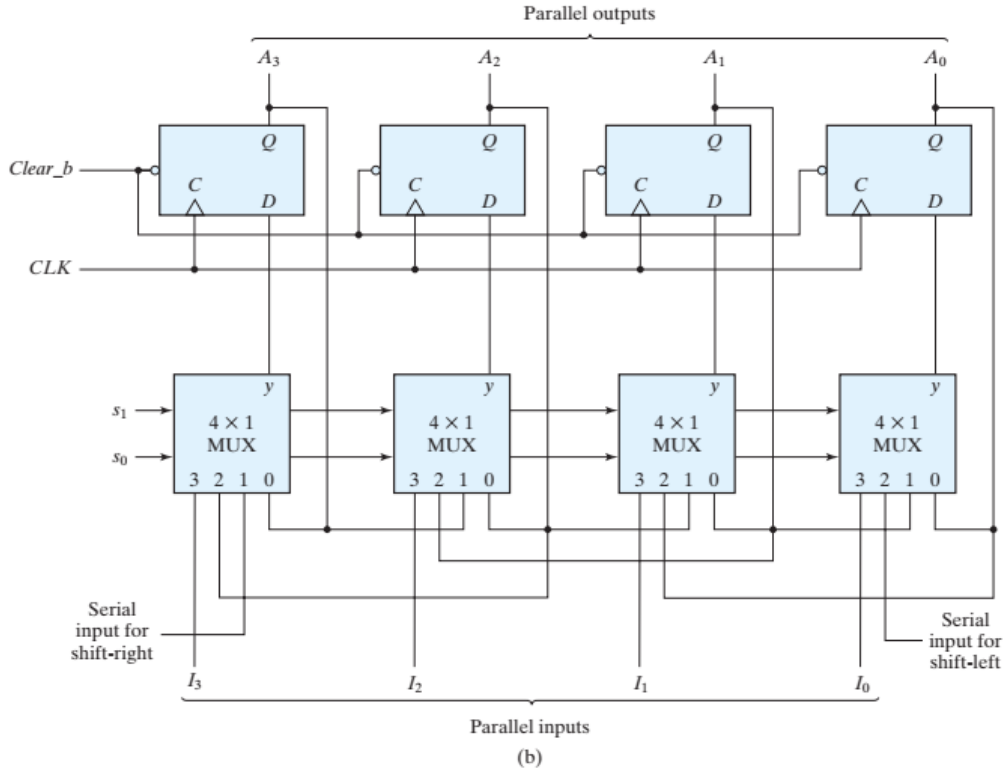
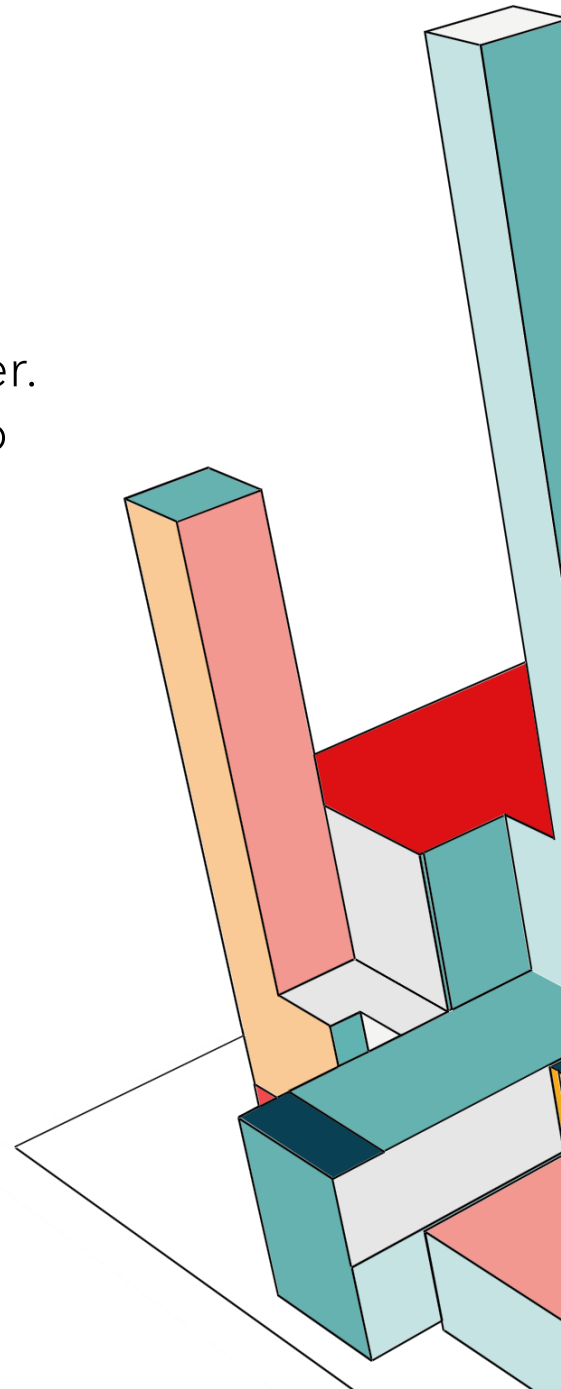
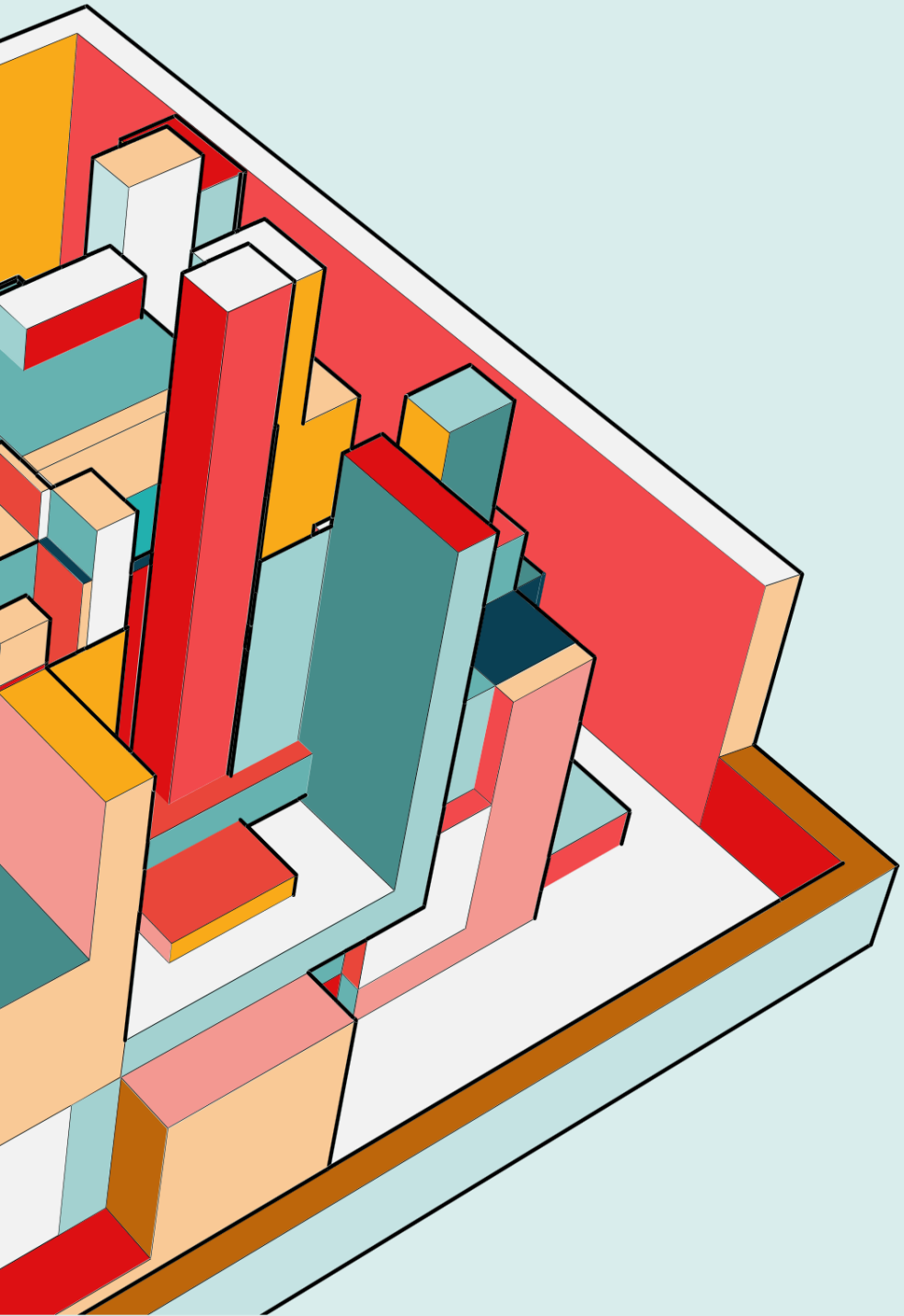


FIGURE 6.7
Four-bit universal shift register





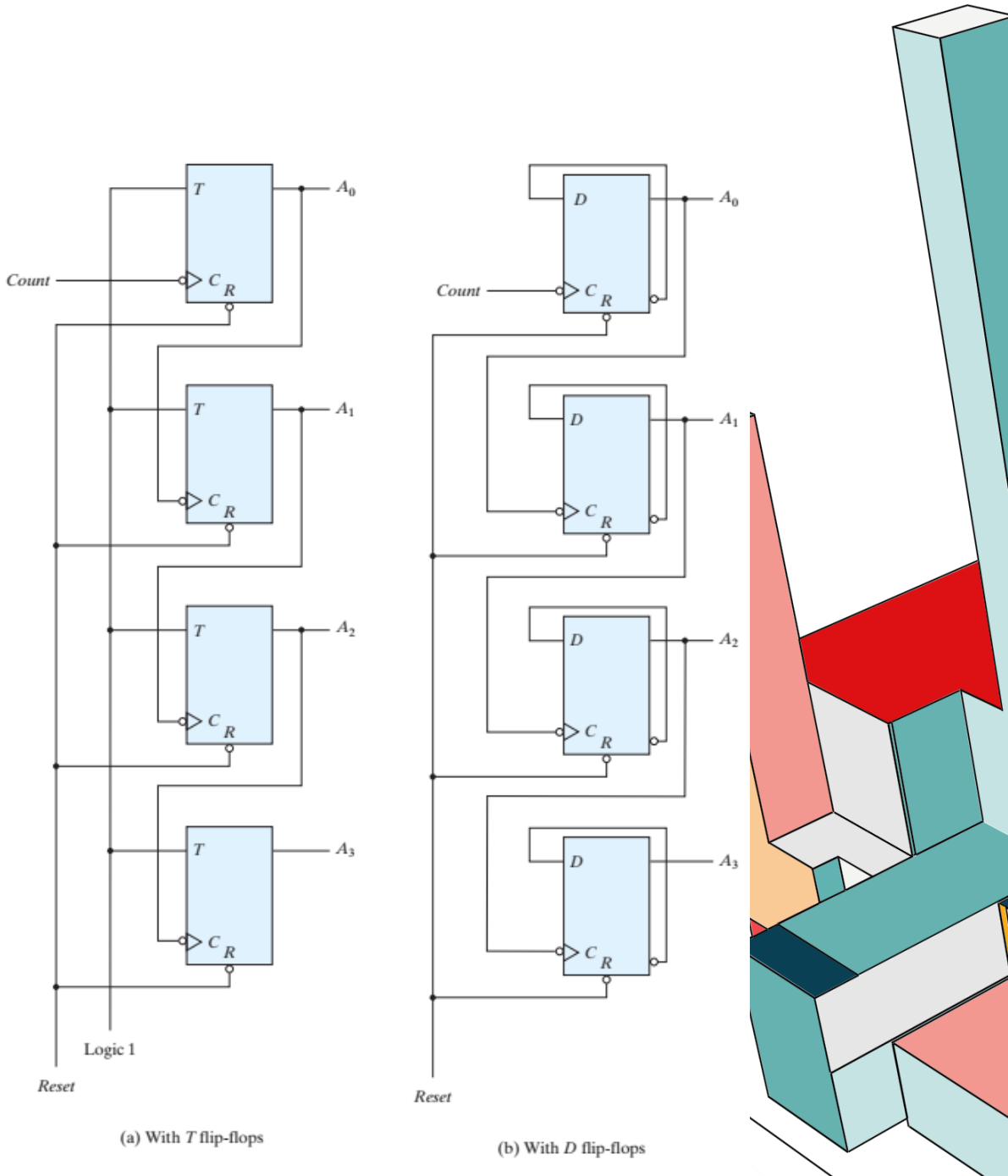
COUNTER

RIPPLE COUNTERS

- A binary ripple counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the *C* input of the next higher order flip-flop. The flip-flop holding the least significant bit receives the incoming count pulses.

Table 6.4
Binary Count Sequence

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

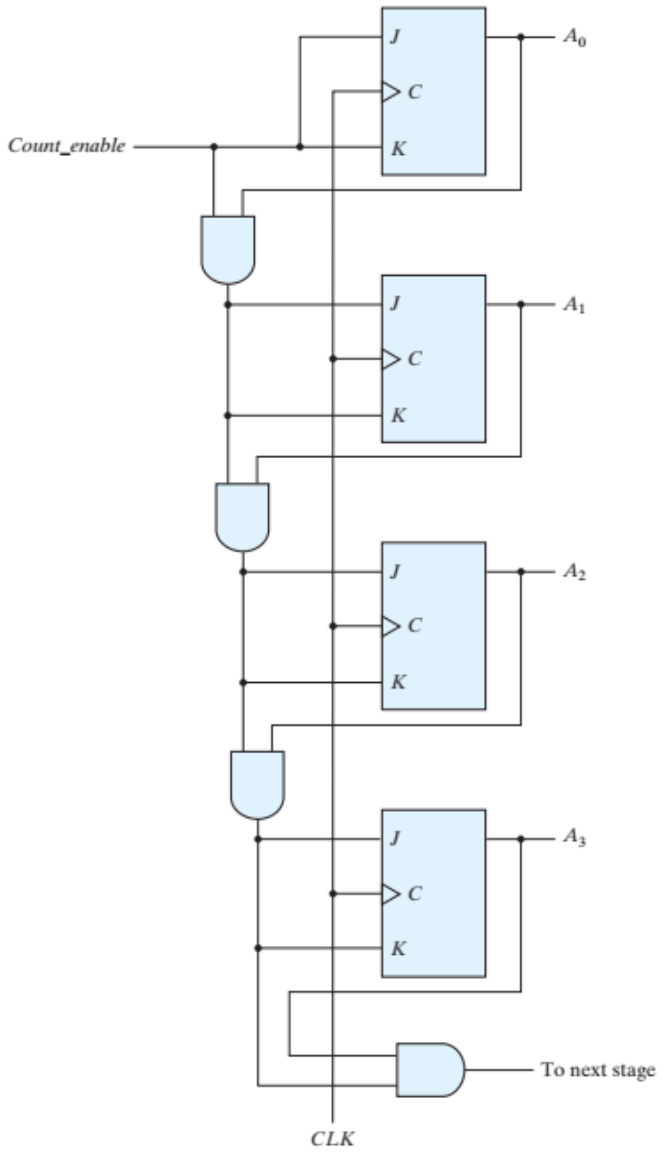


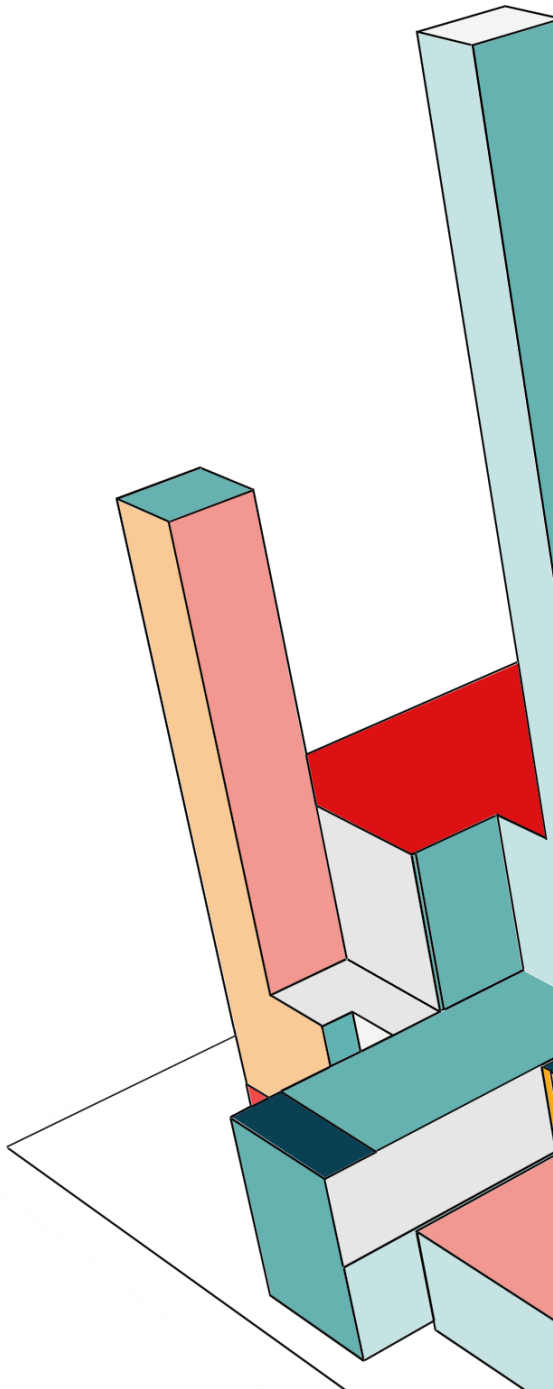
(a) With *T* flip-flops

(b) With *D* flip-flops

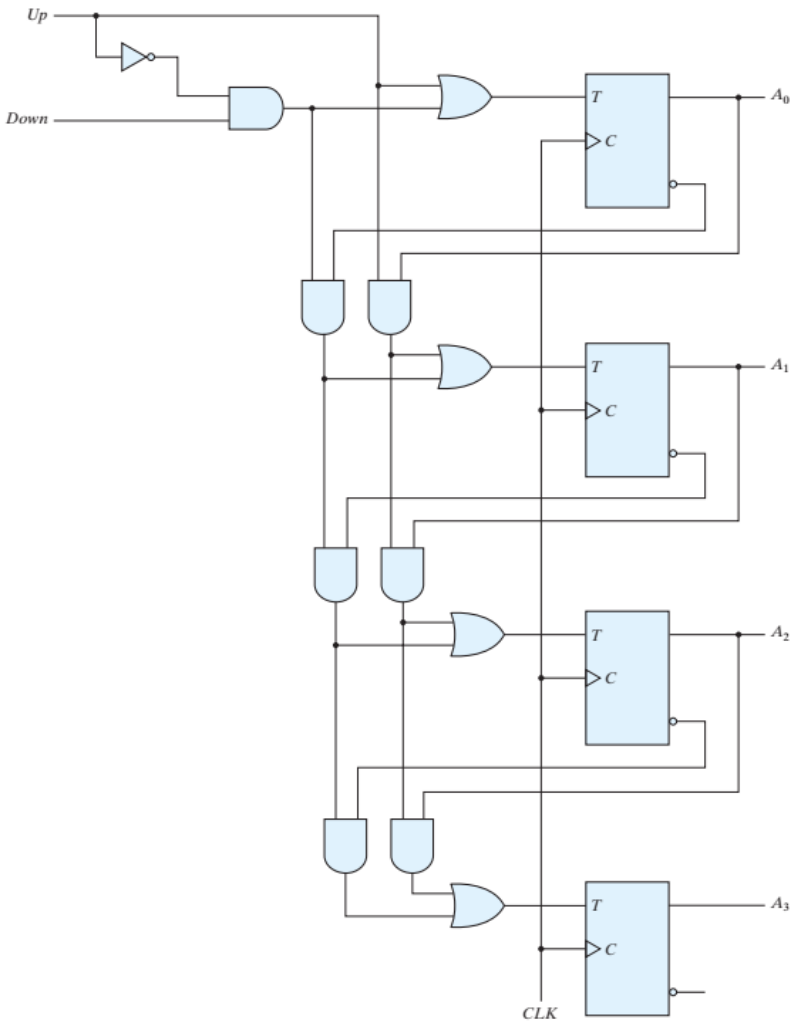
SYNCHRONOUS COUNTERS

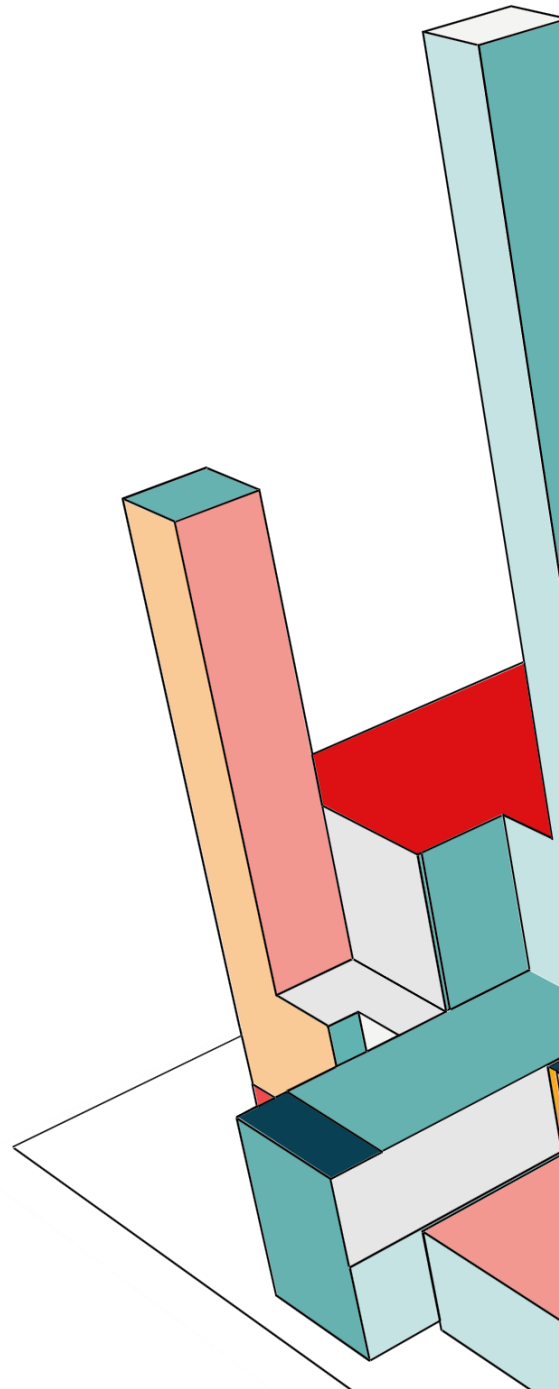
- Synchronous counters are different from ripple counters in that clock pulses are applied to the inputs of all flip-flops. A common clock triggers all flip-flops simultaneously.





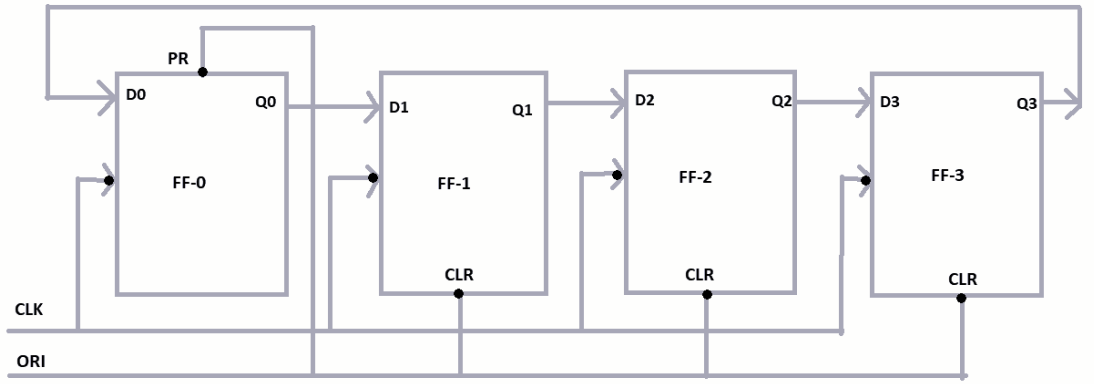
UP & DOWN COUNTERS





RING COUNTER

- The ring counter is almost the same as the shift register. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter.
- The clock pulse (CLK) is applied to all the flip-flops simultaneously, therefore, it is a Synchronous Counter.
- Overriding input (ORI) for each flip-flop. Preset (PR) and Clear (CLR) are used as ORI.
- When PR is 0, then the output is 1. And when CLR is 0, then the output is 0. Both PR and CLR are active low signal that always works in value 0.
- ORI is connected to Preset (PR) in FF-0 and it is connected to Clear (CLR) in FF-1, FF-2, and FF-3.
- Thus, output Q = 1 is generated at FF-0, and the rest of the flip-flop generates output Q = 0. This output Q = 1 at FF-0 is known as Pre-set 1 which is used to form the ring in the Ring Counter.



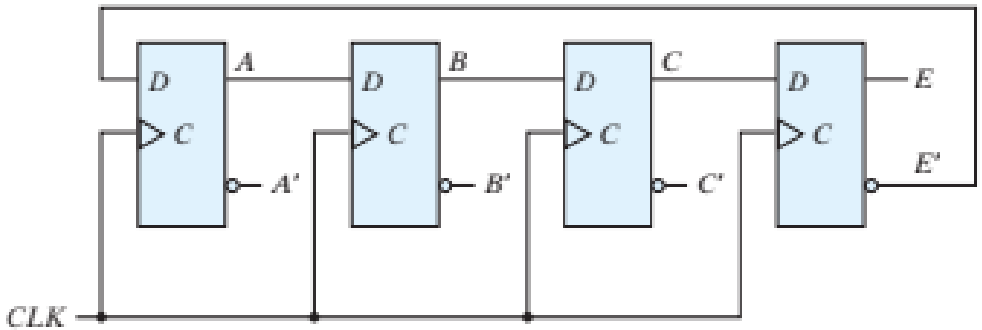
PR = 0, Q = 1 CLR = 0, Q = 0

PRESETED 1

ORI	CLK	Q0	Q1	Q2	Q3
low	X	1	0	0	0
high	low	0	1	0	0
high	low	0	0	1	0
high	low	0	0	0	1
high	low	1	0	0	0

JOHNSON COUNTER

- A Johnson counter is a synchronous counter variant.
- Within this counter, the inverted output of the final flip-flop is linked to the first flip-flop's input.
- Johnson counter is a self-decoding circuit.



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs			
	A	*B*	*C*	*E*
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

THANKS YOU

Digital Design, With an Introduction to the Verilog HDL
M. Morris Mano