Course Outline (includes lecture plan and course outcome)

Course Schedule/Timing: Lecture – 3 Hours/week, Lab – 3 Hours/week

1. Course Number and Title: CSE231 Digital Logic Design

CSE231L Digital Logic Design Laboratory

Instructor: Tanjila Farah (TnF)

Office: SAC 929

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Lab Room: 5th Floor of SAC Building and 8th floor OAT

2. Course Summary:

This course provides an introduction to logic design and basic tools for the design of digital logic systems. A basic idea of number systems will be provided, followed by a discussion on combinational logic: logic gates, Boolean algebra, minimization techniques, arithmetic circuits (adders, subtractors), basic digital circuits (decoders, encoders, multiplexers, shift registers), programmable logic devices (PROM, PAL, PLA). The course will then cover sequential circuits: flip-flops, state transition tables and diagrams, state minimization, state machines, design of synchronous/asynchronous counters, RAM/ROM design. An introduction to programmable logic will also be provided. Hands-on experience will be provided through project on design of a sequential logic system. This course has separate mandatory laboratory session every week as CSE 231L.

3. Course Objective:

The objectives of this course are

- a. to introduce Boolean logic operation and Boolean Algebra
- b. to teach students how to use Boolean Algebra and K-maps to realize two-level minimal/optimal combinational circuits
- c. to exposed students in the introductory design process of combinational and sequential circuits
- d. to teach the operation of latches, flip-flops, counters and registers.
- e. to explain how to analyze and design sequential circuits built with various flip-flops.
- f. to introduce using simulation tool for digital system design.

4. Course Outcomes (COs):

Upon successful completion of this course, students will be able to

Sl.	CO Description	Weightage (%)
CO1	Apply principles of Boolean algebra to logic functions.	10%
CO2	Analyze combinational and sequential circuits.	20%
CO3	Design combinational and sequential circuits. construct gate-	40%
	level implementation of a combinational logic function using	
	fundamental logic gates (AND/OR/NOT), Multiplexers,	
	Decoders and Programmable logic gates (ROMs, PLAs and	
	PALs)	
CO4	use simulation tool (e.g. Logisim) to construct Digital Logic	10%
	Circuit in schematic level	
CO5	operate laboratory equipment build, and troubleshoot simple	20%
	combinational and sequential circuits	

5. Mapping of CO-PO:

Sl.	CO Description	PO	KP	Bloom's taxonomy domain/ level	Delivery methods and activities	Assessment tools
CO1	Apply principles of Boolean algebra to logic functions.	a	К3	Cognitive/ Apply	Lectures, notes	Assignment, Exam
CO2	Analyze combinational and sequential circuits.	b	К3	Cognitive/ Analyze	Lectures, notes	Assignment, Exam
CO3	Design combinational and sequential circuits. construct gate-level implementation of a combinational logic function using fundamental logic gates (AND/OR/NOT), Multiplexers, Decoders and Programmable logic gates (ROMs, PLAs and PALs)	c	K5	Cognitive/ Create	Lectures, notes	Assignment, Exam
CO4	use simulation tool (e.g. Logisim) to construct Digital Logic Circuit in schematic level	e	K6	Cognitive/ Apply, Psychomotor/ Manipulation	Lab class	Design Project
CO5	operate laboratory equipment build, and troubleshoot simple combinational and sequential circuits	e	K6	Cognitive/ Remember, Psychomotor/ Precision	Lab class	Lab work

6. Resources

Text books:

No	Name of	Year of	Title of	Editio	Publisher'	ISBN
	Author(s)	Publication	Book	n	s Name	
1	M Morris	2012	Digital	5 th ed.	Pearson	ISBN-13: 978-0-13-
	Mano &		Design		Education	277420-8
	M D					
	Ciletti					

Reference books:

No	Name of	Year of	Title of	Edition	Publisher's	ISBN
	Author(s)	Publication	Book		Name	
1	JF	2005	Digital	4 th ed.	Prentice	ISBN-13: 978-
	Wakerly		Design:		Hall	0131863897
			Principles			
			and			
			Practices			

Reference Software:

No	Software	
1	Logisim	Available online

7. Weightage Distribution among Assessment Tools

Assessment Tools	Theory Weightage (%)
Class Performance	5
Assignment	NON CREDIT
Quizzes	15
Midterm Exam	25
Final Exam	30
Term Project	10
Lab work	15

8. Grading policy: As per NSU grading policy available in

 $\underline{http://www.northsouth.edu/academic/grading-policy.html}$

Make-up Policy:

No make-up testes for the missed Quizzes.

Lecture Plan:

Course Topics	Min.
	Coverage
Numerical representation of numbers	4.5 hours
Binary, octal, decimal, hexadecimal, complements, signed/unsigned numbers, binary	
codes, error detecting/correcting codes	
Boolean algebra	3 hours
Logic gates, Boolean algebra, Boolean functions, canonical and standard forms	
Combinational logic design	4.5 hours
Minimization techniques (Boolean algebra, Karnaugh map), don't care conditions, universal gate implementation	
Combinational circuits	6 hours
Analysis, design procedure, binary adder/subtractor, decoders, encoders,	
multiplexers, combinational logic implementation using decoders and multiplexers	
Synchronous sequential logic	6 hours
Sequential circuits, flip-flops, timing diagrams, state transition tables, state transition	
diagrams (Mealy and Moore models), state minimization and assignment, design implementation	
Sequential circuits: Registers and counters	6 hours
Synchronous/Asynchronous counters, registers, shift registers	o nours
Synchronous counters, registers, sinit registers	
Memory design (RAM, ROM)	3 hours
Programmable logic:	
Implementation of logic functions using programmable logic devices ROM, PLA,	
PAL	

Class Structure:

- **1. Lectures:** Attendance and participation of all of them is strongly encouraged.
- **2. Laboratory:** You must pass in your lab to attain a passable grade in theory. 20% marks from your lab will be directly added to your theory
- **3. Assignments:** You will be given some design assignments. You will use pen and papers and tools to solve those problems.
- **4. Projects:** You will have to submit a hardware design project at the end of the semester. You will work on the project as a group.
- **5. Exams:** There will be one midterm, one final exam and no make-ups.