Field-Effect Transistors

Topic 6 (Chapter 6)

Basic Difference Between BJT and FET

- The BJT is a current-controlled device
- The FET is a voltage-controlled device.

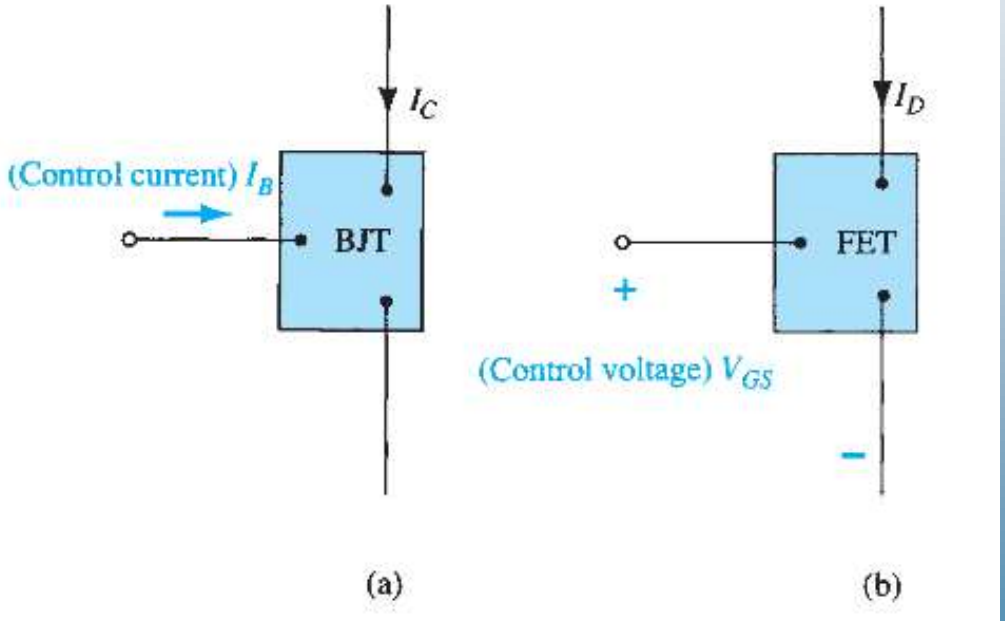


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

FETs vs. BJTs

Similarities:

1. Both are Transistors
2. Amplifiers
3. Switching devices
4. 3 terminal devices

Differences:

1. BJTs are bipolar. FETs are unipolar.
2. FETs are voltage controlled devices. BJTs are current controlled devices.
3. FETs have higher input impedance. BJTs have higher gain.
4. FETs are less sensitive to temperature variations and are better suited for integrated circuits.
5. FETs are smaller than BJTs.
6. FET have faster switching speed than BJT.

FET Types

JFET: Junction FET (Not in our syllabus. Not used NOW)

MOSFET: Metal–Oxide–Semiconductor FET

D-MOSFET: Depletion MOSFET

E-MOSFET: Enhancement MOSFET

MOSFET TYPES

- Two types:
  1. Depletion type
  2. Enhancement type

- Both of the above types have two sub-types:
  1. N-channel or simply n-type (also called NMOS in short)
  2. P-channel or simply p-type (also called PMOS in short)

Some Facts..

- The name MOSFET is derived from its physical structure.
  - Metal Oxide Semiconductor Field Effect Transistor
- However, MOSFET's gates do not actually use any "metal", polysilicon is used instead.
- Another name for MOSFET is insulated gate FET, or IGFET.

ENHANCEMENT-TYPE MOSFET

E-MOSFET

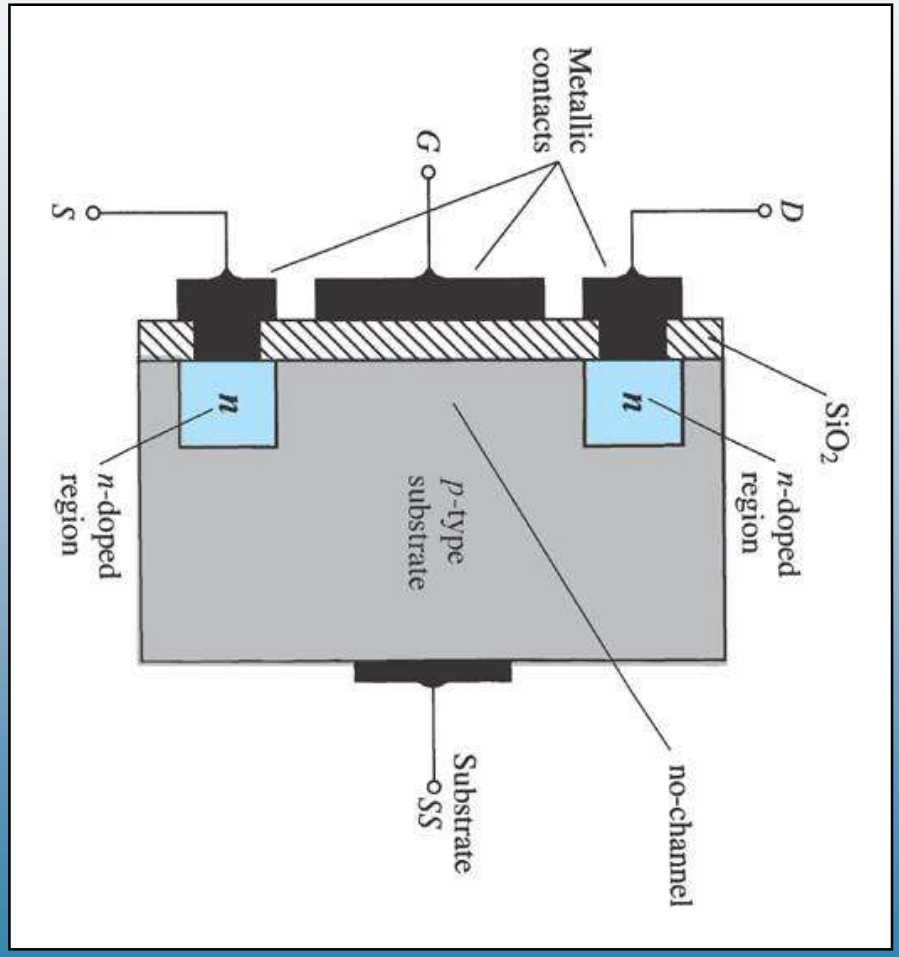
E-Type MOSFET Construction

The **Drain (D)** and **Source (S)** connect to the to *n*-type regions.

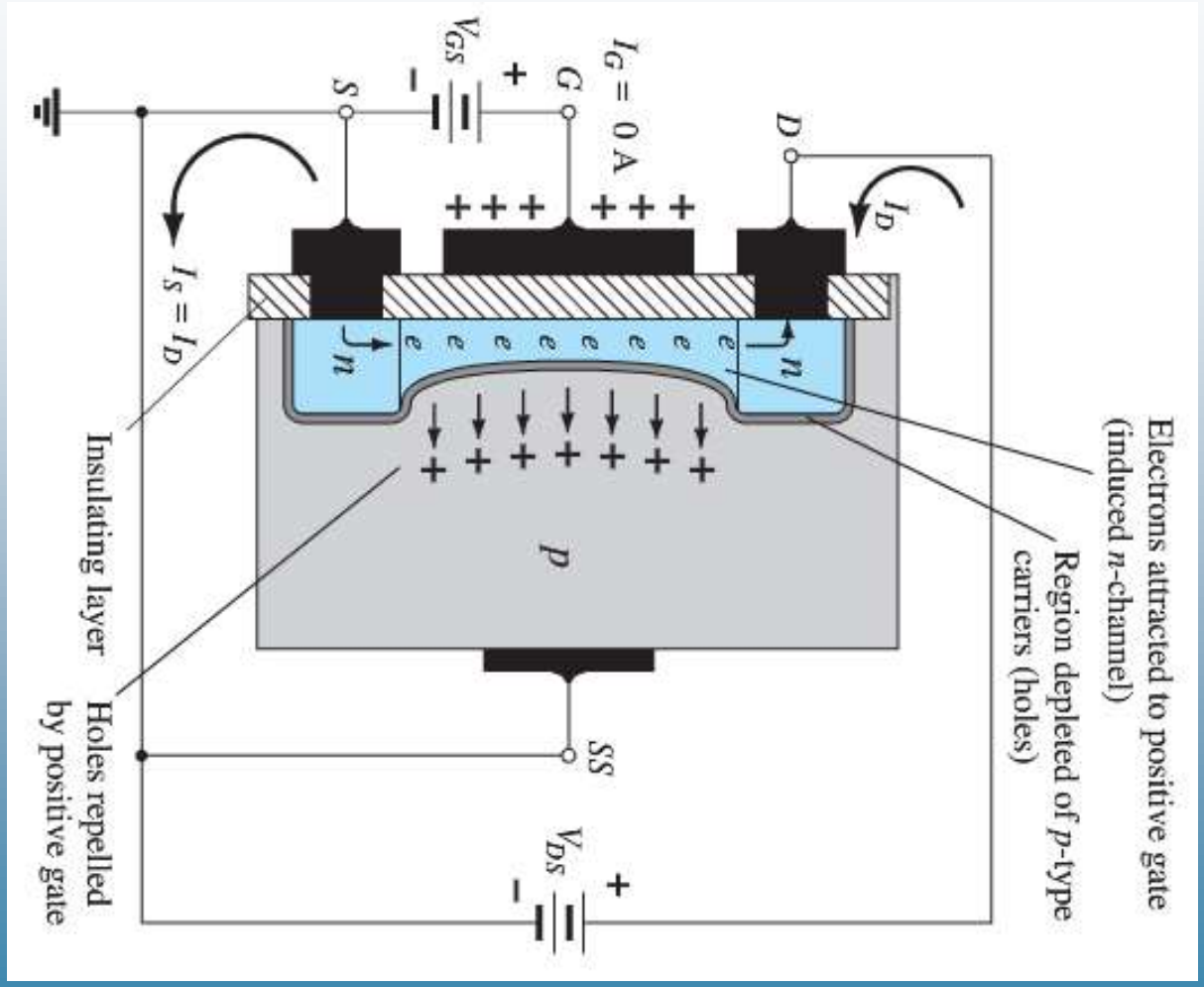
The **Gate (G)** connects to the *p*-type substrate via a thin insulating layer of silicon dioxide (SiO_2)

There is no channel!

The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate (SS)** **or** **Body (B)**



Channel formation in the n-channel enhancement-type MOSFET



Threshold Voltage, V_t

minimum

- The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage
  - Denoted as V_t
  - Positive for an n-channel FET
- The value is controlled during device fabrication
  - Typically V_t lies in the range of 0.3 V to 1.0 V

Field-Effect

- The gate and the channel region of the MOSFET form a parallel-plate capacitor
  - The oxide layer acts as the capacitor dielectric
- The channel conductivity and the current that flows through the channel is determined by the electric field in the channel
  - Caused by an applied gate voltage, v_{GS}
  - This is the origin of the name “field-effect transistor” (FET)
- A current flows when a voltage v_{DS} is applied
- Potential difference created by v_{DS}
- Channel created by v_{GS}

Summary of MOSFET Behavior (when v_{DS} is kept small)

- MOSFET behaves as a linear resistance whose value is controlled by the gate voltage v_{GS}
- For MOSFET to conduct, a channel has to be induced.
- Then, increasing above the threshold voltage V_t enhances the channel
  - Hence the names **enhancement-mode operation** and **enhancement-type MOSFET**.
- The current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$

Change in channel and depletion region with V_{DS} increasing and a fixed value of V_{GS}

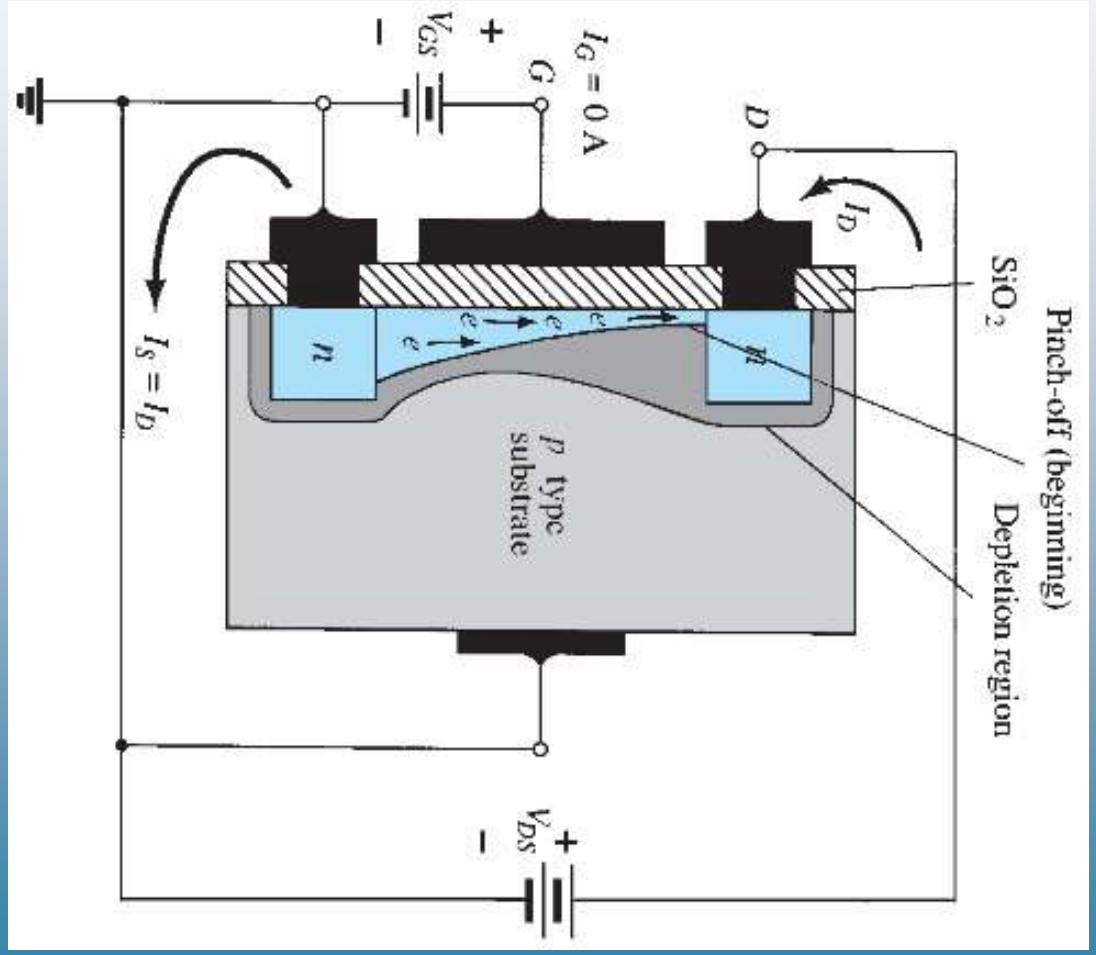
$V_{GD} = V_{GS} - V_{DS}$

V_{GS} fixed

V_{DS} increases

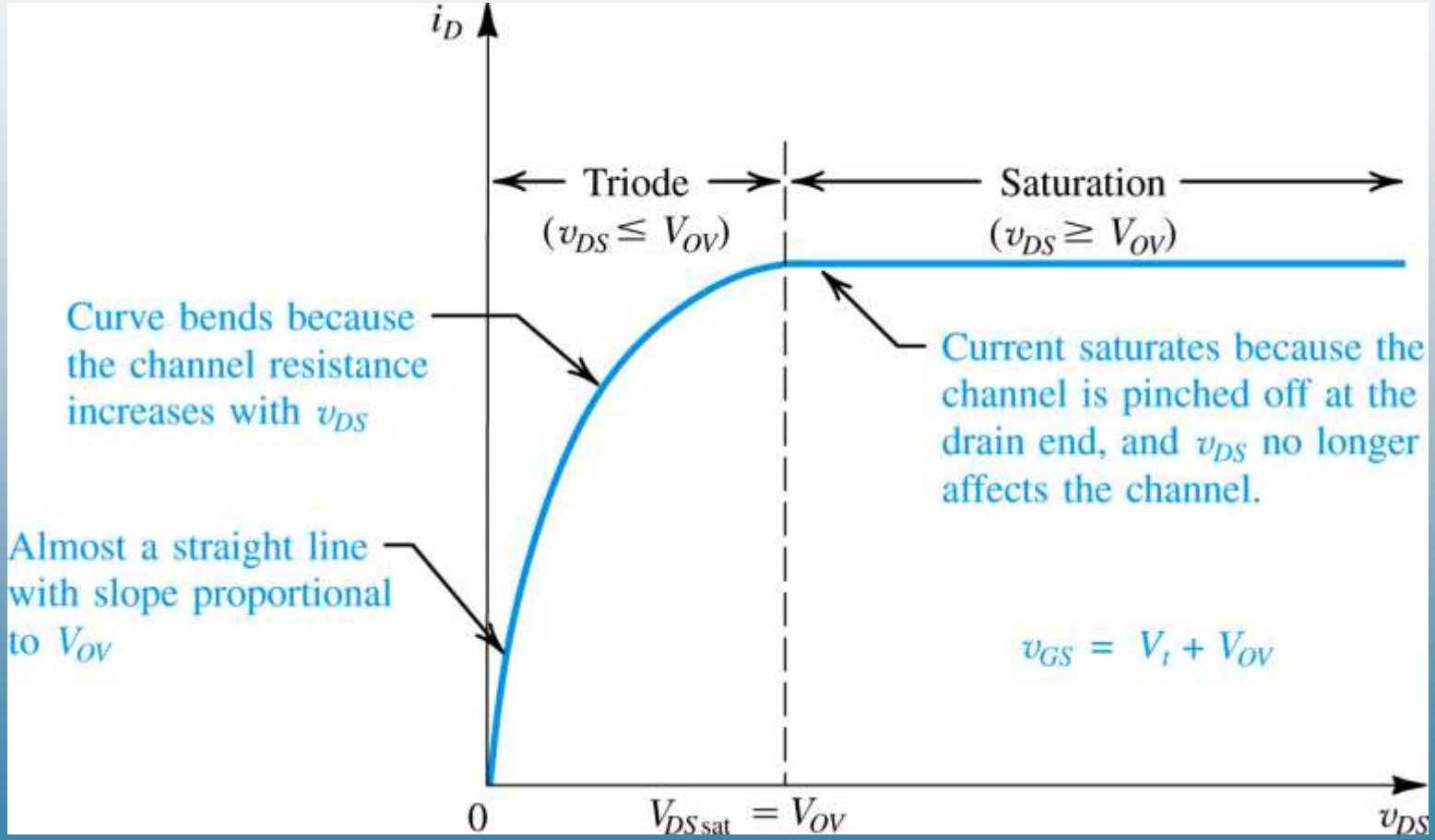
V_{GD} decreases

Channel width decreases at drain



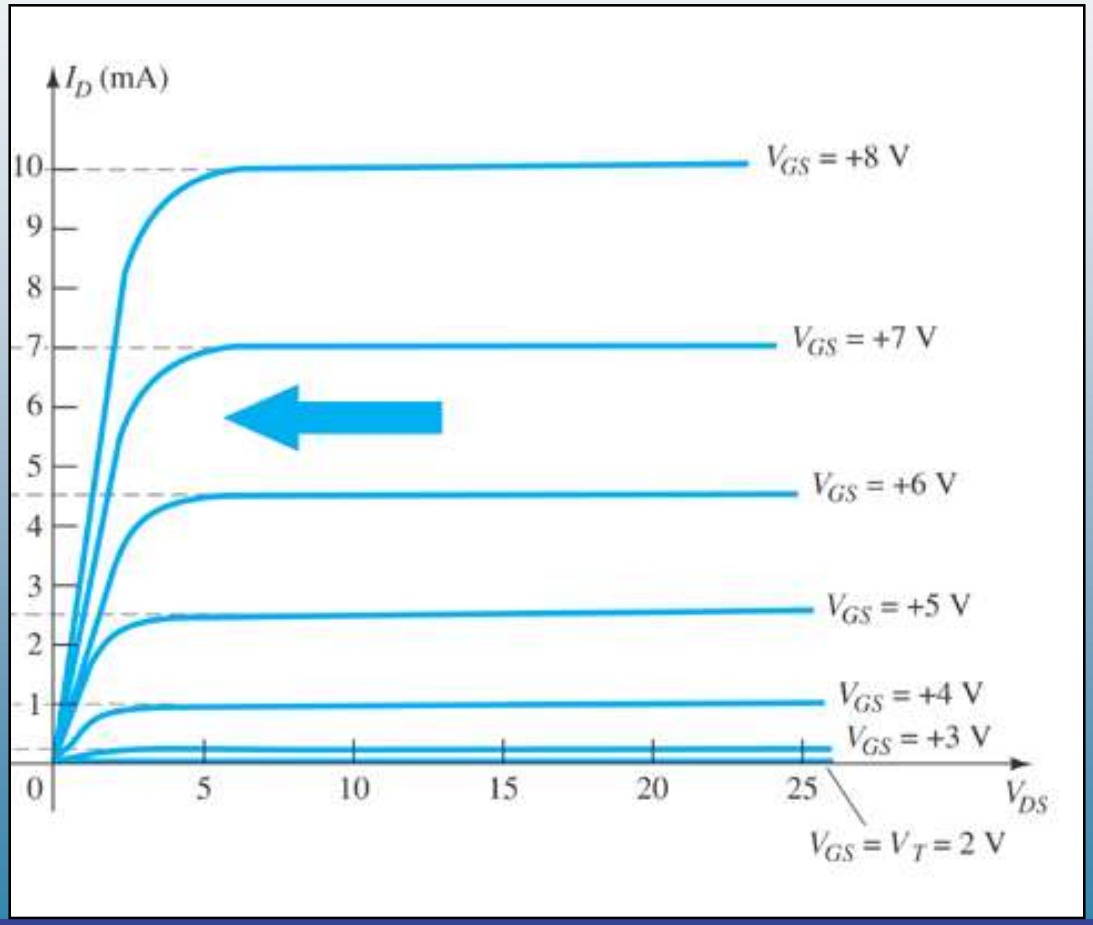
i_D versus v_{DS}
[Enhancement-Type NMOS Transistor]

$$v_{GS} = V_t + V_{OV}$$

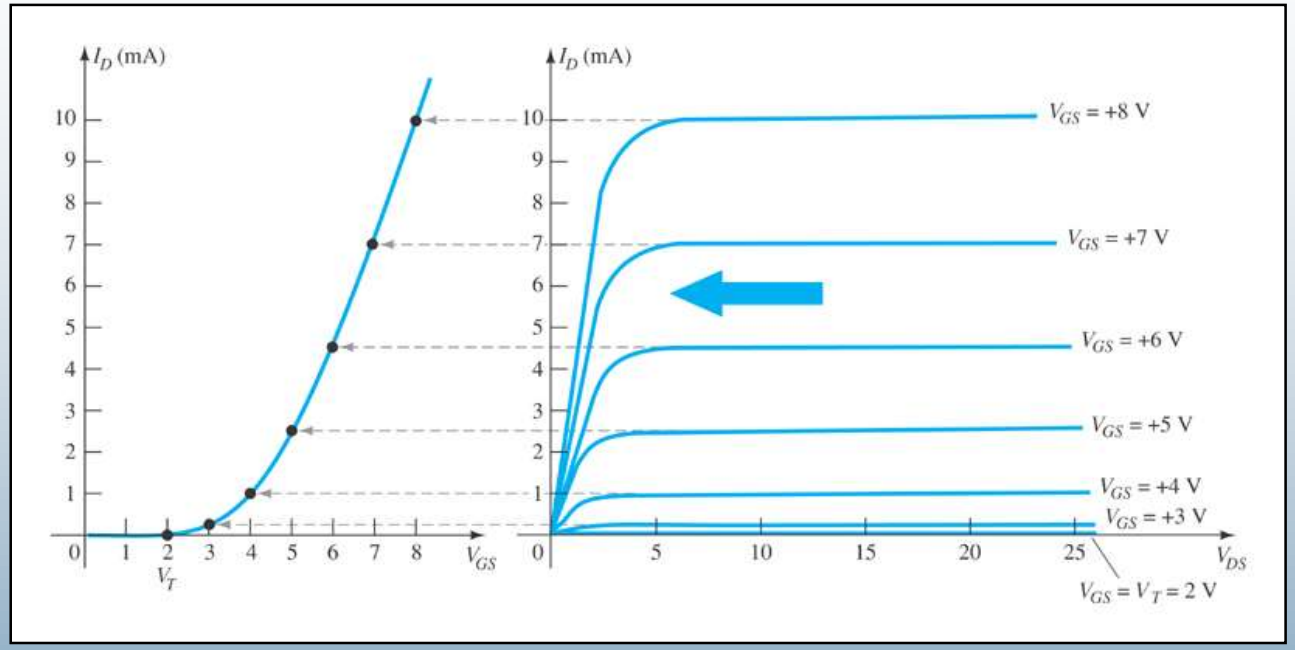


E-Type MOSFET Operation

The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.



E-Type MOSFET Transfer Curve



$$I_D = k(V_{GS} - V_T)^2$$

Where, V_T = the E-MOSFET threshold voltage

k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

EMOSFET Current Equation

- Off Region ($V_{GS} < V_t$) OR ($V_{DS} = 0V$)

$$I_D = I_S = 0$$

- Linear/Triode/Ohmic Region ($V_{DS} < V_{GS} - V_t$) & ($V_{GS} > V_t$)

$$I_D = I_S = 2k\left\{(V_{GS} - V_t)V_{DS} - \frac{1}{2}{V_{DS}}^2\right\}$$

$$\cong 2k\left\{(V_{GS} - V_t)V_{DS}\right.$$

- Saturation Region ($V_{DS} \geq V_{GS} - V_t$) & ($V_{GS} > V_t$)

$$I_D = I_S = k\,(V_{GS} - V_t)^2$$

k = Transconductance parameter (A/V^2)

$V_{GS} - V_t = V_{OV}$ = Overdrive or Effective voltage

EMOSFET Current Problem

- For an enhancement NMOS, k = 1 mA/V^2, V_t = 3 V.

(a) V_{GS} = 2 V, V_{DS} = 10 V; (b) V_{GS} = 5 V, V_{DS} = 0 V

(c) V_{GS} = 5 V, V_{DS} = 1 V; (d) V_{GS} = 5 V, V_{DS} = 6 V

- The NMOS is in which region? Why? Find I_D, I_S and I_G. Write unit.

(a) V_{GS} = 2 V $< V_t$ = 3 V. OFF Region.

- $I_D = I_S = 0$. $I_G = 0A$. Always

(b) V_{GS} = 5 V $> V_t$ = 3 V, **BUT: V_{DS} = 0 V.**OFF Region.

- $I_D = I_S = 0$. $I_G = 0A$. Always

EMOSFET Current Problem

(c) V_{GS} = 5 V > V_t = 3 V. $V_{DS} = 1\text{V} \neq 0$ V.

- Linear/Ohmic/Triode Region ($V_{DS} = 1V < V_{GS} - V_t = 2V$)

$$I_D = I_S = 2k\left\{(V_{GS} - V_t)V_{DS} - \frac{1}{2}{V_{DS}}^2\right\} = 3mA$$

$$\cong 2k\left\{(V_{GS} - V_t)V_{DS} = 4\text{mA}\right.$$

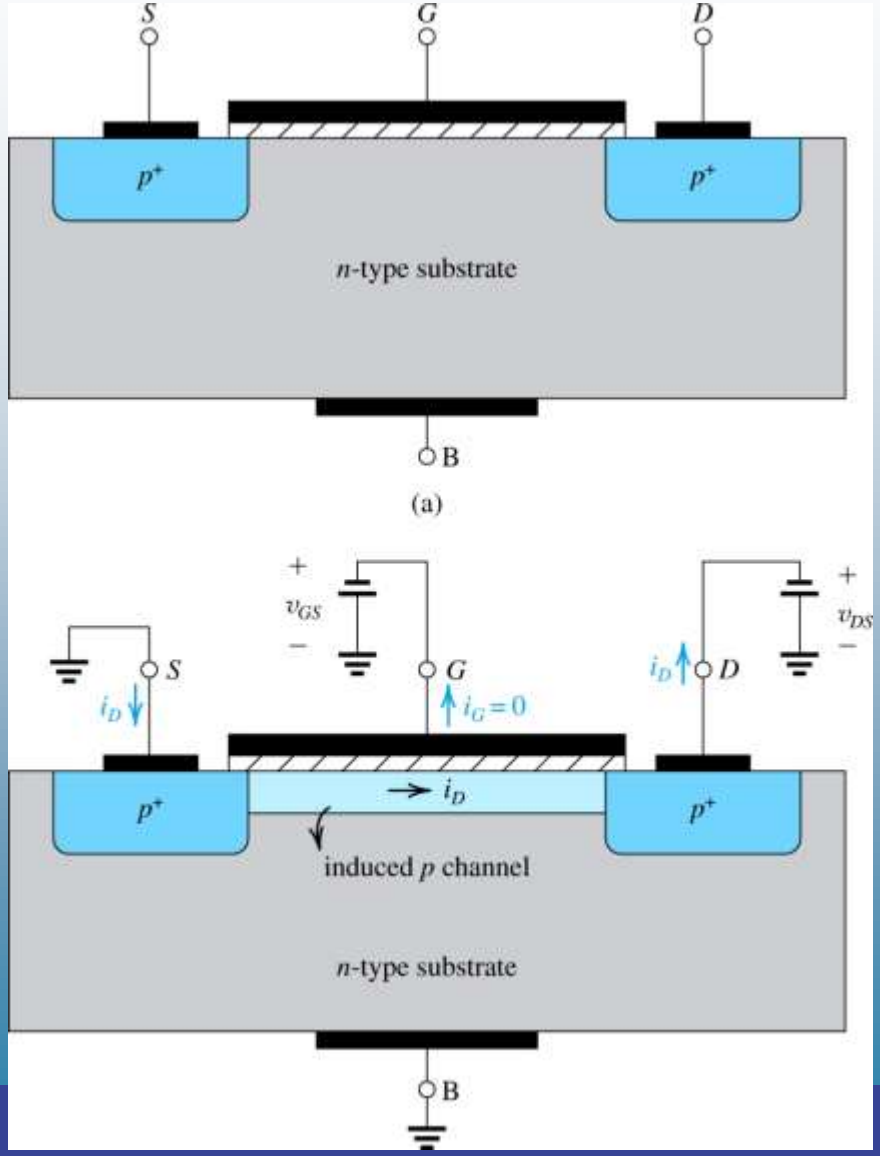
$I_G = 0A$. Always

(d) V_{GS} = 5 V > V_t = 3 V. $V_{DS} = 6\text{V} \neq 0$ V.

- Saturation Region ($V_{DS} = 6V \geq V_{GS} - V_t = 2V$)

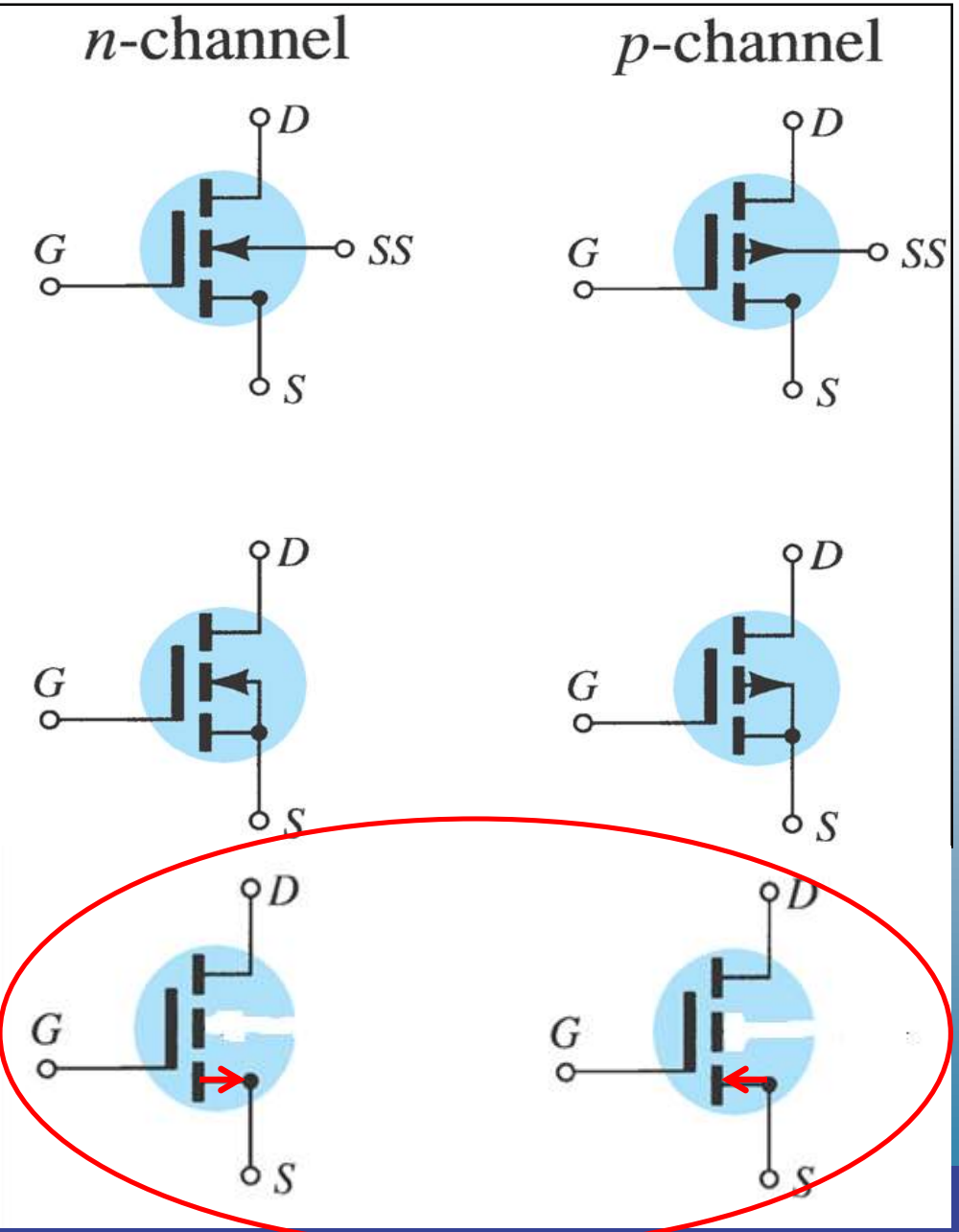
$I_D = I_S = k\,(V_{GS} - V_t)^2 = 4\text{mA}$. $I_G = 0A$. Always

PMOS transistors Enhancement Type



- Similar to the NMOS transistor
  - except that all semiconductor regions are reversed in polarity

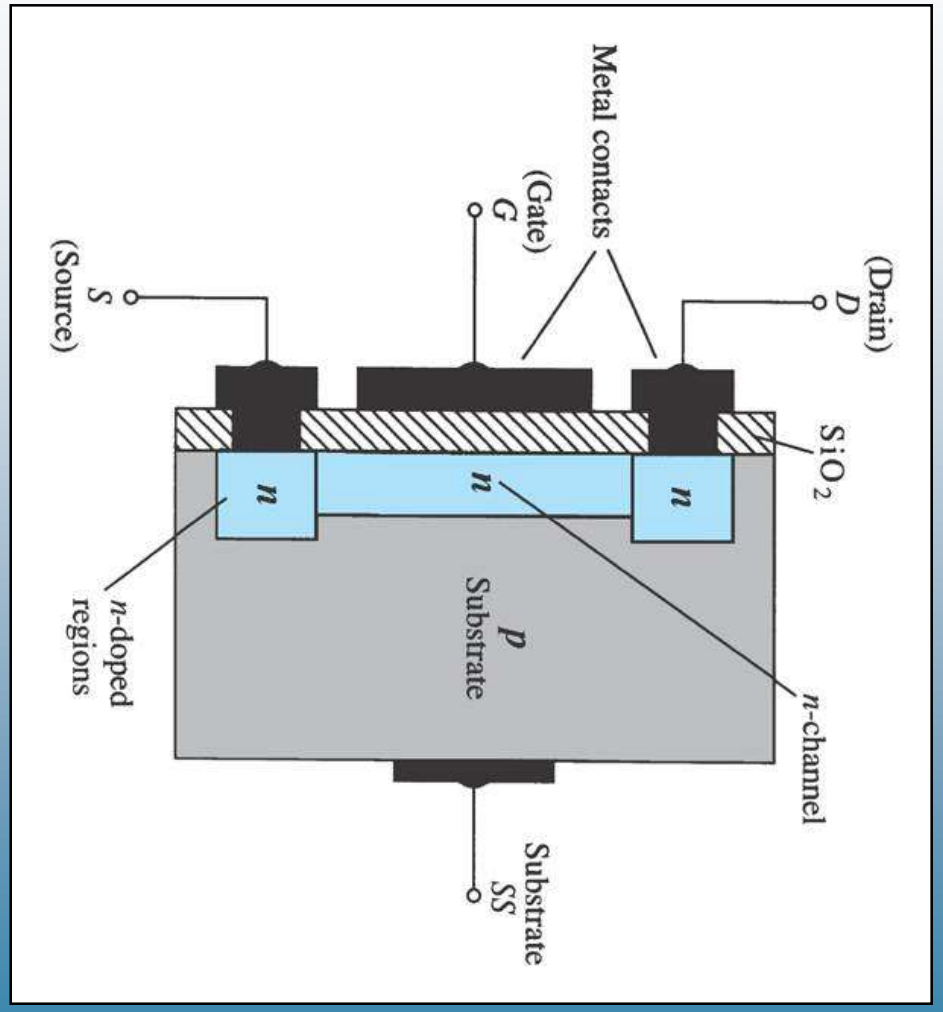
MOSFET Symbols



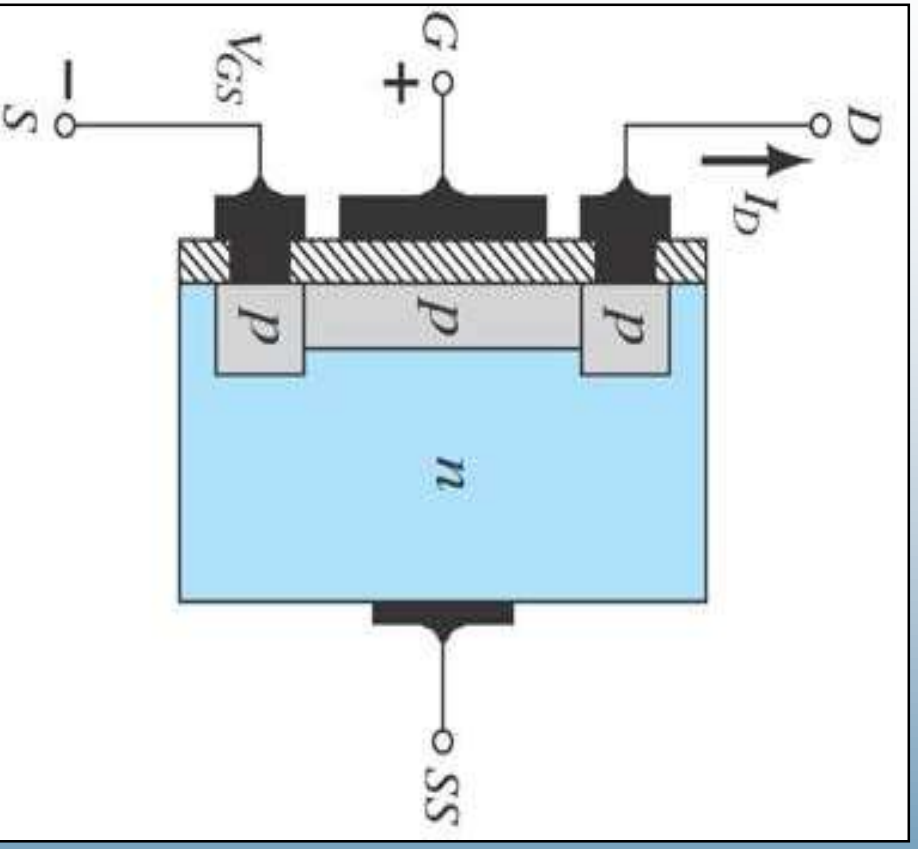
- The symbols try to reflect the actual construction of the device.
- The dashed line between drain and source is chosen to reflect the fact that a channel does not exist between the two under no-bias conditions.
- It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.
- NMOS: source current i_S leaves the NMOS.
- PMOS: source current i_S enters the PMOS.

6.7 Depletion-Type MOSFET Construction

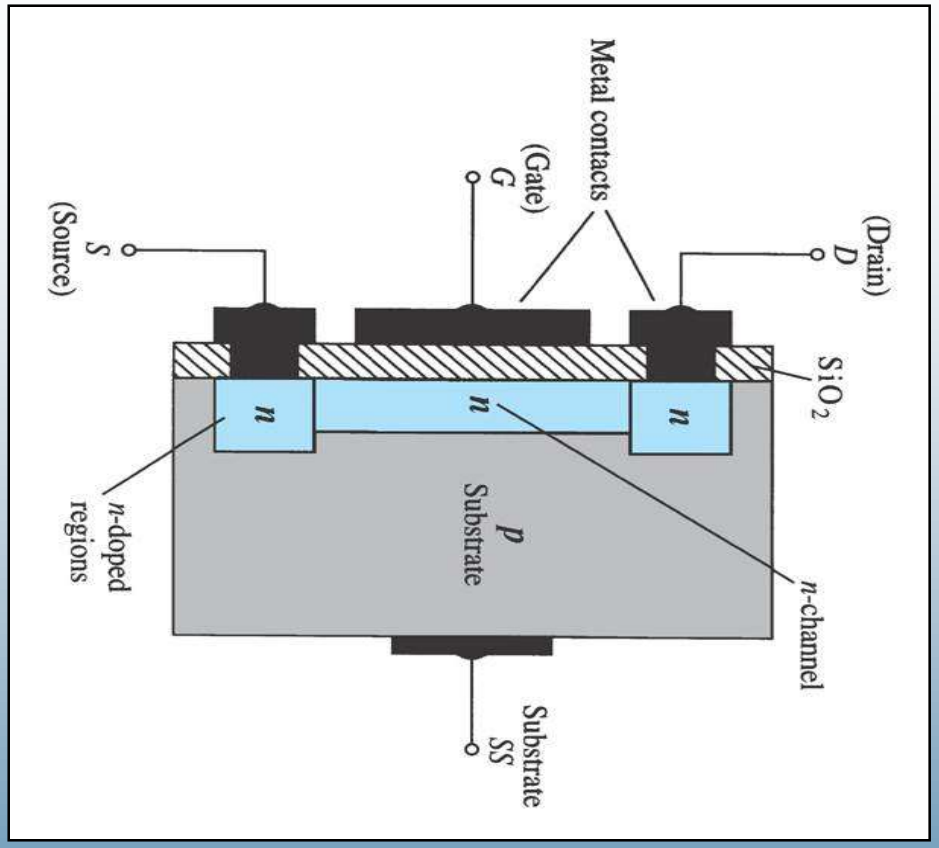
- The **Drain (D)** and **Source (S)** connect to the to *n*-type regions.
  - The *n*-typed regions are connected via an *n*-channel.
  - The *n*-channel is connected to the **Gate (G)** via a thin insulating layer of silicon dioxide (SiO_2).
- The *n*-type material lies on a *p*-type substrate or body that may have an additional terminal connection called the **Substrate (SS)**.



D-Type MOSFET Structures



P-channel DMOS

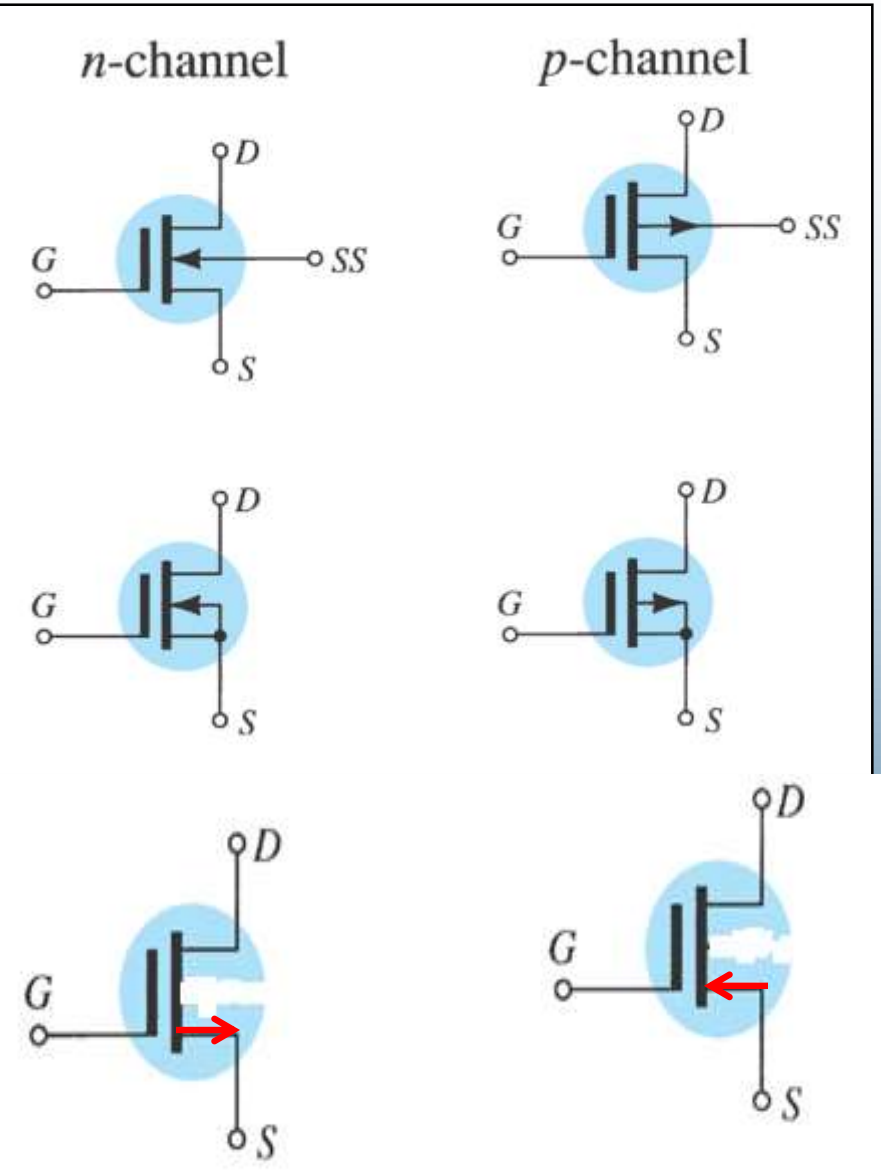


N-channel DMOS

Same as Enhancement EMOS.

Only difference: N/P channel exists between drain and source before applying any voltage

D-Type MOSFET Symbols



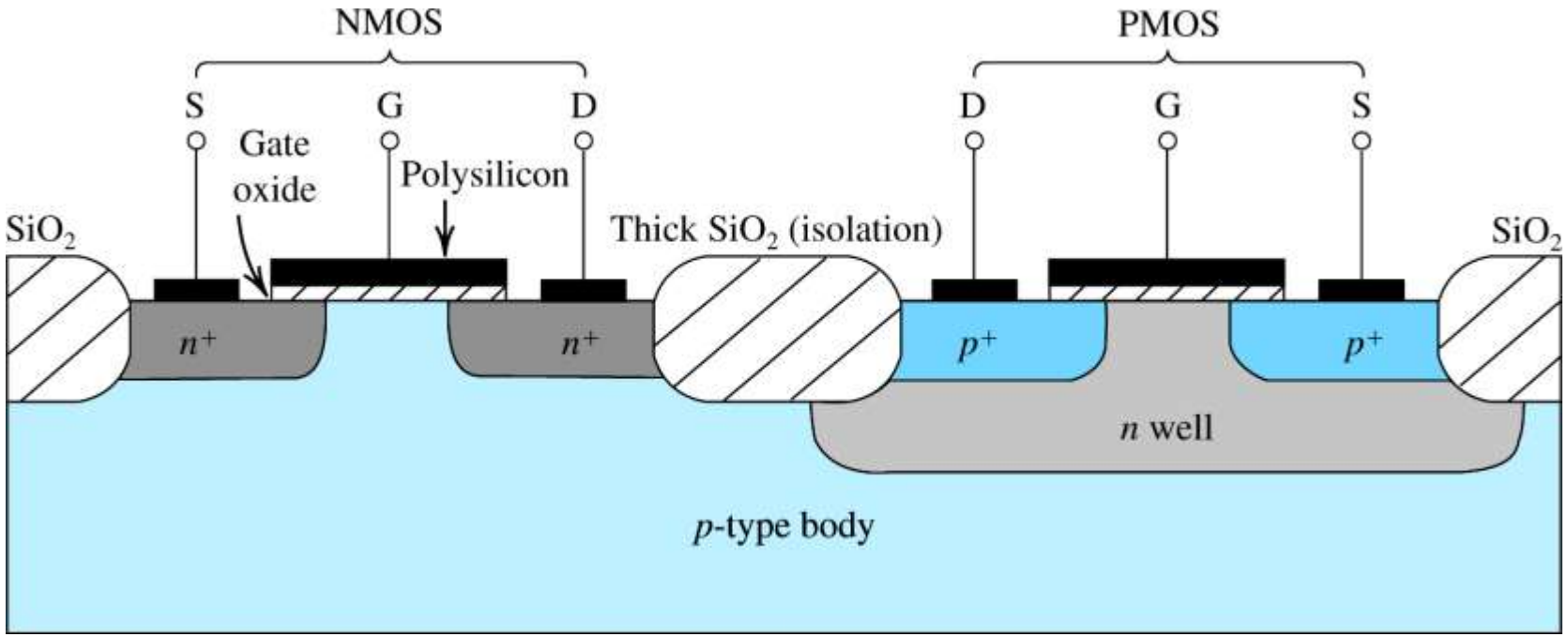
- The symbols try to reflect the actual construction of the device.
- The lack of a direct connection (due to the gate insulation) between the gate and the channel is represented by a space between the gate and the other terminals of the symbol.
- The vertical line representing the channel is connected between the drain and the source and is “supported” by the substrate.
- Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available, whereas in others it is not.
- For most of our analysis, the substrate and the source will be connected and the lower symbols will be employed.

Complementary MOS or CMOS

- Most widely used of all the IC technologies
  - Applies to both analog and digital circuits
- CMOS is preferred over BJT in digital applications:
  - Less power.
  - Higher input impedance.
  - Scaling is easier

CMOS Devices

CMOS (complementary MOSFET) uses a p-channel and n-channel MOSFET; often on the same substrate.



- **Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well**

Digital Logic Inverters

- Most basic element in design of digital circuits.

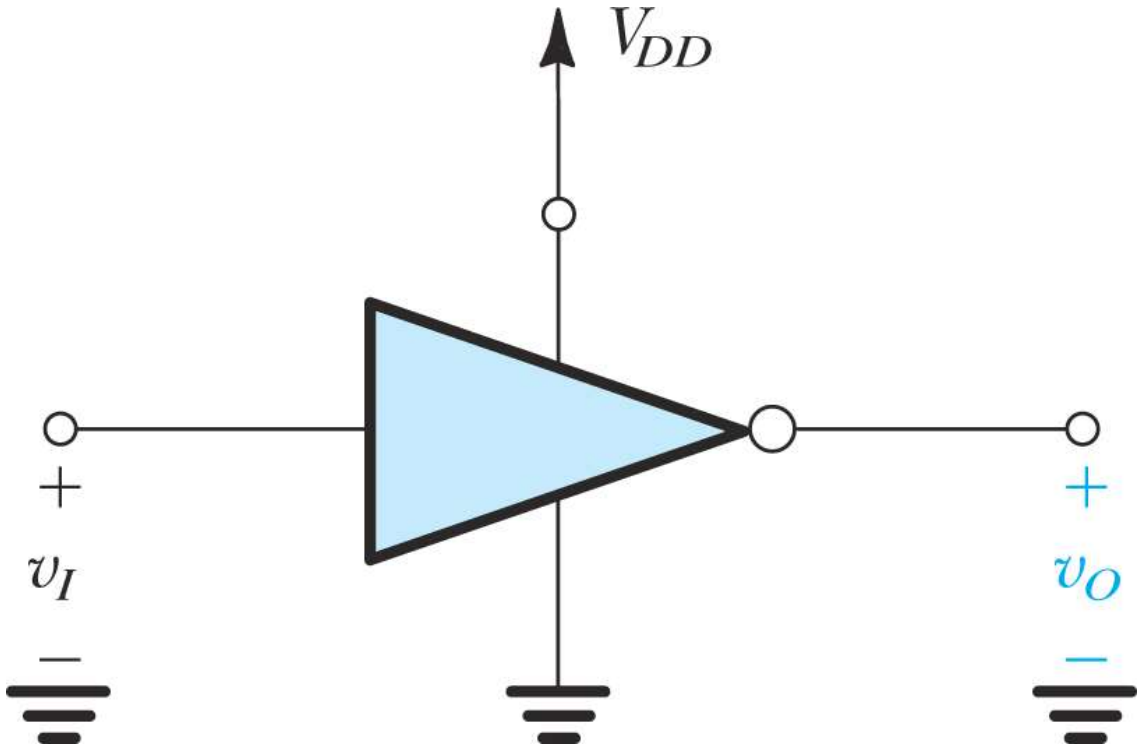
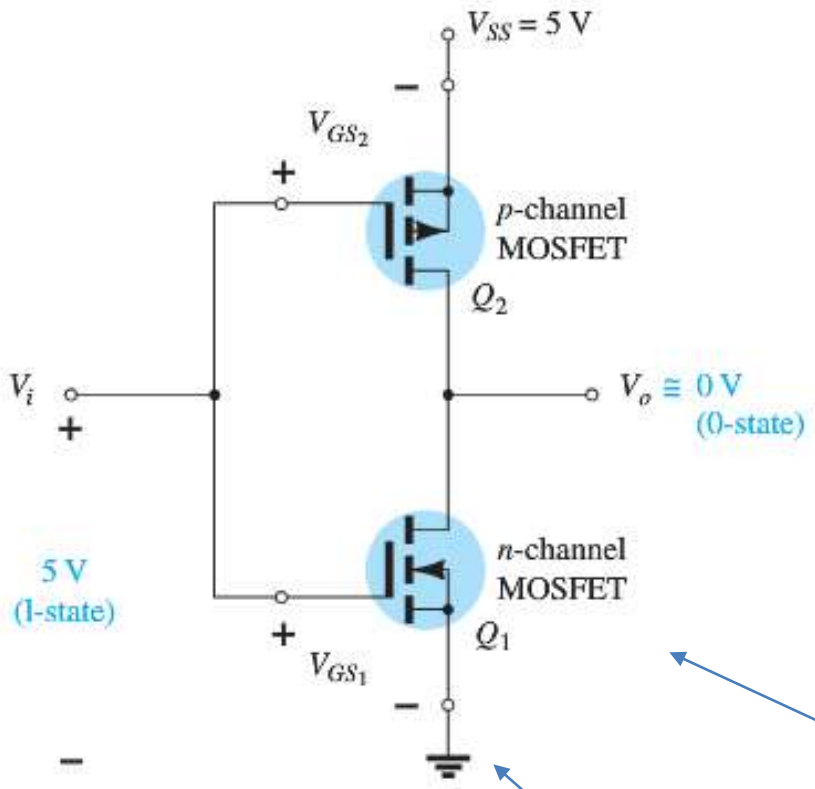
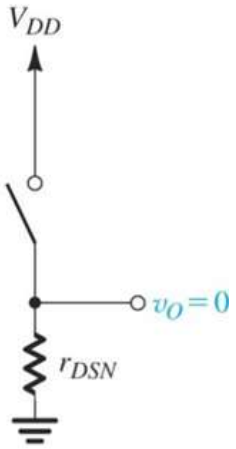
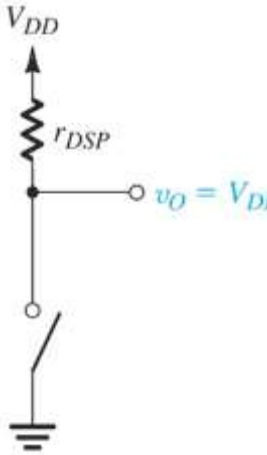


Figure: A logic inverter operating from a dc supply V_{DD}.

CMOS Logic Design: CMOS Inverter







Input 1, Output 0

Input 0, Output 1

FET Biasing

(We will limit our discussion to only E-MOSFET.)

Mathematical Vs. Graphical Approach

- The relationship between input V_{GS} and output I_D is nonlinear, which complicates the mathematical approach to the dc analysis.
- We want to design Amplifier with MOSFET
- MOSFET will be in Saturation Region
- Current is constant in Saturation region
- $I_D = I_S = k\,(V_{GS} - V_t)^2$
- A graphical approach is less accurate but quicker
- We will use graphical solutions rather than mathematical solutions.

FET General Relationships for DC Analysis

$$I_G \cong 0\,\text{A}$$

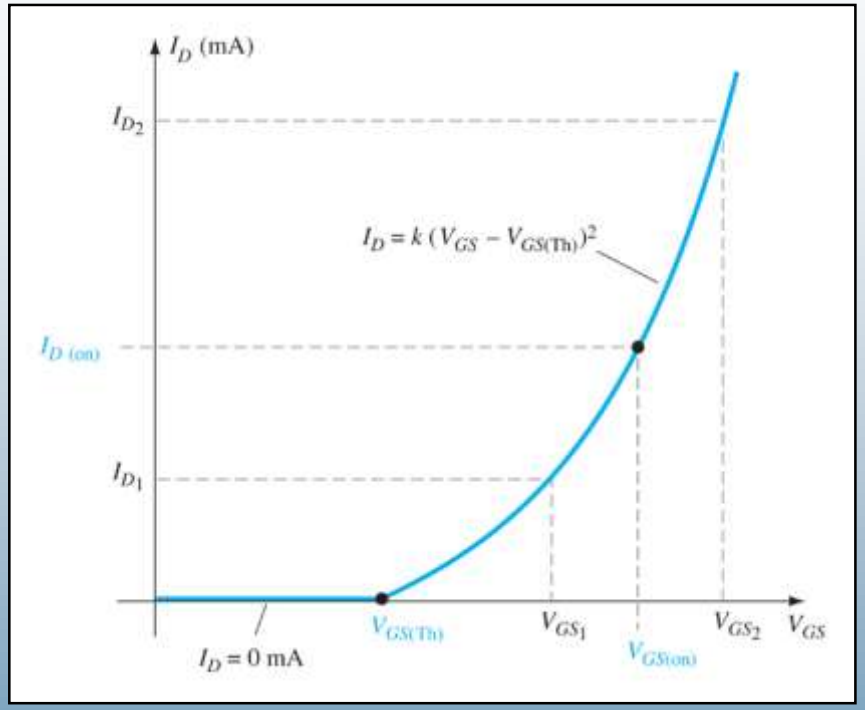
$$I_D = I_S$$

$$I_D = k(V_{GS} - V_T)^2$$

Plotting The E-MOSFET Transfer Curve

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$



- Once *k* is defined, other levels of I_D can be determined for the chosen values of V_{GS}
- Determining about 3 to 4 points enables drawing the device transfer characteristics.

Voltage-Divider Biasing

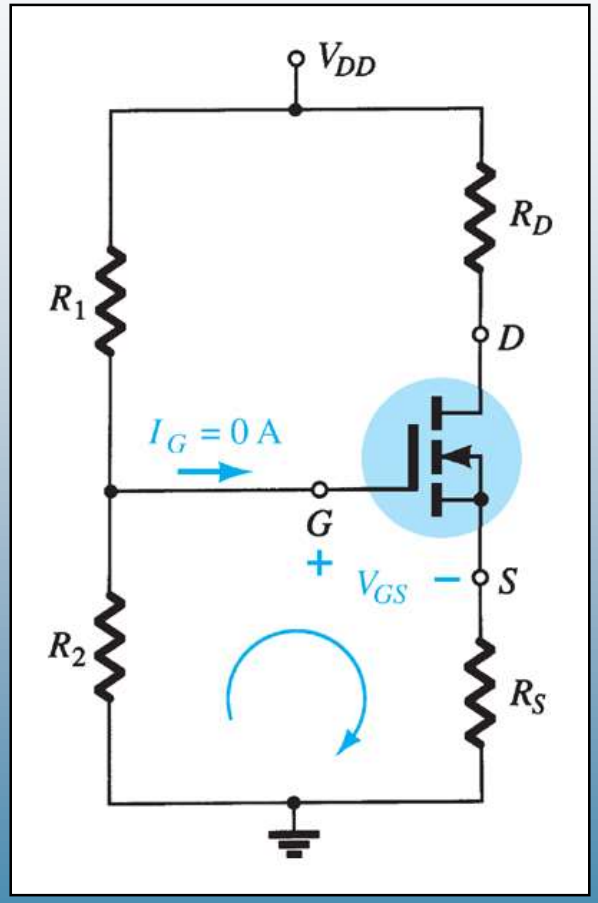
Plot the line and the transfer curve to find the Q-point using these equations:

$$I_G = 0;\ I_D = I_S$$

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$



Voltage-Divider Bias Q-Point (E-MOSFET)

Network: Plot the line using

$V_{GS} = V_G$, $I_D = 0$ A

$I_D = V_G / R_S$, $V_{GS} = 0$ V

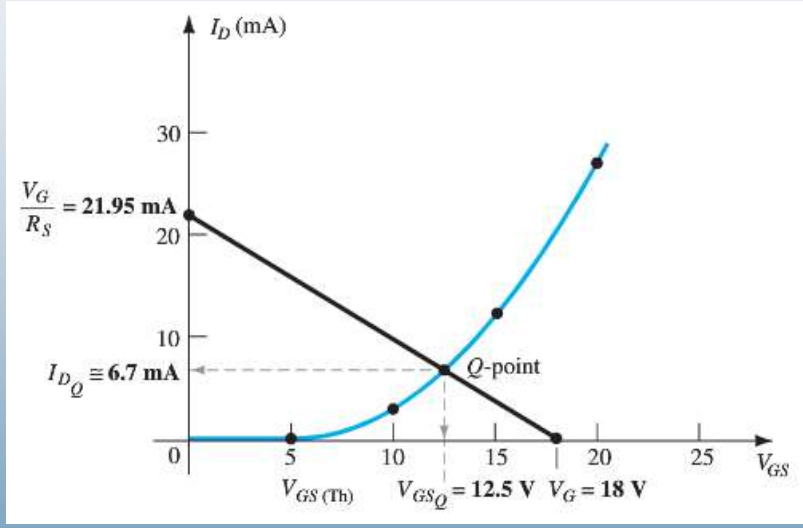
Device: Using the following values from the spec sheet, plot the transfer curve:

V_{GSTh}, $I_D = 0$ A

$V_{GS(on)}$, $I_{D(on)}$

The point where the line and the transfer curve intersect is the *Q*-point.

Using the value of I_D at the *Q*-point, solve for the other circuit values.



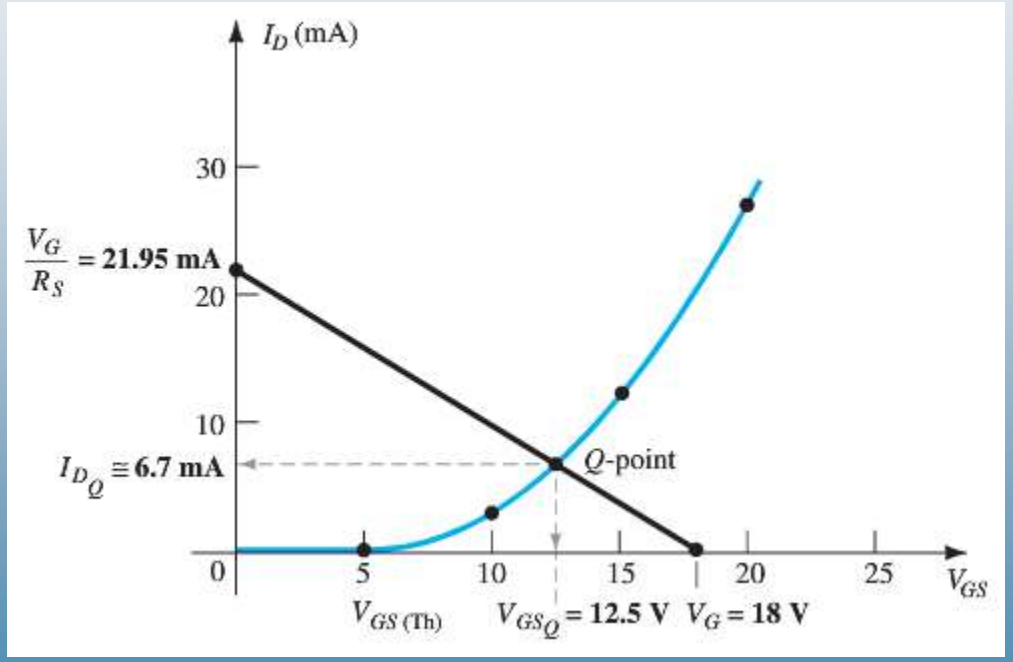
EXAMPLE 7.11 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

Solution:

Network

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$



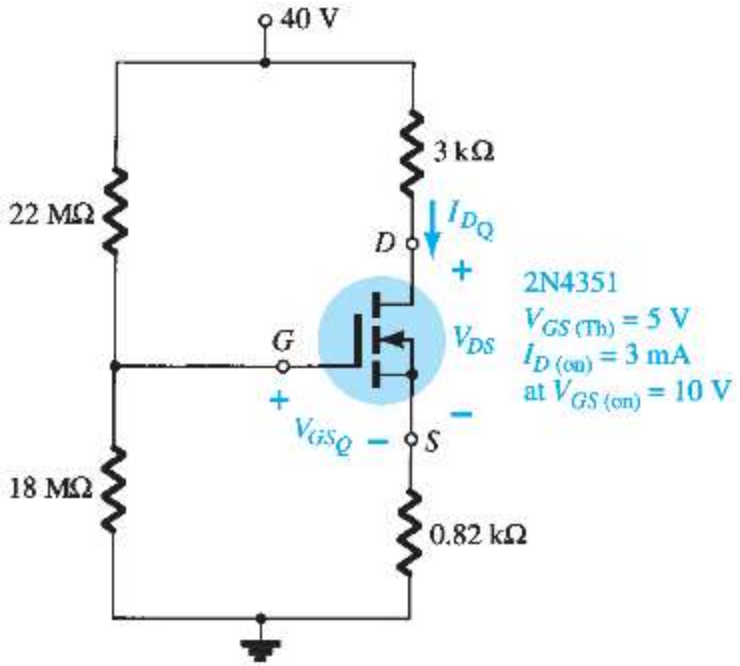


FIG. 7.44
Example 7.11.

Device

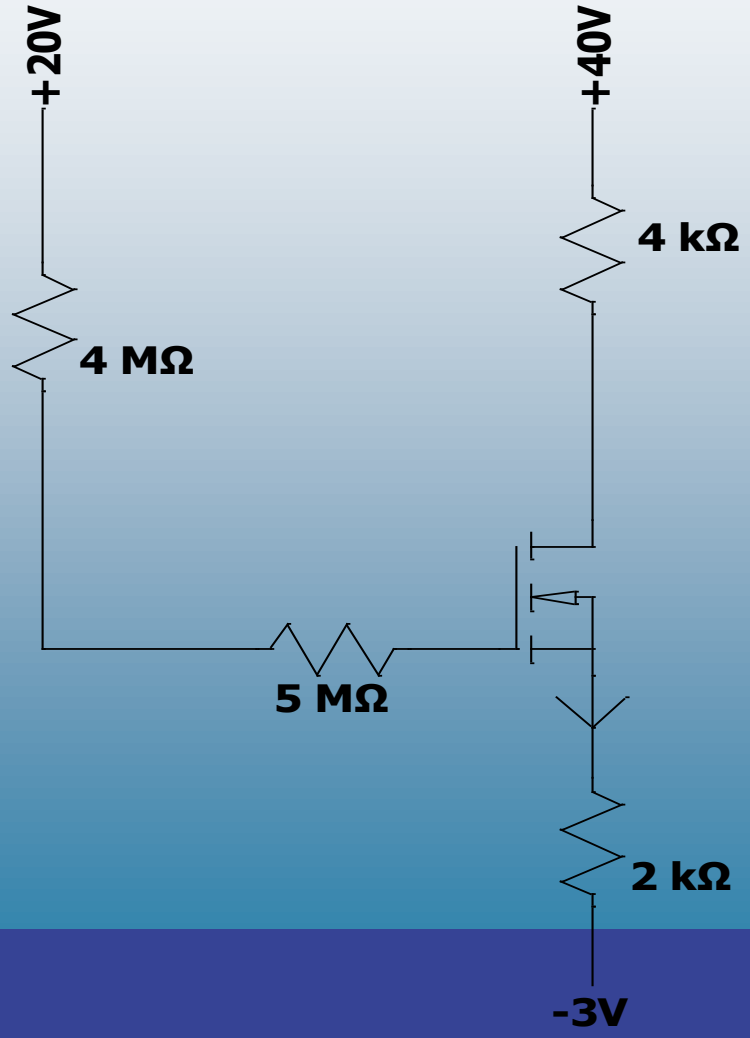
$V_{GS(Th)} = 5\,\text{V}, \quad I_{D(on)} = 3\,\text{mA}$ with $V_{GS(on)} = 10\,\text{V}$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2} = \frac{3\,\text{mA}}{(10\,\text{V} - 5\,\text{V})^2} = 0.12 \times 10^{-3}\,\text{A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(Th)})^2 = 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$I_{D_Q} \cong$ **6.7 mA** $\quad V_{GS_Q} =$ **12.5 V** $\quad V_{DS} = V_{DD} - I_D(R_S + R_D) =$ **14.4 V**

For the NMOS below, $k = 0.2\ mA/V^2$ and $V_t = 3V$.
Draw the device/characteristics curve and load line of the NMOS.
Show the Q-point in the graph.
Find I_{D_Q}, I_{S_Q}, I_{G_Q}, V_{GS_Q} and V_{DS}.



Step 0: Give appropriate current directions for the 3 terminals.

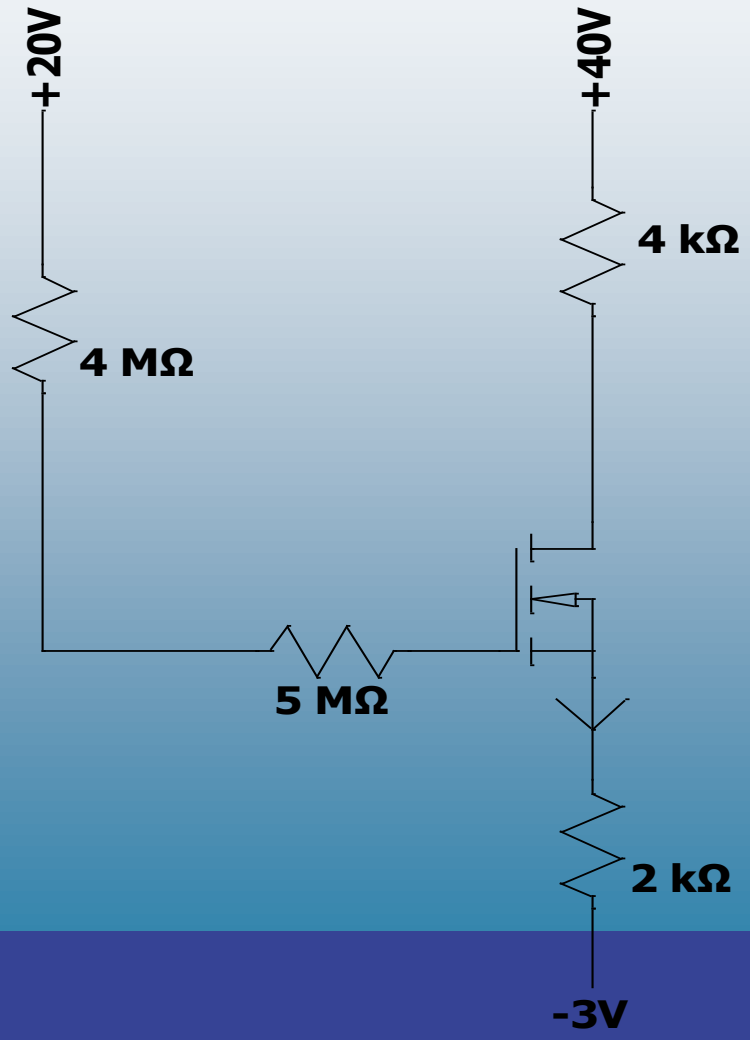
Step 1: Drawing Load Line from KVL at Gate-Source.

Step 2: Draw device/ characteristics curve from MOSFET current equation.

Step 3: Get Q-point from the intercept of Load Line and device/characteristics curve.

Step 4: Find V_{DS} from KVL at Drain-Source

For the NMOS below, $k = 0.2\ mA/V^2$ and $V_t = 3V$.
Draw the device/characteristics curve and load line of the NMOS.
Show the Q-point in the graph.
Find I_{D_Q}, I_{S_Q}, I_{G_Q}, V_{GS_Q} and V_{DS}.



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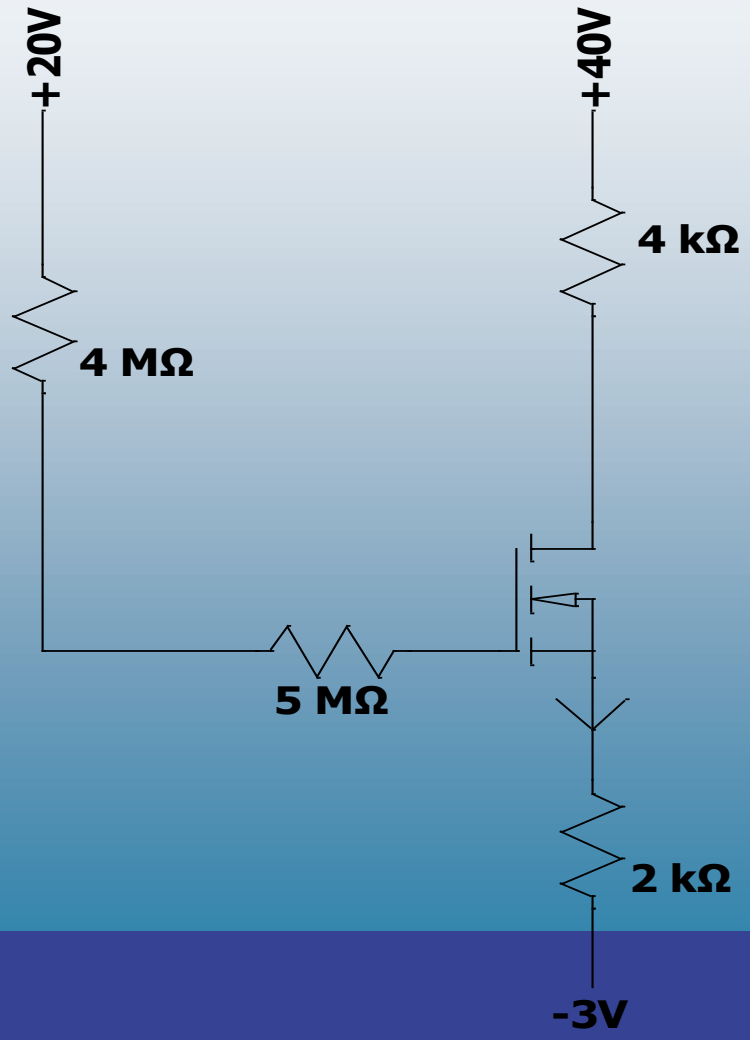
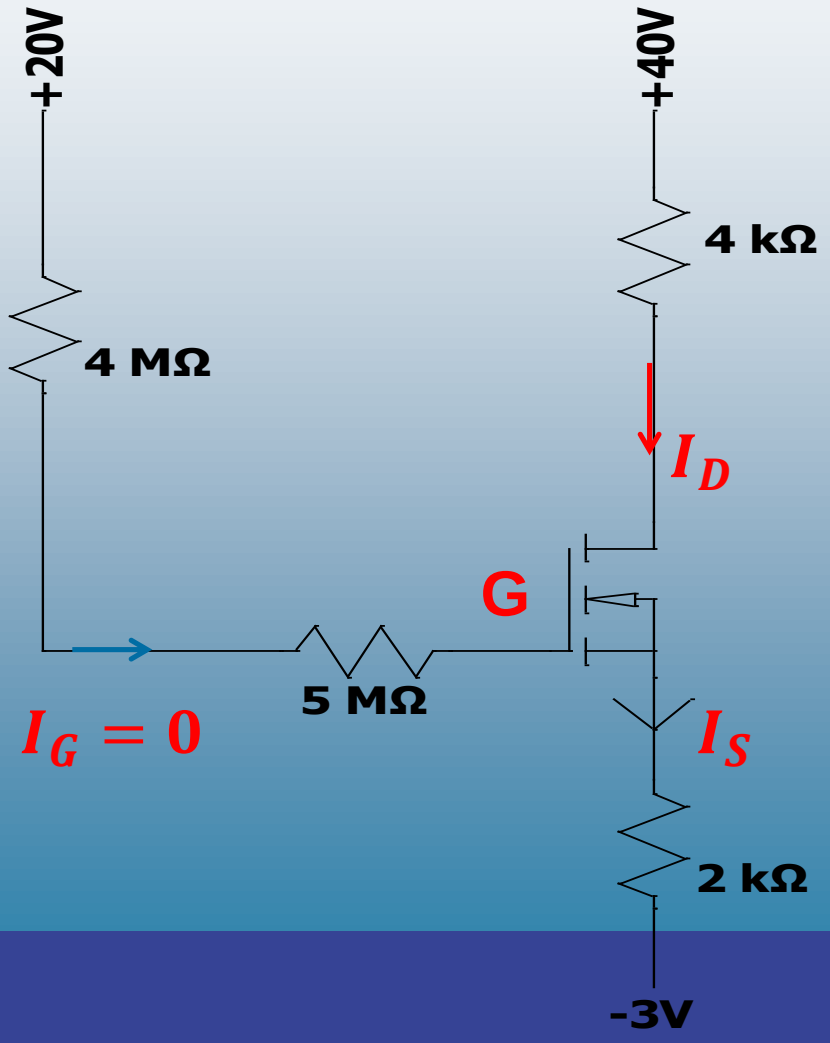




Step 1: Drawing Load Line from KVL at Gate-Source:

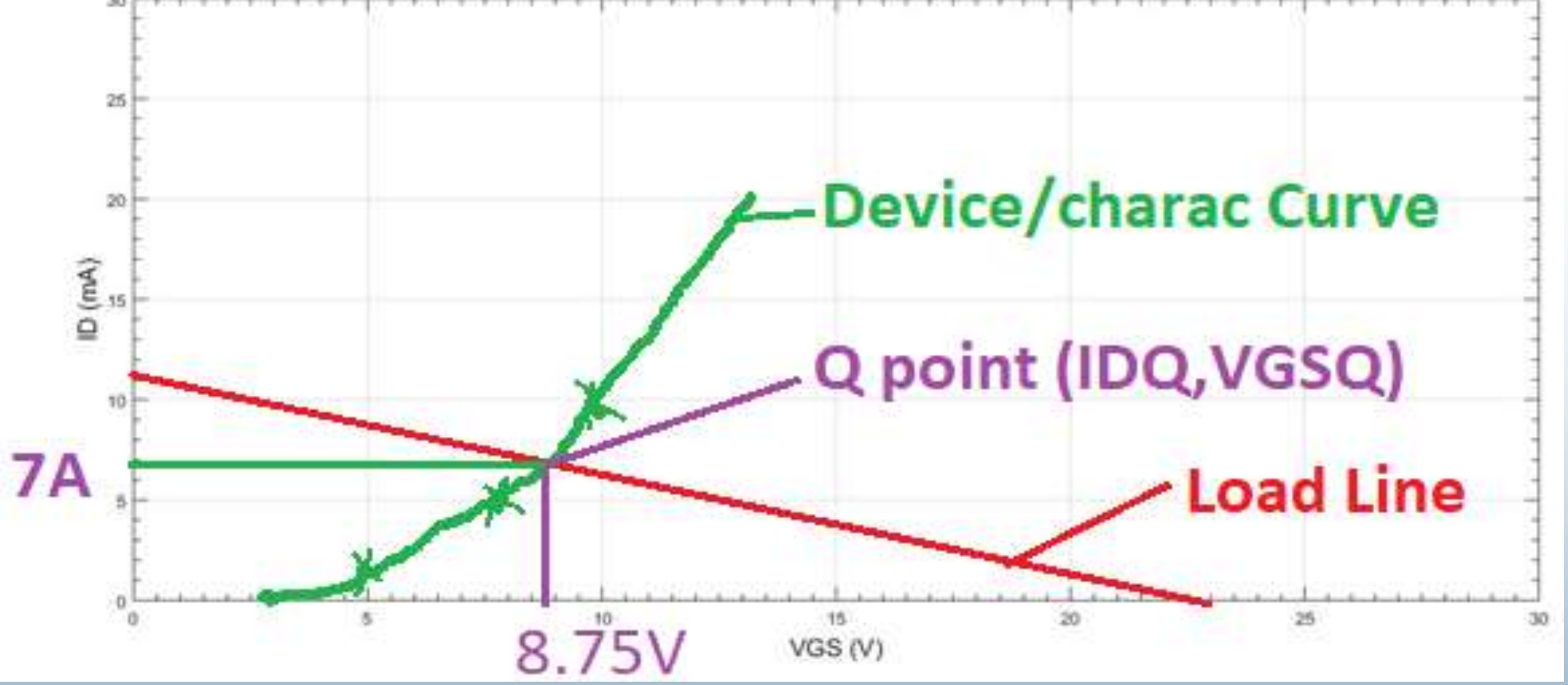
$$I_G = 0A;\ I_D = I_S$$

$$-20V + 0 \times 4M\Omega + 0 \times 5M\Omega + V_{GS} + 2k\Omega \times I_S - 3V = 0$$

$$V_{GS} + 2k\Omega \times I_D = 23$$

$$V_{GS} = 0 \rightarrow I_D = \frac{23}{2k\Omega} = 11.5mA$$

$$I_D = 0 \rightarrow V_{GS} = 23V$$



Step 2: Drawing device/characteristics curve from MOSFET current equation:

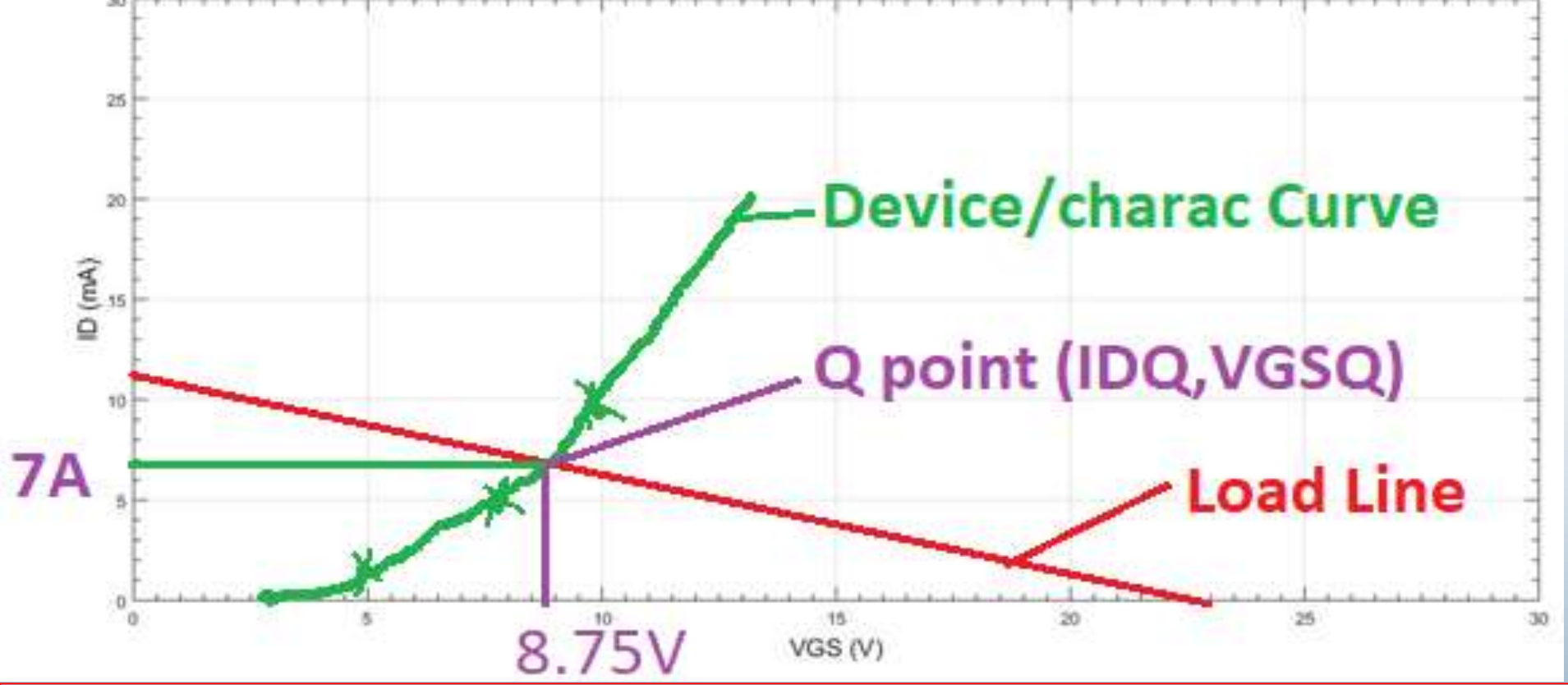
$$I_D = I_S = k(V_{GS} - V_t)^2 = 0.2(V_{GS} - 3)^2\ mA$$

$$V_{GS} \leq 3 \rightarrow I_D = 0\ mA$$

$$V_{GS} = 5V \rightarrow I_D = 0.2(5-3)^2 = 0.8\ mA$$

$$V_{GS} = 8V \rightarrow I_D = 0.2(8-3)^2 = 5\ mA$$

$$V_{GS} = 13V \rightarrow I_D = 0.2(13-3)^2 = 20\ mA$$

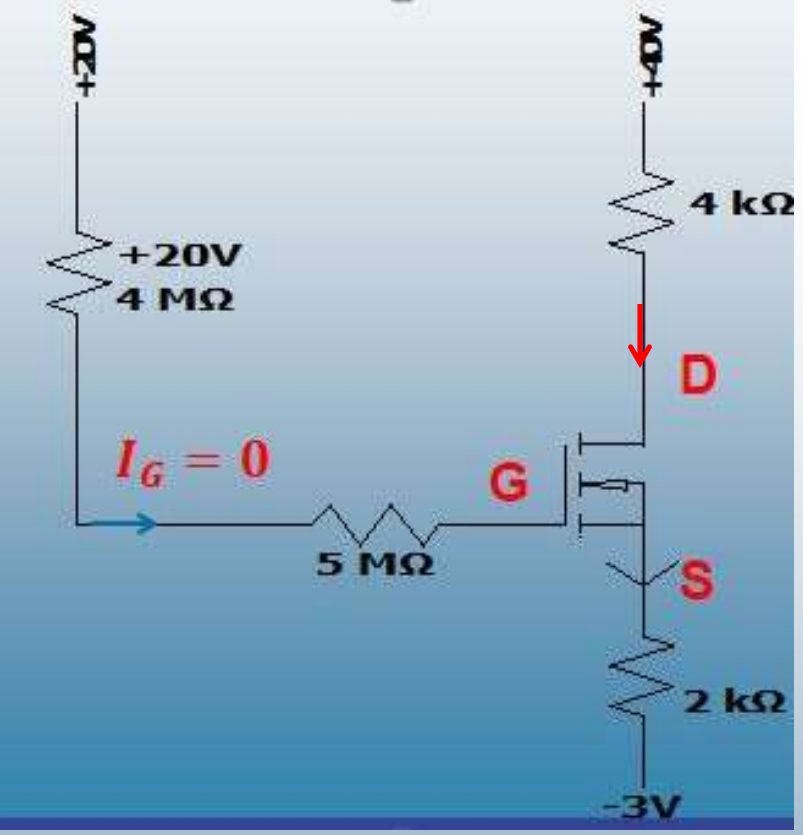


$I_D \neq 11.5mA; V_{GS} \neq 23V$

$I_{D_Q} = I_{S_Q} = 7mA$

$I_{G_Q} = 0mA$, Always

$V_{GS_Q} = 8.75V$



Step 4: Find V_{DS} from KVL at Drain-Source

$$-40V + I_D \times 4k\Omega + V_{DS} + 2k\Omega \times I_S - 3V = 0$$

$$V_{DS} + 6k\Omega \times I_D = 43$$

We know: $I_{D_Q} = I_{S_Q} = 7mA$

$$V_{DS} = 43 - 6k\Omega \times 7mA = 1V$$

Special Case: If k is not given. But $V_t = 5V$ is given

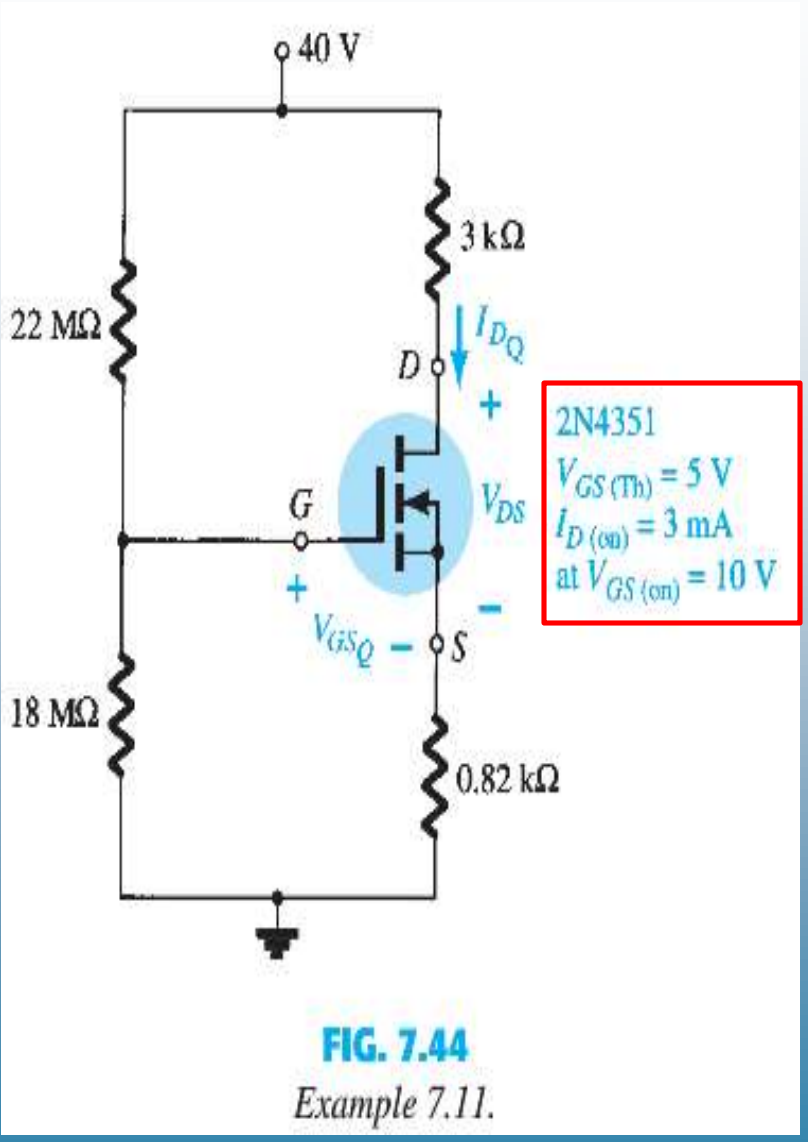


FIG. 7.44
Example 7.11.

Given, $I_D = 3mA$ at $V_{GS} = 10V$

$$I_D = 3\ mA = k(V_{GS} - V_t)^2$$

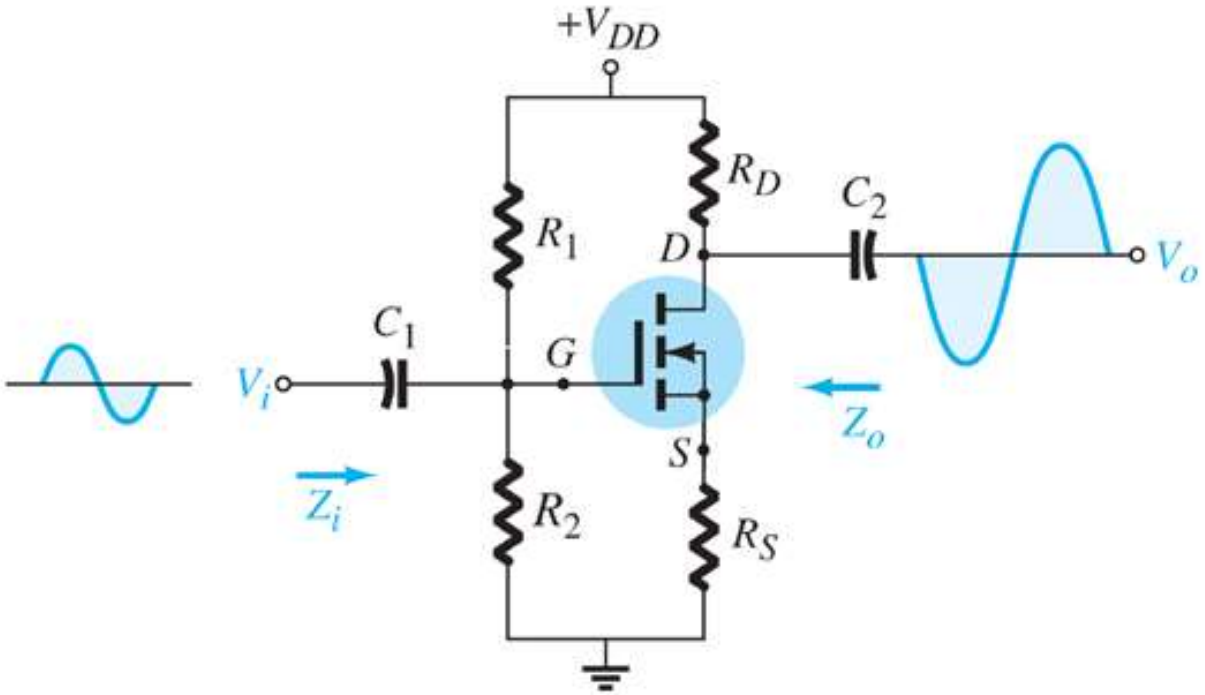
$$3\ mA = k(10 - 5)^2$$

$$k = \frac{3}{(10-5)^2} = 0.12\ mA/V^2$$

FET Amplifiers

(We will limit our discussion to only E-MOSFET.)

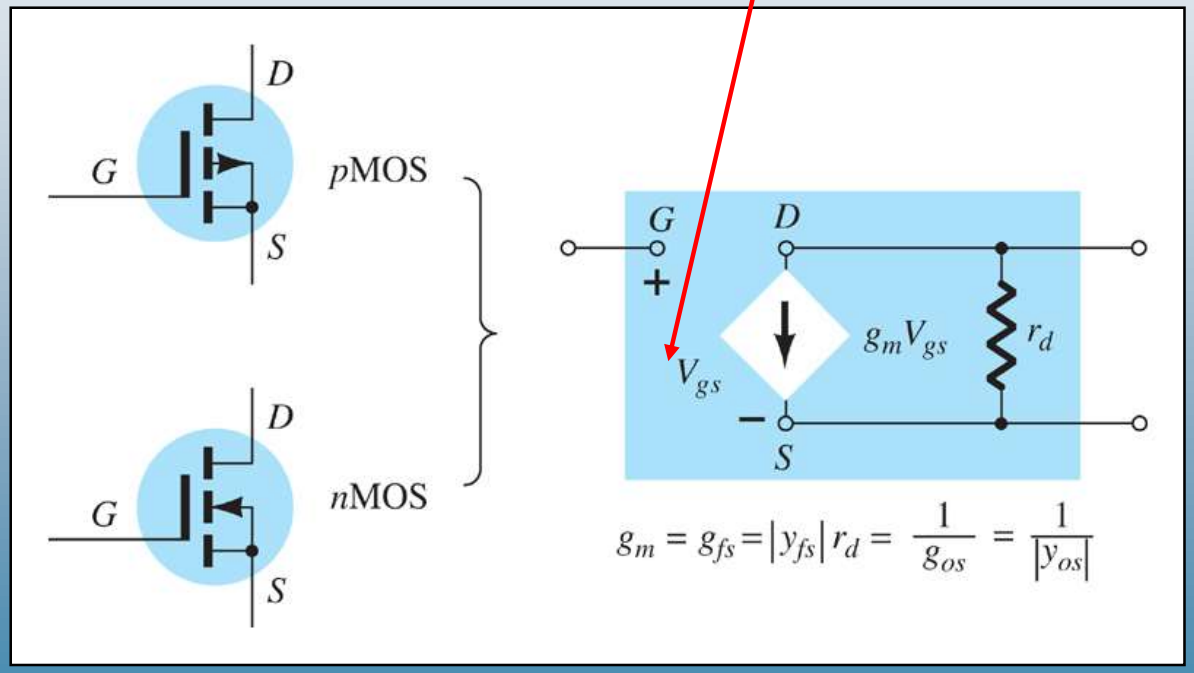
Voltage-divider bias
E-MOSFET



E-Type MOSFET AC Equivalent

An open-circuit between gate and drain–source channel

g_m and r_d can be found in the specification sheet for the FET.



Determining g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

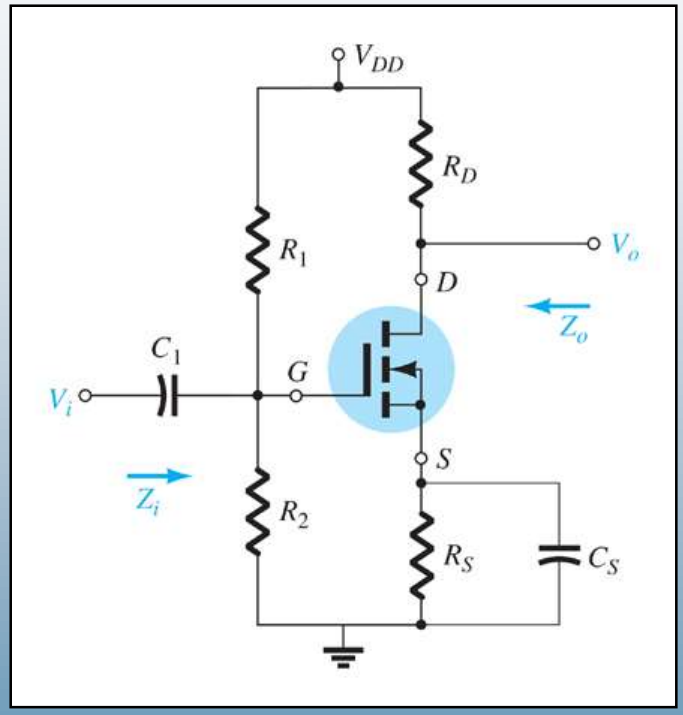
$$g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})$$

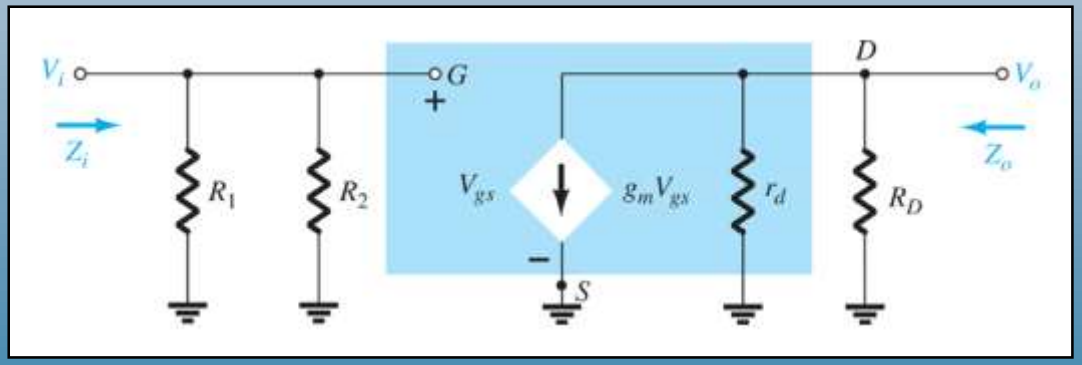
The constant k can be determined from a given typical operating point on a specification sheet

Common-Source Voltage-Divider Bias

The input is applied to the gate and the output is taken from the drain.

There is a 180º voltage phase shift between input and output.

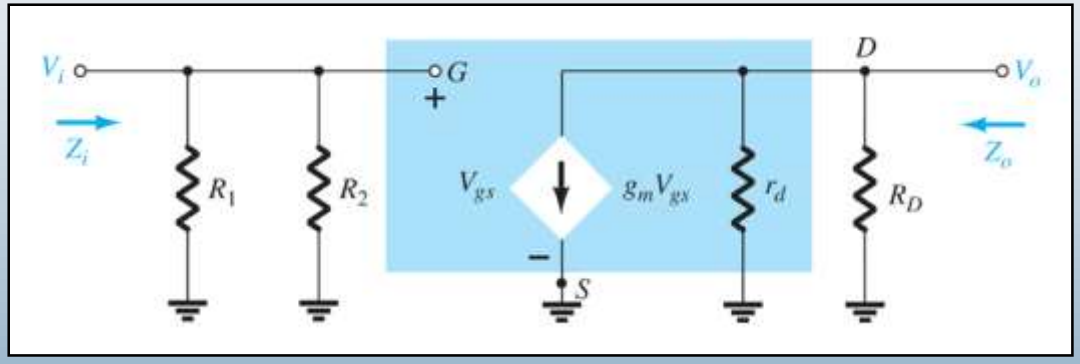




Calculations

Input impedance:

$$Z_i = R_1 \| R_2$$



Output impedance:

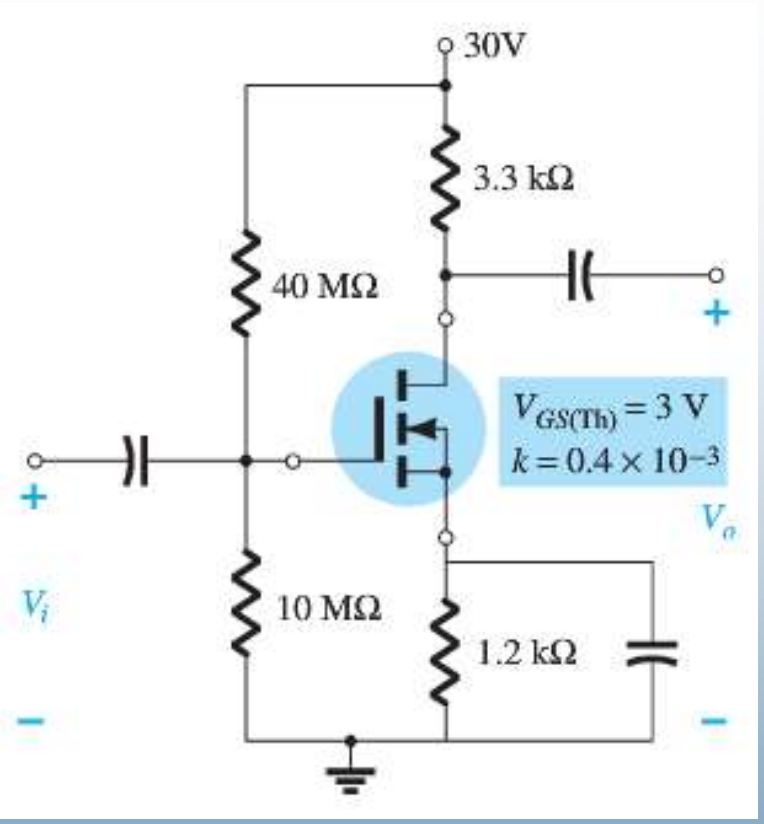
$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10}$$

Voltage gain:

$$A_v = -g_m (r_d \| R_D) \qquad A_v \cong -g_m R_D \Big|_{r_d \geq 10 R_D}$$

Determine the output voltage for the network of Fig. 8.87 if $V_i = 0.8$ mV and $r_d = 40$ kΩ.



Determine the output voltage for the network of Fig. 8.87 if $V_i = 0.8$ mV and $r_d = 40$ kΩ.

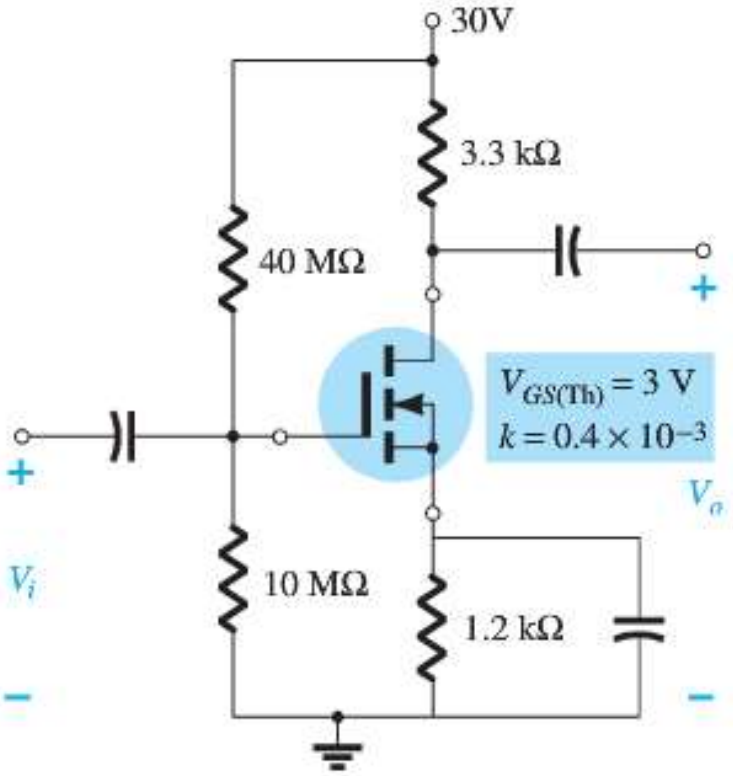


FIG. 8.87

$$V_{GS_Q} = 4.8 \text{ V}, g_m = 2k\left(V_{GS_Q} - V_{GS_{(Th)}}\right) = 2(0.4 \times 10^{-3})(4.8 \text{ V} - 3 \text{ V}) = 1.44 \text{ mS}$$

$$A_v = -g_m(r_d \parallel R_D) = -(1.44 \text{ mS})(40 \text{ k}\Omega \parallel 3.3 \text{ k}\Omega) = -4.39$$

$$V_o = A_v V_i = (-4.39)(0.8 \text{ mV}) = \mathbf{-3.51 \text{ mV}}$$

Thank You!

It was great having you in the class!

Best of luck!