Course Outline & Outcome

CSE332 Computer Organization and Architecture
CSE332L Computer Organization and Architecture Laboratory

1. **Course Schedule/Timing:** Lecture – 3 Hours/week, Lab – 3 Hours/week

Instructor: Tanjila Farah (TnF)

Office: SAC 929

Office Hours: To be announced

E-mail : tanjila.farah@northsouth.edu

Lab Room: 5th Floor of SAC Building, 8th floor OAT, and LIB 6th floor labs

Pre-requisites: CSE 231 and CSE 231L

2. **Course Description:**

Simply, a computer is a set of components (Processor, Memory and Storage, Input/Output Devices) interconnected (by Bus) in such a way as to enable the executionof a program (set of instructions) stored in memory.
This course introduces students to the basic concepts of computers, their design and how they work. It encompasses the definition of the machine's instruction set architecture, its use in creating a program, and its implementation in hardware. The course addresses the bridge between gate logic and executable software, and includes programming both in assembly language (representing software) and HDL (representing hardware).
We will study modern computer principles using a typical processor and emphasize system-level issues, understanding process performance, and the use of abstraction as atool to manage complexity. We then learn how e-cient memory systems are designed to work closely with the processor. Next, we study input/output (I/O) systems which bring the processor and memory together with a wide range of devices. Finally, we introduce systems with many processors.

3. **Course Objective:**

1. to develop basic understanding of computer organization: roles of processors, main memory, and input/output devices.
2. to evaluate/measure the performance of a computing system for comparing with other similar systems
3. to familiar with architectural design concepts related to different building blocks of a processor.
4. to employ specialized knowledge of subsystems like data-path, memory and control unit components to design a RISC processing element
5. to define processor specification and instruction set architecture.
6. to understand memory organization, including cache structures and virtual memory schemes.

4. Course Learning Outcomes (COs):

Upon Successful completion of this course, students will be able to:

Sl.	CO Description	Weightage (%)
CO1	evaluate the performance of a computing system	20%
CO2	analyze instruction set architecture and different building blocks of processor	40%
CO3	Design an instruction set architecture and subsystems of central processing unit.	40%

5. Mapping of CO-PO:

Sl.	CO Description	Program Outcome (PO)	KP	Bloom's taxonomy domain/level	Delivery methods and activities	Assessment tools
CO1	evaluate the performance of a computing system	**a**	K4	Cognitive/ Evaluate	Lectures,Notes	Quiz/Exam
CO2	analyze instruction set architecture and different building blocks of processor	**b**	K5	Cognitive/ Evaluate	Lectures,Notes	Quiz/Exam
CO3	Design an instruction set architecture and subsystems of central processing unit.	**a**	K6	Cognitive/ Evaluate	Lectures, Notes, & Lab	Project demonstration & Report

6. Textbook:

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1	David A. Patterson, John L. Hennessy	2013	Computer Organization and Design, MIPS Edition: The Hardware/Software Interface	5th	Morgan Kaufmann	ISBN-13: 978-0124077263
2	M. Morris Mano	2009	Computer Systems Architecture	3rd	Pearson	ISBN-978-81-317-070-9

Reference:

No	Name of Author(s)	Year of Publication	Title of Book	Edition	Publisher's Name	ISBN
1	William Stallings	2015	Computer Organization and Architecture	3rd	Pearson	ISBN-13: 978-0134101613

7. Weightage Distribution among Assessment Tools:

Assessment Tools	Theory Weightage (%)
Class Performance	5
Assignment	NON CREDIT
Quizzes	15
Midterm Exam	25
Final Exam	30
Term Project	10
Lab work	15

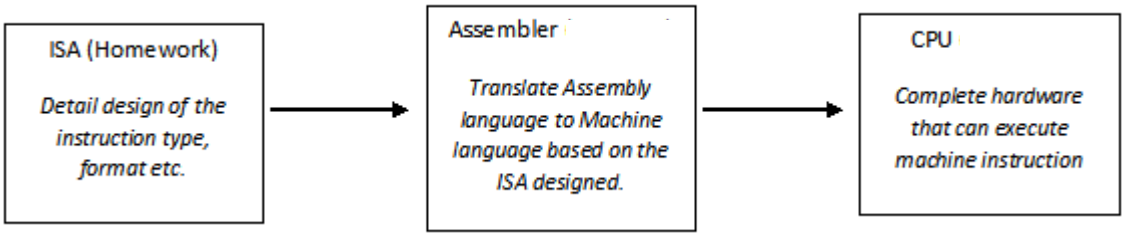
Make-up Policy:
No make-up testes for the missed Quizzes.

8. Lecture plan:

Course Topics	Chapters
• The History of computer, Computer generations, families and development. • Introduction to Computer organizations and architecture	Patterson, Chapter 1
• Basic processing unit of a Single Bus Architecture. • Instruction Set Design & Instruction representation. • Execution of complete instruction cycle in a single Bus system. • Control Unit operation in Single Bus system, Hardwired control unit	Mano, Chapter 4 & 5
• Basic operation of assembler. • Translation from Symbolic code to binary program	Mano, Chapter 6
Microprogrammed control unit	Mano, Chapter 7
Midterm	
• Introduction to MIPS instruction set. • Datapath and Control • Datapath Design • Register transfer and Interconnection • Control Unit Design • Single & Multi cycle Datapath Design	Patterson, Chapter 4
• Pipeline • Data Hazard • Stall & Forward • Branch Hazard	Patterson, Chapter 4
Computer performance metrics and Evaluation	
• Memory • Memory hierarchy • Cache Memory • Performance issues • Virtual Memory	Patterson, Chapter 5
Final Exam	

Design Your Own CPU

One of the course objectives is to be able to design a complete CPU system. It starts with learning about ISA, advanced ALU, data path and control, pipelining in theory. In order to make this learning more effective a step by design of the complete CPU system is carried out through pen and paper, simulation tools etc. Students work in a group and try to develop small pieces and finally connect them together to get their cpu as explained in the following diagram.



Further details are explained in due time.