Version 1.3

Namal University, Mianwali

Department of Electrical Engineering

Communication Systems (Lab)

Lab – 8

Phase Locked Loop (PLL)

Student Name	Student ID

Instructor: Dr. Sajjad Ur Rehman

Lab Engineer: Faizan Ahmad

Version 1.0 – 27/03/2021 – Engr. Arbaz
Version 1.1 – 27/03/2022 – Engr. Arbaz
Version 1.2 – 20/03/2023 – Engr. Imtiaz Ul Hassan
Version 1.3 – 26/02/2024 – Engr. Faizan Ahmad

Introduction

The purpose of this lab is to enable the students to write a code for frequency modulation and Demodulation using MATLAB. The students will also observe the modulation and demodulation using Communication Trainer, CT-3000.

Course Learning Outcomes

CLO1: Perform hardware experiments for modulation/ demodulation techniques as well as sampling of analog signals.

CLO2: Develop software simulations to observe the performance of analog and digital communication systems.

CLO4: Report desired results proofs and calculations.

Equipment

- Software
    - Proteus
- Hardware
    - CT-3000 Trainer

Instructions

- This is an individual lab. You will perform the tasks individually and submit the required files at the end of the lab.
- Plagiarism or any hint thereof will be dealt with strictly. Any incident where plagiarism is caught, both (or all) students involved will be given zero marks, regardless of who copied whom. Multiple such incidents will result in disciplinary action being taken.

Phase Locked Loop

The phase-locked loop, or PLL, is one of the most useful blocks in modern electronic circuits. It is used for many different applications, ranging from communications (FM modulation, demodulation), noise reduction, and by using PLL it is possible to generate output frequency which is multiple of input frequency.

A PLL is a closed-loop system, which maintains same phase between input and output signal Close loop means that there is the feedback to the input from output. This whole loop system involves three main steps called, phase detection, loop filter, and voltage controlled oscillator.

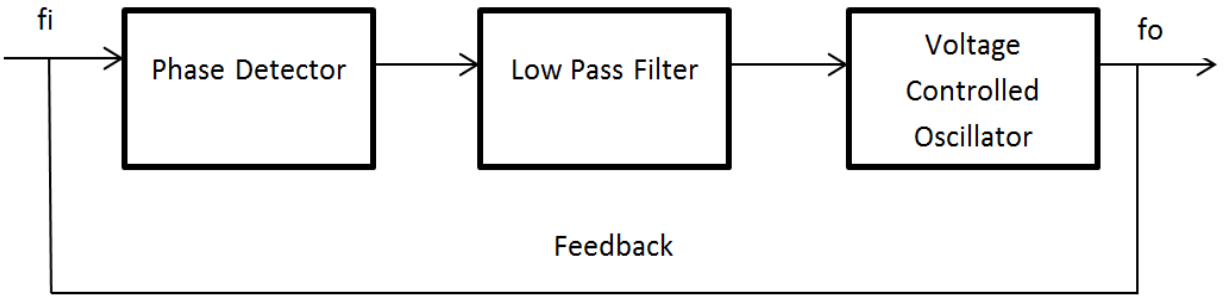


Figure 1: PLL Block Diagram

1. Phase Detector

Phase detector is basically a comparator based circuit to which when an input signal is applied it compares phase and frequency of this input signal with the phase and frequency of the VCO free running frequency (reference frequency) the center frequency of the PLL, which is the frequency that the VCO runs at when not locked to the input frequency. After comparator action it represents the phase difference in the form of pulsating-DC waveform with a duty-cycle proportional to the phase difference ("error") between the given signal and reference signal. The bigger the phase difference becomes (within certain limits), the larger the duty cycle of the phase comparator's output becomes. If the two signals differ in phase and/or frequency, an error voltage is generated.

2. Voltage Controlled Oscillator

Voltage controlled oscillator is connected next to the output of phase detector through a loop filter. Its primary function is to convert the output of phase detector (which is in digital form) into the analogue frequency with respect to the error generated by phase detector. It is a special oscillator called a VCO, or Voltage Controlled Oscillator. The output frequency of the VCO is directly proportional to the error voltage. Any deviation in the frequency and/or phase of the two input signals to the phase comparator will generator error voltage which is further converted to the deviation in free running frequency of the VCO. In short, the VCO in effect converts the control voltage into frequency. The PLL under normal conditions attempts to make the VCO output frequency exactly equal to a second (reference) frequency.

3. VCO

VCO is basically a voltage controlled frequency controlled by input voltage. It needs a nice, steady DC voltage at its control voltage input. Also as phase comparator output is a pulse so it contains higher frequency components which can disturb the tuning of VCO as well as useless for VCO and therefore low pass filter is required to eliminate the useless frequencies. In order to ensure this, the pulsating DC from the phase comparator is fed into a loop filter on its way to the VCO. This filter in effect "smoother" the rough phase comparator output waveform into a fairly steady DC voltage and also rejects the un-necessary frequency components present. The VCO is then able to smoothly track the input reference frequency.

PLL IC (NE-565) Pin Configuration:

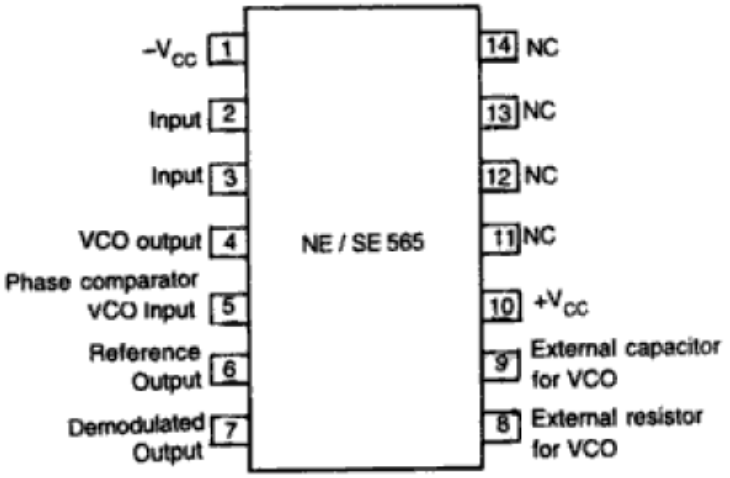


Figure 2: Pin Configration

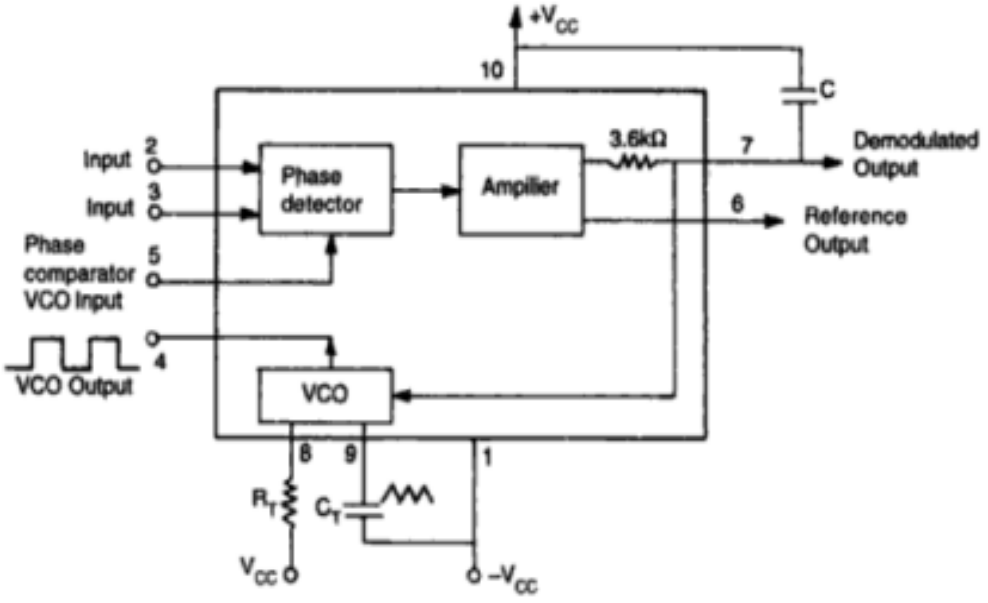
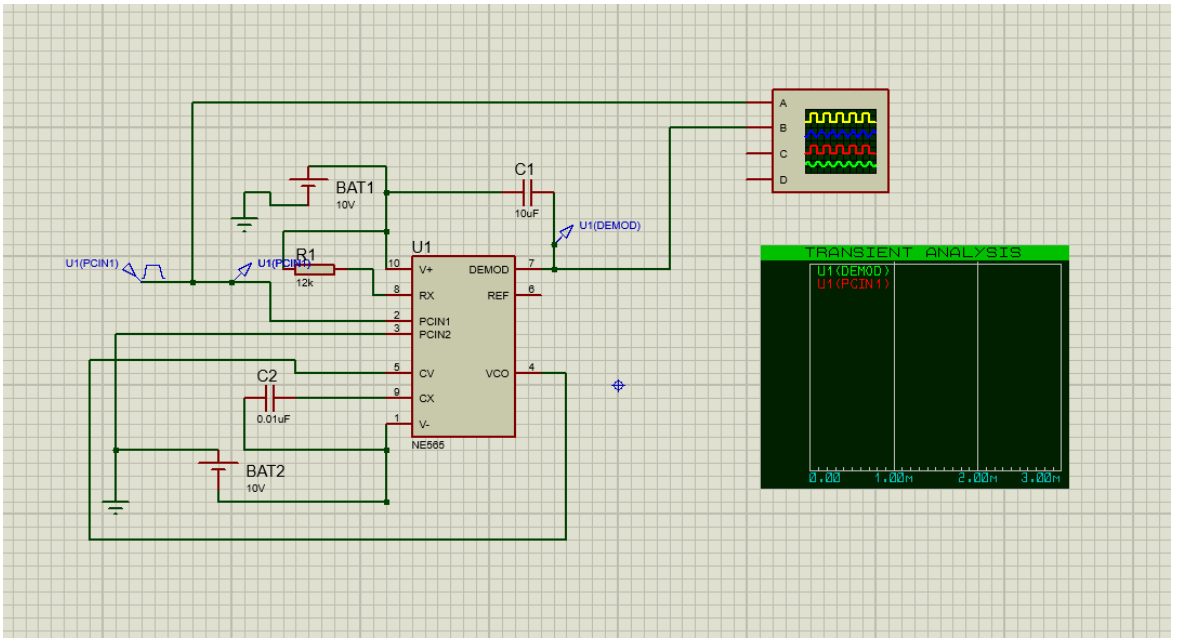


Figure 3: Internal Circuit of IC-565

Task 1 – Simulation



- Implement the given circuit on proteus.
- Take Vcc=10v, Take value of C1 so that the LPF cutoff frequency is 1k.
- Take pulse generator at input with 1k Hz frequency, and R1=12k and C2=0.01uF which set lock frequency at 1 kHz.
- Observe the signal at reference and error signal.
- Write the working of circuit in your report in detail.

Task 2 – Hardware

Procedure

- First of all energize CT-3000 communication Trainer by applying $220V_{AC}$.
- For frequency modulation and demodulation, FM module is inserted in socket 4 and PLL/Frequency Demodulator module is inserted in socket 2.
- Set the message signal AF of 1 KHz and carrier signal RF of 10MHz directly from trainer at J1 port of FM module.
- Then, frequency modulated signal is observed, at J2 of FM module, on oscilloscope by using prob.
- Now, J2 of FM module is connected to J1 of PLL module by using connecting wire and demodulated signal is observed at J2 on oscilloscope by using prob. Show the output to the instructor.
- Observations:

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Report

For each exercise, include the code you write, explanation where asked, all outputs, as well as answers to any questions, as required. Upload your final report (containing general formalities like cover page containing your name and roll number etc.) to QOBE in the report submission folder.

Upload your final report in the separate submission folder on QOBE.

Com. Sys. Lab 8 Rubric

Method of Evaluation: Executable code, Report submitted by students **Measured**
Learning Outcomes:
CLO1: Operate under supervision and practice hardware experiments for modulation/demodulation techniques as well as sampling of analog signals..
CLO2: Develop software simulations to observe the performance of analog and digital communications systems.
CLO4: Report desired results proofs and calculations.

	Excellent 10	Good 9-7	Satisfactory 6-4	Unsatisfactory 3-1	Poor 0	Marks Obtained
Hardware Experiment (CLO1)	Excellent performance in hardware experiments for modulation	Good performance but lack of understanding	Slightly incorrect Hardware setup withproper understanding	Bad performance in hardware experiment	Experiment not performed	
Code (CLO2)	Correct code, easily understandable with comments where necessary	Correct code but without proper indentation or comments	Slightly incorrect code with proper comments	Incorrect code with improper format and no comments	Code not submitted	
Output (CLO2)	Output correctly shown with all Figures/ Plots displayed as required and properly labelled	Most Output/ Figures/ Plots displayed with proper labels	Some Output/ Figures/ Plots displayed with proper labels OR Most Output/ Figures/ Plots displayed but without proper labels	Most of the required Output/ Figures/ Plots not displayed	Output/ Figures/ Plots not displayed	
Answers (CLO2)	Meaningful answers to all questions. Answers show the understanding of the student.	Meaningful answers to most questions.	Some correct/ meaningful answers with some irrelevant ones	Answers not understandable/ not relevant to questions	Wrong Answers	
Lab Report (CLO4)	Report submitted with proper grammar and punctuation with proper conclusions drawn and good formatting	Report submitted with proper conclusions drawn with good formatting but some grammar mistakes OR proper grammar but not very good formatting	Some correct/ meaningful conclusions. Some parts of the document not properly formatted or some grammar mistakes	Conclusions not based on results. Bad formatting with no proper grammar/ punctuation	Report not submitted	
Total						