IET Renewable Power Generation

Research Article

IET Journals
The Institution of Engineering and Technology

Design, analysis and experimental verification of a high voltage gain and high-efficiency DC–DC converter for photovoltaic applications

ISSN 1752-1416
Received on 7th September 2019
Revised 6th March 2020
Accepted on 30th March 2020
E-First on 3rd July 2020
doi: 10.1049/iet-rpg.2019.1020
www.ietdl.org

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Abstract: With the rapid development of photovoltaic systems, high step-up dc–dc converters draw significant attention, which shows the design challenges for simple topology, high efficiency, reduce voltage stress, and long lifespan. This study proposes a new high voltage gain converter that utilises the primary boost conversion cell and integrates with both switched-capacitor and coupled-inductor techniques. The proposed topology is modular and extendable for ultra-high step-up voltage gain. The leakage energy is recycled by a clamp circuit to minimise the switch voltage stress and power loss. One distinctive feature is that the voltage stress on the diodes and switch becomes low as well as constant against the variation of the duty cycle. Furthermore, the coupled inductor alleviates the diodes reverse recovery losses. The steady-state analyses, operation principles, and design guidelines are presented comprehensively. A prototype circuit is constructed to test the maximum power point tracking operation with voltage conversion from 30 to 380 V at 300 W. Experimental results substantiate the theoretical analysis and claimed advantages. The proposed converter demonstrates maximum power point tracking capability and high conversion efficiency over a wide range of power. The prototype shows the weighted efficiency of 96.3% according to the EU standard.

1 Introduction

Renewable energy sources, e.g. photovoltaic (PV), wind turbine, and fuel cell, are widely used around the world [1]. DC nanogrid is the latest concept to accommodate more distributed power generation and meet future energy demands [2]. A typical structure of DC nanogrid is shown in Fig. 1, which includes the power conversion modules (PCMs) to interface various power source and load in parallel onto a shared DC bus, shown as 380 V. The DC bus can be further integrated to utility grids through a centralised inverter or other DC nanogrids.

Alternative energy sources, e.g. PV, usually yield a low and unregulated voltage. For example, a commercially available PV module produces a voltage ranging from 25 to 35 V, which is significantly lower than the standard DC bus voltage, i.e. 380 V [3]. The parallel structure, which integrates each PV module independently, as shown in Fig. 1, is preferred for higher system reliability [3]. Thus, high gain converters are essential to integrate low voltage sources into high voltage DC bus. The challenge is to attain a high conversion ratio of voltage, meanwhile maintain high reliability and efficiency with the maximum power point tracking (MPPT) capability.

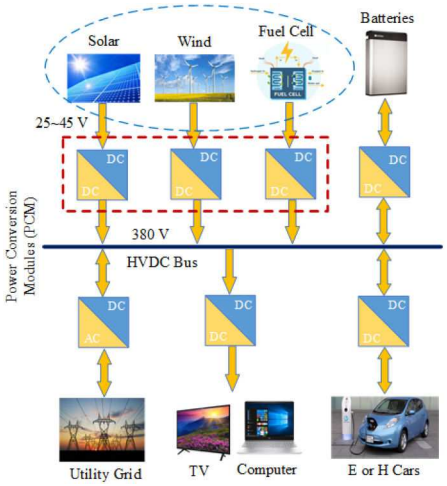

Fig. 1 *Architecture of a DC nanogrid*

The classical boost converter is infeasible to attain both high step-up gain and high conversion efficiency. A dual-output boost converter is proposed for bipolar DC microgrid in [4]. However, the solution is challenging to achieve both high conversion ratio and high efficiency. Therefore, research focuses on the challenge of overcoming the shortcomings to extend voltage gain at a high level. The PCMs are commonly classified as non-isolated and isolated topologies. Transformers are commonly utilised to reach a high voltage gain. Topologies using a switched capacitor and switched-inductor cells have also been proposed for high step-up voltage gain [5]. The voltage multipliers or voltage gain cells are another technique for achieving high conversion gain [6, 7]. The topologies can attain high step-up gain, but in general, suffer from high switch current stress. Thus, the solution does not show a significant advantage due to the relatively high conduction loss.

Non-isolated topologies mainly utilise coupled inductors (CLs) or transformers in the non-isolated form. Through the tapping of inductors, the converter can attain high voltage conversion ratio and low switch voltage stress [8]. The challenge for high conversion efficiency and reliability is that the leakage inductance resonates with the parasitic capacitance of the switch resulting ringing and a significant switch voltage spike. The snubber circuits are employed to recycle the energy of leakage inductor and alleviate parasitic oscillation [5, 8]. The converters presented in [9, 10] utilise the active clamp circuits. The active clamp circuits employ another active switch to realise soft switching.

However, an additional switch increases the system cost and outcomes in high losses. A clamp circuit is combined with the half-wave voltage lift circuit to attain considerable voltage gain in [11]. The converter presented in [12] utilises half-bridge cells connected in series with a flying capacitor to reduce voltage stress; however, the component count is higher. The voltage multipliers are employed in [13–17] to increase the conversion ratio of voltage further. In [13], a voltage doubler circuit is used with the secondary winding to attain high voltage gain. In [14–16], the secondary winding is integrated with two half-wave voltage multipliers to boost the conversion gain of voltage. An asymmetrical voltage

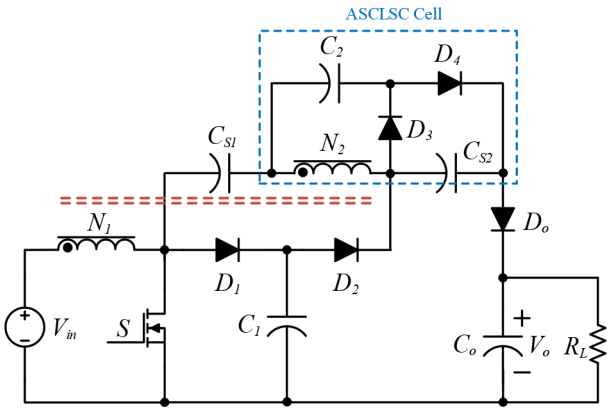

Fig. 2 *Proposed dc–dc converter*

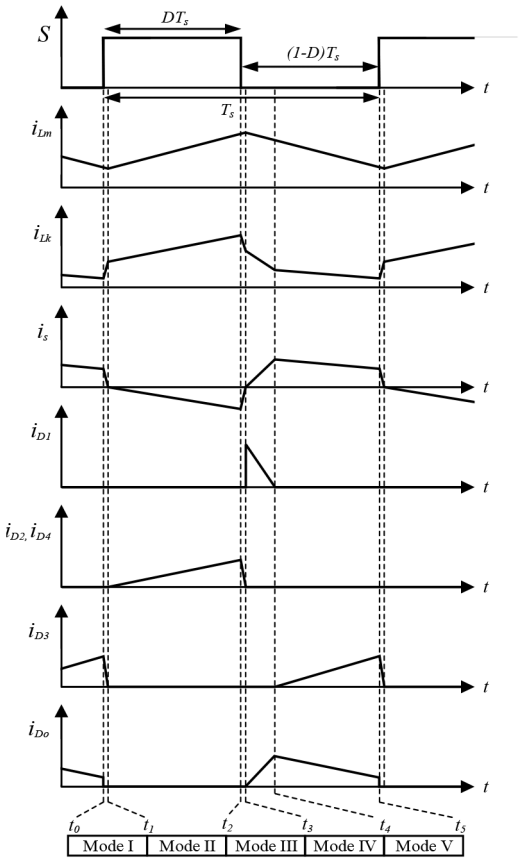

Fig. 3 *Critical waveforms of operating modes*

multiplier network is utilised in [17] to attain a high conversion ratio of voltage.

Furthermore, the switched capacitor and coupled inductor techniques are combined in [18–25] to attain ultra-large step-up voltage gain. For higher efficiency and gain, two voltage multiplier cells are added in [19]. A diode-capacitor-based multiplier is proposed in [20], which is combined with CL to attain high conversion gain. However, the voltage stresses of the above topologies are not constant and change with the duty cycle. The converters proposed in [21, 22] utilise a resonant switched capacitor with the leakage inductance for quasi-resonant operation. In [23], the converter can achieve an ultra-large gain by extending the architecture with voltage multiplier networks; however, active switch experiences high current stress resulting in high conduction losses. A high gain converter combining a negative clamp circuit with the technology of coupled inductor is proposed in [25]. The stresses of voltage on devices are low, but the voltage gain of the converter reduces at a high duty cycle. The efficiency of the converters presented in [22, 24, 25], is relatively low for the renewable energy system. The concept of multi-winding coupled inductor is proposed in the literature to lift the voltage gain further. It also distributes stresses of voltage; however, it increases the complexity as well as cost [26, 27]. The converters presented in [28, 29] are integrated with a single-ended primary-inductor converter to reduce the ripples in the input current. The interleaving solution is used to distribute the devices' thermal and current stresses, achieving high reliability for high power applications. However, it results in high cost, high component count, and limitation of duty cycle [30].

This research proposes a new converter that effectively integrates the coupled-inductor and switched-capacitor technologies to attain high efficiency, high voltage conversion ratio, and low voltage stress. The architecture is modular and extendable with a single active switch to realise ultra-high step-up voltage gain. The voltage stresses on semiconductor devices are low as well as constant against the variation in the duty cycle. The switch voltage stress is significantly suppressed at 1/6 times of the output voltage. Thus, a low voltage rating switch can be utilised to decrease conduction loss and cost. The voltage stress on capacitors is also comparatively low. The MPPT operation is validated experimentally to evaluate the effectiveness of the proposed topology for PV applications. The converter demonstrates the MPPT capability for maximum energy harvesting meanwhile attaining high conversion gain and high efficiency for a wide range of power conversion. The general topology introduction and description, and operating principle are presented in the next section. It is followed by experimental evaluation and finally conclusion at the end.

2 Topology and steady-state analysis

The proposed topology is illustrated in Fig. 2. It comprises of a basic boost unit and voltage multiplier networks. The multiplier network consists of asymmetrical coupled-inductor switched-capacitor (ASCLSC) cells to attain high gain. ASCLSC cell contains two diodes and two capacitors integrated with the coupled inductor winding. A passive clamp circuit is formed to recycle the leakage energy. The leakage energy is stored in the clamp capacitor C_1, and then shifted to switched capacitor C_{S1} to lift the output voltage further. The switched capacitors, C_{S1} and C_{S2}, are employed in series with the secondary winding. The switched capacitors are charged and discharged by the secondary windings, during on and off state of the switch, respectively. The voltages of these capacitors depend on the winding turn ratio. Thus, the switch voltage stress can be significantly minimised.

2.1 Steady-state analysis

The steady-state operation characteristics are analysed based on the following assumptions:

(i) The coupled inductor comprises of an ideal transformer with a leakage inductance L_k, and magnetising inductance L_m. The turns ratio is $n = N_2/N_1$, and the coupling coefficient is defined as $k = L_m/(L_m + L_k)$.
(ii) The diodes and active switch are considered ideal.
(iii) The value of capacitors is considered large; thus, their voltages are constant.

In a steady-state under the continuous current mode (CCM), there are five modes, which are illustrated by the critical waveforms in Fig. 3.

Mode I $t \in [t_0, t_1]$: The converter equivalent circuit and operation are shown in Fig. 4. At $t = t_0$, the switch is turned on, as shown in waveforms depicted in Fig. 3. The current passing through secondary winding, i_s, decreases linearly. The current in the leakage inductor increases linearly. Diodes D_1, D_2, D_4, D_0 are reverse biased, and D_3 is forward biased. Diode D_3 turns off at a low rate of change of current due to the leakage inductance. This mode ends with the forward biasing status of diodes D_2 and D_4.

Mode II $t \in [t_1, t_2]$: The secondary winding current is negative, as shown in Fig. 3. Diodes D_1, D_3, and D_0 are reverse biased, and diodes D_2 and D_4 are forward biased. The clamp capacitor C_1

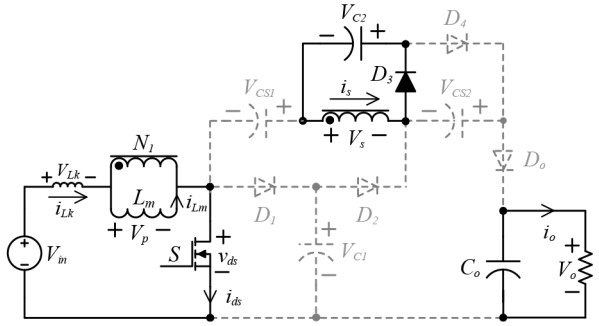

Fig. 4 *Mode I circuit operation*

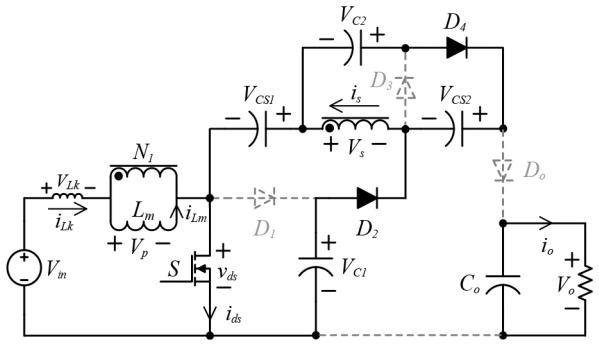

Fig. 5 *Mode II circuit operation*

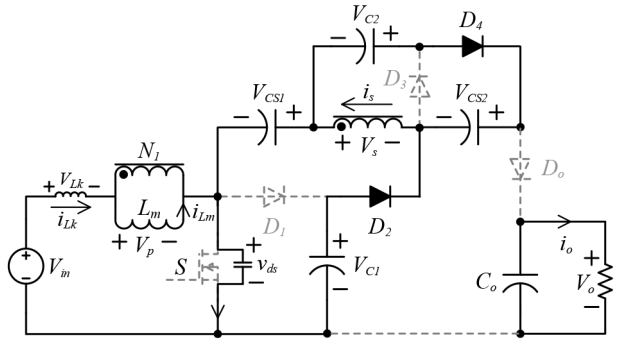

Fig. 6 *Mode III circuit operation*

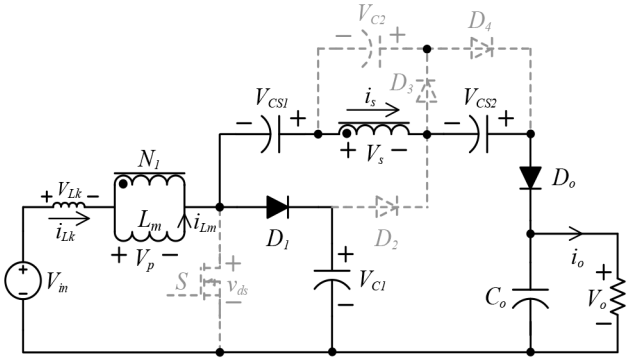

Fig. 7 *Mode IV circuit operation*

transfer its stored leakage energy to the switched capacitor C_{S1}. Similarly, C_2 transfers energy to C_{S2} through the coupled inductor.

The circuit operation is illustrated in Fig. 5. The DC power source charges the leakage inductor L_k and magnetising inductor L_m. The switched capacitors C_{S1} and C_{S2} are getting charged by the secondary winding voltage V_s.

The output capacitor C_o drives the load. The voltage across capacitors C_{S1} and C_{S2} based on Fig. 5 can be expressed as

$$V_{CS1} = V_{C1} + V_s^{II} \tag{1}$$

$$V_{CS2} = V_{C2} + V_s^{II} \tag{2}$$

where V_s^{II} denotes the voltage across the secondary winding in Mode II.

Mode III $t \in [t_2, t_3]$*:* In this mode, the switch is opened. The secondary side current i_s is increasing linearly. Diodes D_1, D_3 and D_0 are reverse biased, and diodes D_2 and D_4 are forward biased, as depicted in Fig. 6. The switch junction capacitance absorbs the leakage energy. The input source voltage charges C_{S1} and C_{S2}. This mode ends with the forward biasing status of diode D_1.

Mode IV $t \in [t_3, t_4]$: Diodes D_1 and D_0 are forward biased, and D_2, D_3 and D_4 are reverse biased, as illustrated in Fig. 7. The switch voltage is fixed at V_{c1}. The clamp capacitor absorbs the energy from the leakage inductor. The switched capacitors C_{S1} and C_{S2} are discharged. This mode ends with the reverse biasing status of diode D_1. In this mode, all leakage energy transfers to C_1. The voltage across the capacitor C_1 and the output voltage can be written as

$$V_{C1} = V_{in} - V_{Lk}^{IV} - V_p^{IV} \tag{3}$$

$$V_o = V_{C1} + V_{CS1} + V_{CS2} - V_s^{IV} \tag{4}$$

where V_p^{IV} and V_s^{IV} denote the voltage across the primary and secondary windings in Mode IV, respectively.

Mode V $t \in [t_4, t_5]$*:* During this mode, diodes D_3 and D_0 are forward biased, and D_1, D_2 and D_4 are reverse biased, as demonstrated in Fig. 8. The capacitor C_2 is getting charged by the magnetising energy through the CL. Switched capacitors C_{S1} and C_{S2} continue to transfer their energies to the output port. This mode is switched to Mode I when the switch is turned on. The voltage across capacitor C_2 can be expressed as

$$V_{C2} = -V_s^V \tag{5}$$

where V_s^V denotes the voltage across the secondary winding in Mode V.

The volt-second balance (VSB) principle on the magnetising and leakage inductors results in the voltage across capacitors and the transfer relationship, which are expressed by

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{1-D}\left[\dfrac{2+D(k-1)+nD(1-k)}{2}\right] \\ V_{CS1} = \dfrac{[2+D(n-1)+k(2n+D-3nD)]}{2(1-D)}V_{in} \\ V_{C2} = \dfrac{nDk}{1-D}V_{in} \\ V_{CS2} = \dfrac{nk}{1-D}V_{in} \end{cases} \tag{6}$$

$$M_{Ideal} = \frac{V_o}{V_{in}} = \frac{2+2nk}{1-D}\left[1 + \frac{nD(1-k)+D(k-1)}{2+2nk}\right] \tag{7}$$

The voltage conversion ratio depends on the duty ratio, coupling coefficient, and turns ratio. The voltage conversion gain at $n = 2$ is illustrated in Fig. 9. It depicts that conversion gain mainly varies with the duty cycle. The coupling coefficient has a negligible effect on the gain.

The actual voltage gain with the parasitic elements is computed and compared with practical voltage gain. The equivalent circuit of the proposed converter with parasitic is illustrated in Fig. 10.

By applying the VSB on the coupled inductor, the voltage conversion gain is formulated by

$$M_{Real} = \frac{2+2n}{1-D} \times \frac{1}{1+A+B+C+E}$$

where

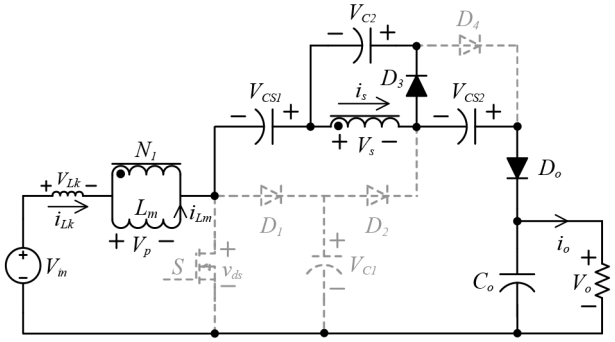

Fig. 8 *Mode V circuit operation*

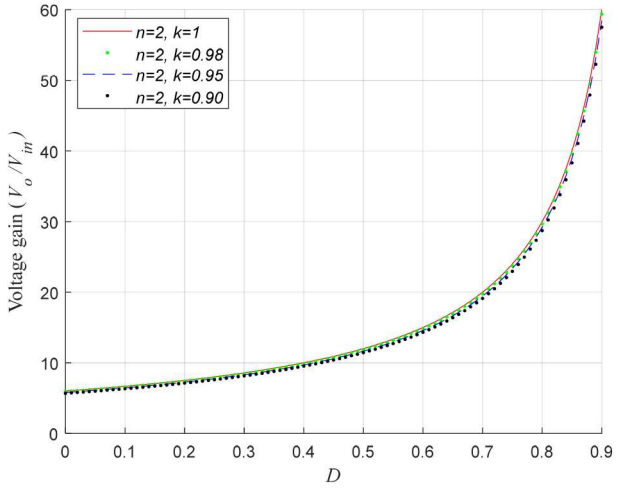

Fig. 9 *Voltage gain characteristics of the proposed converter*

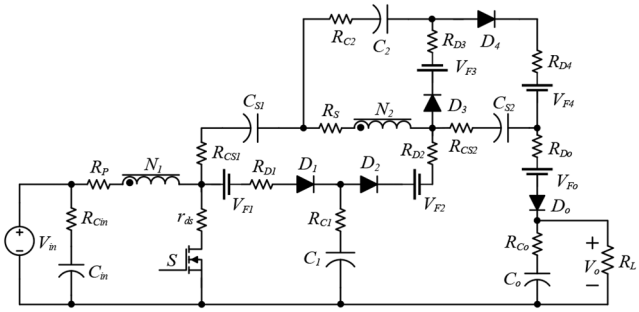

Fig. 10 *Proposed converter equivalent circuit with parasitic*

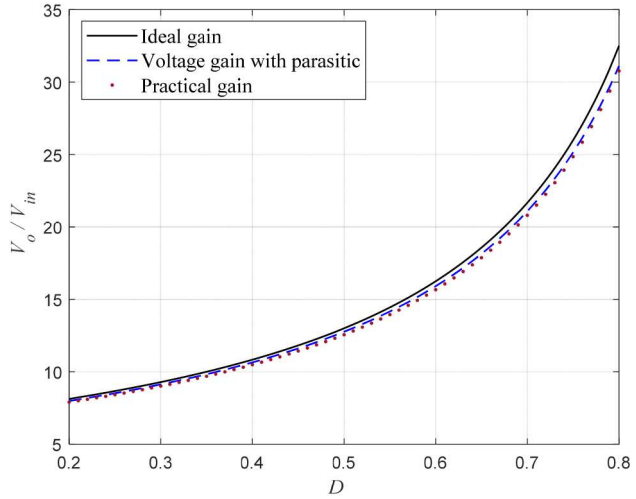

Fig. 11 *Comparison of theoretical and practical voltage gain*

$$A = \frac{D(1+2n+D)^2 r_{DS} + (2+2n)^2 D^2 R_P}{D^2(1-D)^2 R_L}$$

$$B = \frac{(1+n)DR_{D1} + (2+nD-D)R_{C1}}{2D(1-D)R_L}$$

$$C = \frac{1}{D(1-D)R_L}[(1-D)(R_{D2}+R_{D4}) + 4R_S + R_{C2} + R_{CS1} + R_{CS2} + D^2 R_{Co} + D(R_{D3}+R_{Do})] \quad (8)$$

$$E = \frac{(1-D)(V_{F1}+V_{F2}+V_{F3}+V_{F4}+V_{Fo})}{(2+2n)V_{in}}$$

The ideal gain, actual theoretical voltage gain, and practical voltage gain are illustrated in Fig. 11. The parasitic components degrade the voltage gain. The theoretical voltage gain including parasitic is close to practical gain with minimal difference.

2.2 Performance comparison

A comparison is performed to compare the performance with other topologies in this section. The high step-up ability of the proposed topology, along with other topologies, for the similar voltage conditions under $n = 2$ is demonstrated in Fig. 12. A comprehensive comparison including viewpoints of the number of elements, step-up capability, and peak efficiency is tabulated in Table 1. The step-up conversion capability of the proposed configuration is relatively higher than the other converters, except [18]. The converter in [18] has a higher voltage gain for the duty cycle of more than 0.5 but lower for duty cycle less than 0.5. The component count of the proposed topology is lower than [18].

2.3 Current and voltage stress on devices

The average diode current is determined by ampere-second balance (ISB) principle, which results I_o. Therefore, the maximum current in diodes can be obtained as

$$i_{D2} = i_{D4} = \frac{2I_o}{D} \quad (9)$$

$$i_{D3} = i_{Do} = \frac{2I_o}{1-D} \quad (10)$$

$$i_{ds} = \frac{(2n+2D)I_o}{D(1-D)} \quad (11)$$

$$i_{D1} = \frac{2nI_o}{D(1-D)} \quad (12)$$

The voltage stresses on diodes and switch are given by

$$v_{ds} = V_{D1} = \frac{V_o}{2+2n} \quad (13)$$

$$V_{D2} = V_{Do} = \frac{1+n}{2+2n}V_o \quad (14)$$

$$V_{D3} = V_{D4} = \frac{n}{2+2n}V_o \quad (15)$$

The switch voltage stress against the duty ratio is depicted in Fig. 13. The proposed converter shows a low active switch voltage stress.

The switch voltage stress against the duty ratio is depicted in Fig. 13. The proposed converter shows a low active switch voltage stress. Furthermore, the voltage stress remains constant with the change in duty ratio. This salient feature enables designers to utilise low-voltage-rating switches with low on-state resistance $r_{ds(on)}$ to decrease the power loss. The diodes voltage stresses are also constant against the duty cycle, as indicated in (13)–(15).

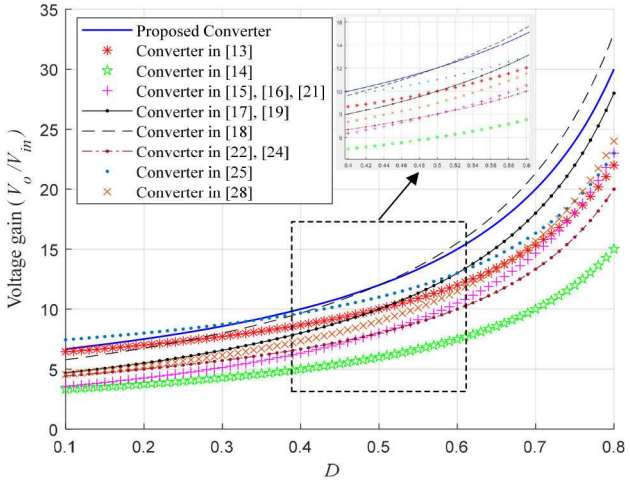

Fig. 12 *Ideal voltage gain comparison in CCM operation at* $n = 2$ *and* $k = 1$

Table 1 Comparison with other converters

Converters	No. of components (switch/core/ windings/ diodes/ capacitors)	Ideal voltage gain	Reported peak efficiency, %
proposed converter	1/1/2/5/5	$\frac{2+2n}{1-D}$	96.72
[13]	1/1/2/4/4	$\frac{2+2n-nD}{1-D}$	96.70
[14]	2/1/2/2/5	$\frac{1+n}{1-D}$	96.60
[15, 16]	1/1/2/4/4	$\frac{1+n+nD}{1-D}$	95.88, 95.50
[17, 19]	1/1/2/4/4	$\frac{2+n+nD}{1-D}$	97.10, 96.90
[18]	1/1/2/6/6	$\frac{1+2n+nD}{1-D}$	95.31
[21]	1/2/2/4/5	$\frac{1+(1+D)n}{1-D}$	97.20
[22, 24]	2/1/2/2/3, 1/1/2/3/3	$\frac{2+n}{1-D}$	93.9093.50
[25]	1/1/2/4/4	$\frac{3+2n-nD-D}{1-D}$	93.70
[28]	1/2/2/4/5	$\frac{2+n+D}{1-D}$	94.00

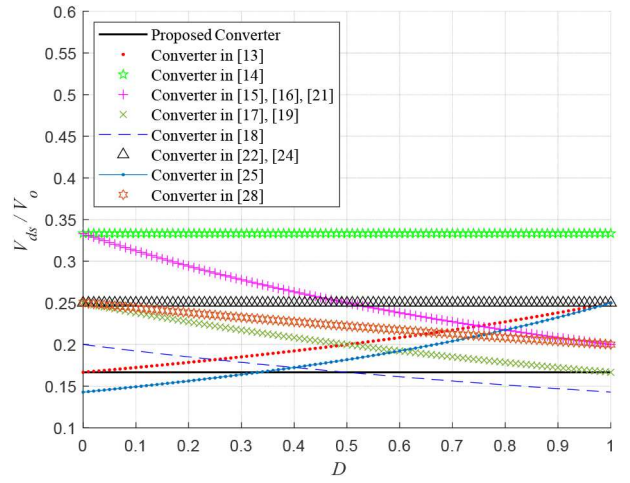

Fig. 13 *Comparison of voltage stress across the active switch under* $n = 2$

2.4 Voltage stress on capacitors

The voltage stresses on capacitors are given as

$$V_{C1} = \frac{V_o}{2+2n} \tag{16}$$

$$V_{CS1} = \frac{1+n-nD}{2+2n}V_o \tag{17}$$

$$V_{C2} = \frac{nD}{2+2n}V_o \tag{18}$$

$$V_{CS2} = \frac{n}{2+2n}V_o \tag{19}$$

A comparison of maximum voltage stress on the capacitor with other high step-up converters is depicted in Fig. 14. The voltage stress analysis reveals that the proposed converter has comparatively lower maximum voltage stress, except [15, 16]. The converters proposed in [15, 16] show lower voltage conversion gain, and lower conversion efficiency. Furthermore, the voltage stress on the active switch is high, as shown in Fig. 13.

2.5 Generalised structure for realisation of ultra-high gain

The architecture of the proposed configuration can be extended by employing more ASCLSC cells for realising an ultra-high gain. The general structure of the proposed configuration with $m-1$ cells is depicted in Fig. 15*a*. Switched capacitors, $C_{S1}, \ldots, C_{Sm}$ are implemented in series with the secondary winding. Switched capacitors are charged and discharged by the respective secondary windings $N_2, \ldots, N_m$ during turned on and off states of the switch, respectively. Their stored energies are shifted to the load and capacitor C_o.

The equivalent circuit during the switch on interval is displayed in Fig. 15*b*. The capacitors' voltage can be described as

$$\begin{cases} V_{CS1} = V_{C1} + n_1 V_{in} \\ V_{CSi} = V_{Ci} + n_{(i-1)}V_{in} \quad i = 2, 3, \ldots, m \end{cases} \tag{20}$$

The turned off corresponding state circuit is displayed in Fig. 15*c*. Similarly, the following voltage can be described as:

$$\begin{cases} V_{C1} = V_{in} - V_p^{II} \\ V_{Ci} = -n_{(i-1)}(V_{in} - V_{C1}) \quad i = 2, 3, \ldots, m \end{cases} \tag{21}$$

The VSB principle results in the following equations:

$$\begin{cases} V_{C1} = \frac{1}{1-D}V_{in} \\ V_{Ci} = n_{(i-1)}\frac{D}{1-D}V_{in} \quad i = 2, 3, \ldots, m \end{cases} \tag{22}$$

$$\begin{cases} V_{CS1} = \frac{1+n_1(1-D)}{1-D}V_{in} \\ V_{CSi} = \frac{n_{(i-1)}}{1-D}V_{in} \quad i = 2, 3, \ldots, m \end{cases} \tag{23}$$

The output voltage during the off period of the switch can be written as

$$V_0 = \sum_{j=1}^{m} V_{Cj} + \sum_{k=1}^{m} V_{CSk} \tag{24}$$

By putting (22) and (23) into (24), the relationship between input and output voltages is given as

$$\frac{V_o}{V_{in}} = \frac{1}{1-D}\left[(2+n_1-n_1D) + (1+D)\sum_{i=1}^{m-1} n_{(i)}\right] \tag{25}$$

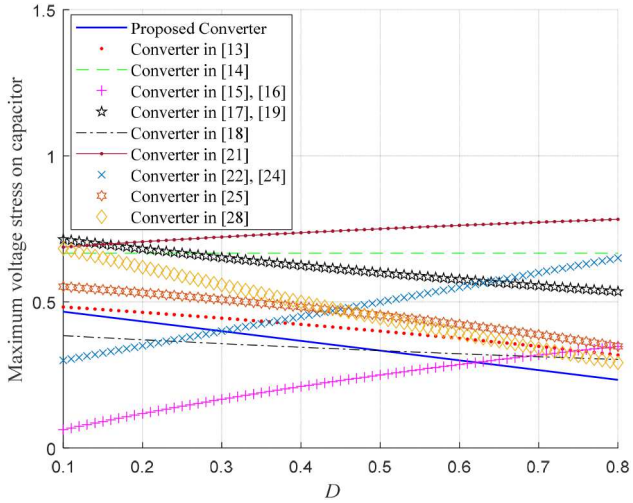

Fig. 14 *Comparison of maximum voltage stress on the capacitor under* $n = 2$

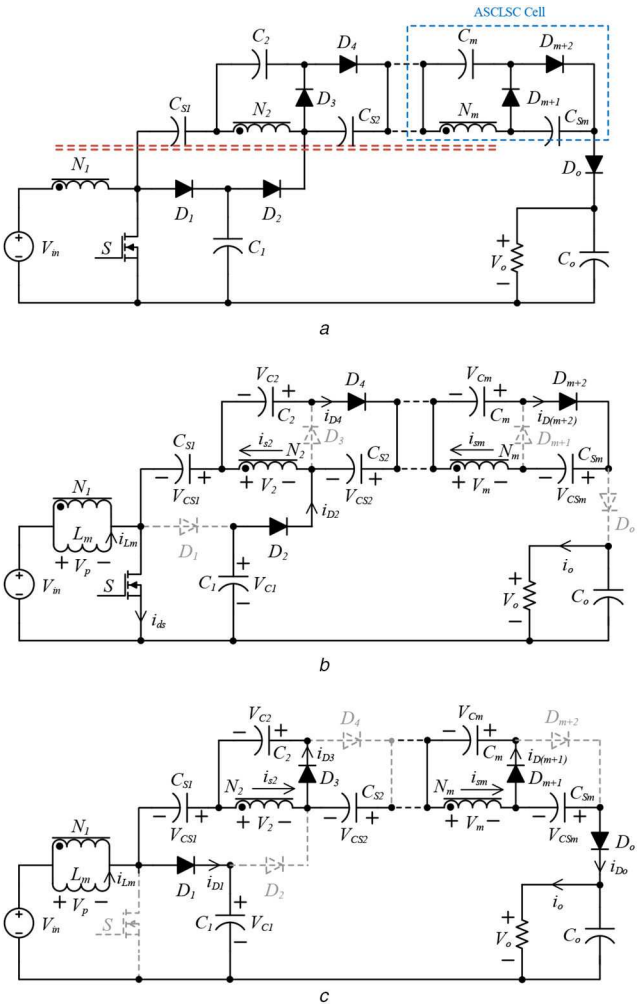

Fig. 15 *Proposed high gain converter*
(a) Schematic, ***(b)*** ON state, ***(c)*** OFF state

The number of ASCLSC cells utilised in the proposed converter are $(m-1)$. For a particular case, when the number of turns ratios are the same for the coupled inductor, i.e. $n = N_2/N_1 = N_3/N_1, \ldots, = N_m/N_1$, the voltage conversion ratio can be simplified as

$$\frac{V_o}{V_{in}} = \frac{2 + n(2 + (m-2)(1+D))}{1-D} \tag{26}$$

The voltage gain characteristics are demonstrated in Fig. 16. The proposed topology can attain ultra-large step-up voltage conversion gain by employing multiple ASCLSC cells. The duty cycle is a crucial parameter to control the output voltage. The turns ratio can also adjust the gain. For practical application, this allows designers to assign the duty ratio within the desirable range and to avoid extremely modulation indices.

2.6 Efficiency analysis

According to Fig. 10, the conduction losses in the parasitic of passive and active components can be calculated by RMS current. The ripple in the capacitors voltage and inductor current is neglected to simplify the mathematical analysis. The average current in each diode is equal to the output current. Thus, the forward voltage drop of the respective diode is multiplied with the average current to compute the diode loss due to forward voltage drop. The RMS current in different converter's components is calculated with the help of theoretical plots in Fig. 3 and expressed as

$$I_{Lk(\text{rms})} = \frac{2I_o}{1-D}\sqrt{\frac{n^2 + 2nD + D}{D}} \tag{27}$$

$$I_{s(\text{rms})} = \frac{2I_o}{\sqrt{D(1-D)}} \tag{28}$$

$$I_{ds(\text{rms})} = \frac{1 + 2n + D}{D(1-D)} I_o\sqrt{D} \tag{29}$$

$$I_{D1(\text{rms})} = I_o\sqrt{\frac{1+n}{1-D}} \tag{30}$$

$$I_{D2(\text{rms})} = I_{D4(\text{rms})} = \frac{I_o}{\sqrt{D}} \tag{31}$$

$$I_{D3(\text{rms})} = I_{Do(\text{rms})} = \frac{I_o}{\sqrt{1-D}} \tag{32}$$

$$I_{Cin(\text{rms})} = \frac{2nI_o}{\sqrt{D(1-D)}} \tag{33}$$

$$I_{C1(\text{rms})} = I_o\sqrt{\frac{1+nD}{D(1-D)}} \tag{34}$$

$$I_{C2(\text{rms})} = I_{CS1(\text{rms})} = I_{CS2(\text{rms})} = \frac{I_o}{\sqrt{D(1-D)}} \tag{35}$$

$$I_{Co(\text{rms})} = I_o\sqrt{\frac{D}{1-D}} \tag{36}$$

According to Faraday's law, the peak flux density in the coupled inductor is obtained as

$$\Delta B = \frac{D(1-D)V_o}{(2+2n)N_1A_cf_s} \tag{37}$$

where A_c represents the cross-sectional area of the core, and N_1 is the number of turns on the primary winding. After calculating the peak flux density, the core losses in the coupled inductor are estimated by the ferrite curve in the datasheet. The typical curve provides the core loss density for a given peak flux density at different frequencies. Thus, the core losses can be estimated by

$$P_{\text{core}} = [\text{core loss density}] \times V_e \tag{38}$$

where V_e denotes the volume of the core.

The switching loss in the switch is predicted by

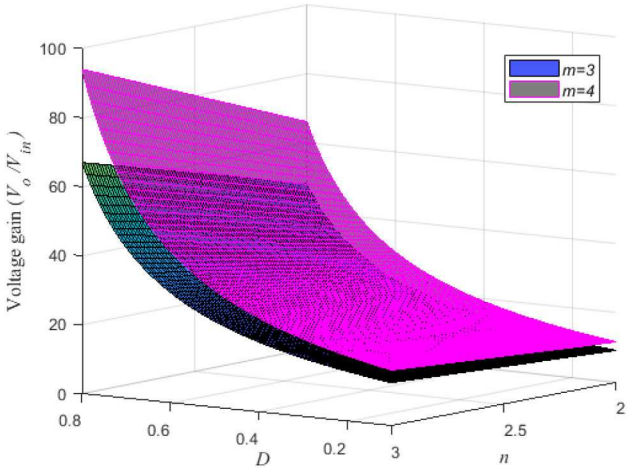

Fig. 16 *Voltage conversion gain under different ASCLSC cells*

Table 2 PV module parameters

Parameters	Nominal values
maximum power – P_{max}	300 W
MPP voltage – V_{mpp}	30 V
MPP current – I_{mpp}	10 A
open-circuit voltage – V_{oc}	38.6 V
short-circuit current – I_{sc}	10.6 A

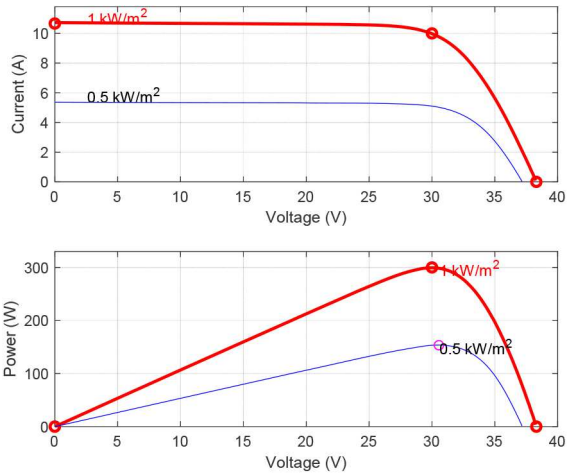

Fig. 17 *I–V and P–V curves at different irradiance*

$$P_{sw\_loss} = \frac{1}{2}V_{ds}[i_{ds-min} \times t_{on} + i_{ds-max} \times t_{off}]f_s \quad (39)$$

where t_{on} and t_{off} are the rise and fall time of the switch, respectively. The overall conversion efficiency includes the conduction, core and switching losses, which is formulated by

$$\eta = \frac{P_o}{P_{in}} = \frac{1}{1 + A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 R_L}$$

where

$$A_1 = \frac{4R_S + 4n^2R_{Cin} + R_{C2} + R_{CS1} + R_{CS2}}{D(1-D)R_L}$$

$$A_2 = \frac{D(1+n)R_{D1} + (1+nD)R_{C1} + 2(1-D)(R_{D2} + R_{D4})}{2D(1-D)R_L}$$

$$A_3 = \frac{(1+2n+D)^2 Dr_{DS} + 4(n^2 + 2nD + D)DR_P}{D^2(1-D)^2R_L}$$

$$A_4 = \frac{(V_{F1} + V_{F2} + V_{F3} + V_{F4} + V_{Fo})}{V_o}$$

$$A_5 = \frac{R_{D3} + R_{Do} + DR_{Co}}{(1-D)R_L}$$

$$A_6 = \frac{(n+D)}{D(2+2n)(1-D)}\left[\left(1 - \frac{R_L D^2(1-D)^2}{2(2+2n)(n+D)L_m f_s}\right)t_{on} + t_{off}\right]f_s$$

$$A_7 = \frac{P_{core}}{V_o^2} \quad (40)$$

2.7 MPPT operation and design guidelines

The proposed topology is specified for a module integrated PV system in DC nanogrid. The objective is to inject maximum power into the grid at any instant. Therefore, the MPPT operation is essential and needs to be validated for maximum energy harvesting from the PV module. Different MPPT algorithms have been proposed in the literature to track maximum power point (MPP) of PV to inject maximum power into DC gird. The MPPT is not the technical contribution in this research; therefore, the regular perturb and observe (P&O) algorithm is employed for the implementation. The parameters of the PV module are listed in Table 2. The *I–V* and *P–V* curves at different insulation levels are illustrated in Fig. 17. The input PV voltage and current at MPP under irradiance 1000 W/m^2 are 30 V and 10 A, respectively. The output voltage is regulated at 380 V, as it is the standard DC bus voltage value in DC nanogrid.

The switching frequency is a vital circuit parameter. Typically, a lower switching frequency results in low switching loss but sparse power density. The higher switching frequency yields better power density. The proposed topology shows low switch voltage stress, which results in low switching losses. Thus, switching frequency can be pushed higher. The switching frequency is specified as 100 kHz.

The coupled inductor is a critical component of the proposed converter. The turn ratio of the coupled inductor is obtained as

$$n = \frac{V_o(1-D) - 2V_{in}}{2V_{in}} \quad (41)$$

The nominal duty ratio is selected as 0.5. The design of coupled inductor consists of three parameters: the magnetic core; wire selection; and the value of magnetising inductance. The choice of the magnetic core is crucial to keep the core losses low in the coupled inductor. For high-frequency operation, the ferrite magnetic core is preferred due to comparatively low losses at high frequencies. A ferrite core is available in different geometries such as E, U, RS and pot cores. In the proposed converter, the ETD 44 ferrite core is used. The core losses can be estimated by (37) and (38).

The selection of magnetic wire is important to keep the ac and dc losses to the low level. For high-frequency operation, Litz wire is commonly used to constrain losses, from skin effect and proximity effect, low in the converter. The prototype utilises standard magnet wire for validation but assures high efficiency. Litz wire can be used to enhance efficiency further. The wire sizing is based on the root mean square (RMS) current, which is expressed in (27) and (28). Therefore, the copper losses in the coupled inductor can be calculated as

$$P_{copper} = I^2_{Lk(rms)} \times R_P + I^2_{s(rms)} \times R_s \quad (42)$$

Table 3 Key parameters and components description

Description	Parameters	Nominal values
input/output voltage	V_{in}/V_o	25–35/380 V
coupled inductor	ETD-44	Ferrite Core, N97
magnetising inductance	L_m	70 μH
leakage inductance	L_k	0.89 μH
turns ratio	$n = N_1:N_2$	10:23
wire cross-sectional area	primary/secondary	5.26/3.31 mm^2
switching frequency	f_s	100 kHz
tracking frequency	f_{mppt}	10 Hz
switch – MOSFET	S	IPB027N10N3 (100 V)
diode	D_1	STPS30SM100SG-TR
diodes	D_3, D_4	TST40L200CW
diodes	D_2, D_o	MBR40250TG
capacitors	C_1, C_2, C_{S1}, C_{S2}	40 μF
input/output capacitor	C_{in}, C_o	220 μF

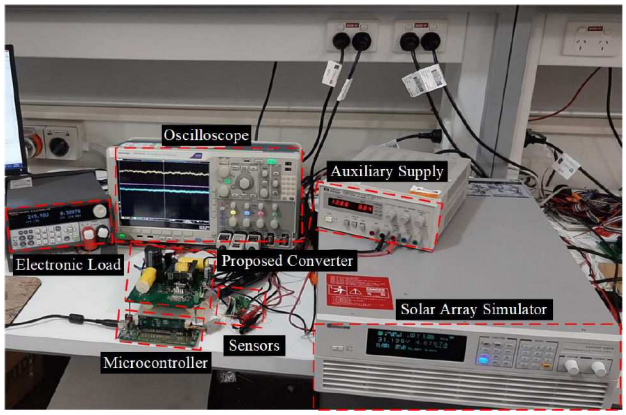

Fig. 18 *Experimental setup in the laboratory*

The magnetising inductance is designed to assure continuous conduction mode (CCM) operation. The boundary-value of magnetising inductance is derived and expressed as

$$L_m \geq \frac{D(1-D)^2(1+n)R}{(2+2n)^3 f_s} \tag{43}$$

The high value of magnetising inductance also results in low ripple current. However, it increases the size and cost of the coupled inductor. Moreover, it also increases the leakage inductance. Therefore, by considering the trade-off, the optimum value is obtained, which is listed in Table 3.

The semiconductor devices are chosen according to the voltage and current stresses from (9) to (15). The selection of capacitors is based on the capacitor's voltage stress and ripple in the capacitor voltages. The voltages across capacitors are calculated by (16)–(19). The capacitance value is determined to bound the ripple to an appropriate domain. Thus, the capacitance is obtained as

$$C \geq \frac{P_{max}}{V_C \Delta V_C f_s} \tag{44}$$

where ΔV_C represents ripple in the capacitors' voltage. The input PV side capacitor is required to regulate the input voltage to ensure MPPT. The value of the capacitor is calculated to allow ripple in the input PV voltage within an acceptable range. Therefore, it is calculated as

$$C_{in} \geq \frac{2(n+D)I_o}{8\Delta V_{in} f_s D(1-D)} \tag{45}$$

where ΔV_{in} represents ripple in the input PV voltage.

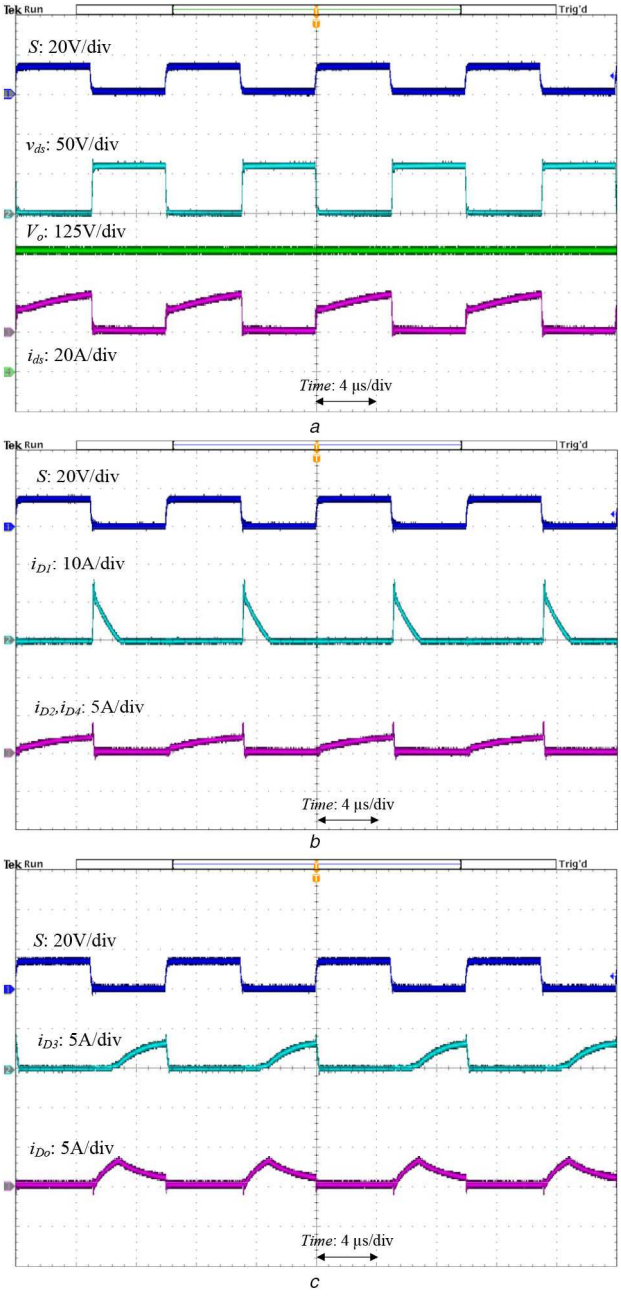

Fig. 19 *Experimental results under full load*

3 Experimental evaluation

A hardware prototype is constructed and tested to validate the MPPT performance and theoretical analysis. It is rated at 300 W with the switching frequency at 100 kHz. Due to the advantage of high conversion gain, as expressed in (7), the winding turns ratio of the CL is designed low as $n = 2.25$, even though the rated voltage conversion ratio is from 30 to 380 V. The components are listed in Table 3. A picture of the experimental setup is shown in Fig. 18. The solar array simulator (62050H-600S) is used to emulate the PV operation. The simulator can be programmed, and the desired parameters such as MPP voltage and current can be configured. The electronic load is used to model a constant dc bus voltage. The microcontroller (TMS320F28035) is utilised for MPPT implementation. Based on the maximum power rating, the recorded waveforms are illustrated in Fig. 19. The switching function S, switch current and voltage, and output voltage are displayed in Fig. 19*a*. The switch voltage waveform shows consistency with (13). The voltage across the switch is clamped at 62 V, which is 15% of the output voltage of 380 V, which proves the anticipated performance. A minor spike can be seen in the waveform of v_{ds} at the turn off instant due to the leakage energy. However, the leakage

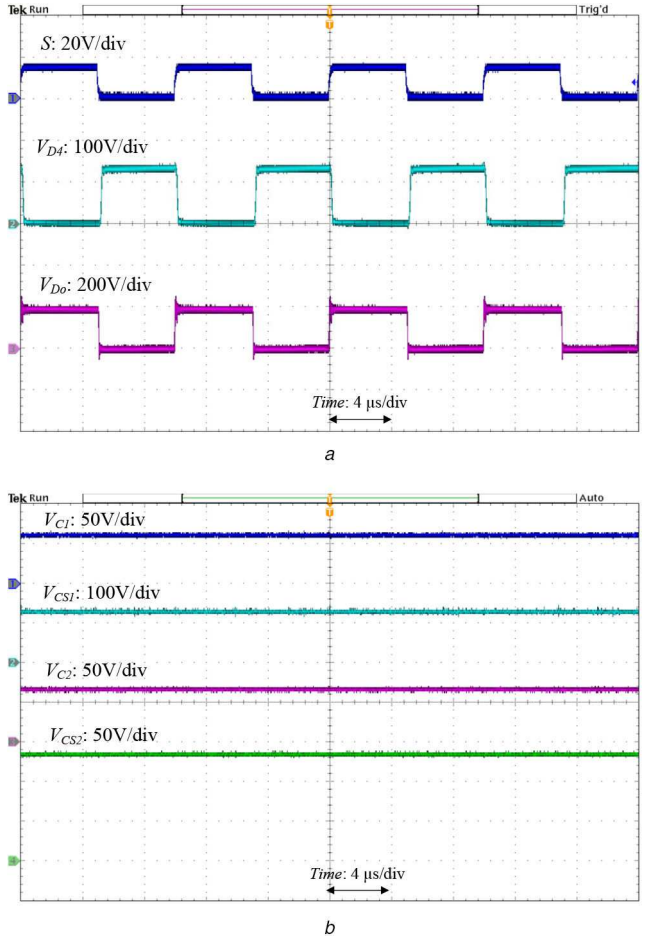

Fig. 20 *Experimental waveforms of the voltage across diodes and capacitors*

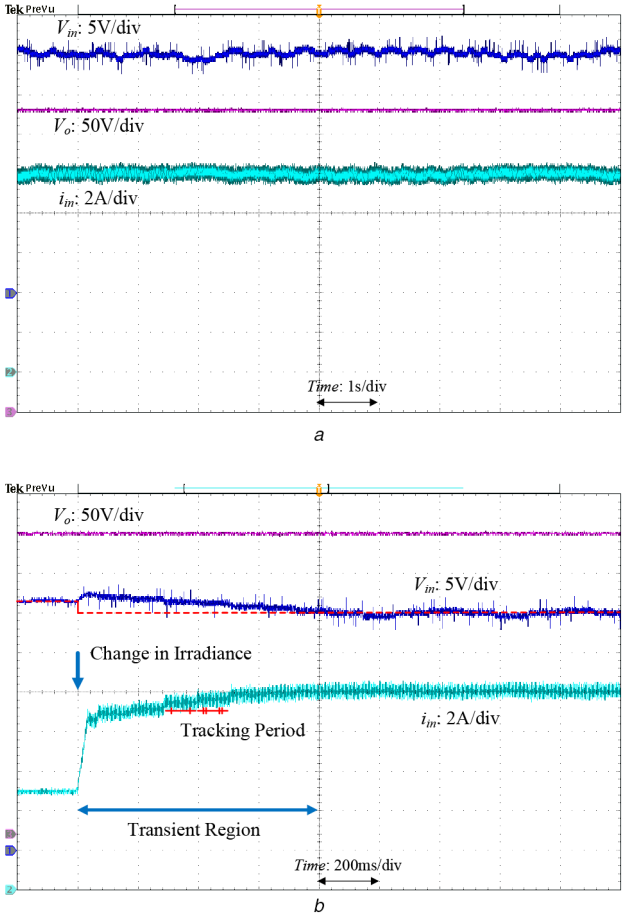

Fig. 21 *PV input voltage and current, and output voltage with MPPT operation*

(a) Constant irradiance: 1000 W/m^2, ***(b)*** Irradiance changed from 500 to 1000 W/m^2

energy is mostly absorbed by capacitor C_1. The stored energy is then moved to the output through the clamping path. This proves the utilisation of the MOSFET model of IPB027N10N3, which is rated for 100 V. The output voltage is consistent with the theoretical expectation. The current flowing through diodes D_1, D_2, D_4 are depicted in Fig. 19*b*. The current waveforms of output diode and diode D_3 are displayed in Fig. 19*c*. The diode current waveforms show consistency with theoretical waveforms. The voltage across diodes D_4 and D_o are shown in Fig. 20*a*. The voltage waveforms of capacitors are demonstrated in Fig. 20*b*. The measured waveforms satisfy the expectation in (16)–(19). In general, the experimental waveforms are analogous to the theoretical results and substantiate the theoretical analysis. The MPPT operation is based on the tracking frequency, which is demonstrated in Fig. 21. The MPPT controller tracking frequency f_{mppt}, also called perturbation frequency, is set 10 Hz. The PV input voltage and current, and output voltage waveforms at constant irradiance, 1000 W/m^2, are shown in Fig. 21*a*. The input voltage is regulated at MPP, i.e. 30 V and the input current is 10 A, which corresponds to MPP, as portrayed in PV module *I*–*V* and *P*–*V* characteristics in Fig. 17. Thus, the maximum power is extracted from the PV module. One drawback of the P&O algorithm is steady-state oscillation around MPP, as shown in Fig. 21*a*. The smaller step size improves the performance in steady-state as the oscillation becomes close to MPP, resulting in a smaller ripple in PV voltage and current; however, the tracking speed becomes slow. There is a trade-off between accuracy and tracking speed. The step size in terms of duty cycle perturbation is chosen as 0.005 in the proposed design.

Fig. 21*a* shows that ripple in the PV module voltage and current is small, less than 5%, in steady-state due to relatively low step size. There are many improved algorithms proposed in the literature, such as modified P&O and Incremental Conductance, which can be employed to improve the MPPT performance further [31, 32].

As the PV power changes with insolation; therefore, the MPPT operation at different insolation is shown in Fig. 21*b*. The converter is operating at the MPP and extracting 150 W power under an insolation level of 500 W/m^2. The PV module voltage is regulated at 31.2 V, which corresponds to MPP at 500 W/m^2. The solar irradiance is changed from 500 to 1000 W/m^2. The MPPT algorithm tracks and regulates the PV module voltage at 30 V, which corresponds to new MPP at 1000 W/m^2, as indicated in Fig. 21*b*. The transient and steady-state operations are illustrated in Fig. 21*b* to demonstrate the MPPT performance under a change in irradiance. The controller is tracking MPP. The change in the PV module voltage at different irradiance level is small. The topology demonstrates the MPPT performance with the change in irradiance, which is expected in PV systems. A power loss analysis is carried out as in [8], and a model is made. The model identifies the losses in each component. The percentage distribution of losses of the proposed converter at rated power is depicted in Fig. 22. The switch contributes almost 20% of the power losses. The diodes and capacitors reveal comparatively low losses. The Litz wire can be used in future research to decreases the conduction losses in order to enhance efficiency further. The theoretical efficiency based on the efficiency analysis in (40) is plotted along with the experimental conversion efficiency, and shown in Fig. 23 with a wide range of load conditions. The evaluation shows that the peak efficiency is 96.7%, which is less than the peak theoretical efficiency (97.3%) that is obtained from the theoretical analysis in (40). The full load practical efficiency is 95.2%, and full load theoretical efficiency is 96.1%. Both efficiency curves follow the same fashion; however, the practical system displays lower efficiency than theoretical prediction due to miscellaneous losses such as PCB losses. The significant power variation can be expected since the alternative energy source, such as PV, shows

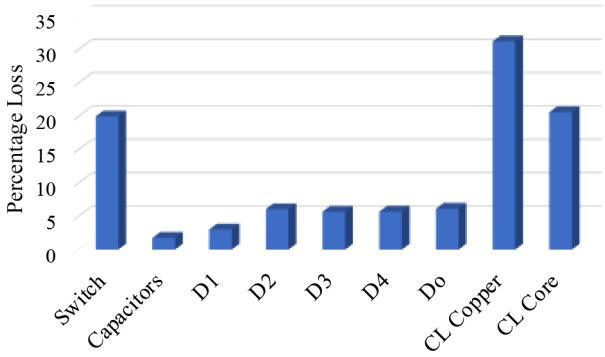

Fig. 22 *Theoretical percentage loss distribution at full power*

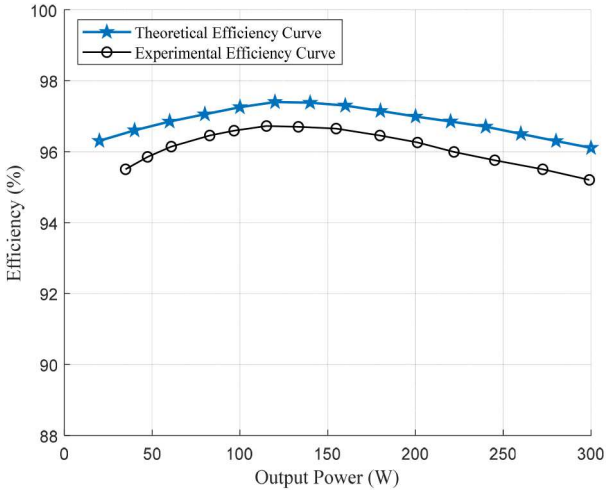

Fig. 23 *Comparison of theoretical and experimental conversion efficiencies*

intermittent nature in terms of power output. Therefore, the weighted efficiencies like the European Efficiency (EU) and California Energy Commission efficiency (CEC) are applied to evaluate the effectiveness of the proposed topology for PV applications. The EU efficiency is computed to be 96.3%, and the CEC is 96.1%.

4 Conclusion

This research has presented a new high gain DC–DC converter to interface solar PV sources into DC nanogrid. The topology utilises both switched capacitor and coupled inductor techniques to attain high efficiency and high voltage gain. The architecture of the proposed configuration is also extendable for an ultra-large conversion ratio of voltage. The switch voltage stress is significantly reduced, which is measured to be one-sixth of the output voltage. Moreover, the voltage stresses on devices are constant against the entire duty cycle operation. The theoretical analysis and design guidelines are elaborated in detail. Moreover, a comprehensive comparison is conducted to show the advantages of the proposed solution. The performance expectation of the proposed topology is substantiated experimentally in the laboratory. The converter demonstrates the MPPT capability for maximum energy harvesting. The efficiency curve shows a flat pattern with the improvement of low power levels. The converter prototype shows a peak efficiency of 96.7% and a weighted efficiency of 96.3% according to the EU standard. The proposed solution has demonstrated high efficiency, high voltage gain, and low and constant voltage stresses with the MPPT function.

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