Question:

Q1. (a) Suppose you have a new device, i.e., microprocessor 80XY, which is designed and operated similarly
to microprocessor 8086 architecture with only the following differences: [6]
• Number of address lines A0 - A11
• All the internal registers hold 8-bit data
I. How much is the total memory space available in the new device?
II. Explain in detail how the internal registers are going to be used in order to access any random physical
location of the new device? Create a general formulation in order to estimate the physical address in this
case.
III.Specify the range in hexadecimal scale for the physical address, segment part of the address, and offset
part of the address of the new device.
(b) Suppose, the above-mentioned new device, i.e., microprocessor 80XY, is connected with two external
identical memory devices, i.e., RAM 61XY, through a Primary Memory Decoder (PMDEC). The total number
of address lines and data lines available in the architecture of RAM 61XY are 10 (i.e., A1 - A10) and 8 (i.e., D0
– D7) respectively. Draw a neat connection diagram between 80XY and two RAM 61XY in order to map the
addresses. If the System Base Address (SBA) of RAM 61XY is 800 H, what will be the last even memory
address of RAM 61XY? Is it possible to map all the addresses of RAM 61XY with microprocessor 8086 with
given SBA? Justify your answer

Answer:

8oxy:

No. of Address lines: A0-A11

No. of Data lines: D0-D7

(a)

I → Total Memory Space available $= 2^{12} = 4KB$

II → To address any location, 11 bits are needed

All Internal registers have 8 bits only.

So, a similar segmentation approach, as that of 8086, can be followed.

Offset Reg. can have the lower 8bits

Base Reg. will be having 4 bits in upper nibble

For example:

Base Reg: | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Empty

Offset Reg: | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

Address is calculated as

1011 0000 0000 ← Hardwired 0000

1110 0011

1011 1110 0011 ⇒ 12 bits

Each segment can have 2^8 bytes = 256 Bytes memory

Total, 2^4 segments = 16 segments can be possible

(ii) →

Physical address range: ~~0000 H to FFFF H~~

000 H to FFF H

Segment Base: 00 H, 10 H, 20 H, 30 H, 40 H, 50 H,
60 H, 70 H, 80 H, 90 H, A0 H, B0 H,
C0 H, D0 H, E0 H, F0 H

Total = 16

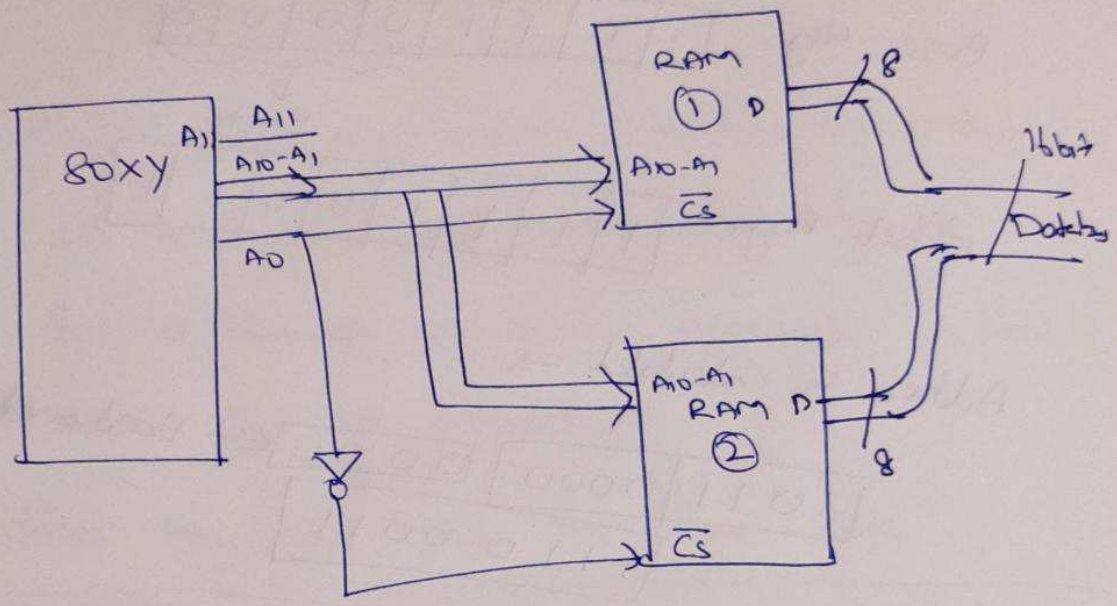
Offset address range: 00H to FF H

(b) Interfacing 80XY with 2 RAM 61XY.

Since Data bus is ~~only~~ ~~8 bits~~ 16-bits.

RAM 1 can supply even locations,

RAM 2 can supply odd locations.



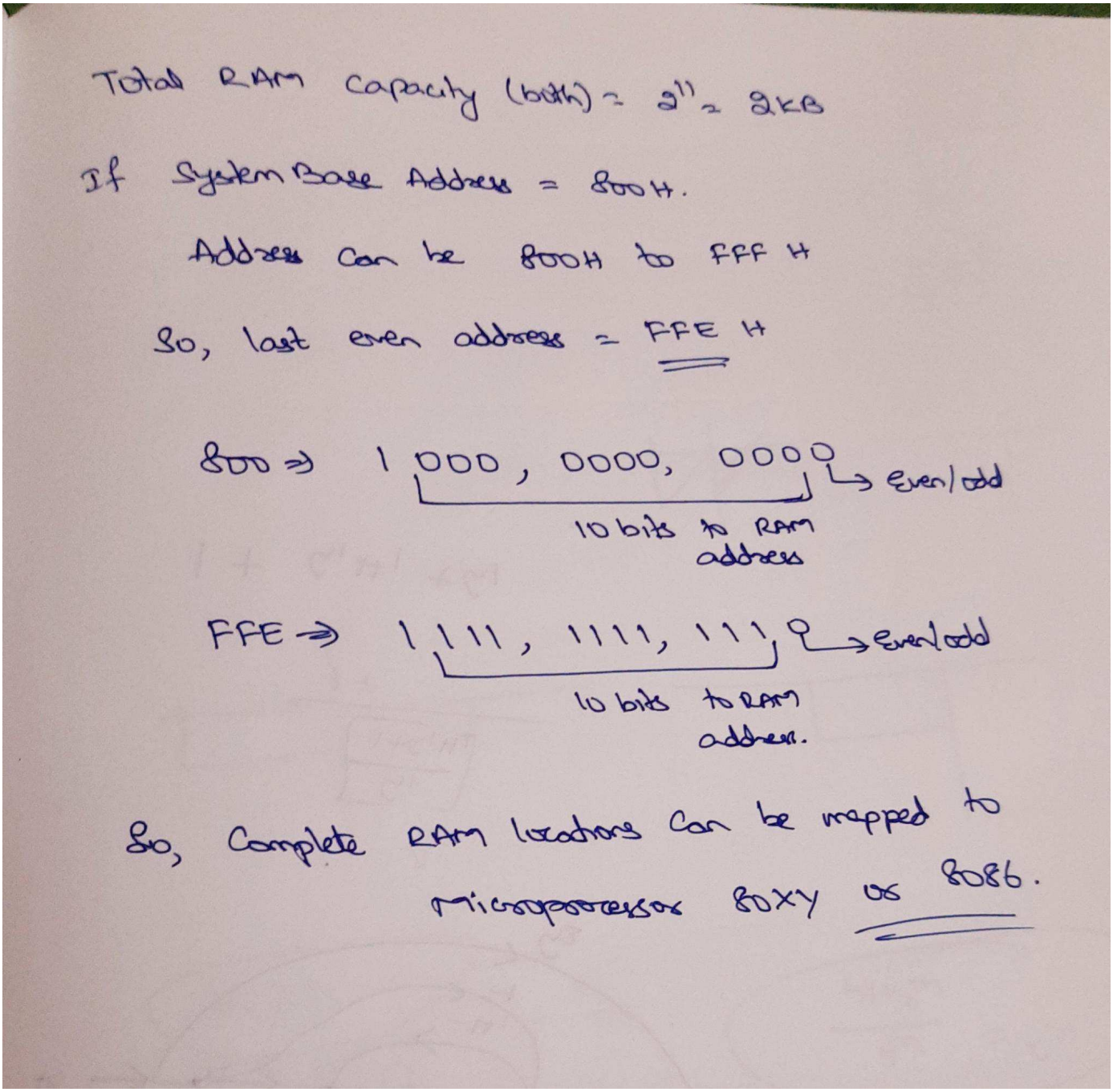
For RAM 1 (even locations), $\overline{\text{chipselect}} = A_0$

When $A_0 = 0$, RAM 1 is enabled

For RAM 2 (odd loc), $\overline{\text{chipselect}} = \overline{A_0}$

When $A_0 = 1$, RAM 2 is enabled.

A_{10}-A_1 bits correspond to address lines of both RAM.



All parts answered.