CSE 306

Computer Architecture Sessional

Assignment on Floating Point Adder

In this assignment, you are required to design a floating point adder circuit which takes two floating points as inputs and provides their sum, another floating point as output. Each floating point will be 16 bits long with following representation:

Sign **1 bit**	Exponent **4 bit**	Fraction **11 bit**

You have to implement your design in any simulator software of your choice. Please note that, if your chosen simulator does not provide support for 16 bit ALU, you can construct one by cascading number of smaller ALUs. Moreover, since construction of ALU is not major focus of this assignment, you can take help from the Internet or other sources (or even use someone else's implementation) for the 16 bit ALU part only. The rest of the circuit design and implementation must be done by yourselves.

The deadline for submission of this assignment is August 1, 2018. You have to submit the block diagram and software simulation of your design. For this assignment, you will work in a group of six persons (same as the group for assignment on ALU)