VALUES OF CONTROL BITS

~~~*~*~~~FETCH AND EXECUTION CYCLE~~~*~*~~~

--> NOP(00)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> return to the fetch cycle again.

--> IN(01)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> press enter to take input and load input to accumulator

--> OUT(02)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> load data from accumulator to output register

--> LDA address(03)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> load PC value to MAR
5. 5th cycle -> load RAM value to MDR & increase PC value 1
6. 6th cycle -> load MDR value to TMP_ADDRESS as lower 4 bit
7. 7th cycle -> load PC value to MAR
8. 8th cycle -> load RAM value to MDR & increase PC value 1
9. 9th cycle -> load MDR value to TMP_ADDRESS as higher 4 bit
10. 10th cycle -> load TMP_ADDRESS value to MAR
11. 11th cycle -> load RAM value to MDR
12 12th cycle -> load MDR data to accumulator
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--> STA address(04)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> load PC value to MAR
5. 5th cycle -> load RAM value to MDR & increase PC value 1
6. 6th cycle -> load MDR value to TMP_ADDRESS as lower 4 bit
7. 7th cycle -> load PC value to MAR
8. 8th cycle -> load RAM value to MDR & increase PC value 1
9. 9th cycle -> load MDR value to TMP_ADDRESS as higher 4 bit
10. 10th cycle -> load TMP_ADDRESS value to MAR
11. 11th cycle -> load accumulator to MDR
12 12th cycle -> load MDR data to RAM

--> MOV Acc, B(05)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> load data from register B to accumulator

--> MOV B, Acc(06)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> load data from accumulator to register B

--> MOV Acc, immediate(07)

---Fetch Cycle
1. 1st cycle -> load PC value to MAR
2. 2nd cycle -> load RAM value to MDR & INC PC
3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

---Execution Cycle
4. 4th cycle -> load PC value to MAR
5. 5th cycle -> load RAM value to MDR & INC PC
6. 6th cycle -> load MDR value to accumulator

--> ADD B(08)

---Fetch Cycle

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    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
    5. 5th cycle -> Load data from address bus to accumulator.

--> ADC B(09)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
    5. 5th cycle -> Load data from address bus to accumulator.

--> SUB B(10)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
    5. 5th cycle -> Load data from address bus to accumulator.

--> SBB B(11)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
    5. 5th cycle -> Load data from address bus to accumulator.

--> ADC immediate(12)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> load PC value to MAR
    5. 5th cycle -> load RAM value to MDR & increase PC value 1
    6. 6th cycle -> load MDR value to B register
    7. 7th cycle -> Enable ALU
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    8. 8th cycle -> Load data from address bus to accumulator

--> SBB address(13)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> load PC value to MAR
    5. 5th cycle -> load RAM value to MDR & increase PC value 1
    6. 6th cycle -> load MDR value to TMP_ADDRESS as lower 4 bit
    7. 7th cycle -> load PC value to MAR
    8. 8th cycle -> load RAM value to MDR & increase PC value 1
    9. 9th cycle -> load MDR value to TMP_ADDRESS as higher 4 bit
    10. 10th cycle -> load TMP_ADDRESS value to MAR
    11. 11th cycle -> load RAM value to MDR
    12 12th cycle -> load MDR data to B register
    13. 13th cycle -> Enable ALU
    14. 14th cycle -> Load data from address bus to accumulator

--> RCL(14)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
    5. 5th cycle -> Load data from address bus to accumulator.

--> RCR(15)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
    5. 5th cycle -> Load data from address bus to accumulator.

--> OR B(16)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU
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    5. 5th cycle -> Load data from address bus to accumulator.

--> AND immediate(17)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> load PC value to MAR
    5. 5th cycle -> load RAM value to MDR & increase PC value 1
    6. 6th cycle -> load MDR value to B register
    7. 7th cycle -> Enable ALU
    8. 8th cycle -> Load data from address bus to accumulator

--> CMP B(18)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> Enable ALU

--> DEC(19)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> enable ALU
    5. 5th cycle -> load data from address bus to accumulator

--> PUSH(20)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> DEC SP and load accumulator data to MDR
    5. 5th cycle -> load SP value to MAR
    6. 6th cycle -> write MDR data to RAM address

--> POP(21)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
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    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> load SP value to MAR
    5. 5th cycle -> load RAM value to MDR & INC SP
    6. 6th cycle -> load data from MDR to accumulator

--> CALL ADDRESS(22)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> load PC value to MAR
    5. 5th cycle -> load RAM value to MDR & increase PC value 1
    6. 6th cycle -> load MDR value to TMP_ADDRESS as lower 4 bit
    7. 7th cycle -> load PC value to MAR
    8. 8th cycle -> load RAM value to MDR & increase PC value 1
    9. 9th cycle -> load MDR value to TMP_ADDRESS as higher 4 bit
    10. 10th cycle -> load PC value to MDR (lower 4 bit) & DEC SP
    11. 11th cycle -> load SP value to MAR
    12. 12th cycle -> write MDR data to RAM memory
    13. 13th cycle -> hold on to ensure data is written
    14. 14th cycle -> load PC value to MDR (higher 4 bit) & DEC SP
    15. 15th cycle -> load SP value to MAR
    16. 16th cycle -> write MDR data to RAM memory
    17. 17th cycle -> hold on to ensure data is written & load address from TMP_ADDRESS to PC

--> RET(23)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> load SP value to MAR
    5. 5th cycle -> load RAM value to MDR & INC SP
    6. 6th cycle -> load MDR value to TMP_ADDRESS as higher 4 bit
    7. 7th cycle -> load SP value to MAR
    8. 8th cycle -> load RAM value to MDR & INC SP
    9. 9th cycle -> load MDR value to TMP_ADDRESS as lower 4 bit
    10. 10th cycle -> load address from TMP_ADDRESS to PC

--> JMP address(24)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER
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    ---Execution Cycle
    4. 4th cycle -> load PC value to MAR
    5. 5th cycle -> load RAM value to MDR & INC PC
    6. 6th cycle -> load MDR value to TMP_ADDRESS as lower 4 bit
    7. 7th cycle -> load PC value to MAR
    8. 8th cycle -> load RAM value to MDR & INC PC

--> HLT(25)

    ---Fetch Cycle
    1. 1st cycle -> load PC value to MAR
    2. 2nd cycle -> load RAM value to MDR & INC PC
    3. 3rd cycle -> load MDR data to INSTRUCTION_REGISTER

    ---Execution Cycle
    4. 4th cycle -> make HLT pin active into controller sequencer
    9. 9th cycle -> load MDR value to TMP_ADDRESS as higher 4 bit
    10. 10th cycle -> load TMP_ADDRESS value to PC
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