PRODUCT BRIEF

GPL32705B

Advanced Multimedia Processor Solution

Nov. 18, 2013

Version 1.0

Table of Contents

PAGE

ADVANCED MULTIMEDIA PROCESSOR SOC SOLUTION

1. GENERAL DESCRIPTION

The Generalplus GPL32705B, a highly integrated SoC (System-On a Chip), offers a great cost-effective and high performance ratio solution for multimedia processor applications. It is embedded the ARM7TDMI with 4K-byte unified ID-cache and many tremendous features such as JPEG CODEC engine, TFT-LCD interface, CMOS sensor interface, scalar engine, SDRAM controller, UART interface, 4-channel DMA controller, 6-channel 16-bit timers, RTC, SD/MMC card interface, USB 2.0 mini-host/device, interrupt controller, SPI (master/slave) controller, programmable I/O ports, stereo 16-bit DAC for audio playback, 2-channel 12-bit ADC, MIC, PLL, and 1K-byte embedded SRAM.

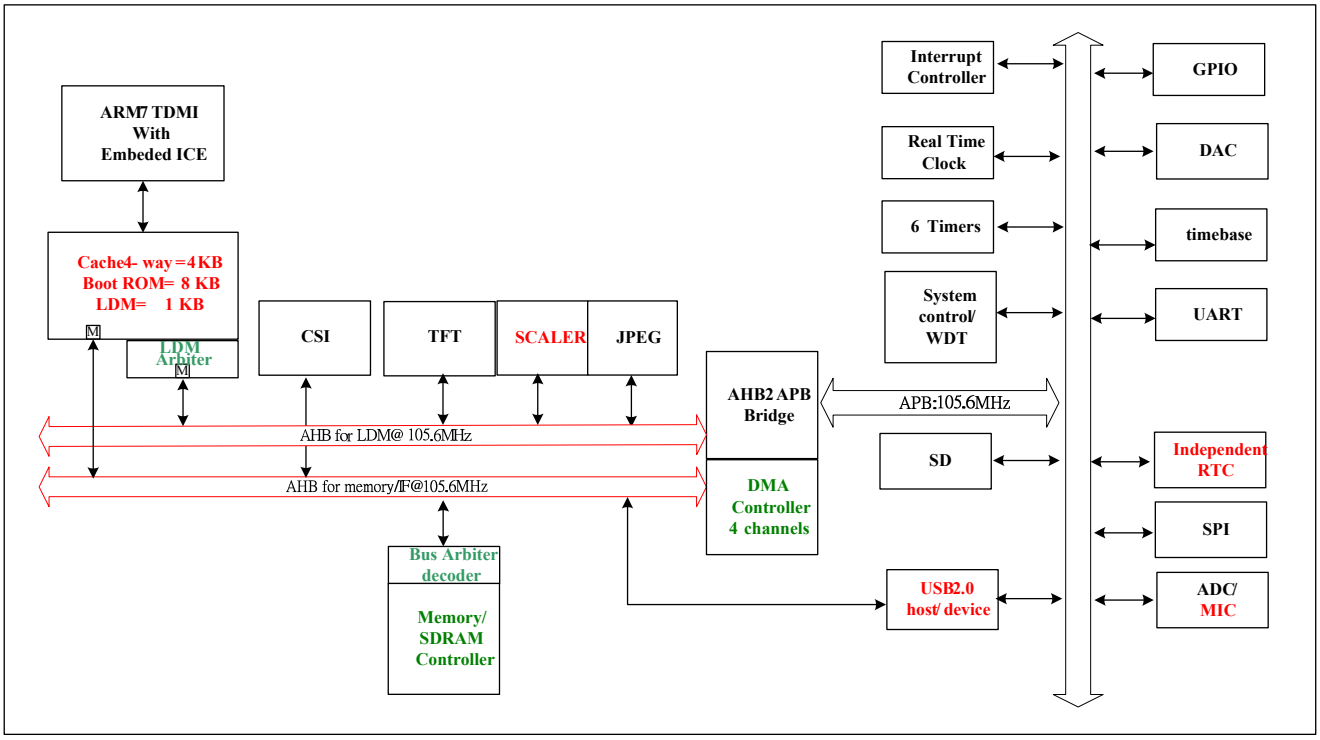
With a complete set of common system peripherals, the GPL32705B chip minimizes overall system cost and no additional component needs to be added. Not only does GPL32705B feature the high-speed performance, but it is also a cost-effective system and the most importantly - compatible with all ARM based programs.

2. FEATURES

- ARM7TDMI CPU with 4KB unified ID-cache, write buffer, embedded JTAG ICE, and working frequency up to 105.6MHz.
- 1KB SRAM for local data buffer.
- JPEG CODEC.
  - ISO/IEC 10918-1 baseline JPEG.
  - High-speed Decoding and Encoding with resolution up to 8000x8000 64MPixel.
  - Hardware Motion JPEG Decoding and Encoding (up to D1@30fps*1) for real-time video record and playback application.
- Video-in & CMOS sensor interface and CCIR601/CCIR656 standard supported.
- 105.6 MHz 16Mbit SDRAM inside
- Four-channel DMA controller.
- TFT-LCD controller.
  - UPS051. (serial RGB)
  - UPS052. (serial RGB dummy)
  - I80 (8-bit/16-bit/18-bit system bus) I/F type.
  - CCIR601/CCIR656.
  - Scalar engine inside with programmable up-scaling and down-scaling factor.
- Interrupt Controller.
- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB mini-host with built-in transceiver.
- Watchdog timer.
- Six 16-bit timers/counters.
- SD/SDHC/MMC card interface.
- SPI (master/slave) interface with data rate up to 24Mbps.
  UART (asynchronous serial I/O) interface with baud rate up to 1.8432Mbps and 115.2Kbps.
- 45 Programmable general I/O ports (GPIO) with pull-high/low control.
- Power manager.
- Built-in 3.0V to 1.8V Regulator.
- Low voltage reset.
- Real-time clock (RTC) with independent power supply.
- 105.6MHz PLL.
- 16-bit stereo DAC (2-channel) for audio playback.
- 12-bit ADC with 1 line-in channels.
- MIC with PGA. (Programmable Gain Amplifier)

Note: Can scale up to 1280x720

3. BLOCK DIAGRAM



4. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

5. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 18, 2013	1.0	First edition	6