Working with Altera Quartus:

1. Open Quartus.

2. Click File->New Project Wizard->Next

3. Fill out the following:

What is the working directory for this project? – Browse->Create a folder in desktop->Select the folder

What is the name of the project->Type a name and **remember it**(Say “expt1”). Same name is going to be copied to the next box automatically.

Press next.

4. Press next

5. Select Device Family: FLEX10KE and press next.

6. Fill out the following in all three pair of boxes:

Tool name: Custom

Format: Verilog HDL

Press Next->Finish

7. File->New->Verilog HDL File->OK

8. Write the code and save it with the same name as that given in expt1 3 with extension of .v (Example: expt1.v)

9. File->New->Vector Waveform File

10. Right click on Name->Insert->Insert Node or BUS

11. Click Node Finder.

Filter: Pins: all

Look in: Filename (Example expt1.v)

Click list->Click ">>" -> OK -> OK

12. Right click on each input->Value->Clock and set up the clocks.

13. Save with the same filename as the .v file (Example: expt1.vwf)

14. Assignment->Settings->Simulator Settings

Simulation Mode: Functional (If you miss this step, there will be delays and spiked in the output waveforms)

Click OK.

15. Processing-> Generate Functional Simulation Netlist

16. Processing-> Start Simulation

17. tools> netlist viewers > RTL Viewer (Watch Logic Diagram)