Brac University

Mid Term Exam

Fall 2023

CSE251

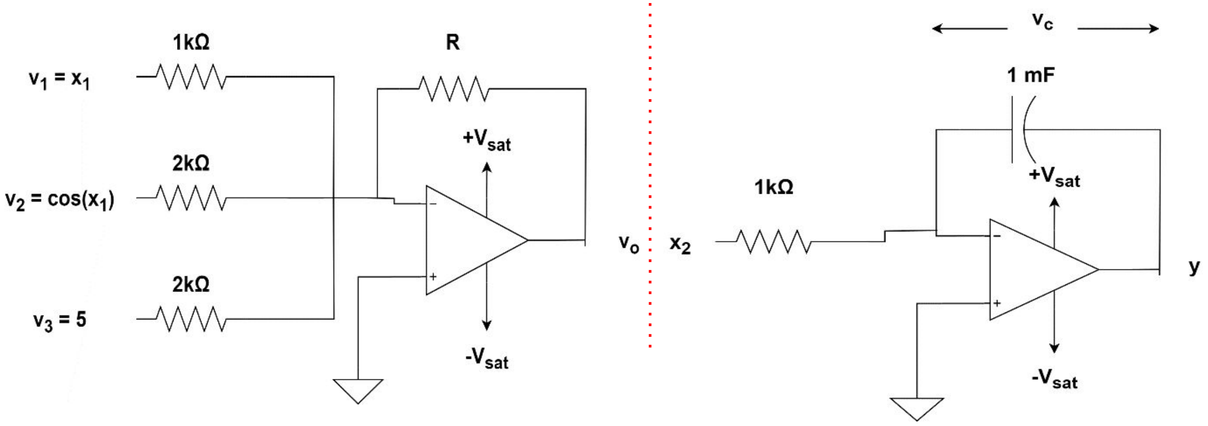
Electronic Devices and Circuits

Date: 04 November 2023

Time: 1 hour 30 minutes (4:30 PM - 6:00 PM)

Marks: 30 (***Answer any 3 out of 4 questions)***

Q1



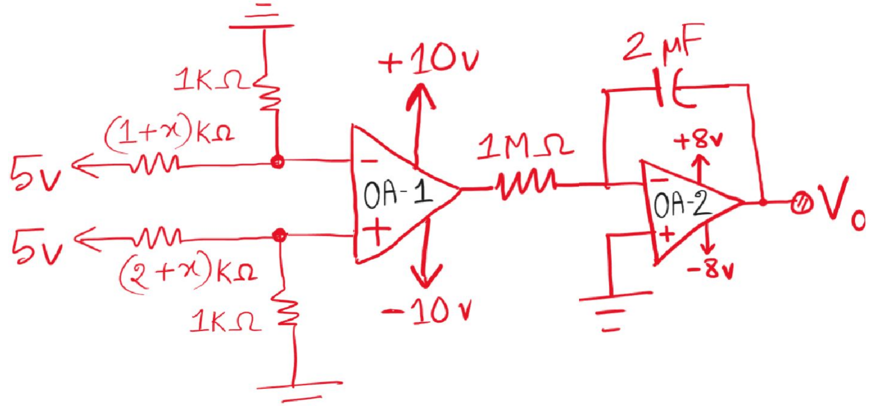
(a) **Determine** the expressions for V_o and y. [3+1]

(b) **Assume,** $V_o = X_2$, $V_1 = y$. **Rewrite** the expressions found in part-(a). [1+1]

(c) **Draw** the circuit for the expressions found in part-(b). [2]

(d) **Define** and **explain** "virtual ground" in an Ideal Op-Amp. [2]

Q2



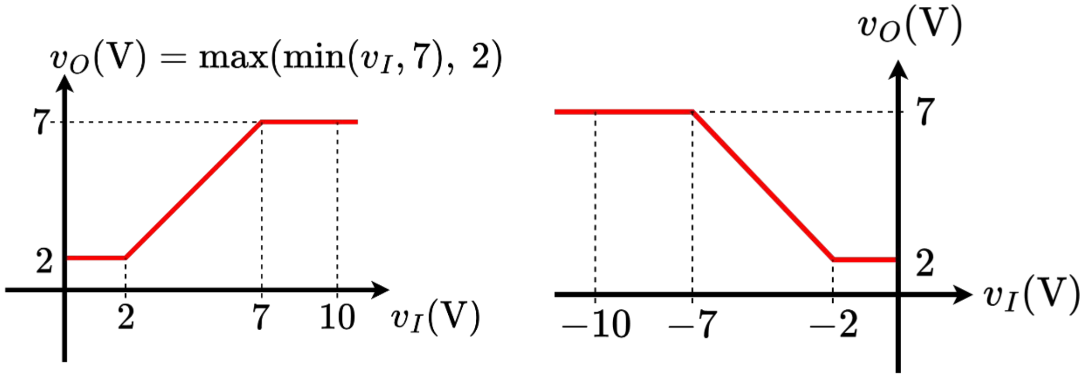
In the circuit given above, ***x = last digit of your student ID***

(a) **Analyze** the circuit and **determine** the voltage at the inverting, non-inverting terminals and the output of OA-1. [2+2+2]

(b) **Determine** the highest V_O you can get from this circuit. **Explain** briefly. [1]

(c) **Analyze** the circuit to **determine** the output voltage, V_O of OA-2 and **plot** V_O vs. time. **Label** the plot appropriately. [at t = 0, V_O = 0] [3]

Q3



(a) Design separate circuits, using only diodes, to implement the following functions,

z = min(v_I, 7) and **v_O = max(z, 2)**. [3+3]

(b) Design a circuit using Op-Amp to implement the VTC on the right. [3]

(c) Determine which of the following logic gates can be built with diodes and **explain** briefly: (i) XOR, (ii) XNOR. [1]

Q4

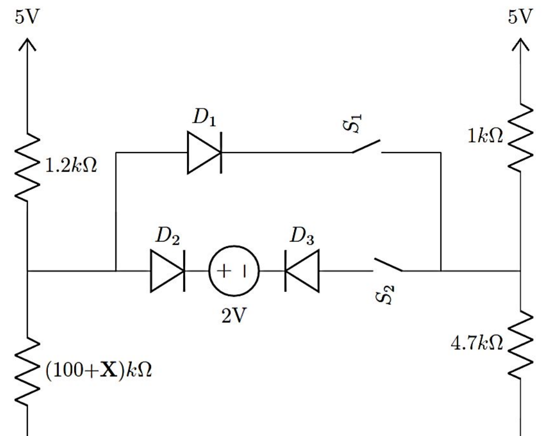


Fig. 01

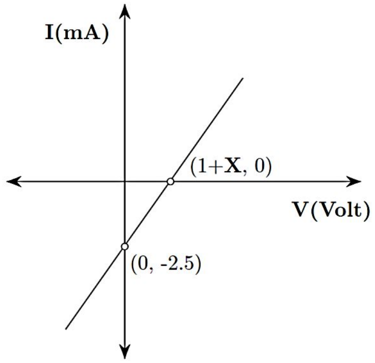


Fig. 02

In Fig.01, a circuit is shown with two 'off' switches, S_1 and S_2 where V_{D0} = 0.7V.

Fig.02 represents the IV-curve of an unknown device.

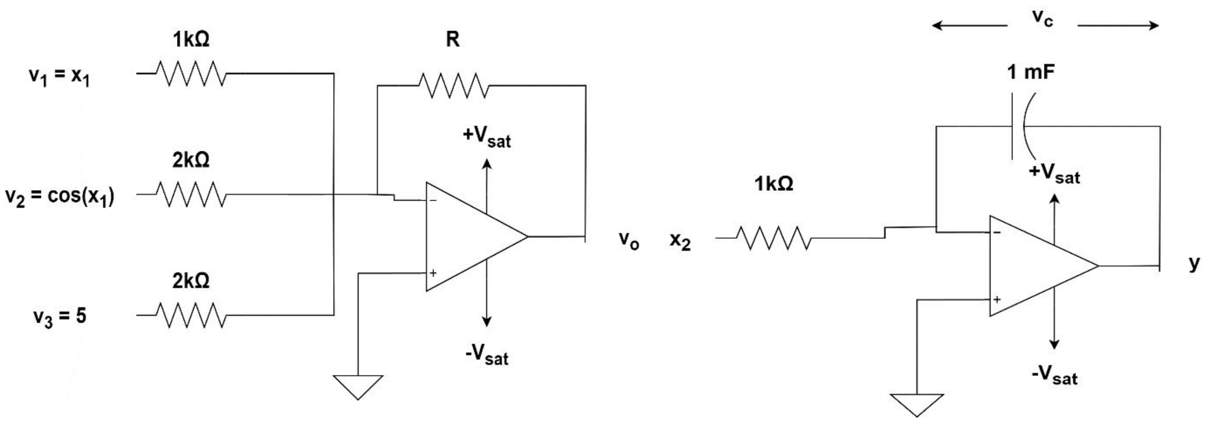
Assume, X = Last digit of your Student ID.

(a) Calculate the current passing through the diode D_1, if only S_1 is 'on'. [03]

(b) Calculate the current passing through the diodes D_2 and D_3 If only S_2 is 'on'. [04]

(c) Determine and **draw** the unknown component of Fig. 02 with parameters. [02+01]

Q1



(a) **Determine** the expressions for V_o and y. **[3+1]**

(b) **Assume,** $V_o = X_2$, $V_1 = y$. **Rewrite** the expressions found in part-(a). **[1+1]**

(c) **Draw** the circuit for the expressions found in part-(b). **[2]**

(d) **Define** and **explain** "virtual ground" in an Ideal Op-Amp. **[2]**

(a)

$$t_1 = x_1 \sim 10x_1$$
$$t_2 = 0.5\cos(x_1) \sim 5\cos(x_1)$$
$$t_3 = 2.5 \sim 25$$

$$\boldsymbol{V_O = -t_1 - t_2 - t_3}$$

$$\boldsymbol{y = -\int x_2(t)\, dt}$$

(b)

$$\boldsymbol{y = -\int x_2(t)\, dt}$$
$$\boldsymbol{y = -\int V_O(t)\, dt}$$
$$\boldsymbol{V_O(t) = -\frac{dy}{dt}}$$

$$\boldsymbol{\frac{dy}{dt} = y + 0.5\cos(x_1) + 2.5 \quad \sim \quad \frac{dy}{dt} = 10y + 5\cos(x_1) + 25}$$

$$\boldsymbol{y = \int (y + 0.5\cos(x_1) + 2.5)\, dt}$$

$$\boldsymbol{V_1 = \int (V_1 + 0.5\cos(x_1) + 2.5)\, dt} \qquad \boldsymbol{x_2 = -\int x_2\, dt}$$

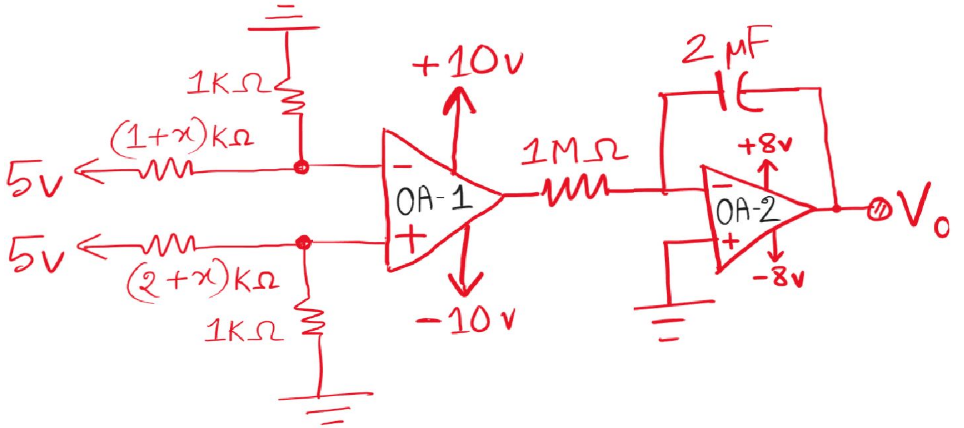
(c)

Just join $V_O - x_2$ and $y - V_1$

(d)

The concept of $V_+ \approx V_-$ in Op-Amp input terminals.

Q2



In the circuit given above, ***x* = *last digit of your student ID***

(a) **Analyze** the circuit and **determine** the voltage at the inverting, non-inverting terminals and the output of OA-1. **[2+2+2]**

(b) **Determine** the highest V_O you can get from this circuit. **Explain** briefly. **[1]**

(c) **Analyze** the circuit to **determine** the output voltage, V_O of OA-2 and **plot** V_O vs. time. **Label** the plot appropriately. [at $t = 0$, $V_O = 0$] **[3]**

(a)

At OA-1

$$V^+ = 5v \times \frac{1k\Omega}{(1+2+x)k\Omega} = \left(\frac{5}{3+x}\right)v$$
$$V^- = 5v \times \frac{1k\Omega}{(1+1+x)k\Omega} = \left(\frac{5}{2+x}\right)v$$

$\because V^- > V^+$

$\therefore$ The output voltage of OA-1, $\boldsymbol{V_{O_{(OA-1)}} = -10v}$

(b)

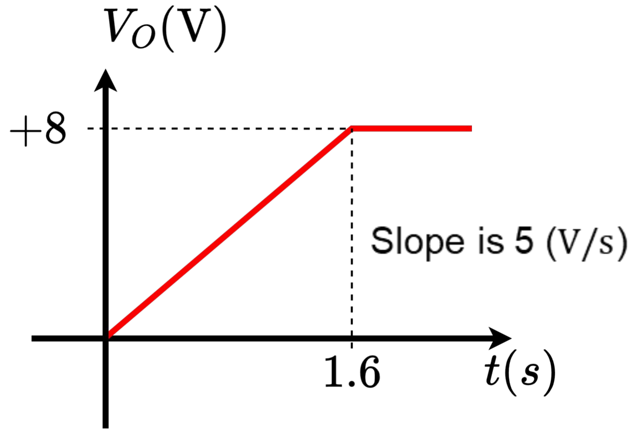
Since, the output voltage of an op-amp cannot exceed it's supply voltage,

$$\boldsymbol{V_O(\text{max}) = 8\ \text{V}}$$

(c)

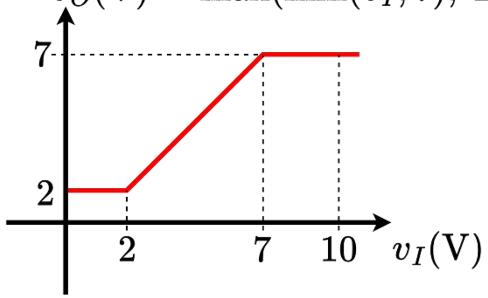
$$V_O = -\frac{-10}{2}\int_0^t \mathbf{d}t$$

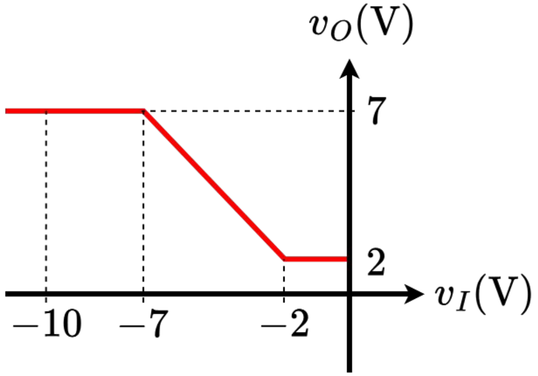
$$V_O = \begin{cases} 5t, & t < \frac{5}{8}\ \text{s} \\ 8, & t \geq \frac{5}{8}\ \text{s} \end{cases}$$



Q3

$v_O(\mathrm{V}) = \max(\min(v_I, 7),\ 2)$





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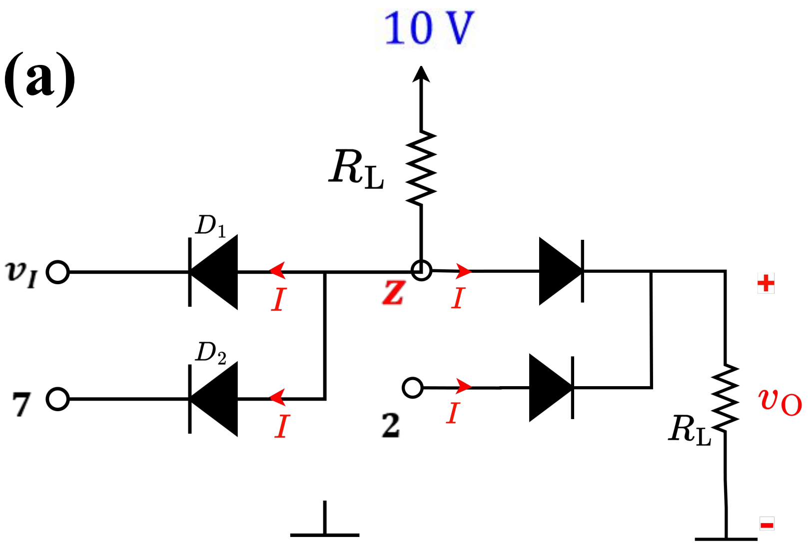
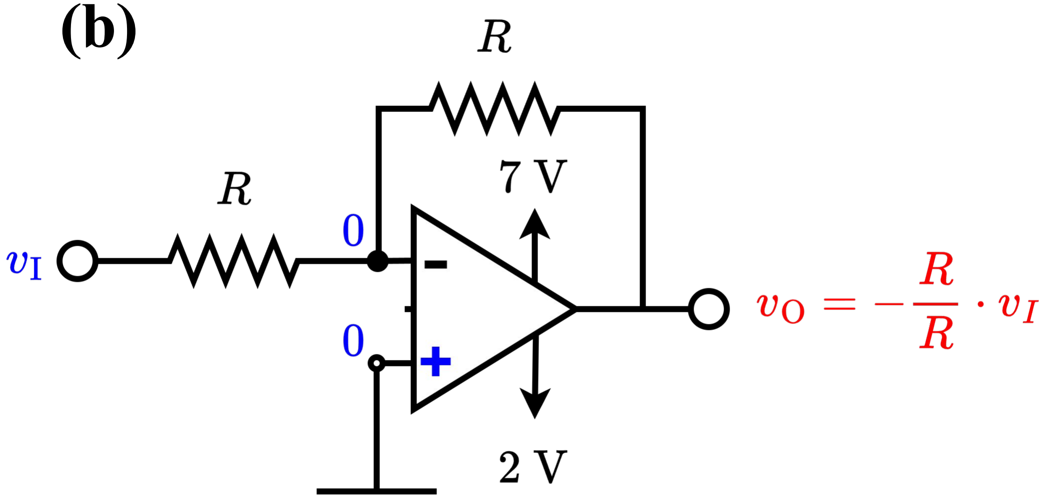
(a)



(b)



(c)

None of the logic gates can be build using just diodes, because diodes alone cannot be used for creating the **inverter** logic needed for composing the XOR or XNOR logic function.

Soln: (a) Only S_1 is ON : Assume the diode 'ON', (Nodal Analysis) *Vx = right-side node of the diode*

$$\Rightarrow v_x = 4.171\text{V} \sim 4.173\text{V}\ [100\text{k}\Omega \sim 109\text{k}\Omega]$$

$$\Rightarrow I_{D1}\,\textbf{(left to right)} = \frac{5-(v_x+0.7)}{1.2} + \frac{0-(v_x+0.7)}{100+X} = 0.059 \sim 0.061\ mA > 0\ mA$$

$\therefore$ D1 **conducts (short)** current and $I_{D1} = 0.059\text{ mA} \sim 0.61\text{ mA}\ [100\text{k}\Omega \sim 109\text{k}\Omega]$

(b) Only S_2 is ON: Back to back diodes. $I_{D23} = 0\ mA$

Q4

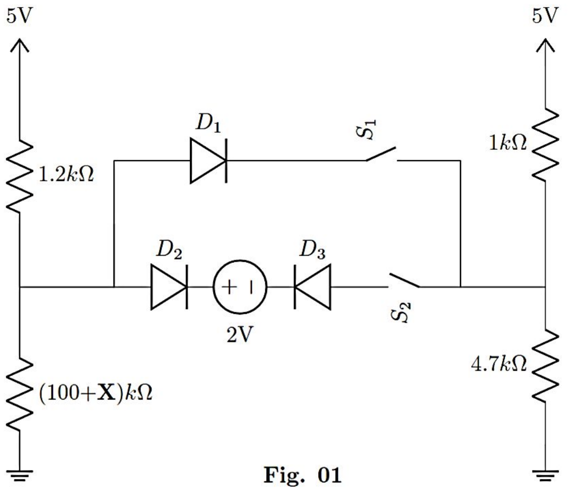


Fig. 01

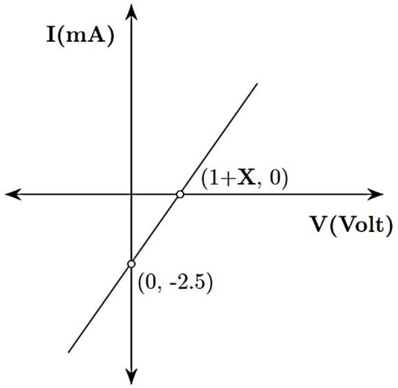


Fig. 02

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Fig.02 represents the IV-curve of an unknown device.
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(c) Determine and **draw** the unknown component of Fig. 02 <u>with parameters</u>. **[02+01]**

(c) Line Equation: $I = 2.5\,V - 2.5 \sim I = 0.25\,V - 2.5\ [(1,0) \sim (10,0)]$

$\therefore$ R = (1/m) k Ω = 0.4 kΩ ~ 4 kΩ [(1,0) ~ (10,0)]

$\therefore$ [Either] Series Voltage Source, $V_0 = 2.5 \times R = 1\text{ V} \sim 10\text{V}$

[or] Parallel Current Source, $I_0 = 2.5\text{ mA}$