

Lecture 16

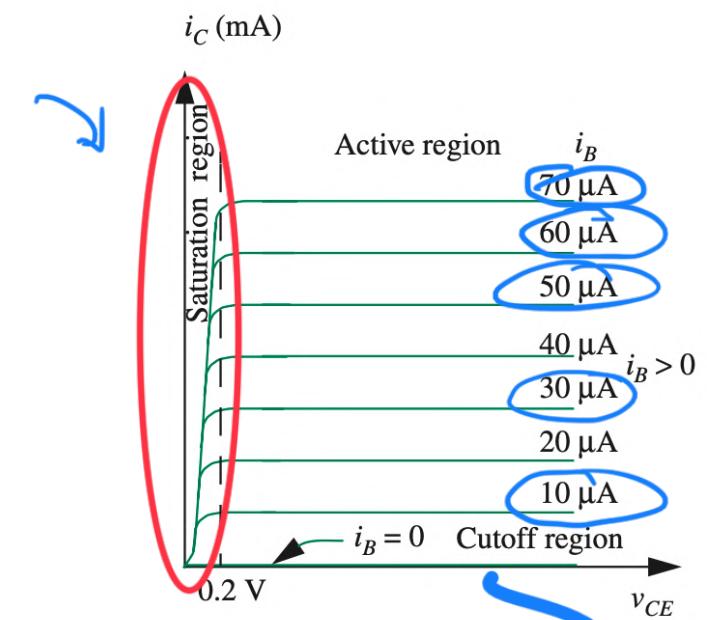
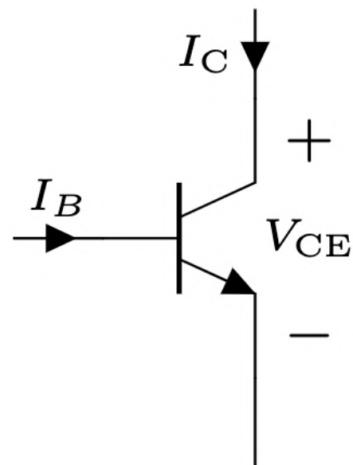
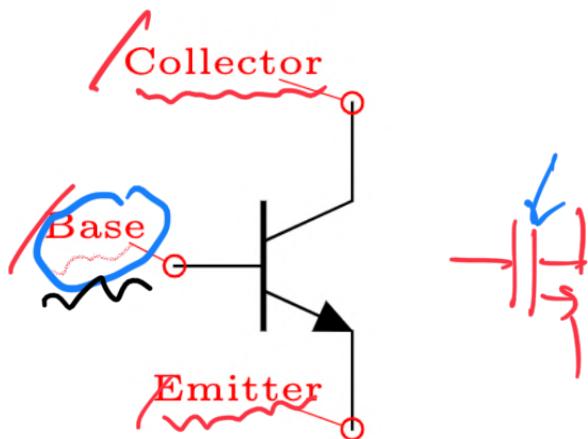
Introduction to BJT, Logic Gates

Bipolar Junction Transistor BJT

BJT

- **Current-controlled** transistor, 3 terminals – Base, Emitter, Collector
 - IV between C and E (I_C vs V_{CE}) is controlled by base current, I_B
 - IV quite similar to MOSFET, but there are some differences
 - We can use a S-model here too, but controlled by I_B (instead of V_{GS})

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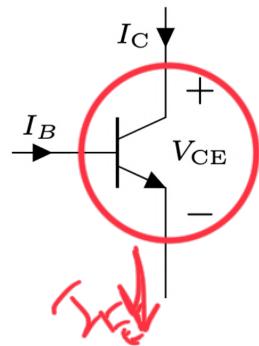


BJT vs MOSFET - Differences

$$\text{Slope} = \frac{I}{R}$$

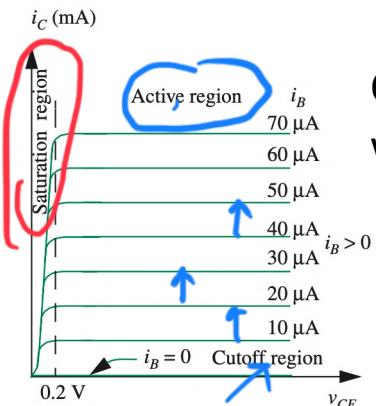


BJT



Current controlled, I_B controls I_C vs V_{CE}

Base current, I_B , is the control. Hence $I_E \neq I_C$, rather
 $I_E = I_C + I_B$

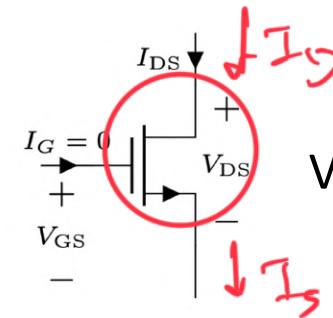


Current in active region changes linearly with control I_B . Hence, $I_C \propto I_B$

$$I_C = \beta I_B$$

Slope in the saturation region is high, hence very small resistance when "ON"

MOSFET

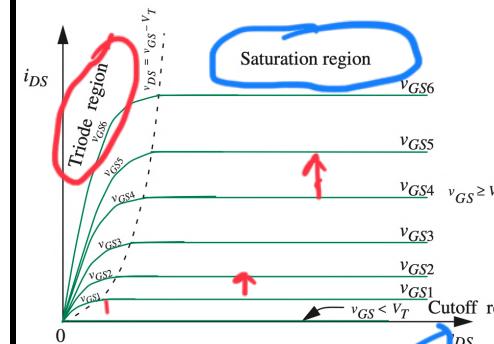


Voltage controlled, V_{GS} controls I_C vs V_{CE}

$$I_S = I_D$$

Gate current, I_G , is always zero. Therefore, $I_S = I_D = I_{DS}$

$$I = \frac{k}{2} [V_{GS} - V_T]^2$$

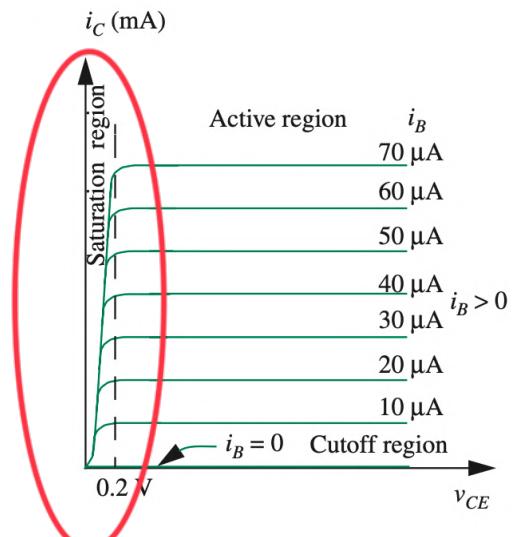


Current in active region changes with control V_{GS}^2 . Hence, $I_{DS} \propto V_{GS}^2$

Slope in the saturation region is low, hence significant resistance when "ON"

BJT vs MOSFET - Similarities

BJT



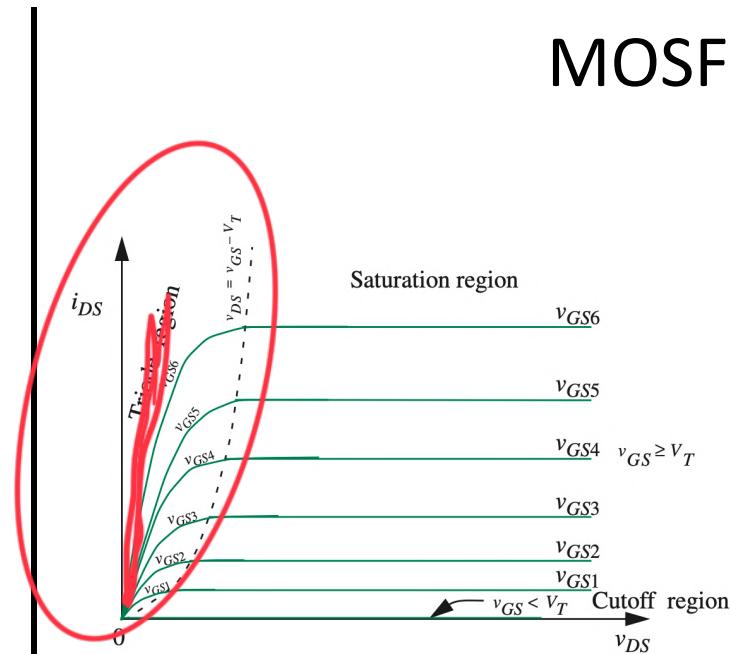
Saturation mode for small V_{CE} ($< 0.2V$)

Approximately short circuit in **Saturation** mode ($I_B = \text{High}$)

Open circuit in **Cutoff** mode ($I_B = 0$)

Can use as a switch \Rightarrow S-Model!

MOSFET



Triode mode for small V_{DS} ($< V_{OV}$)

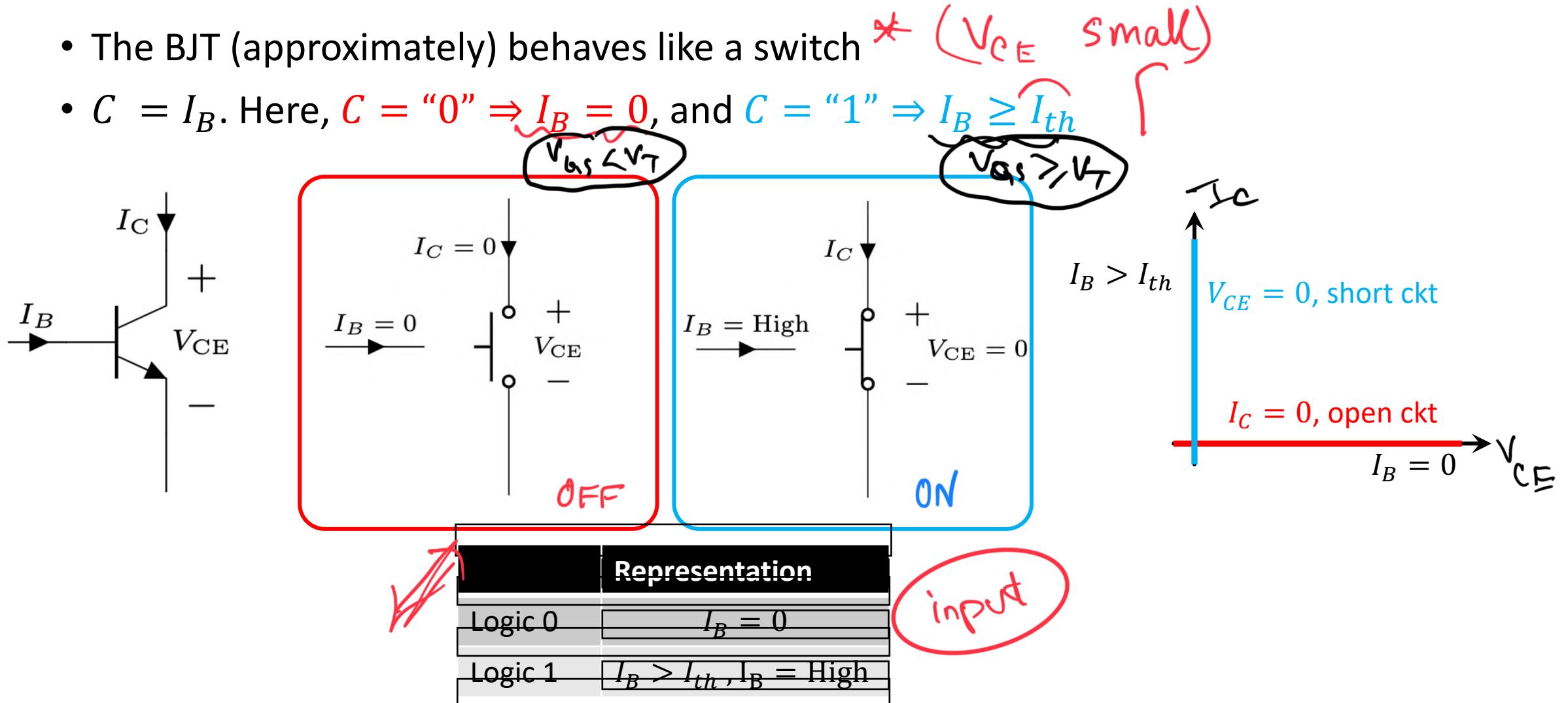
Approximately short circuit in **Triode** mode ($V_{GS} = \text{High}$)

Open circuit in **Cutoff** mode ($V_{GS} < V_T$, e.g., $V_{GS} = 0$)

Can use as a switch \Rightarrow S-Model!

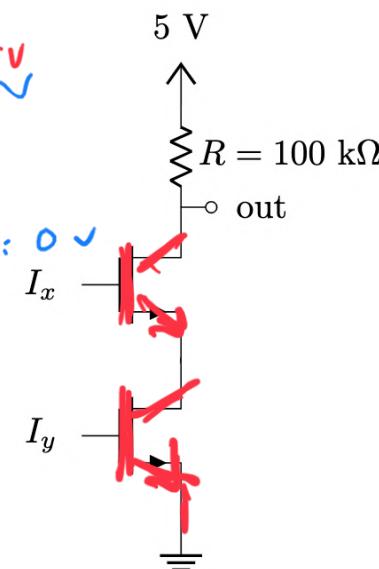
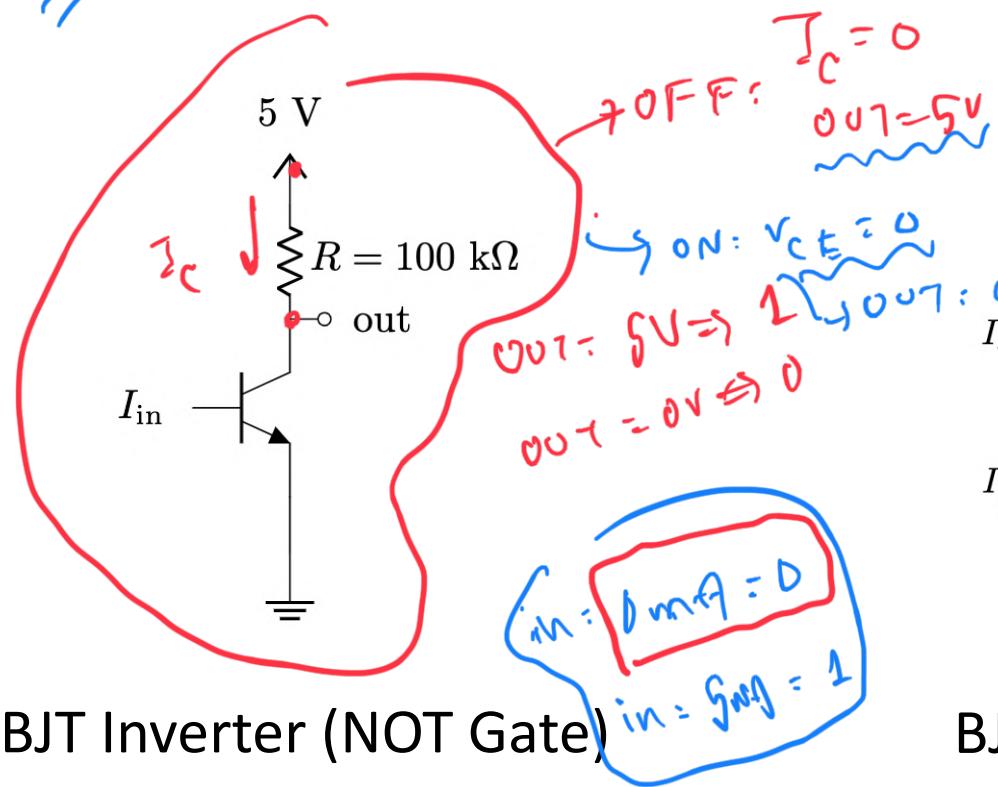
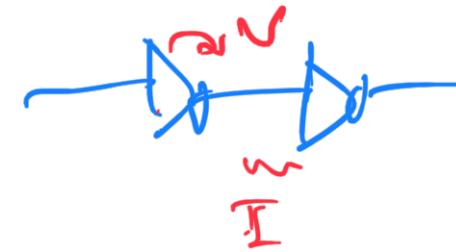
BJT S-Model

- The BJT (approximately) behaves like a switch $\star (V_{CE} \text{ small})$
- $C = I_B$. Here, $C = "0" \Rightarrow I_B = 0$, and $C = "1" \Rightarrow I_B \geq I_{th}$

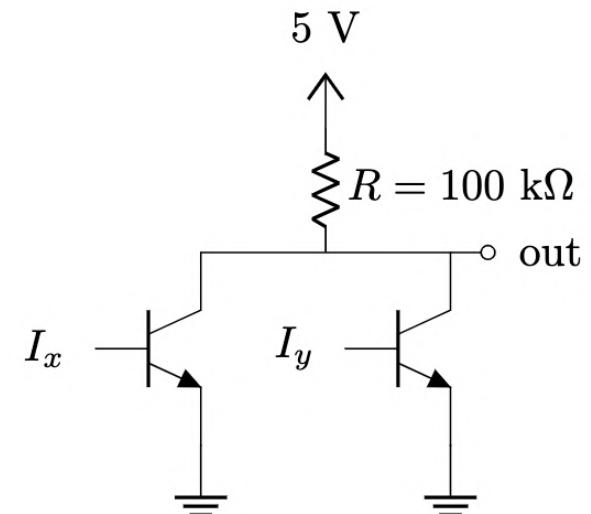


Current-Controlled Logic Gates using BJTs

- Just replace switches with BJTs!
- Major problem: Cannot cascade! (Why?)



BJT NAND Gate



BJT NOR Gate

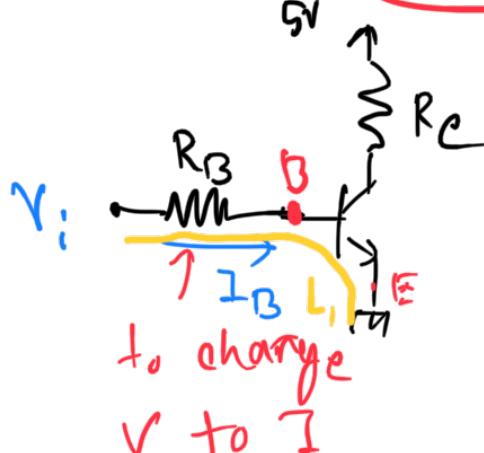
From Current Controlled to Voltage Controlled

$\checkmark \quad I \rightarrow R = 1 \text{ k}\Omega$

$$V = IR = I \times 1$$

$\Rightarrow V = I$ $V \propto I$

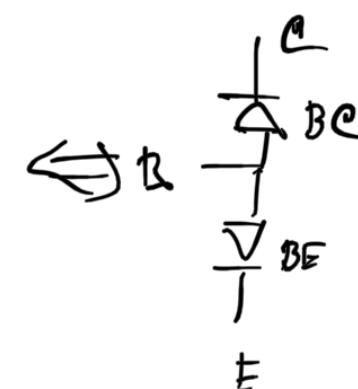
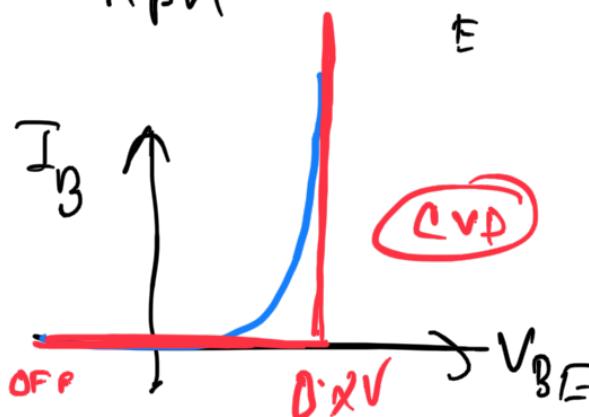
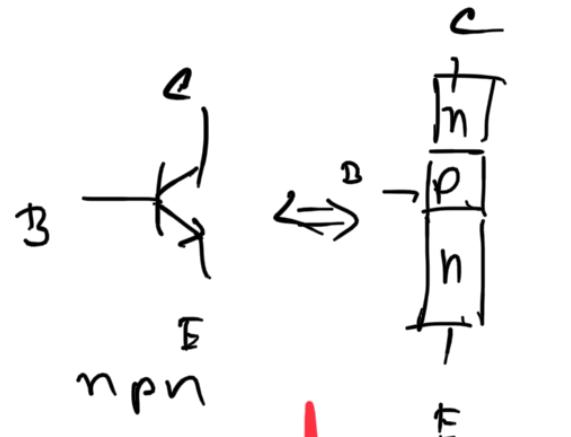
$I \propto V$



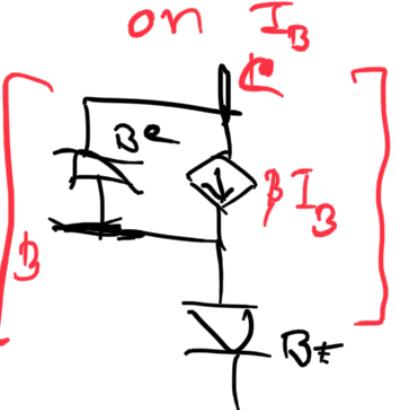
KVL along L_1 : $I_B R_B + V_{BE} = V_i - 0$

$$\Rightarrow I_B = \frac{V_i - V_{BE}}{R_B} \rightarrow \text{OV, } S_V$$

\hookrightarrow depends on I_B

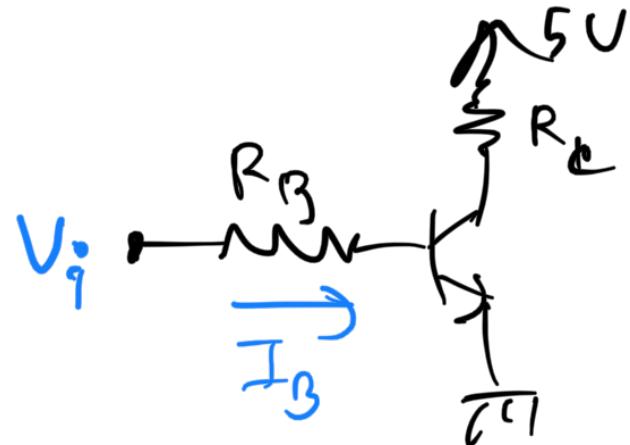


structural similarity



$\therefore \begin{cases} I_B > 0 \Rightarrow V_{BE} = 0 \times V \\ V_{BE} < 0 \times V \Rightarrow I_B = 0 \end{cases}$

From Current Controlled to Voltage Controlled



$$I_B = \frac{V_i - V_{BE}}{R_B}$$

Two cases for V_{BE} :

- $I_B > 0 \Rightarrow V_{BE} = 0.2V$
- $V_{BE} \leq 0.2 \Rightarrow I_B = 0$

$$I_B > 0 \Rightarrow V_i - V_{BE} > 0$$

$$\Rightarrow V_i > V_{BE}$$

$$\Rightarrow V_i > 0.2V$$

$\therefore I_B = 0 \Leftrightarrow V_i \leq 0.2V$

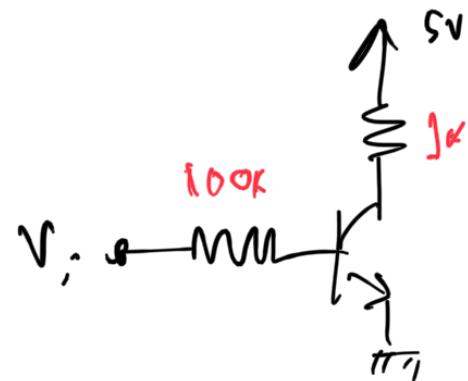
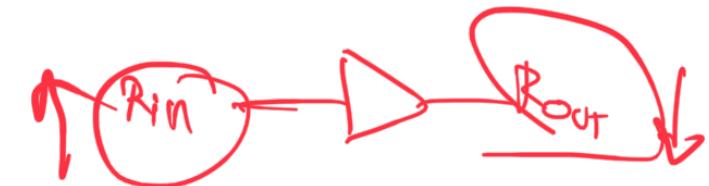
$I_B > I_{th} \Leftrightarrow V_i > V_{th}$

Logic 0: $V_i \leq 0.2V$

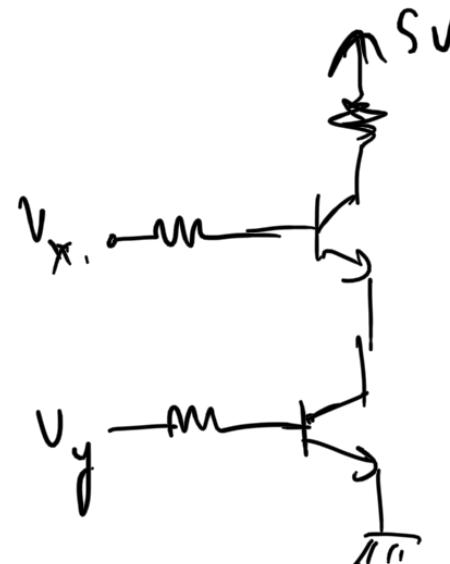
Logic 1: $V_i \geq 0.2V$

$V_{IL} = 0.2V$
 $V_{IH} = V_T$
 $V_{OL} = 0V$
 $V_{OH} = 5V$

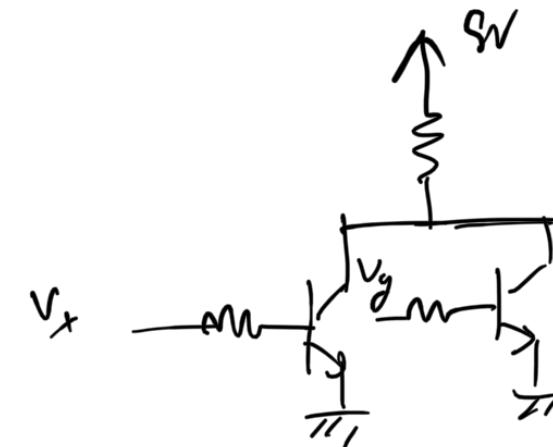
Voltage Controlled Logic Gates



NOT



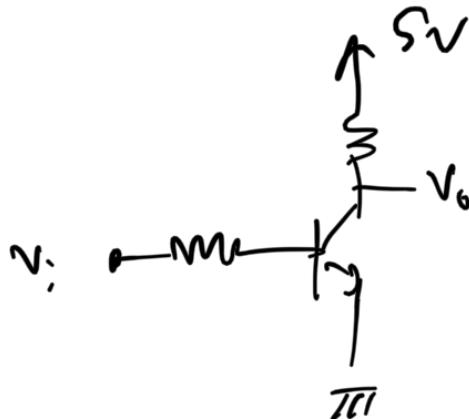
NAND



NOR

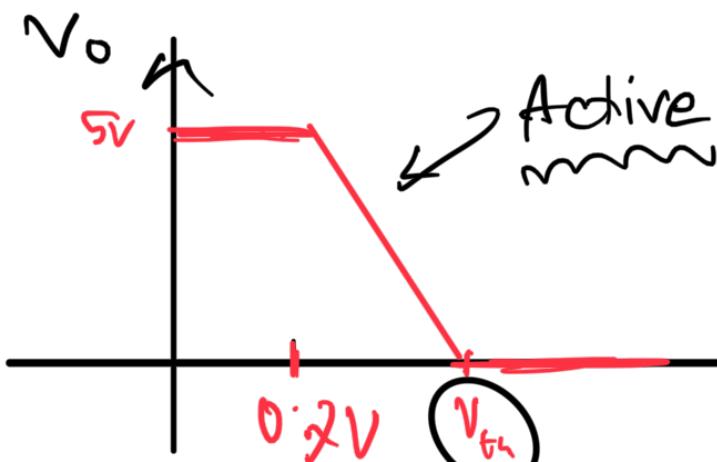
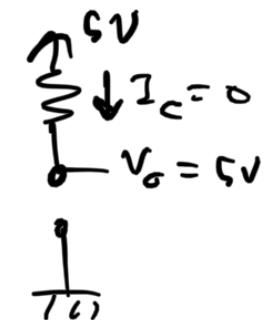
$$I_B = \frac{V_i}{R_B} - ()$$

Voltage Transfer Characteristics – S-model



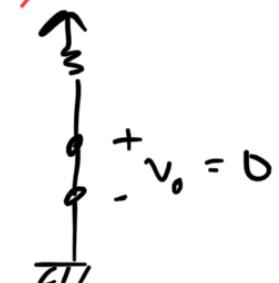
$I_n = \text{Low} \Leftrightarrow \text{Logic 0} \Rightarrow V_i < 0.2$

$$\hookrightarrow V_o = 5V$$



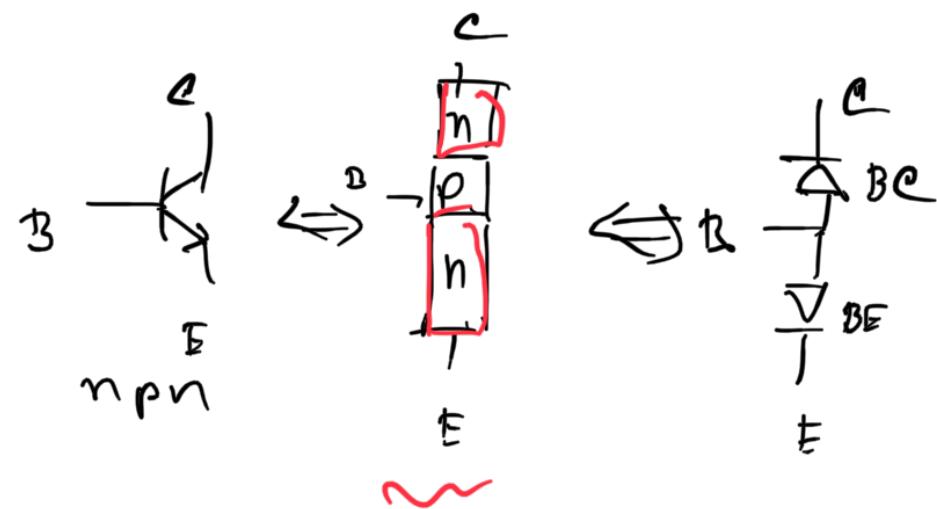
$I_n : \text{High} \Leftrightarrow \text{Logic 1} \Leftrightarrow V_i > V_{th}$

$$\hookrightarrow V_o = 0V$$



$$0.2 + \left(\frac{V_{cc} - 0.2}{\beta R_C} \right) R_B = V_{th}$$

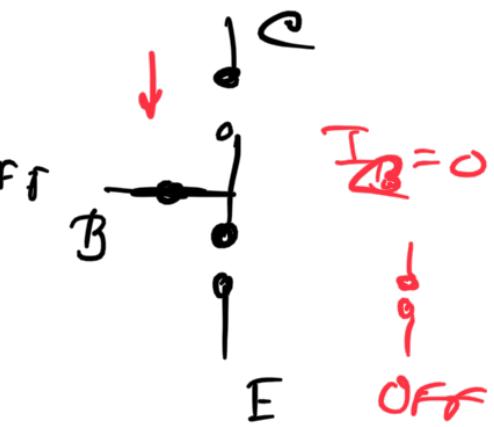
BJT SV Model



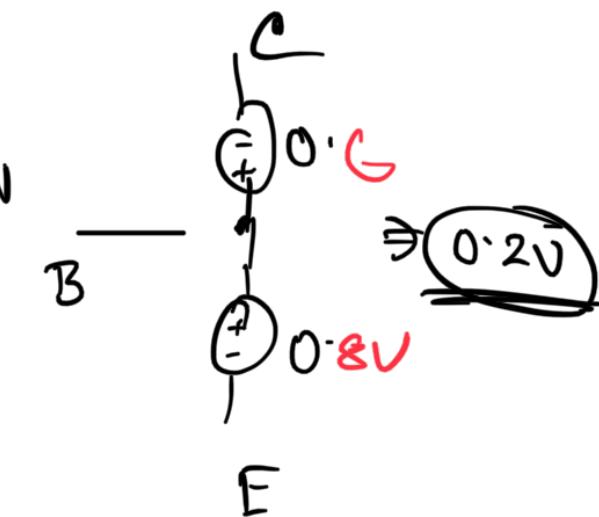
Cutoff

Saturation

$$V_{BE} = OFF, V_{BC} = OFF$$

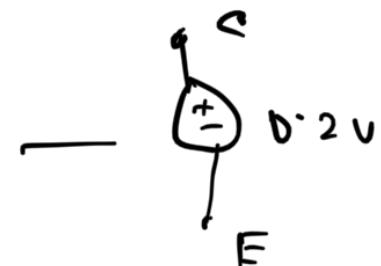


$$V_{BE} = ON, V_{BC} = ON$$

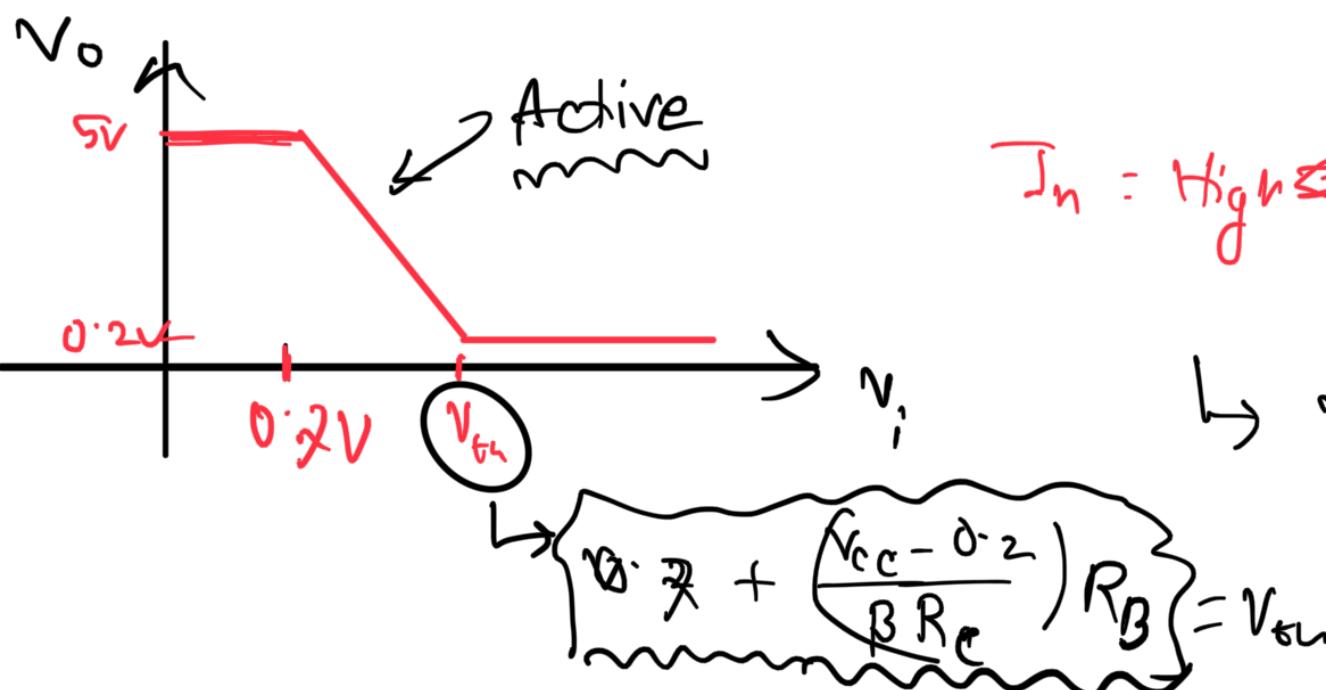
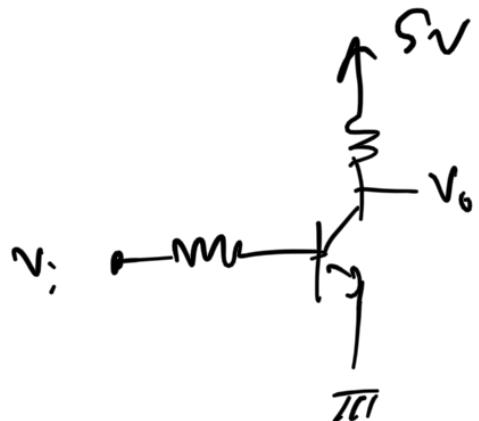


$$I_B = 0$$

$$I_B = High$$

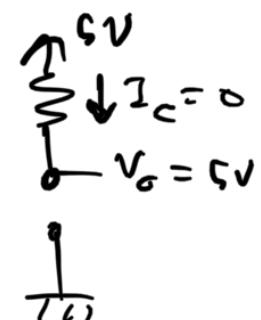


Voltage Transfer Characteristics – SV-model



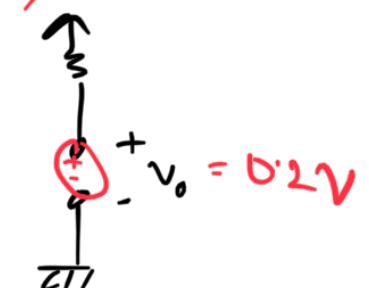
$$I_n = \text{Low} \approx \text{Logic 0} \Rightarrow V_i < 0.2$$

$$\hookrightarrow V_o = 5V$$

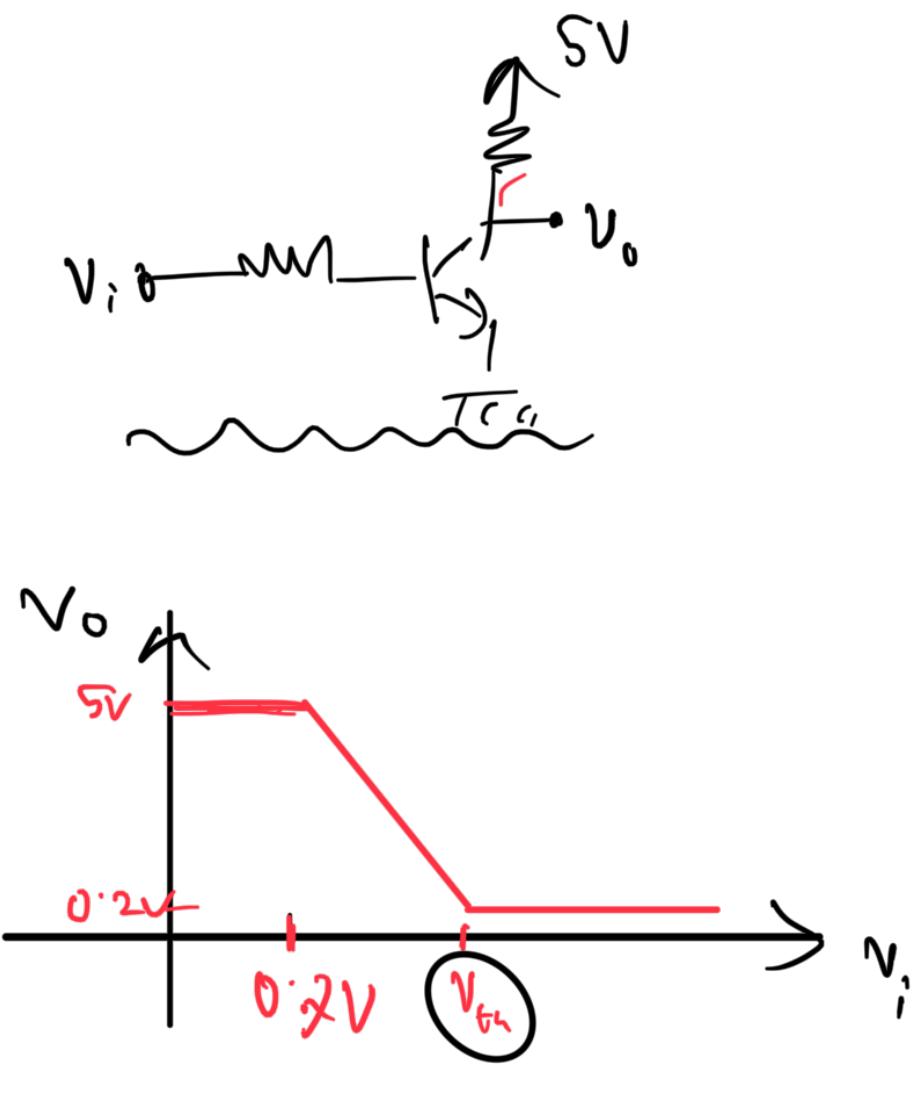


$$I_n = \text{High} \approx \text{Logic 1} \Leftrightarrow V_i \geq V_{th}$$

$$\hookrightarrow V_o = 0V$$



Improving Noise Margin – BJT Inverter



$$V_{I_L} = 0.2V$$

$$V_{O_L} = 0.2V$$

$$V_{I_H} = V_{th}$$

$$V_{O_H} = 5V$$

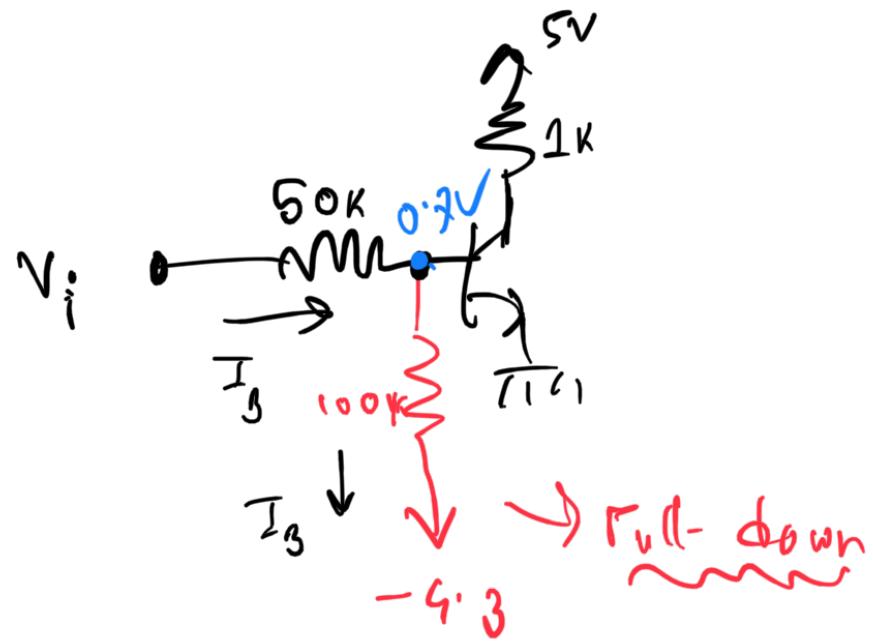
$$\underline{NM_0 = V_{I_L} - V_{O_L}}$$

$$= 0.2 - 0.2$$

$$= 0.5V$$

- Logic Family
- ① Fan-in and Fan-out
 - ② Noise margin

RTL Logic



$$V_{IL} = \cancel{0.2V} \quad 3.2V$$

$$N_MO = 3.2 - 0.2 = 3V$$

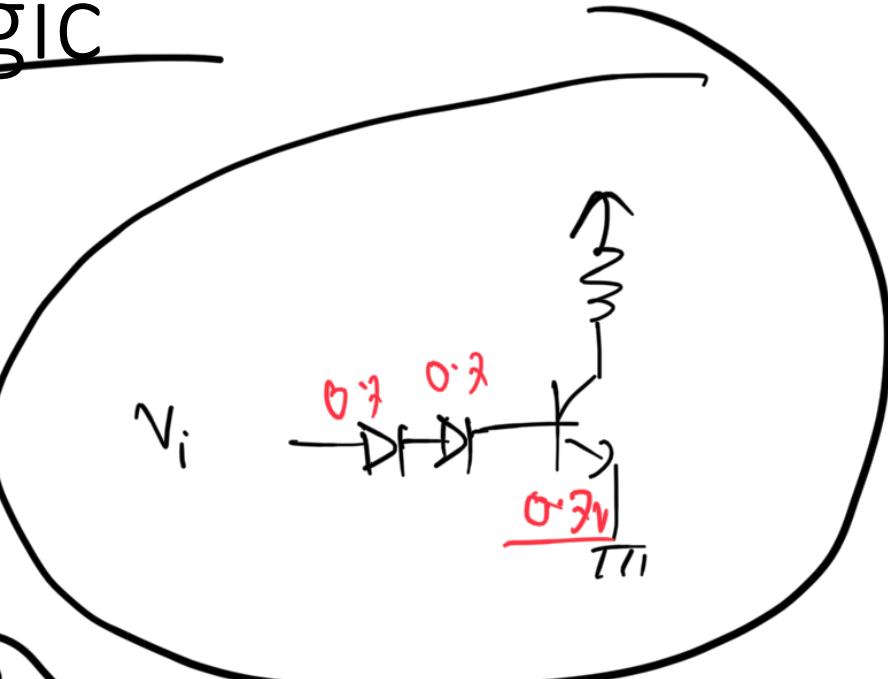
$$I_B = \frac{0.2 - (-0.2)}{100K}$$

$$= \frac{5}{100} = 0.05mA$$

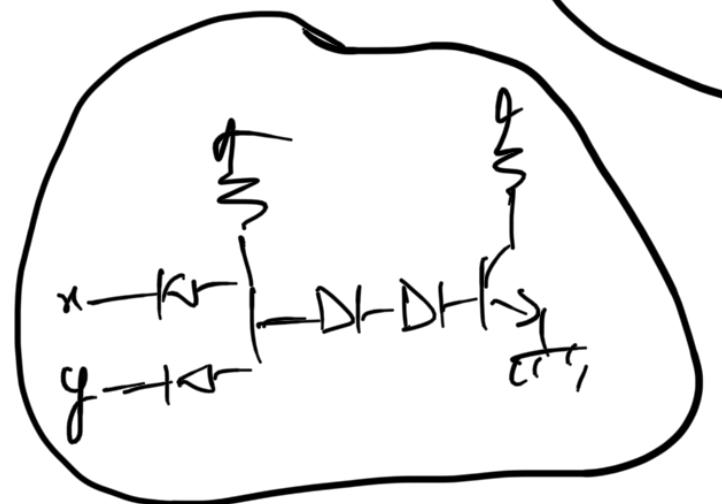
$$I_B = \frac{V_i - 0.2}{50} = 0.05$$

$$\Rightarrow V_i = 50 \times 0.05 + 0.2 = 2.5 + 0.2 = 3.2$$

DTL Logic



DTL inverter



DTL NAND

$$V_{IL} = 0.2V + 0.2 + 0.2$$

$$= 2.1V$$

$$V_{OL} = 0.2$$

$$NM_O = 2.1 - 0.2$$

$$= 1.9V$$