Name:	ID:

Brac University

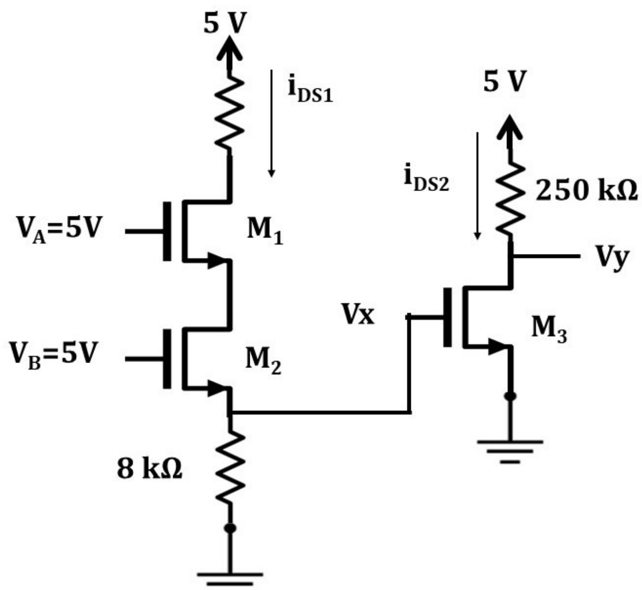
Set - B

Semester: Fall 2023
Course No: CSE251
Course Title: Electronic Devices and Circuits
Sections: 1 to 24

Final Examination
Full Marks: 30
Time: 1.5 hours
Date: Dec 15, 2023

Answer any **3** questions. All the questions carry equal marks.

Question 1



For the following circuit with MOSFETs, assume that V_T=**1 V**, $k_n{}' = 20\ \mu A/V^2$ and the aspect ratio **W/L** is 1 for all the MOSFETS.

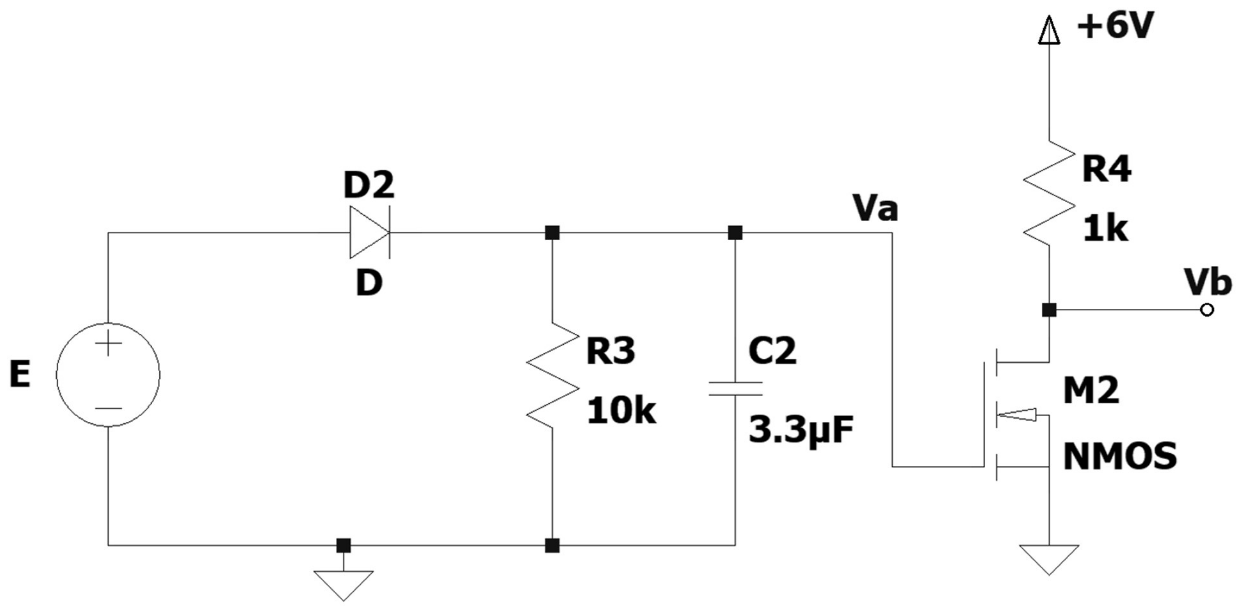
a) If the gate voltage to **M3** MOSFET, $V_x = 0.492$ **V**, and MOSFET **M2** is in triode mode, find the voltage V_1. Verify the modes for both **M1 and M2** *[3]*

b) Find V_y. *[2]*

c) If **W/L=4**, then V_1 = 2.04 V. Find V_x for this case. *[2]*

d) Can you explain, whether there will be any changes in the output voltage at V_y for **W/L** = **4** from that in **'b)'**. Also, comment on whether a larger or smaller value of **W/L** ratio is preferred in this case. *[2+1]*

Question 2



The Half-wave rectifier circuit has been cascaded with an inverter. You are given the following information about the circuit: **[For HW: $V_o = V_{dc} \pm V_{ripple}/2$]**

$E = 6\,sin(400\pi t)\ V$	$K_n = 2\ mA/V^2$	$V_T = 1\ V$	$V_{Do} = 0.7\ V$

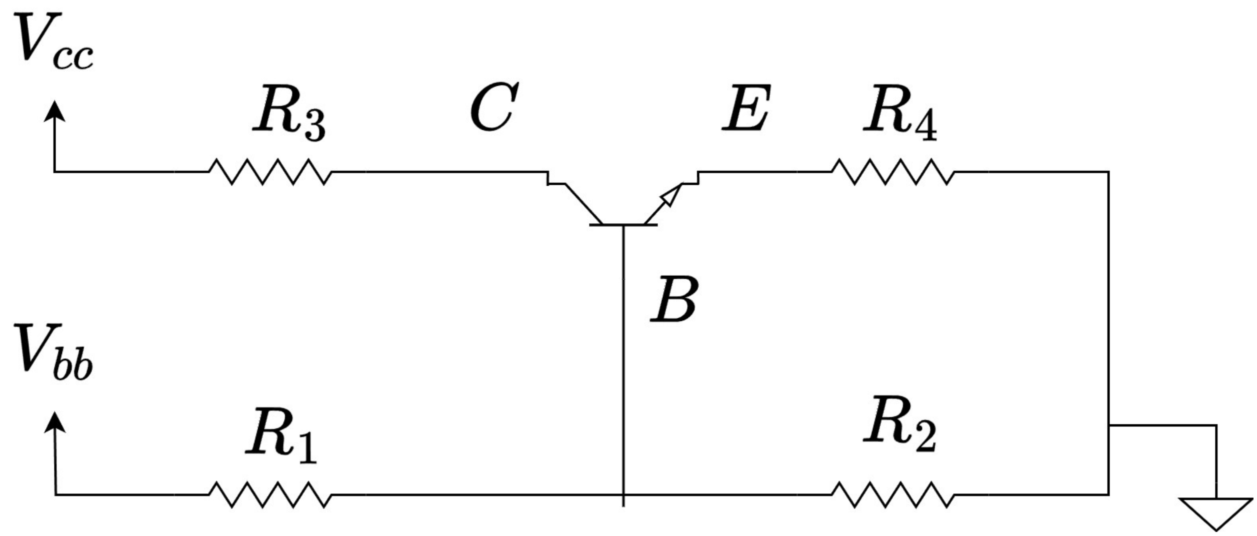
(a) **Determine** the peak-to-peak ripple value of the half-wave rectifier output, V_a . What is the lowest value of V_a? *[3+1]*

(b) At the lowest value of V_a , **determine** the output V_b of the inverter. *[4]*

(c) Now disconnect the capacitor. In this case, **find out** the voltage V_b for the lowest value of V_a. *[2]*

(d) ***[BONUS]*** Draw an approximate plot of V_b without the capacitor connection. *[2]*

Question 3



In the circuit above, $V_{bb} = 5\ V$, $V_{cc} = 15\ V$, $R_1 = 40\ k\Omega$, $R_2 = 60\ k\Omega$, $R_3 = 2\ k\Omega$ and $R_4 = 1\ k\Omega$. Also, the current gain, $I_C/I_B =$ **100.**

a) **Draw** the equivalent circuit of BJT during saturation and active modes. *[1]*

b) A**nalyze** the following circuit to **calculate** the values of $I_b, I_{C,} I_E, V_{CE}$ and V_C using the method of assumed states. <u>You must validate your assumptions</u>. [Hint: try to find the Thevenin equivalent of the bottom circuit from the B terminal and ground] *[6]*

c) Assume, V_{bb} is changed **<u>from 5V to 5.1V</u>**, what happens to the outputs of the circuits? Calculate $I_b, I_{C,} I_E, V_{CE}$ and V_C again. Now for a 0.1V increase in input V_{bb}, what is the change of I_c? Use $\Delta I_C = I_{C(NEW)}$ -$I_{C(OLD)}$ *[3]*

d) ***[BONUS]*** Explain any use case of the differences in voltage increase between input and output. What could the use case be to such a phenomenon? *[1]*

Question 4

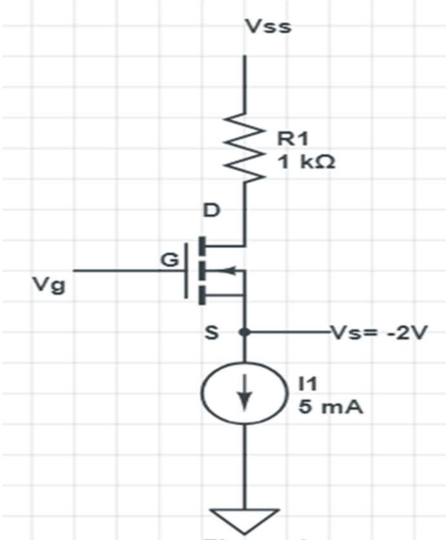


Figure-1

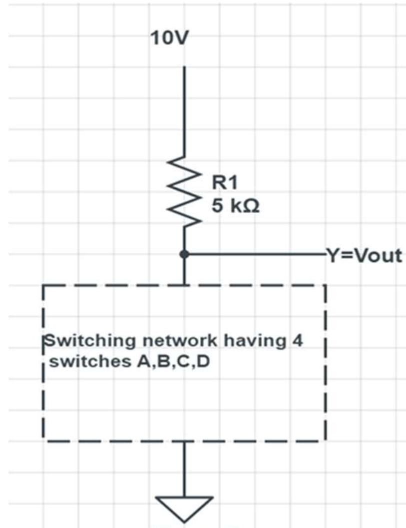


Figure-2

a) For the MOSFET in Figure-1, $V_T = 1\ V$ and $k_n{}' = 2\ mA/V^2$. Assume that the MOSFET is in **Saturation mode**. **Determine** the gate voltage, V_g and the minimum supply voltage, V_{ss} to operate the device in this condition. [Hint: $V_{OV} = V_{DS}$] *[3+2]*

b) In Figure-2, the MOSFET switching network turns ON the following conditions MUST be fulfilled -

i. 'A' MUST be ON

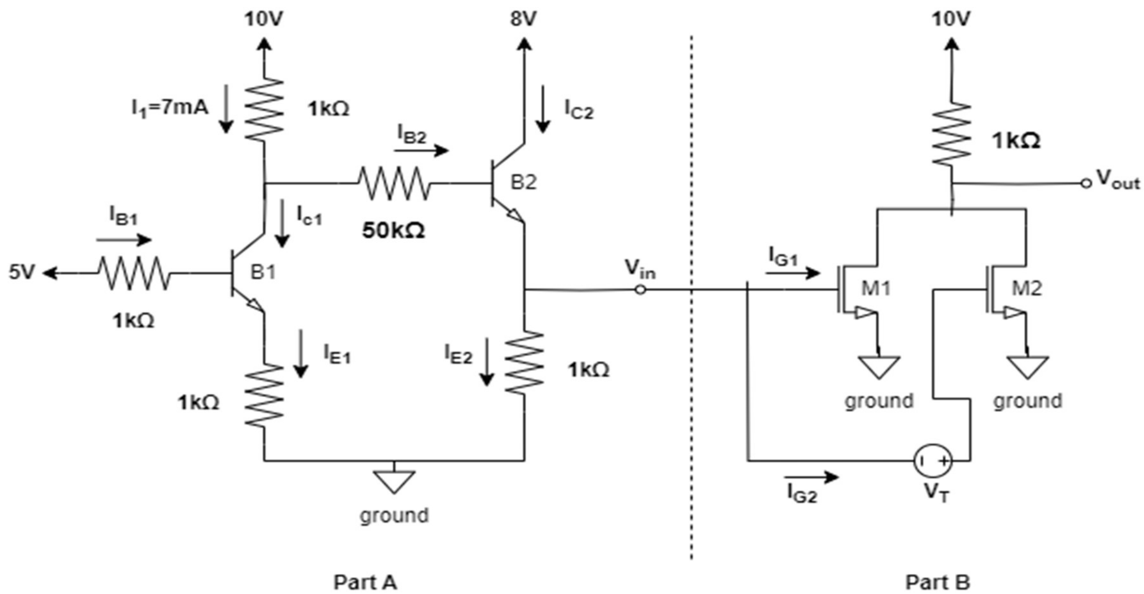
ii. 'B' and 'C' MUST be ON or 'D' MUST be ON

Deduce the logic function, F, using Boolean variables A, B, C, and D to implement these conditions. *[2]*

c) Assume, only A and D switches are ON in the switching network of Figure-2. **Find out** the output voltage, V_{out}. Let, $R_{ON} = 0.1\ k\Omega$ and use the SR model. *[3]*

d) ***[BONUS]*** In Figure-2, assume the input on a NOT gate is connected to V_{out}. **Explain** mathematically whether it will be possible to turn OFF the NOT gate when V_{out} is LOW. Assume, $V_T = 0.5\ V$, $V_{out} = V_{out(LOW)}$ of question(b). *[2]*

Question 5



In the circuit above, the BJTs have the following specification: β=100, Forward Active Region: $V_{BE} = 0.7\,V,\ I_C = \beta I_B$, Saturation Region: $V_{BE} = 0.8\,V,\ V_{CE} = 0.2\,V$,or the MOSFETs: $V_T = Threshold\ Voltage\ of\ M1\ and\ M2$.

a) **Determine** i_{g1} and i_{g2}. *[1]*

b) The SR model of MOSFET is more efficient than the S model- Justify this statement. *[1]*

c) Assume, B1 and B2 are in the **Saturation region. Calculate i_{c2}.** *[2]*

d) Assume, B1 is in the **Forward Active region. Calculate Vin.** *[4]*

e) **Draw the VTC** of Part- B assuming, $V_T = 8\,V$. [Use <u>S model</u> of MOSFETs]. *[2]*

Equations for MOSFET

$$I_D = 0,\ \text{if } V_{GS} < V_T$$

$$I_D = k\left[(V_{GS} - V_T)\,V_{DS} - \frac{1}{2}V_{DS}^2\right],\ \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{1}{2}k\,(V_{GS} - V_T)^2,\ \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq (V_{GS} - V_T)$$