BRAC University
Dept. of Computer Science and Engineering

Assessment: Assignment 5
Due: 11:59 PM 13 December 2023
Full Marks: **70**

Semester: Fall 2023
Course Code: CSE251
Section: **15/21**
Course Name: Electronic Devices and Circuits

Name: _____

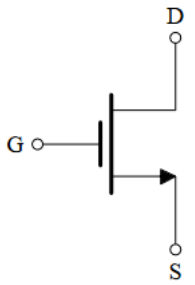
Student ID: _____

- ✓ Write down your student ID on the **top right corner of each of the pages**.
- ✓ Clearly write the solutions, along with the questions, on white paper with black ink (no need to use color pen, don't use pencils).
- ✓ Use **CamScanner**, or **Adobe Scan**, or **Microsoft Office Lens**, or any other software to scan the pages and make a **single PDF file**.
- ✓ After creating the PDF, make sure that **(a)** there are no pages missing, **(b)** all of the pages are legible, **(c)** your student ID on each page are visible.
- ✓ Please note, **collaboration ≠ copying**. You are allowed to discuss the questions and clear confusion you might have, but you have to write your solutions independently and be able to explain your answers during a random viva.
- ✓ **[Very Important]** Rename the PDF in the following format: **"A5_StudentID_FullNameWithoutSpace.pdf"**. For example, if my student ID is 12345678 and my name is Shadman Shahid, the filename should be **"A5_12345678_ShadmanShahid.pdf"**
- ✓ **ONE OF THE QUESTIONS IS BONUS (I.E., ONE OF THE QUESTION'S MARKS WONT BE COUNTED). I WON'T DISCLOSE WHICH ONE. THIS IS JUST SO THAT YOU WOULD NOT BE TENSED ABOUT THIS ASSIGNMENT. DO NOT WORRY ABOUT THE MARKS FOR NOW.**
- ✓ **Submission Link: Section-15 - https://forms.gle/6uLBBoCJUbTqiTC39, Section-21 - https://forms.gle/Kqs1L95qR1hqt4tm6**

Question 1: **CO1** 10 Marks

a) Consider an n-channel MOSFET with $k' = 0.2\ \text{mA/V}^2$ and $V_t = 0.7\ \text{V}$ and $\frac{W}{L} = 10$. Find the drain current for the following cases:

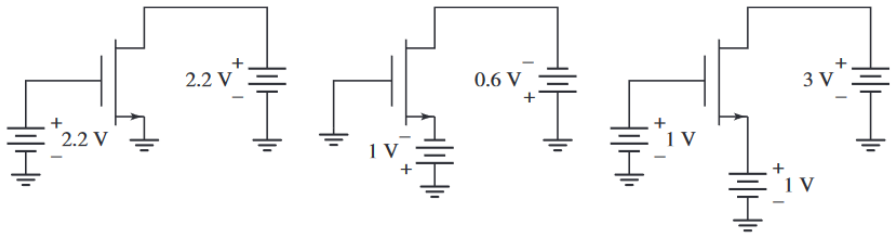
(a) $v_{GS} = 5\ \text{V}$ and $v_{DS} = 1\ \text{V}$
(b) $v_{GS} = 2\ \text{V}$ and $v_{DS} = 1.3\ \text{V}$
(c) $v_{GS} = 5\ \text{V}$ and $v_{DS} = 0.2\ \text{V}$
(d) $v_{GS} = v_{DS} = 5\ \text{V}$



b) The table below lists 5 different cases labeled (a) to (e) for operating an NMOS transistor with V. In each case the voltages at the source, gate, and drain (relative to the circuit ground) are specified. You are required to complete the table entries. Note that if you encounter a case for which is negative, you should exchange the drain and source before solving the problem. You can do this because the MOSFET is a symmetric device.

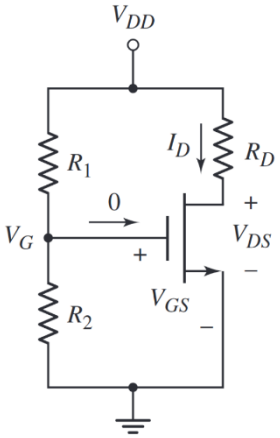
Case	Voltage (V)						Region of operation
	V_S	V_G	V_D	V_{GS}	V_{OV}	V_{DS}	
a	+1.0	+1.0	+2.0				
b	+1.0	+2.5	+2.0				
c	+1.0	+2.5	+1.5				
d	+1.0	+1.5	0				
e	0	+2.5	1.0				

c) The threshold voltage of each transistor in Figure P3.5 is $\boldsymbol{V_{TN} = 0.4\ \text{V}}$. Determine the region of operation of the transistor in each circuit.



Question 2: 10 Marks

a. Calculate the **drain current** and **drain-to-source voltage** of a common source circuit with an **n-channel** enhancement-mode MOSFET. Find the power dissipated in the transistor. (Power dissipated in the transistor is $P_{\text{NMOS}} = \boldsymbol{I_D \cdot V_{DS}}$) [CO2] 4



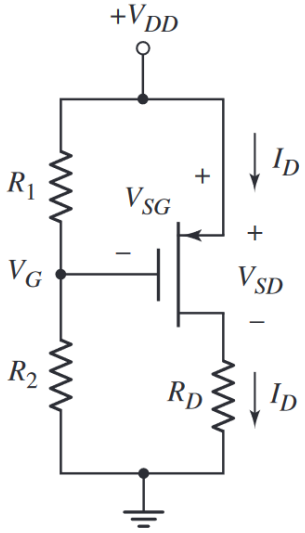
For the circuit shown in, assume that $R_1 = 30\ \text{k}\Omega$, $R_2 = R_D = 20\ \text{k}\Omega$, $V_{DD} = 5\ \text{V}$, $V_{TN} = 1\ \text{V}$, and $k_n = 0.1\ \text{ma/V}^2$

b. Calculate the **drain current** and **drain-to-source voltage** of a common source circuit with an **p-channel** enhancement-mode MOSFET. Find the power dissipated in the transistor. (Power dissipated in the transistor is $P_{\text{PMOS}} = \boldsymbol{I_D \cdot V_{SD}}$) [CO2] 6

For the circuit shown in, assume that $R_1 = R_2 = 50\ \text{k}\Omega$, $R_D = 7.5\ \text{k}\Omega$, $V_{DD} = 5\ \text{V}$, $V_{TP} = -0.8\ \text{V}$, and $k_p = 0.2\ \text{ma/V}^2$

****PS**: For PMOS the current equations are:

PMOS is **NOT** in Cut-off when $\boldsymbol{V_{GS} < V_{TP}}$ or $\boldsymbol{V_{SG} > |V_{TP}|}$.



i. **Triode mode ($\boldsymbol{V_{DS} < V_{GS} - V_{TP}}$ or $\boldsymbol{V_{SD} > V_{SG} + V_{TP}}$)**

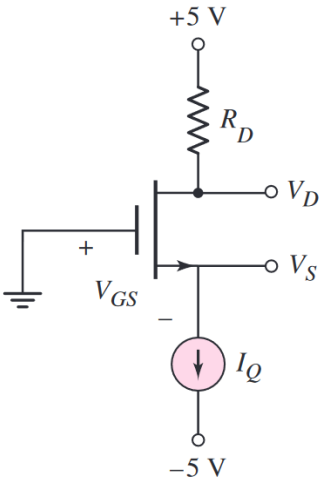
$$I_D = k_p\left(V_{SG} + V_{TP} - \frac{1}{2}V_{SD}\right)V_{SD}$$

ii. **Saturation mode ($\boldsymbol{V_{DS} > V_{GS} - V_{TP}}$ or $\boldsymbol{V_{SD} < V_{SG} + V_{TP}}$)**

$$I_D = \frac{k_p}{2}(\boldsymbol{V_{SG} + V_{TP}})^{\boldsymbol{2}}$$

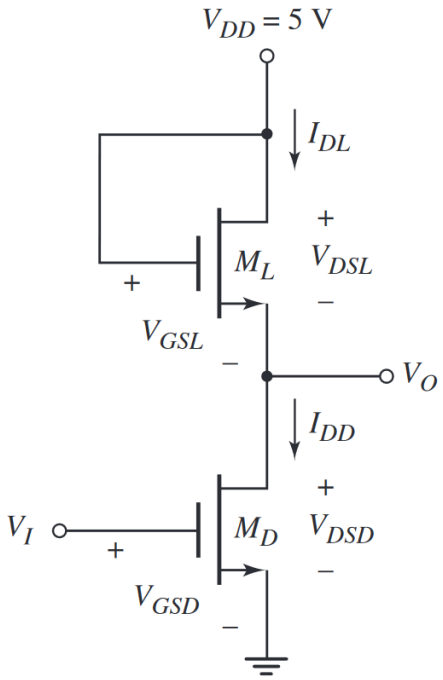
Question 3: 20 Marks

a) Find the W/L sizing of the MOSFET when $\boldsymbol{R_D = 10\ k\Omega}$, $I_Q = 250\ \mu A$, and $V_D = 2.5\ V$. Assume that the MOSFET has a threshold voltage of $V_{TN} = 0.8\ V$ and a transconductance of $k_n = 80\ \mu A/V^2$ [CO3] 5

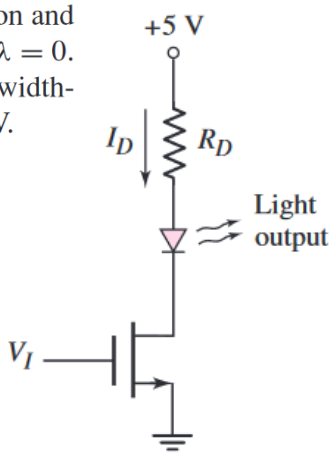


b) Determine the dc transistor currents and voltages in the given circuit. (Determine $\boldsymbol{V_O}$, $\boldsymbol{I_{DL}}$ and $\boldsymbol{I_{DD}}$ for $\boldsymbol{V_I} =$ 5 V) [CO3] 5

For the transistors, $V_{TNL} = V_{TND} = 1\ V$, $k_{nD} = 50\ \mu a/V^2$, $k_{nL} = 10\ \mu a/V^2$, , $V_{DD} = 5\ V$, (The subscript D applies to the lower transistor and the subscript L applies to the upper transistor.)

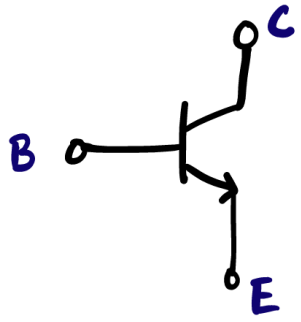


c) The transistor in the circuit in Figure P3.51 is used to turn the LED on and off. The transistor parameters are $V_{TN} = 0.6\ V$, $k_n' = 80\ \mu A/V^2$, and $\lambda = 0$. The diode cut-in voltage is $V_\gamma = 1.6\ V$. Design R_D and the transistor width-to-length ratio such that $I_D = 12\ mA$ for $V_I = 5\ V$ and $V_{DS} = 0.15\ V$. [CO3] 7



Question 4: **CO1** 8 Marks

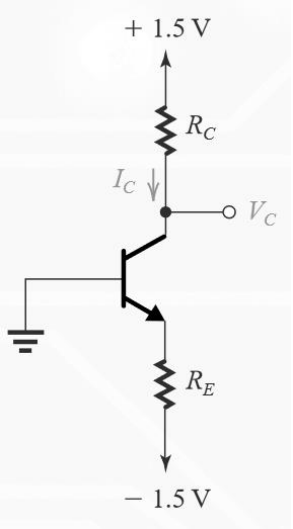
The terminal voltages of various npn transistors are measured during operation in their respective circuits with the following results. In this table, where the entries are in volts, 0 indicates the reference voltage. For each case, identify the mode of operation of the transistor.



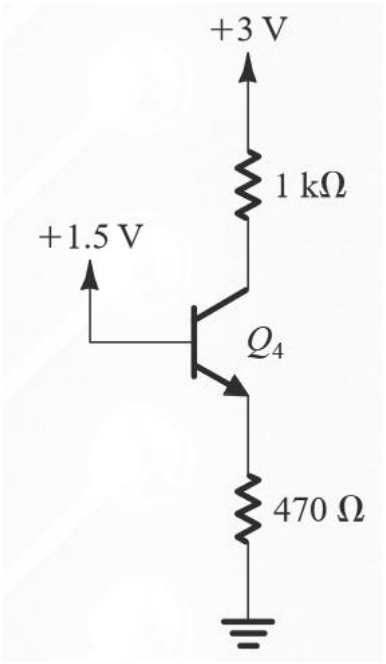
Case	E	B	C	Mode
1.	0	0.7	0.7	
2.	0	0.8	0.1	
3.	-0.7	0	0.7	
4.	-2.7	-2	0	

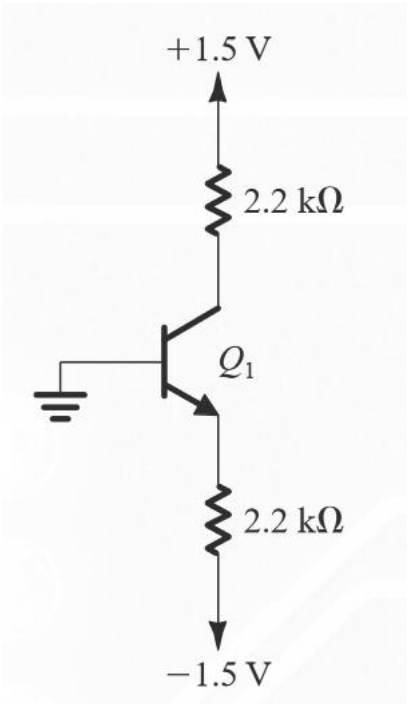
Question 5 — 10 Marks

a. Design the circuit, i.e., determine the Resistor values, to establish $I_C = 0.1\ \text{mA}$ and $V_C = 0.5\ \text{V}$. The transistor exhibits $v_{BE} = 0.8\ \text{V}$ at $i_c = 1\ \text{mA}$, and $\beta = 100$. [CO3] 4



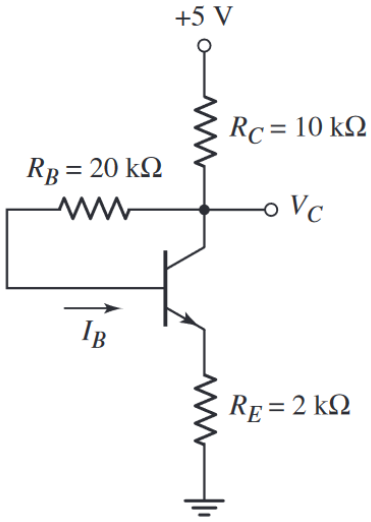
b. For each of the given circuits, find the emitter, base and collector voltages and currents. Use $\beta = 50$ and assume $|V_{BE}| = 0.8\ \text{V}$. [CO3] 6

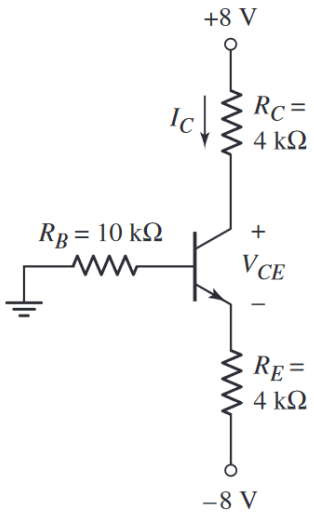




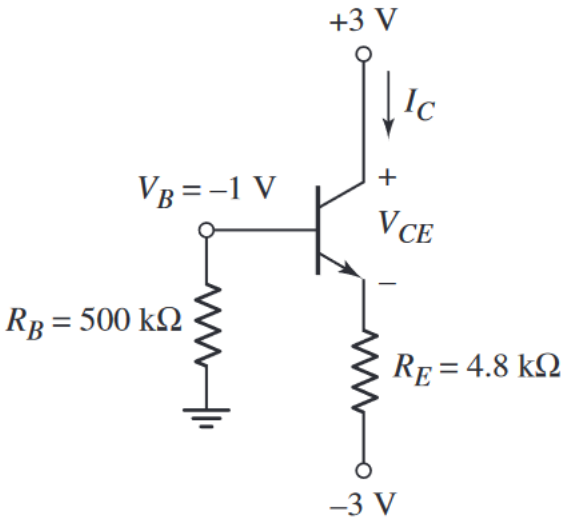
Question 6 — 10 Marks

a. For the transistors in the adjacent figure, $\boldsymbol{\beta = 75}$. Find the labelled voltages and currents [CO2] 6
(Assume $V_{BE_0} = 0.7$ V, $V_{CE(\text{sat})} = 0.2$ V)



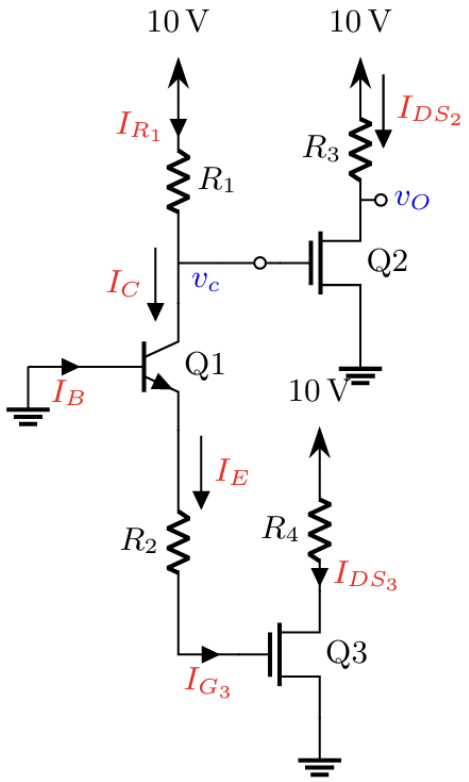


b. In the circuit shown in adjacent figure, the values of measured parameters are shown. Determine $\boldsymbol{\beta, \alpha}$, and the other labeled currents and voltages. [CO2] 4



Question 7: CO2 — 12 Marks

For the following circuit, $R_1 = 1\text{k}\Omega$, $R_2 = 2\text{k}\Omega$, $R_3 = 3\text{k}\Omega$, $R_4 = 4\text{k}\Omega$



For BJT

$\beta = 100$

$\alpha = 0.99$

$v_{BE(\text{Active})} = 0.7\,\text{V}$

$v_{BE(\text{Saturation})} = 0.8\,\text{V}$

$v_{CE(\text{Saturation})} = 0.2\,\text{V}$

for MOSFETs

$V_T = 1\,\text{V}$

$k = 5\,\text{mA/V}^2$

(a) **[5 marks]** **Analyze** the circuit to **determine** the values of I_C, I_B, I_E, v_C.

(b) **[5 marks]** **Analyze** the circuit to determine the value of I_{DS_2}, v_O.