CHITTAGONG UNIVERSITY OF ENGINEERING & TECHNOLOGY

Department of Electronics And Telecommunication Engineering

Lab Report

Experiment Name: Layout Generation of an Inverter using Virtuoso L

Experiment No.: 05

Course Title: VLSI technology Sessional

Course No.: ETE 404

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Objectives:

- To create a layout view of the basic inverter in Virtuoso Layout Editor.
- To design the layout keeping basic design rules in mind.
- To design cell layout of a constant height for use in hierarchical design.

Required Software:

- Cadence Virtuoso

Design Process:

- At first virtuoso was opened from the terminal & a new file was opened.
- Layout display configuration was set up.
- DRD Notify was turned on.
- Contact Layer was drawn. Both width & height is 0.12µm
- Same contact was copied at a distance of 0.3µm
- Now, oxide was drawn & contact to oxide spacing is minimum 0.06 µm
- Nimp layer was drawn, which must extend from the oxide layer by a minimum of 0.14 µm.
- The whole layer now was copied at the bottom of the layout. The distance is 2 µm.
- Upper portion of the layer was converted to pimp layer.
- A poly layer was created. This layer must be of 0.1 µm in width and in between the two contacts, extending from the oxide layer by 0.18 µm
- Drain regions of the NMOS and PMOS was connected. Also the source of both MOS's to respective body terminals using 'Metal1 (drw)' layer was connected. Drains of the MOS's using 'Metal1 (drw)' layer was also connected.
- PMOS should be in 'Nwell (drw)'. So, An 'Nwell (drw)' rectangle surrounding both the PMOS and the body contact for PMOS was drawn.
- Pins were placed.
- Now it is time to create a contact between 'Poly' and 'Metal1' layer by pressing 'o' to 'create via' and selecting 'M1_POv' under 'via definition' and placing it on layout.
- Also a 'Metal1 (drw)' rectangle on the via was drawn, because the default Metal1 rectangle area is less than the required minimum.
- Now, Create > Pin was executed to create pins for vdd!, gnd!, in and out. For in, vdd! and gnd! 'input' as 'I/O type' was selected and for out, 'output' as 'I/O type' was selected.

- Rectangles were drawn on the Poly-Metal1 via for ‘in’ pin, PMOS source-to-body ‘Metal1’ connection for ‘vdd!’ pin and NMOS source-to-body connection for ‘gnd!’ pin.
- For ‘out’ pin, rectangle was drawn on the Metal1 layer connecting the two drains of MOS’s.
- Finally, Metal2 paths of 0.5 µm width was added for power rails and connect them to power nets in Metal1 by using Metal1 to Metal2 via by invoking ‘create via’.
- The P-type portion is shown in figure-1, N-type portion is shown in figure-2 & whole layout is shown in figure-3.

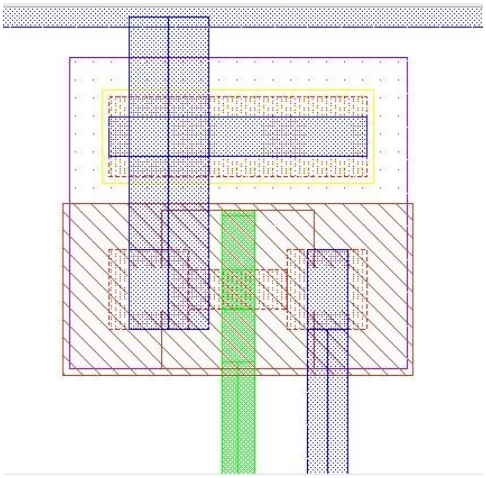

Figure 1 : Layout of P-type portion

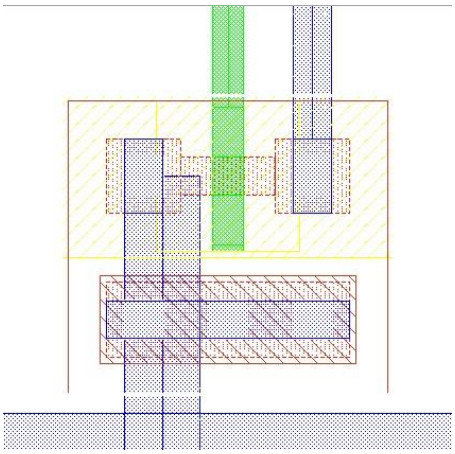

Figure 2 : Layout of N-type portion

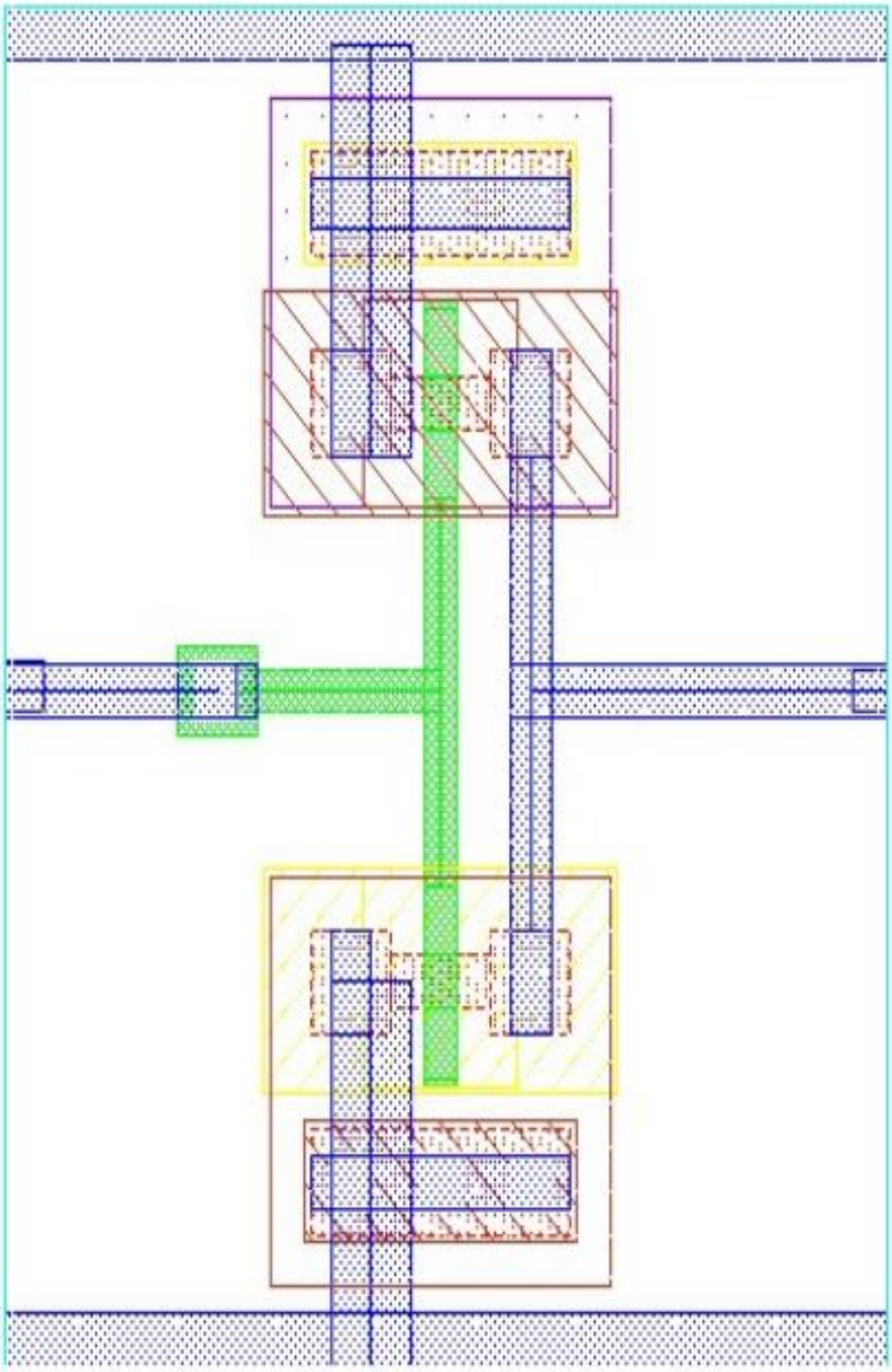

Figure 3 : Final Layout

Home Task:

- A p-substrate contact was created which is shown in figure-4.

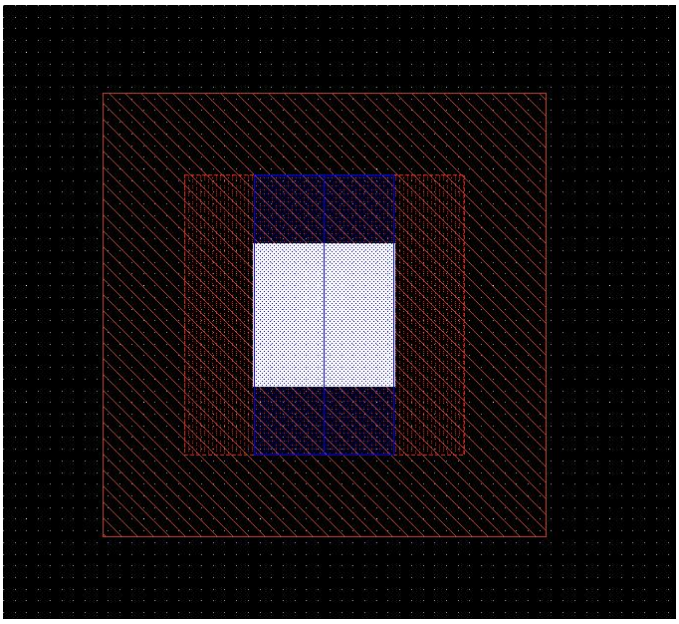

Figure 4 : P-substrate Contact

- An N-substrate contact was created which is shown in figure-5

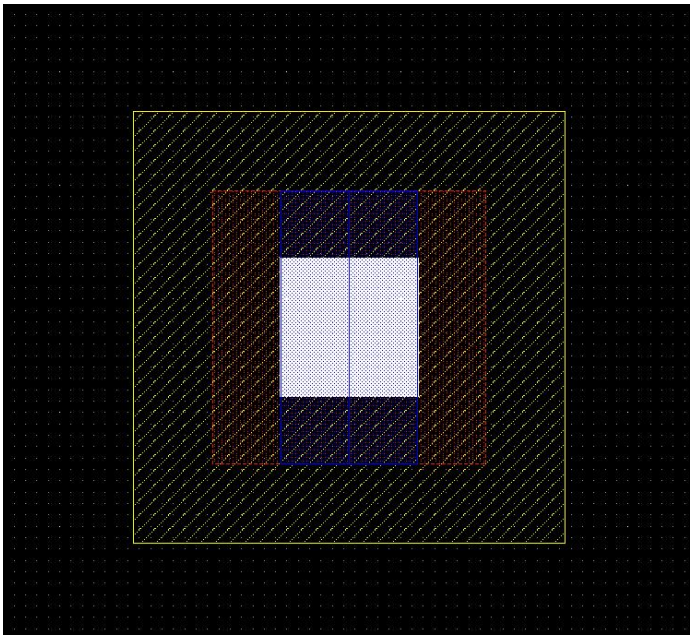

Figure 5 : N-substrate Contact

Discussion:

This experiment involved designing an inverter layout using Virtuoso L, a tool for integrated circuit (IC) design. The layout depicted the circuit with geometric shapes representing different materials and layers like metal, polysilicon, oxide, and diffusion, which form the IC components such as resistors, inductors, capacitors, and transistors. During the design process, performance and size were carefully considered. The project followed an ASIC (Application-Specific Integrated Circuit) design flow, which includes stages like specification, RTL design, synthesis, placement, routing, and verification. Even though a full-custom IC design approach was used, a consistent cell height was maintained throughout the cell library. Full-custom design allows for optimizing performance, power, and area but is more time-consuming and complex. An error was found in the nwell layer size, which was corrected. The nwell is crucial for creating p-type regions in CMOS technology, essential for the proper function of PMOS transistors. After fixing this issue, the design was successful, meeting the intended specifications and performance criteria.