CHITTAGONG UNIVERSITY OF ENGINEERING & TECHNOLOGY

Department of Electronics And Telecommunication Engineering

Lab Report

Experiment Name: DC Analysis and Symbol Creation of Inverter and AND Gate

Experiment No.: 04

Course Title: VLSI technology Sessional

Course No.: ETE 404

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Objective:

- To familiarize with DC sweep and parametric simulation in ADE L.
- To familiarize with symbol creation from schematic view.

Required Software:

- Cadence Virtuoso

Design Process:

- At first Virtuoso was started using **virtuoso** & command.
- Then a new library was created and under this library a cell view was created.
- After this a schematic view was showed and under **gpdk090** library design CMOS Inverter using pmos1v, nmos1v, vdd, vdc and gnd shown in figure 1

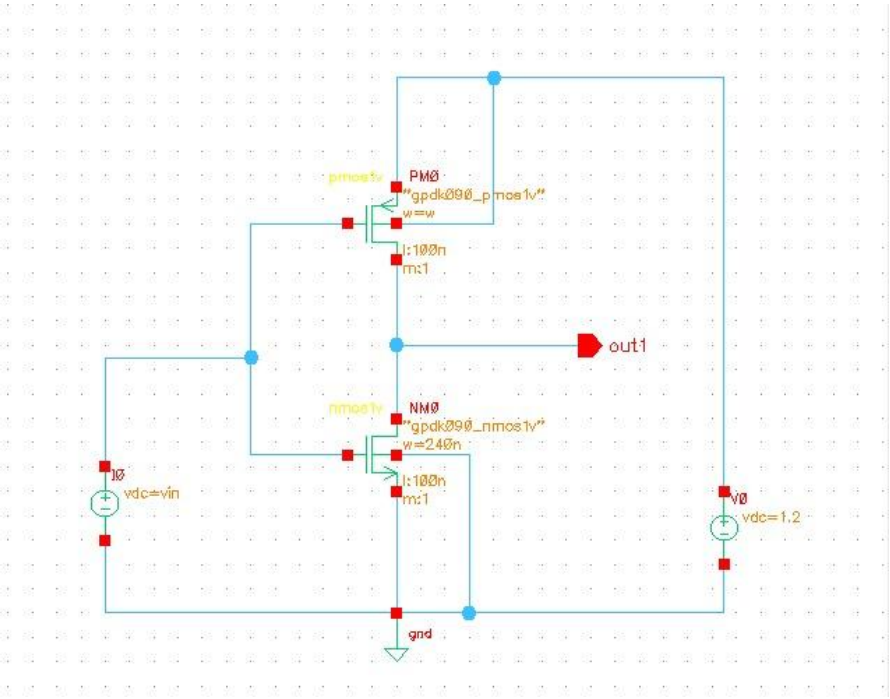

Figure 1: Schematic diagram of CMOS inverter with DC input

After complete the schematic design, it has been "**Check and Save".**

- Then, under Analog Design Environment L (ADE L) transient analysis, vdd, gnd and input voltage was sated.
- In ADE L, under the execute Tools there was an option Parametric Analysis.
- Click on 'Add Variable'. From the drop down menu select 'w'. Put From: 240n and To: 720n. Select Step Mode: Linear Steps from the drop down and put Step Size: 120n.
- Then clicked Net list and Run. And input, output plot has been shown like figure 2.

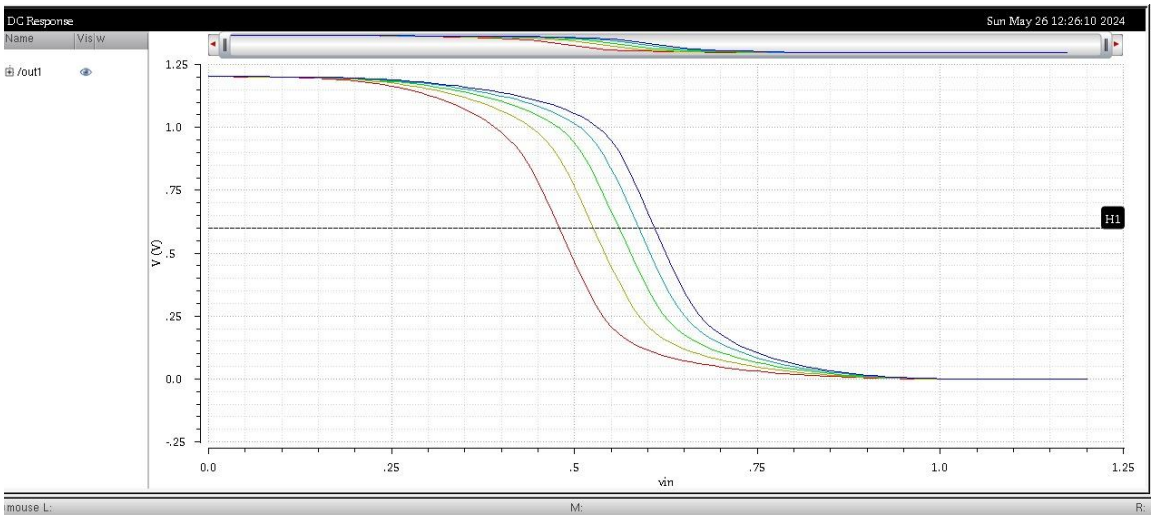

Figure 2: DC response of Inverter for different width of PMOS

- To generate symbol, go to Create > Cellview > From Cellview
- Under shape and polygon option there was different shape. And design a NOT gate. The design of NOT gate or inverter was shown in figure 3.

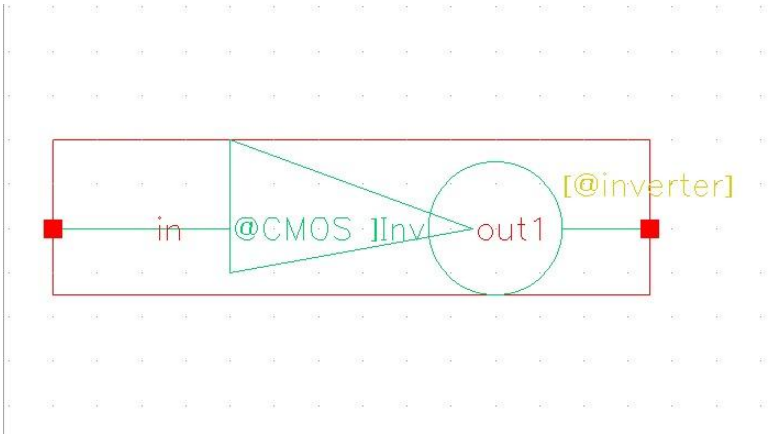

Figure 3: Symbol of CMOS Inverter

- Now it is time to design AND gate using NAND gate and Inverter. The schematic design od NAD gate is shown in figure 4.
- After complete the schematic design, it has been "**Check and Save".**
- Then, under Analog Design Environment L (ADE L) transient analysis, vdd, gnd and inputs voltage was sated.
- The inputs and output plot was shown in figure 5.

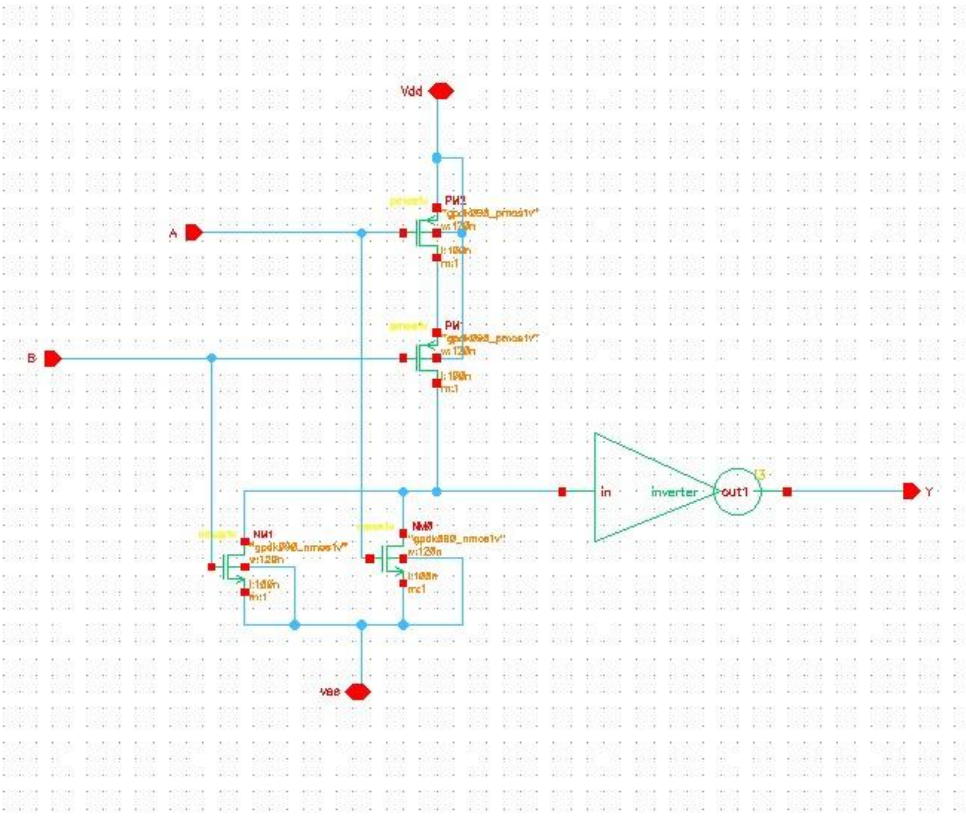

Figure 4: Schematic diagram od CMOS AND gate

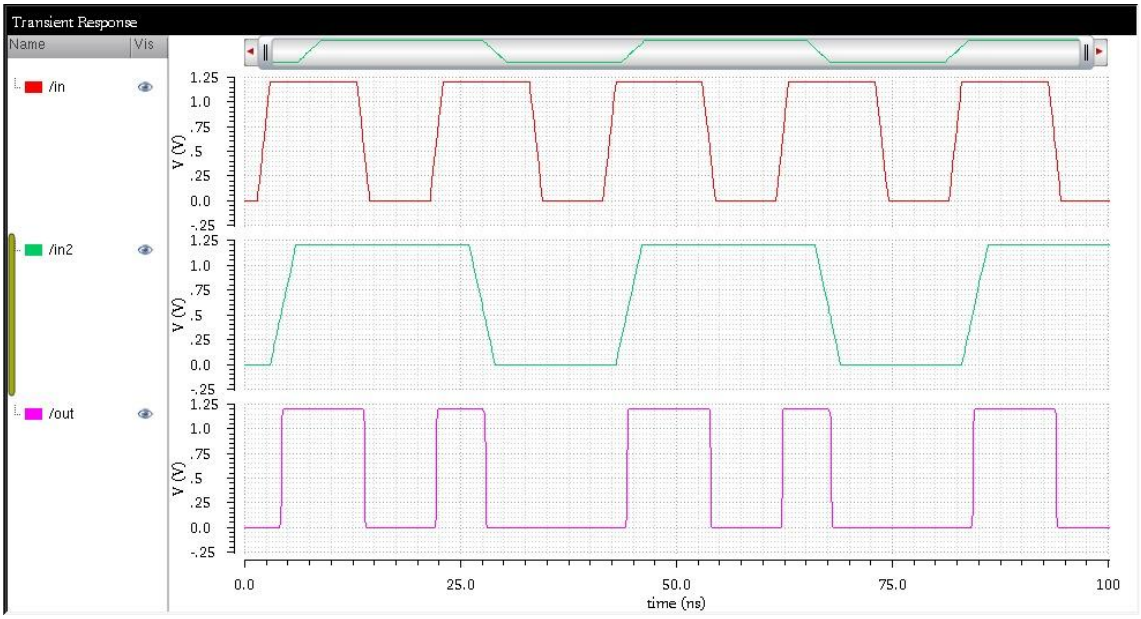

Figure 5: Inputs and output plot of CMOS AND gate

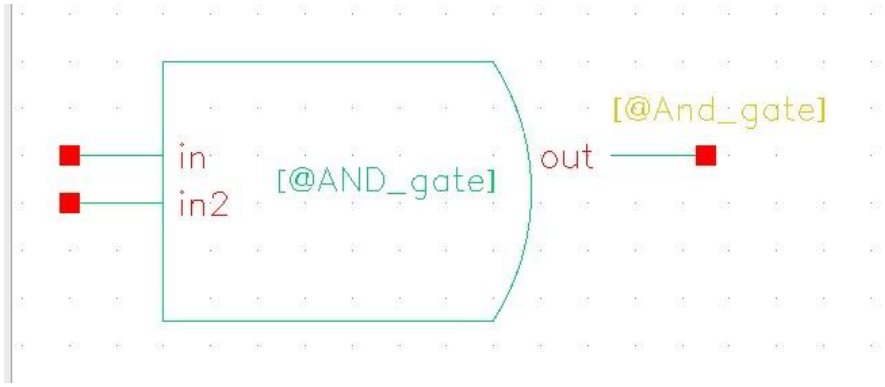

Figure 6 : Symbol of AND gate

Home Task:

Using the similar process of PMOS parametric sweep we calculate value of NMOS voltage for different width. The width was 120n to 480n. The result of DC parametric sweep was given in figure 6

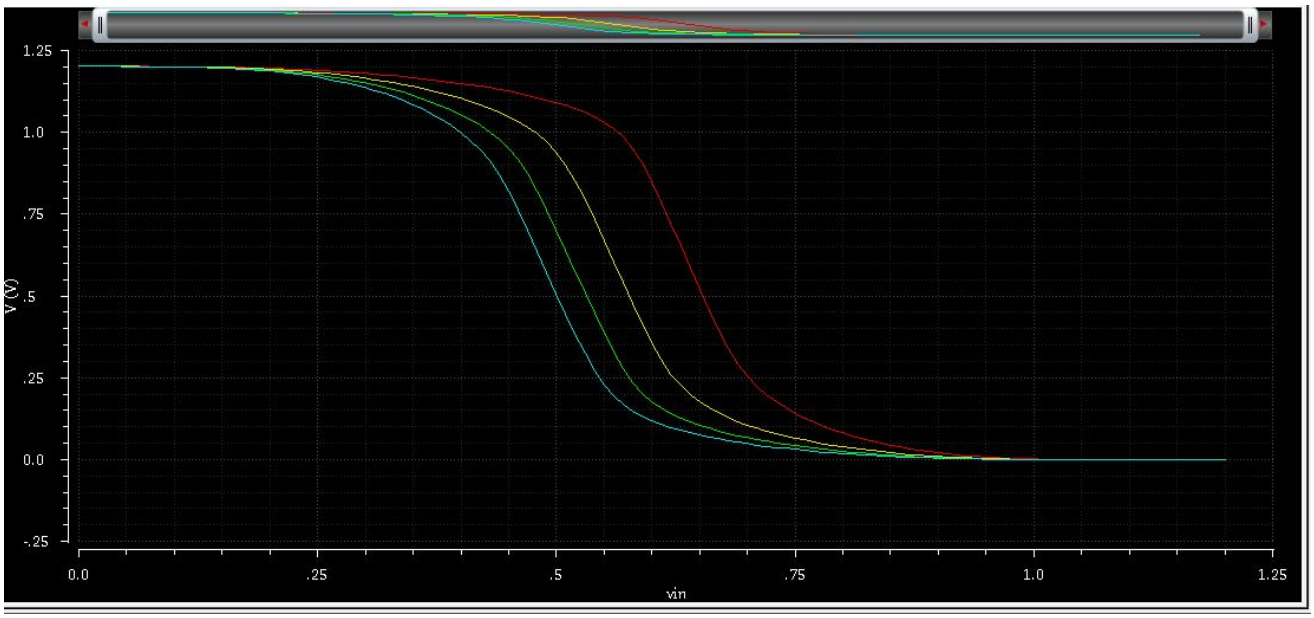

Figure 7: DC response of Inverter for different width of NMOS

- After this we have to design schematic diagram od OR gate using NMOS, PMOS, and symbol of Inverter.
- The schematic of OR gate was shown in figure 7.

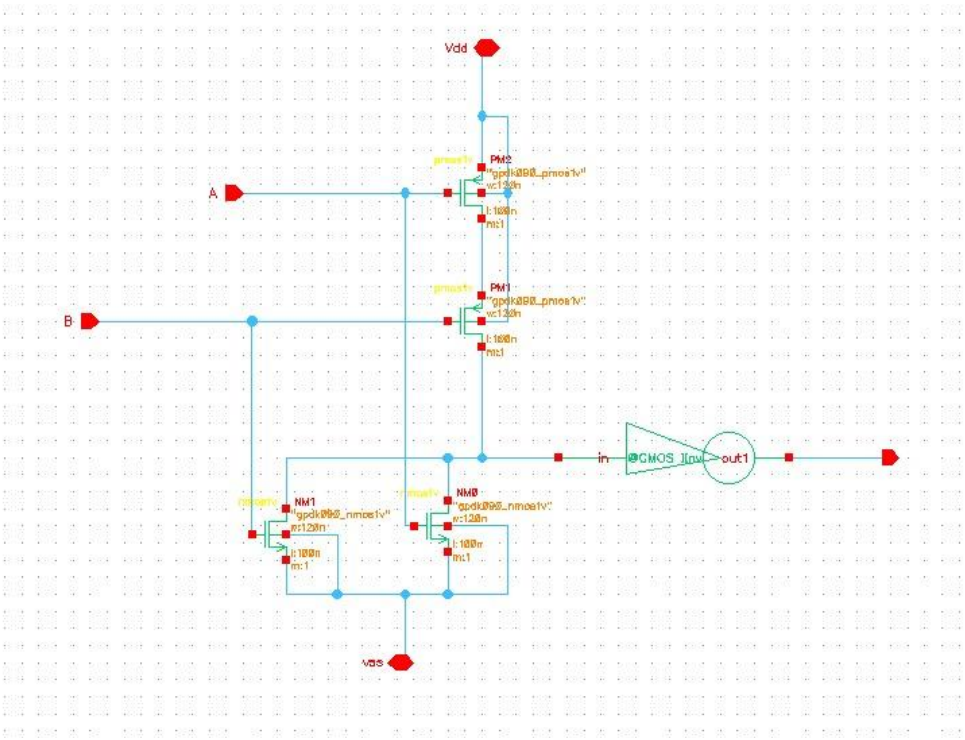

Figure 8: Schematic diagram of CMOS OR gate

- Same process as AND gate was applied to create symbol of OR gate and to setup the value for OR gate.
- The inputs and output plot of OR gate was given in figure 8.

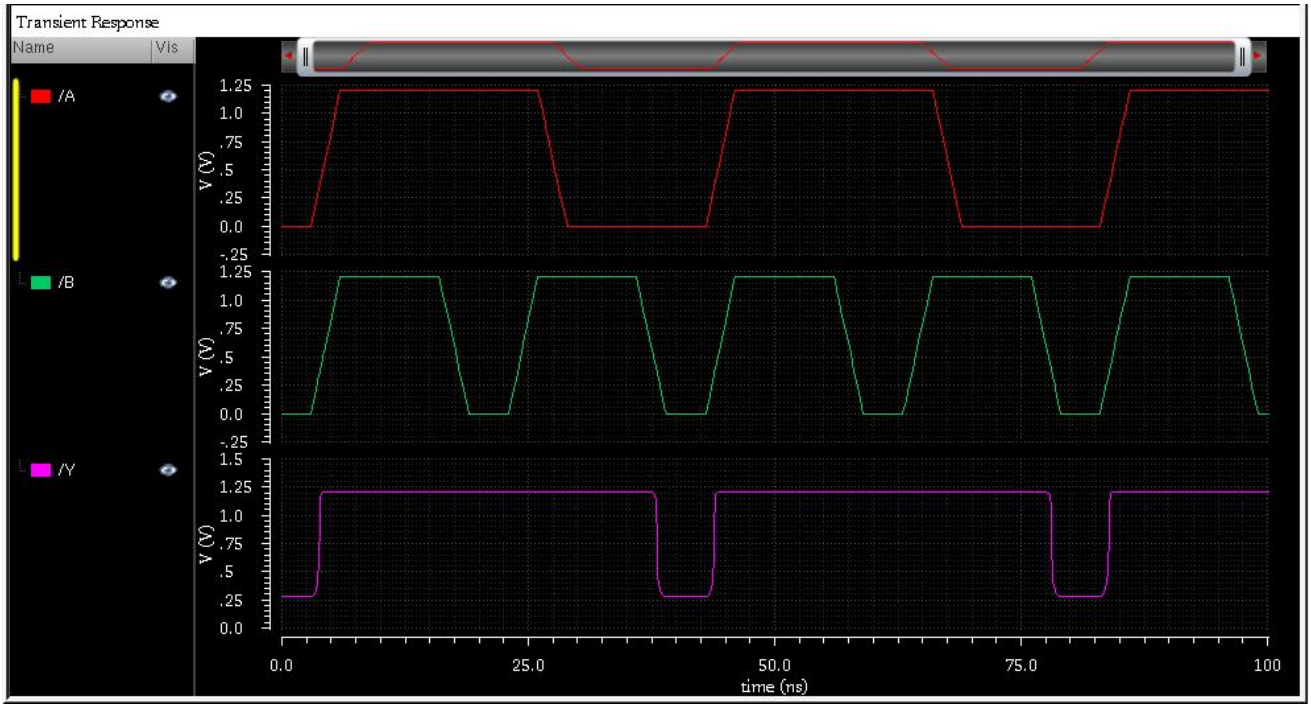

Figure 9: Inputs and output plot of CMOS OR gate

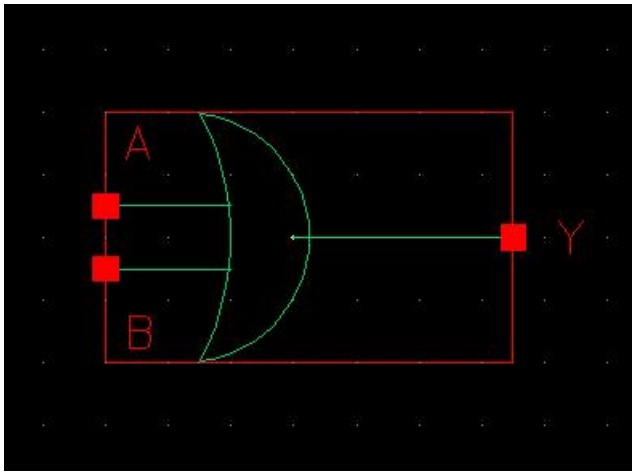

Figure 10 : Symbol of OR gate

Discussion:

This project focused on the DC analysis and symbol creation for an inverter and an AND gate. It detailed the steps for conducting DC analysis and creating symbols for an inverter circuit using Cadence Virtuoso. During the DC analysis of the PMOS transistor, it was observed that power dissipation decreased with an increase in the PMOS width and increased with a decrease in width. Additionally, the project included a brief discussion on the schematic diagram and symbol creation process for both AND and OR gates within the same software.