CHITTAGONG UNIVERSITY OF ENGINEERING & TECHNOLOGY

Department of Electronics And Telecommunication Engineering

Lab Report

Experiment Name: DRC, LVS, RCX and Post-Layout Simulation of an Inverter

Experiment No.: 06

Course Title: VLSI technology Sessional

Course No.: ETE 404

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Objectives :

- To perform Design Rules Check (DRC) and Layout vs. Schematic (LVS).
- To extract parasitic resistance and capacitance from layout.
- To perform transient simulation of extracted view.

Software Requirements :

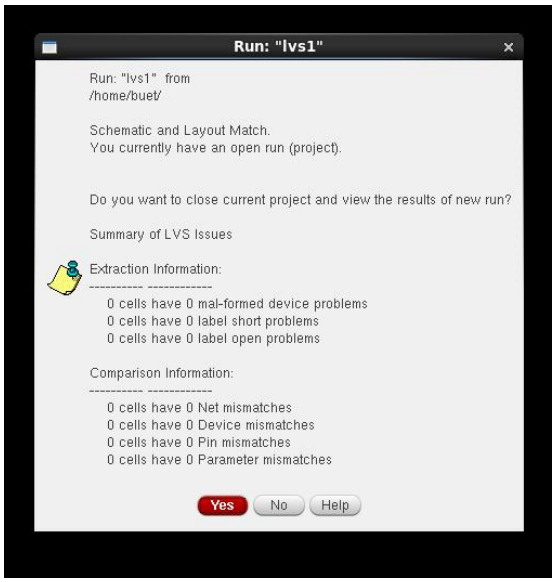
- Cadence Virtuoso

DRC Using Assura :

- Assura technology lib was selected by executing Assura > Technology.
- Assura > Run DRC was executed.
- All errors were solved.

LVS Using Assura:

- Assura > Run LVS. Was executed.
- All mismatches were solved.



Parasitic Extraction Using RCX:

- Assura > Open Run was executed.
- Final error free LVS run name was selected.
- Assura > Run RCX was executed.
- Extracted View in the output field under Setup tab was selected.
- RC as Extraction Type was selected.
- Name of the reference node was given as ‘gnd!’
- Finally we have the extracted view.

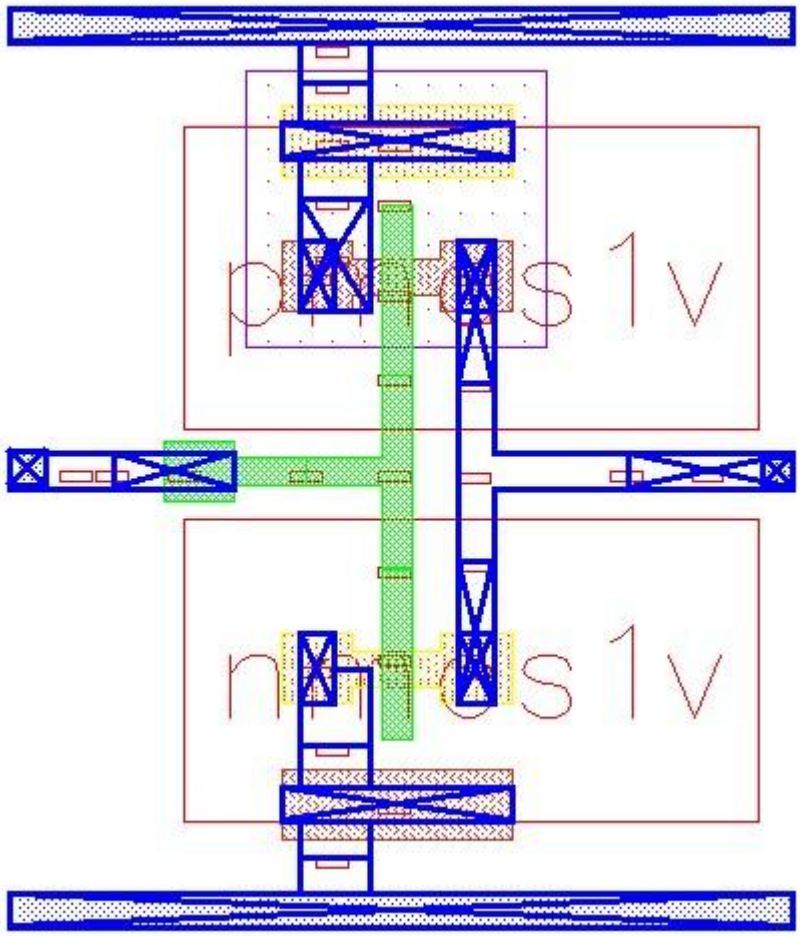


Figure : Extracted View

- ADE L from the av_extracted view was launched.
- After setting everything else, Outputs > To be plotted > Select on design was executed.
- Final result was simulated and observed which is shown in the following two figures :

Figure : Delay Result

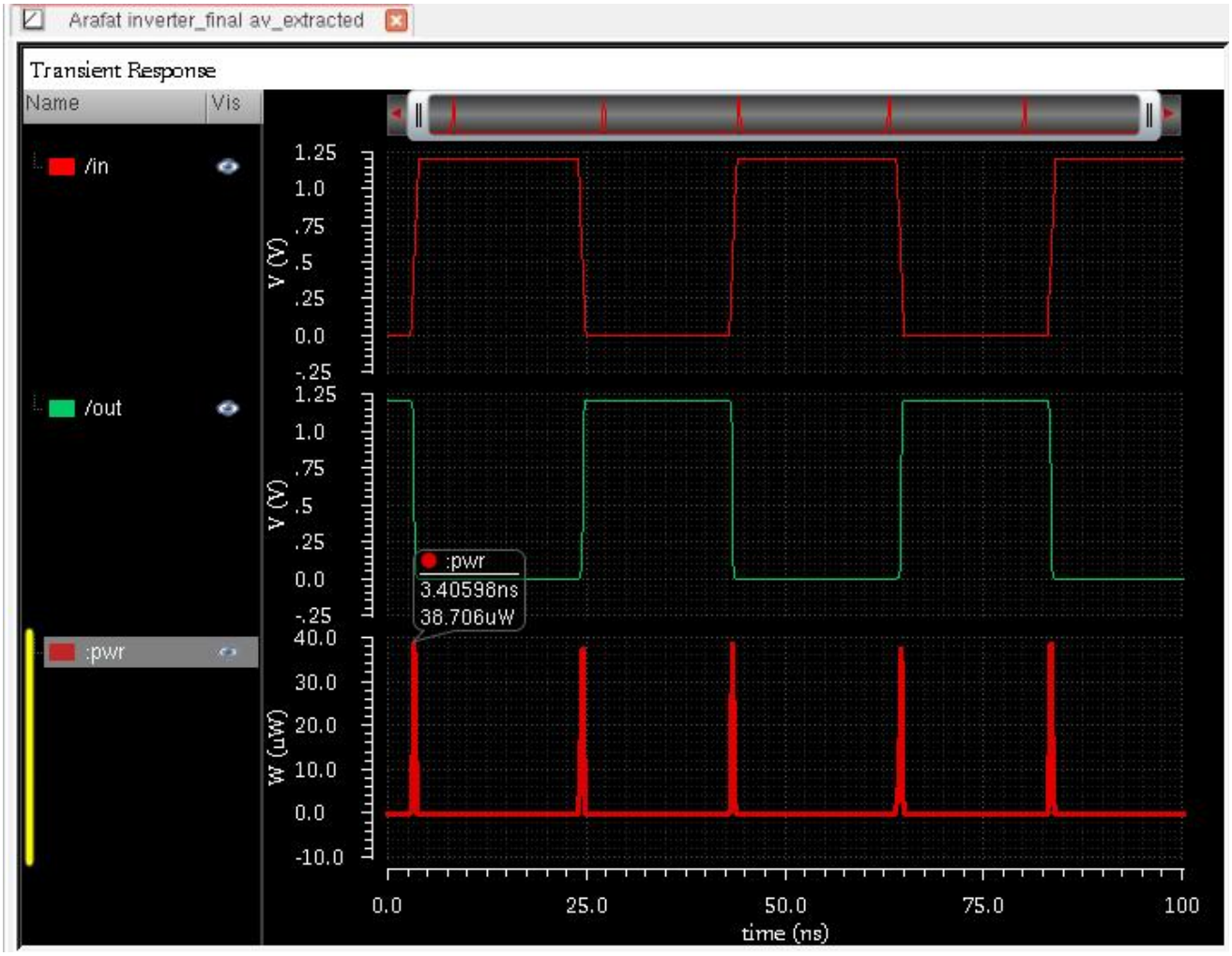


Figure : Output Curve & Power Result

From above two figure, it is seen that delay is 116ps and maximum power draw is 38.7 μW.

Home Task :

An inverter's power consumption and propagation delay are increased by parasitic RC components. Resistive effects lead to static power dissipation and affect signal rise and fall times, while capacitive effects slow the charging and discharging of the output node, increasing dynamic power dissipation. To mitigate these parasitic effects, designers can optimize the layout and interconnect lengths, and employ strategies such as buffering, shielding, and impedance matching throughout the design process.

Discussion :

In this experiment, DRC (Design Rule Check), LVS (Layout vs. Schematic), RCX (Resistor-Capacitor Extraction), and Post-Layout simulation of an inverter were performed. A few errors were identified in the Error Layer Window. These errors were corrected by locating them via the error window and navigating to their positions using the right arrow key. During the LVS check, two mismatches were found: pin mismatch and parameter mismatch. The parameter mismatch was due to the PMOS width being different in the layout and the schematic. To resolve this, the PMOS width in the inverter layout was adjusted to match the schematic. Once these adjustments were made, the schematic and layout matched. The remainder of the experiment proceeded without significant difficulties.