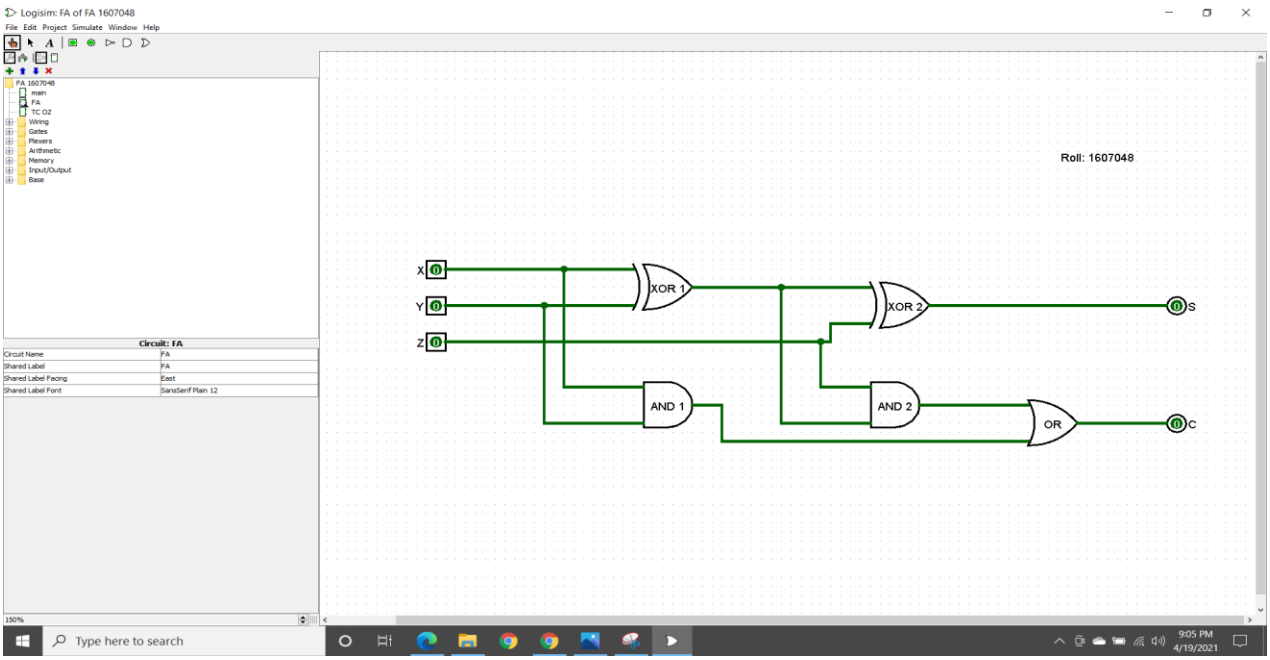
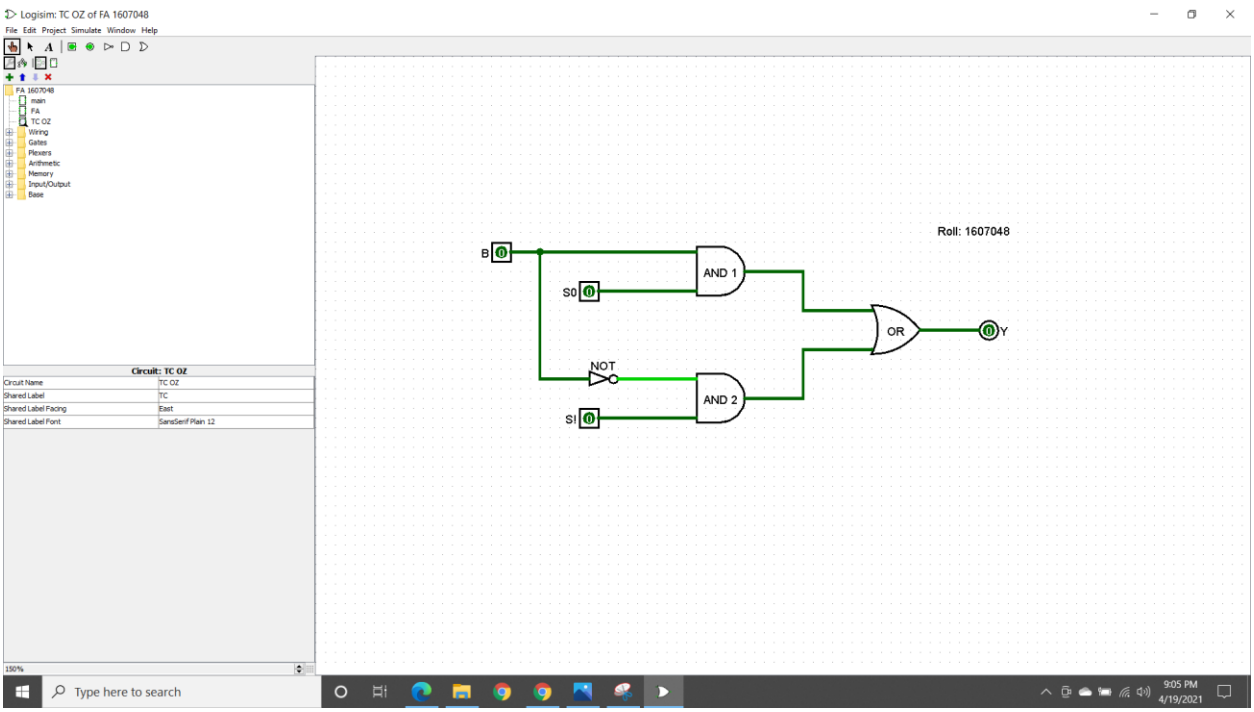
Name: Faisal Ahmed, Roll: 1607048

Circuit Design

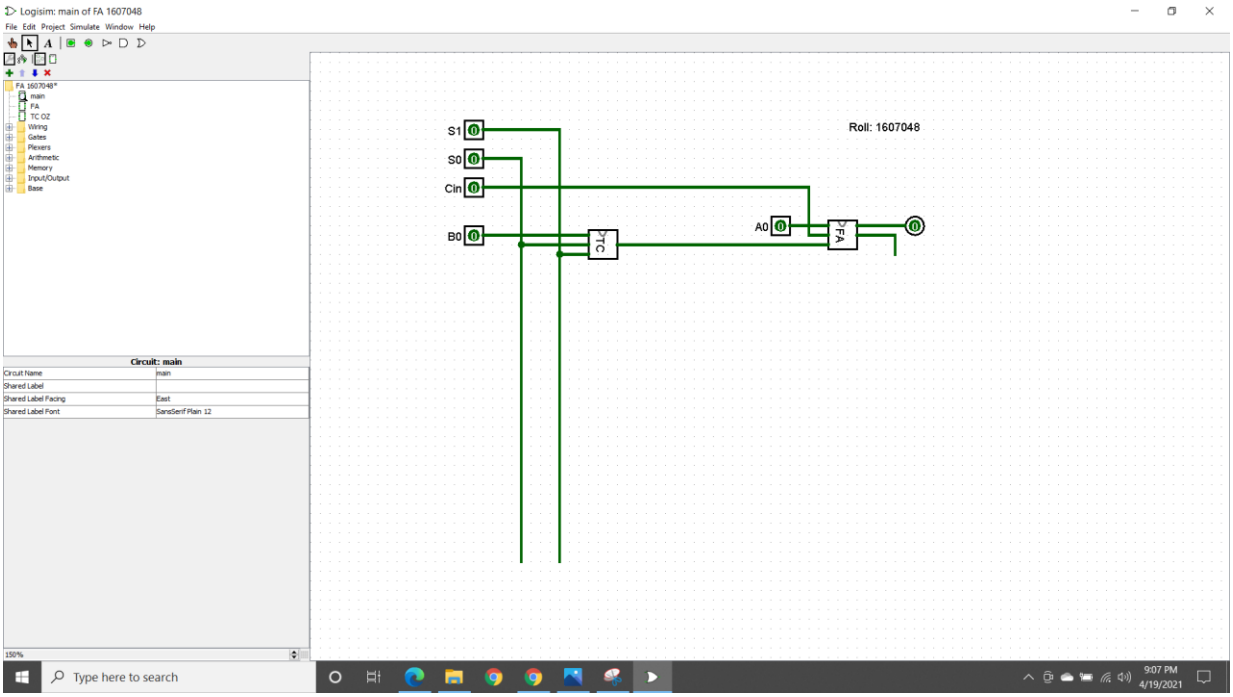
X-OR Gate



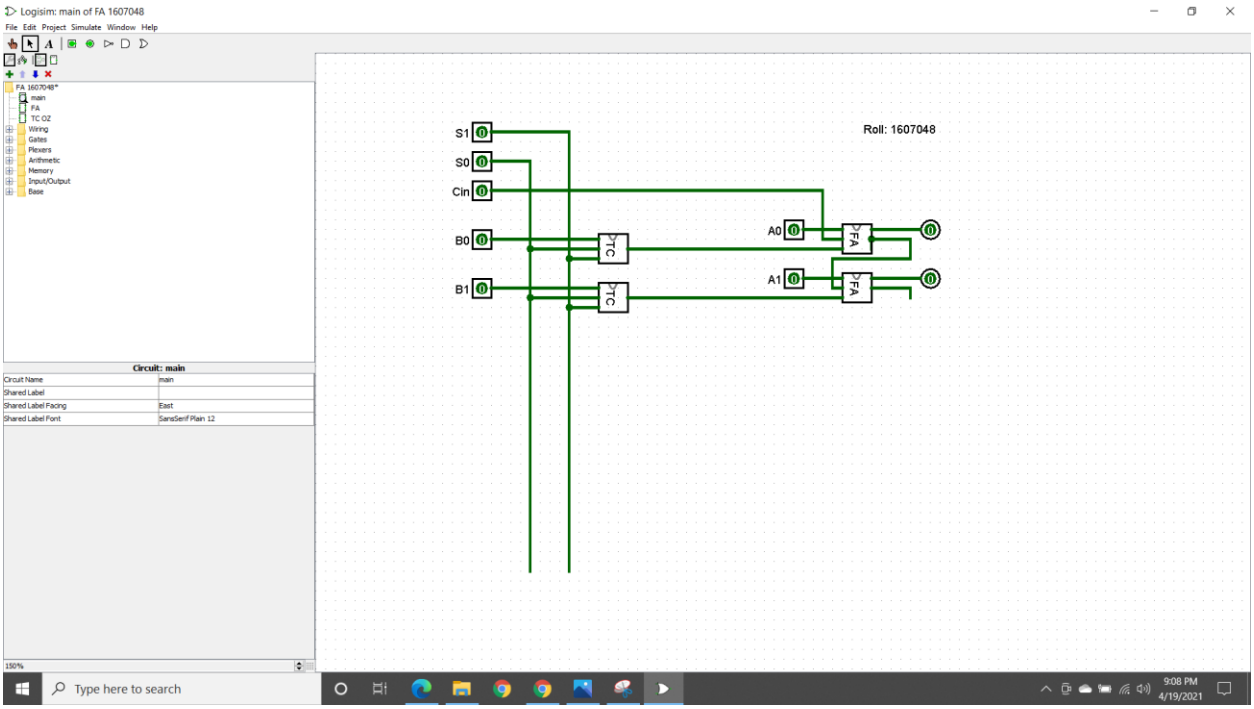
True Compliant or One Zero Circuit



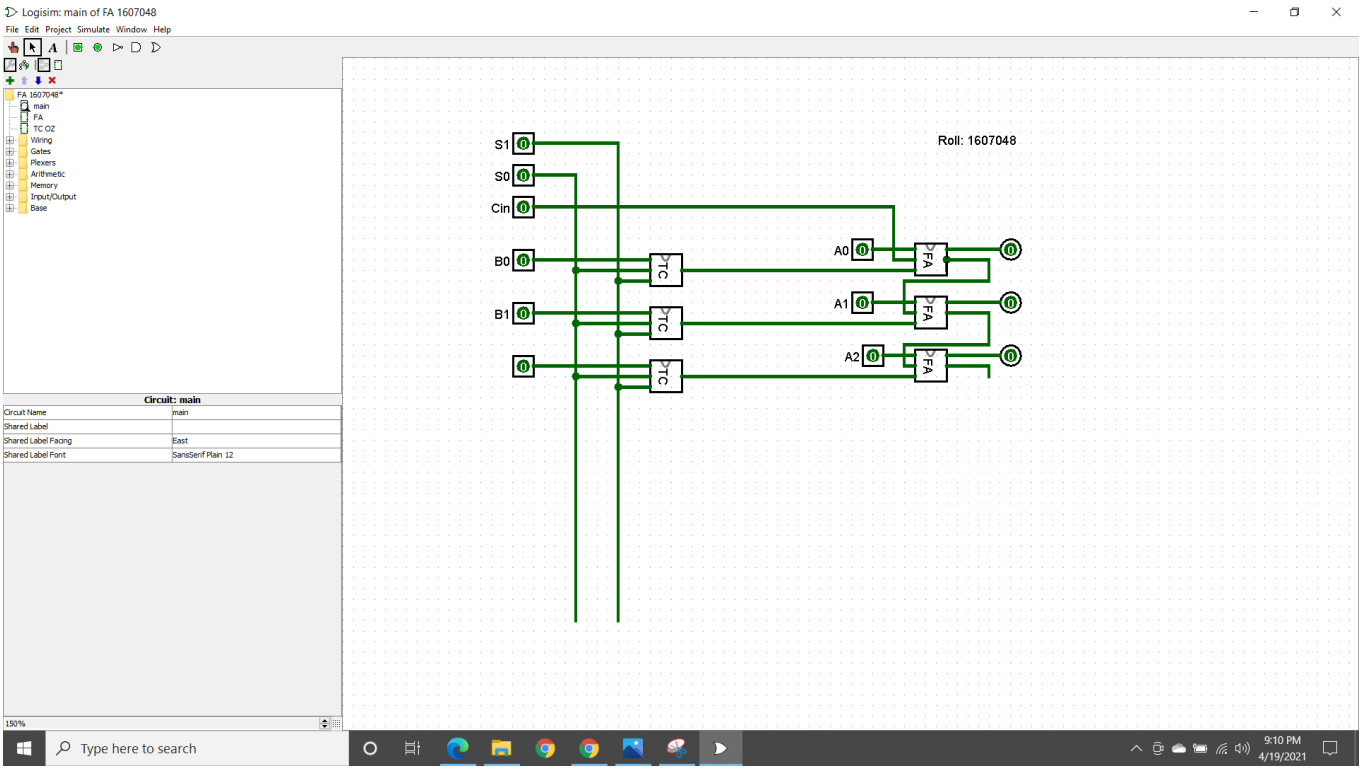
Step 1


Logisim: main of FA 1607048
File Edit Project Simulate Window Help
Roll: 1607048
S1
S0
Cin
B0
A0
TC
FA
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Type here to search
9:07 PM
4/19/2021

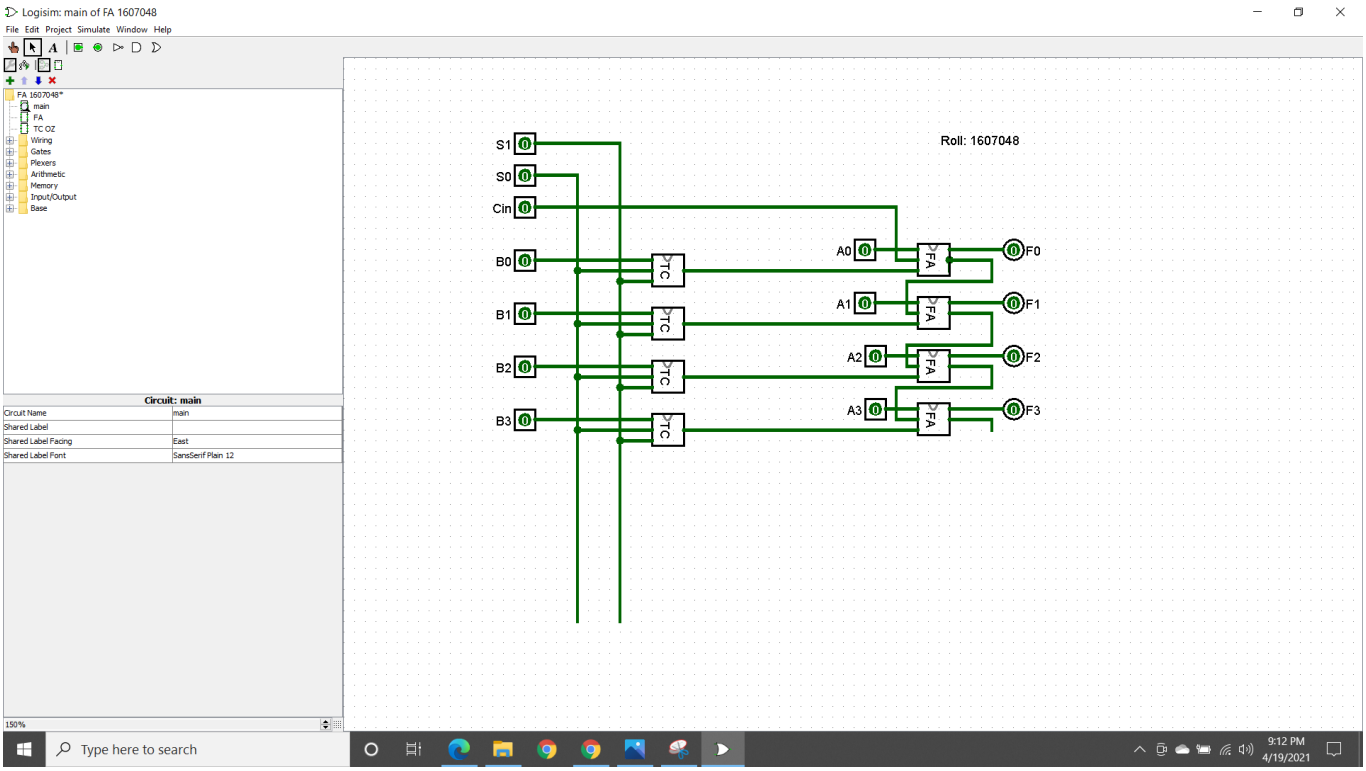
Step 2


Logisim: main of FA 1607048
File Edit Project Simulate Window Help
Roll: 1607048
S1
S0
Cin
B0
B1
A0
A1
TC
FA
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Type here to search
9:08 PM
4/19/2021

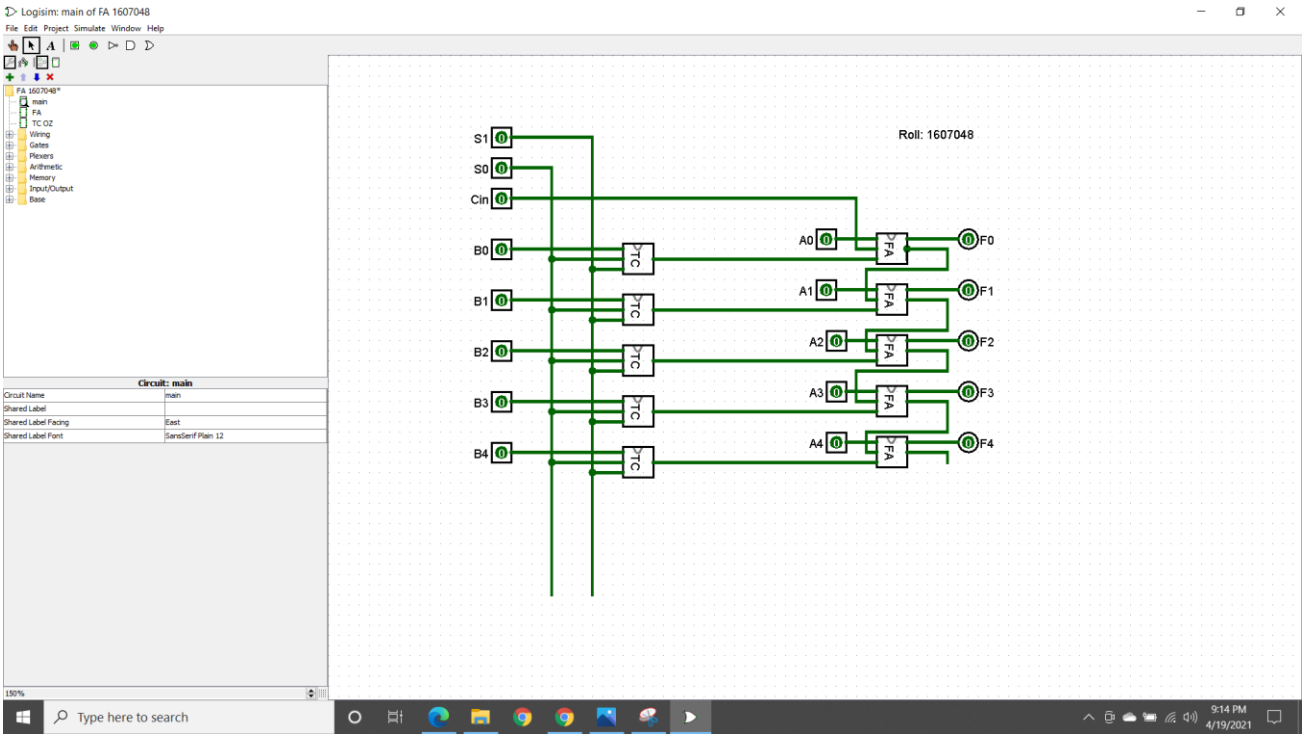
Step 3


Logisim: main of FA 1607048
File Edit Project Simulate Window Help
FA 1607048*
main
FA
TC OZ
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
150%
Roll: 1607048
S1
S0
Cin
B0
B1
A0
A1
A2
TC
FA
Type here to search
9:10 PM
4/19/2021

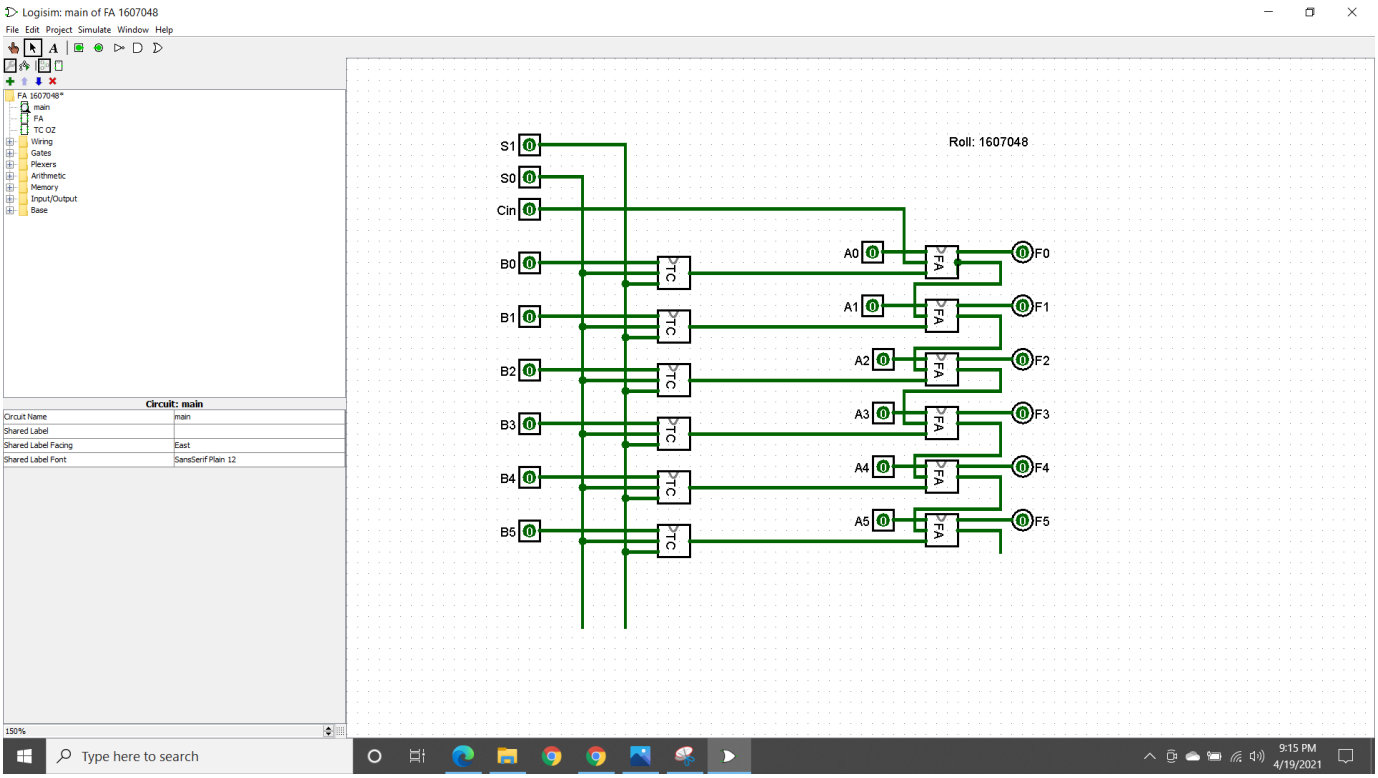
Step 4


Logisim: main of FA 1607048
File Edit Project Simulate Window Help
FA 1607048*
main
FA
TC OZ
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
150%
Roll: 1607048
S1
S0
Cin
B0
B1
B2
B3
A0
A1
A2
A3
F0
F1
F2
F3
TC
FA
Type here to search
9:12 PM
4/19/2021

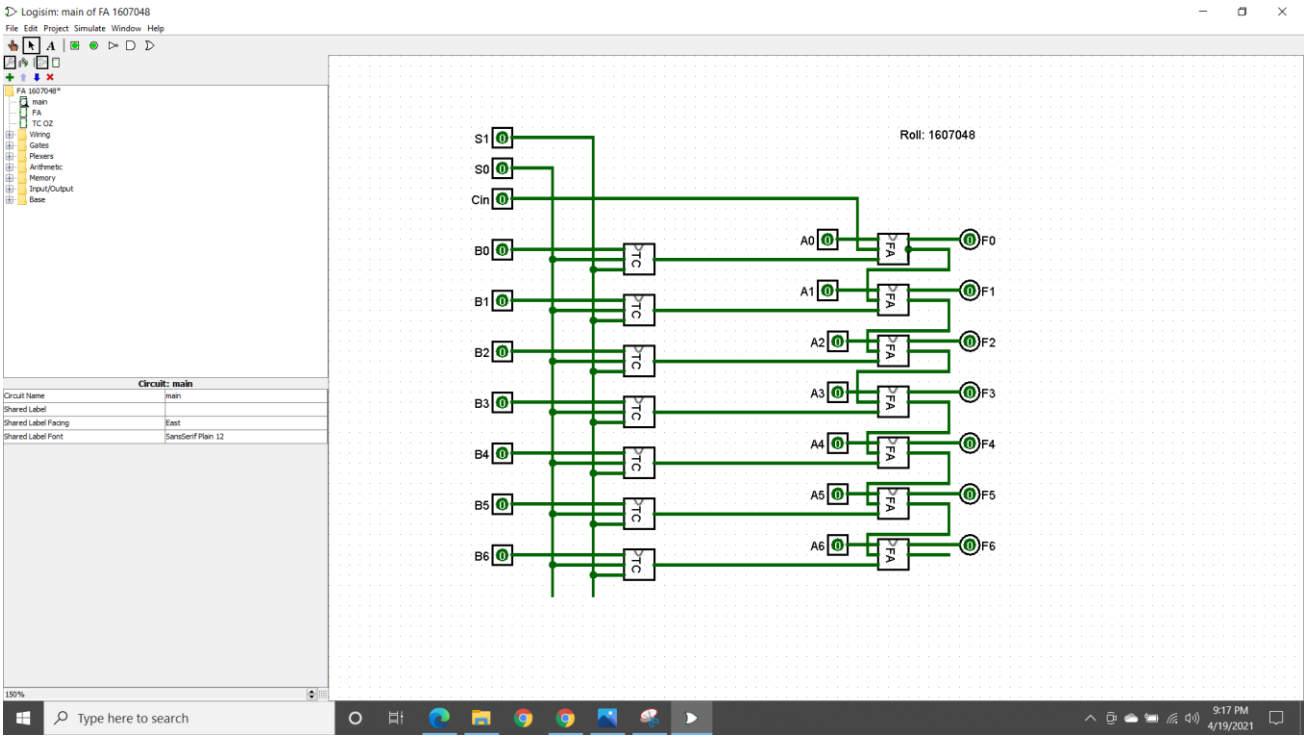
Step 5


Logisim: main of FA 1607048
File Edit Project Simulate Window Help
Roll: 1607048
S1
S0
Cin
B0
B1
B2
B3
B4
A0
A1
A2
A3
A4
F0
F1
F2
F3
F4
TC
FA
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Type here to search
9:14 PM
4/19/2021

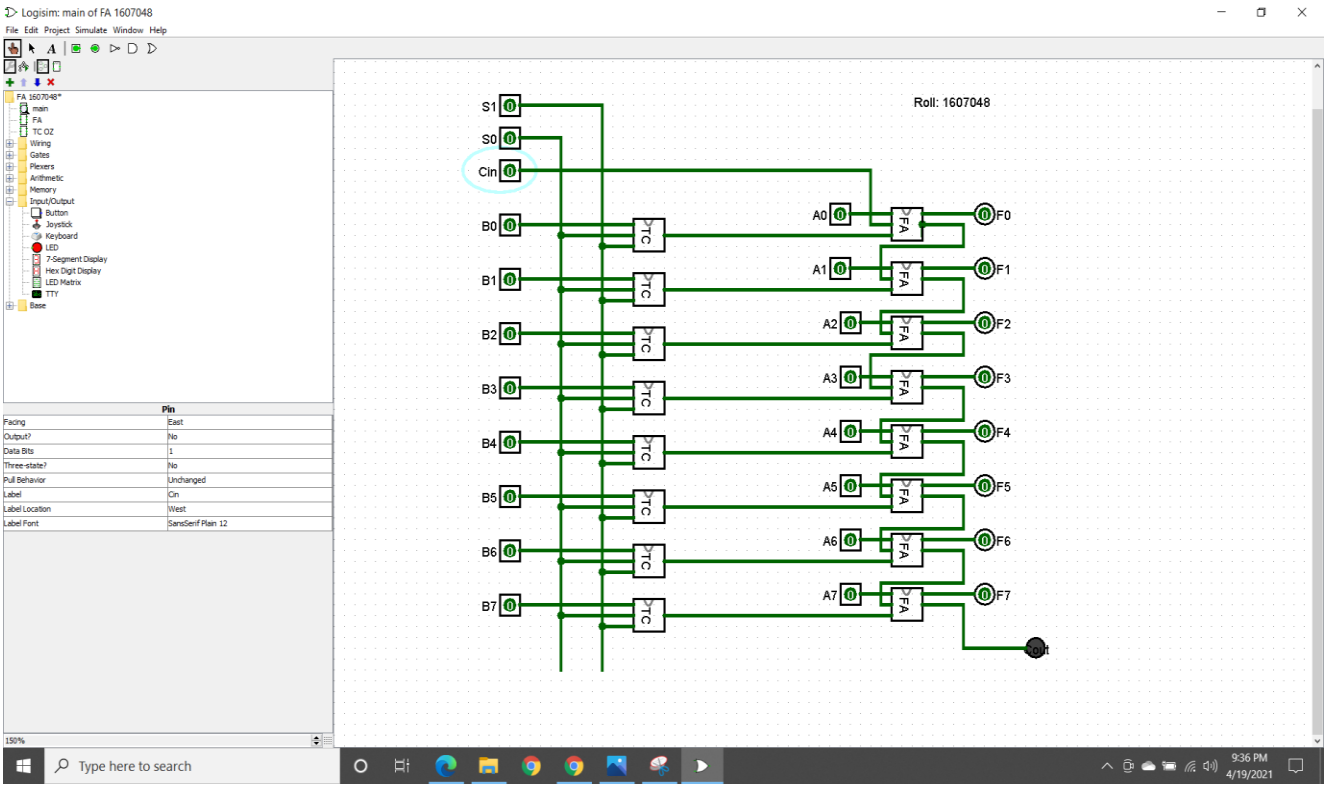
Step 6


Logisim: main of FA 1607048
File Edit Project Simulate Window Help
Roll: 1607048
S1
S0
Cin
B0
B1
B2
B3
B4
B5
A0
A1
A2
A3
A4
A5
F0
F1
F2
F3
F4
F5
TC
FA
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Type here to search
9:15 PM
4/19/2021

Step 7

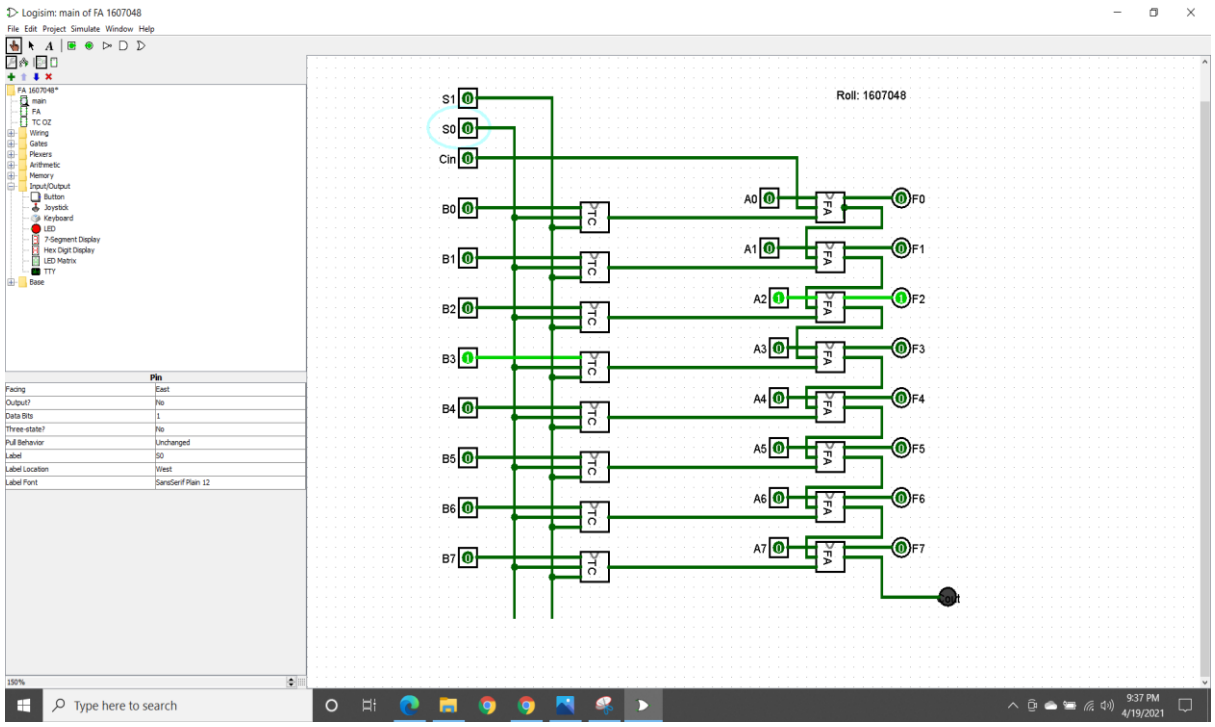

Logisim: main of FA 1607048
File Edit Project Simulate Window Help
Roll: 1607048
S1
S0
Cin
B0
B1
B2
B3
B4
B5
B6
TC
A0
A1
A2
A3
A4
A5
A6
FA
F0
F1
F2
F3
F4
F5
F6
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Type here to search
9:17 PM
4/19/2021

Step 8

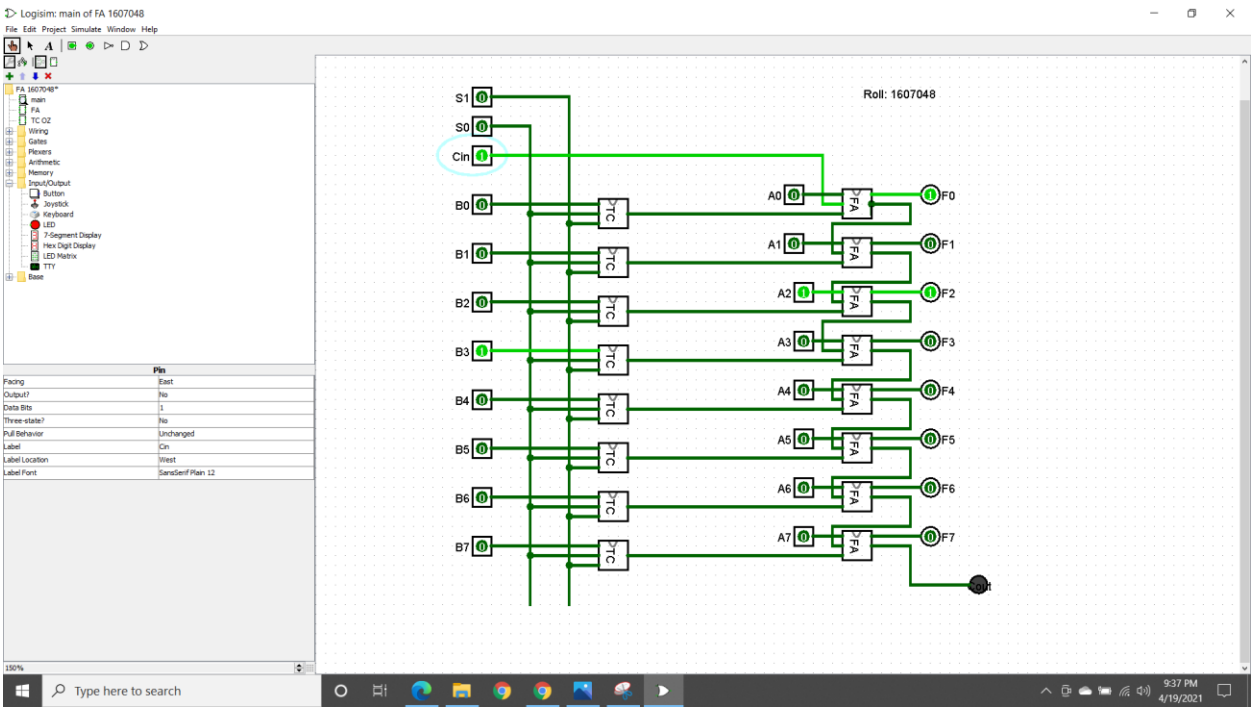

Logisim: main of FA 1607048
File Edit Project Simulate Window Help
Roll: 1607048
S1
S0
Cin
B0
B1
B2
B3
B4
B5
B6
B7
TC
A0
A1
A2
A3
A4
A5
A6
A7
FA
F0
F1
F2
F3
F4
F5
F6
F7
Cout
Pin
Facing East
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label Cin
Label Location West
Label Font SansSerif Plain 12
Type here to search
9:36 PM
4/19/2021

Output Analysis: A=4 and B=8

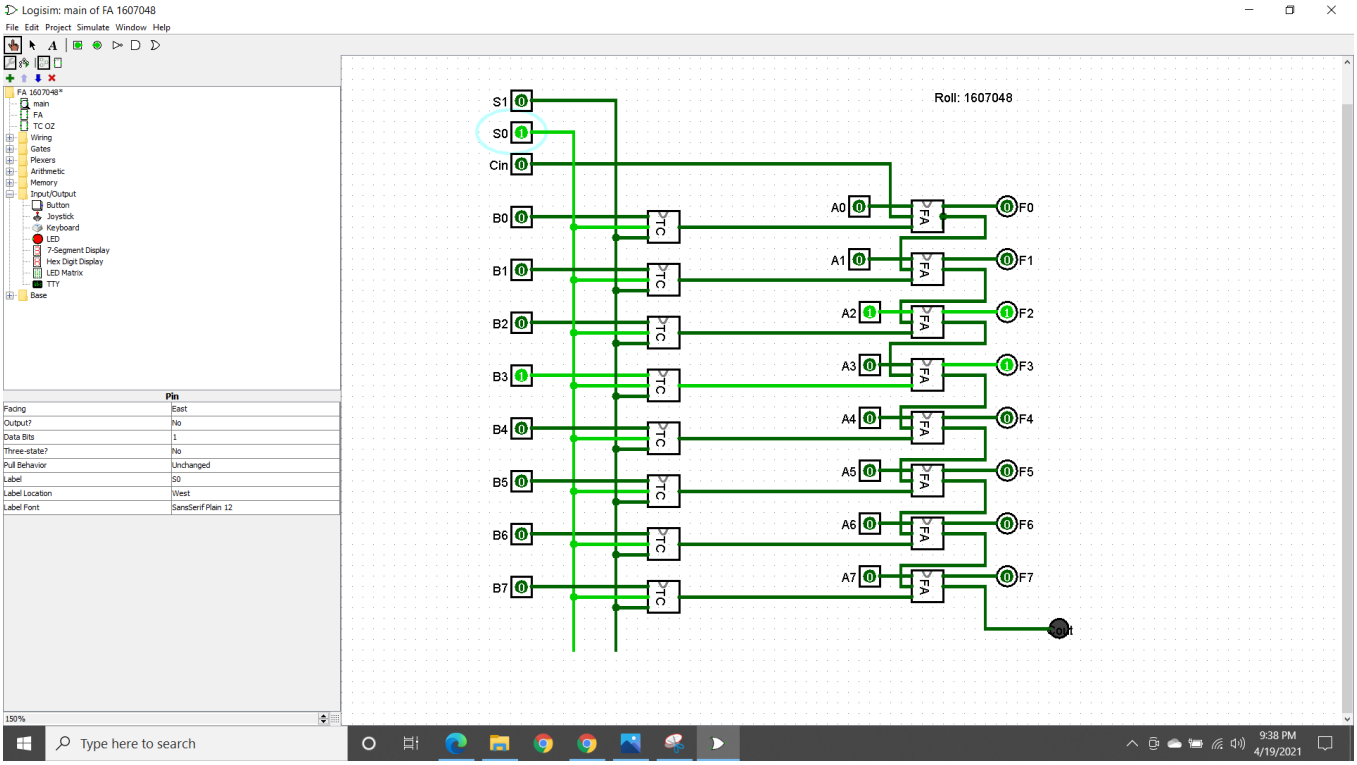
Step 0: S1=0, S0=0, Cin=0



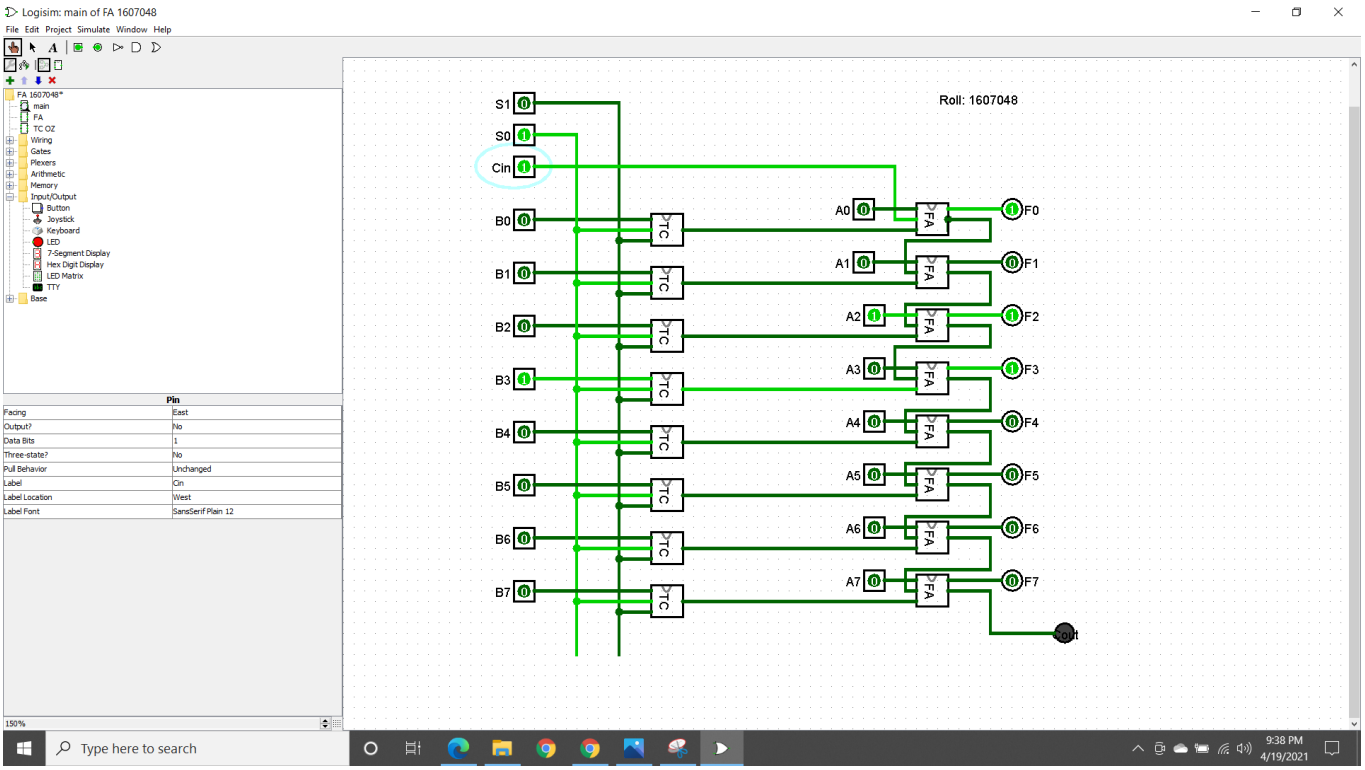
Step 1: S1=0, S0=0, Cin=1



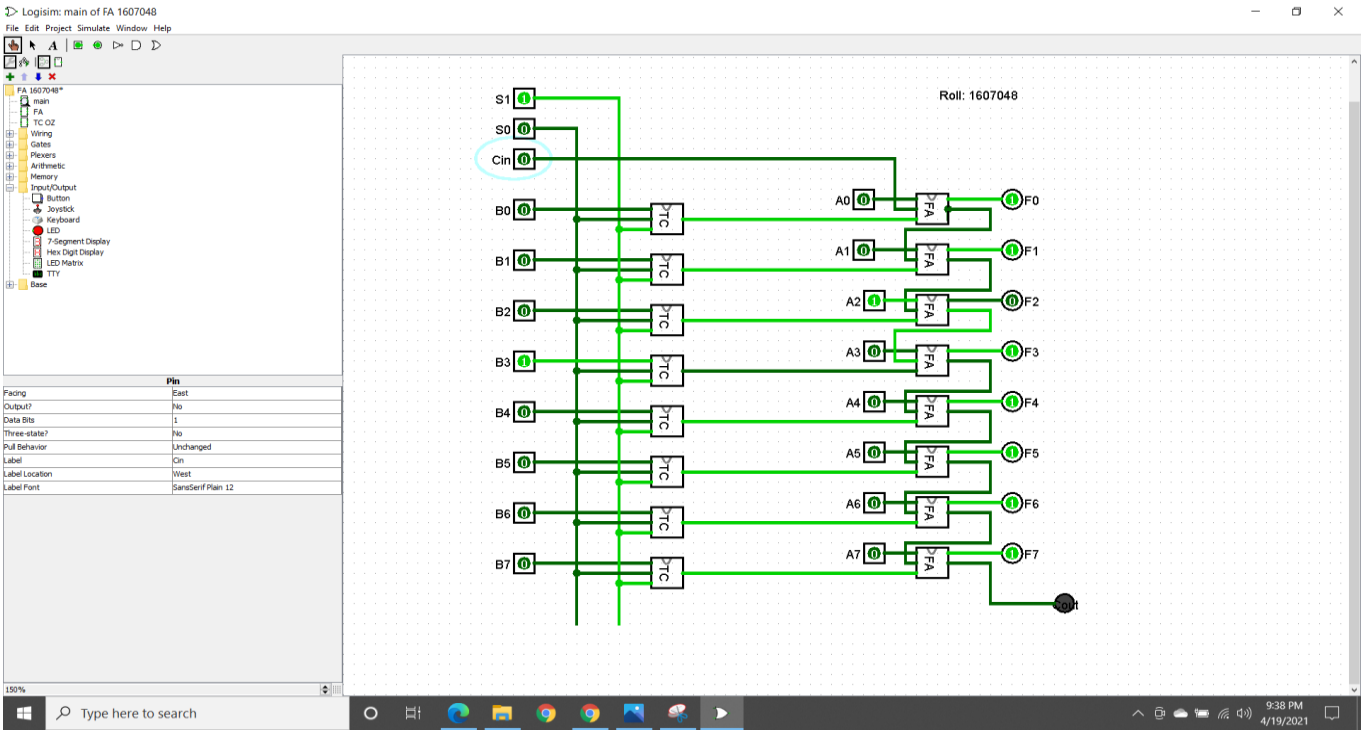
Step 2: S1=0, S0=1, Cin=0



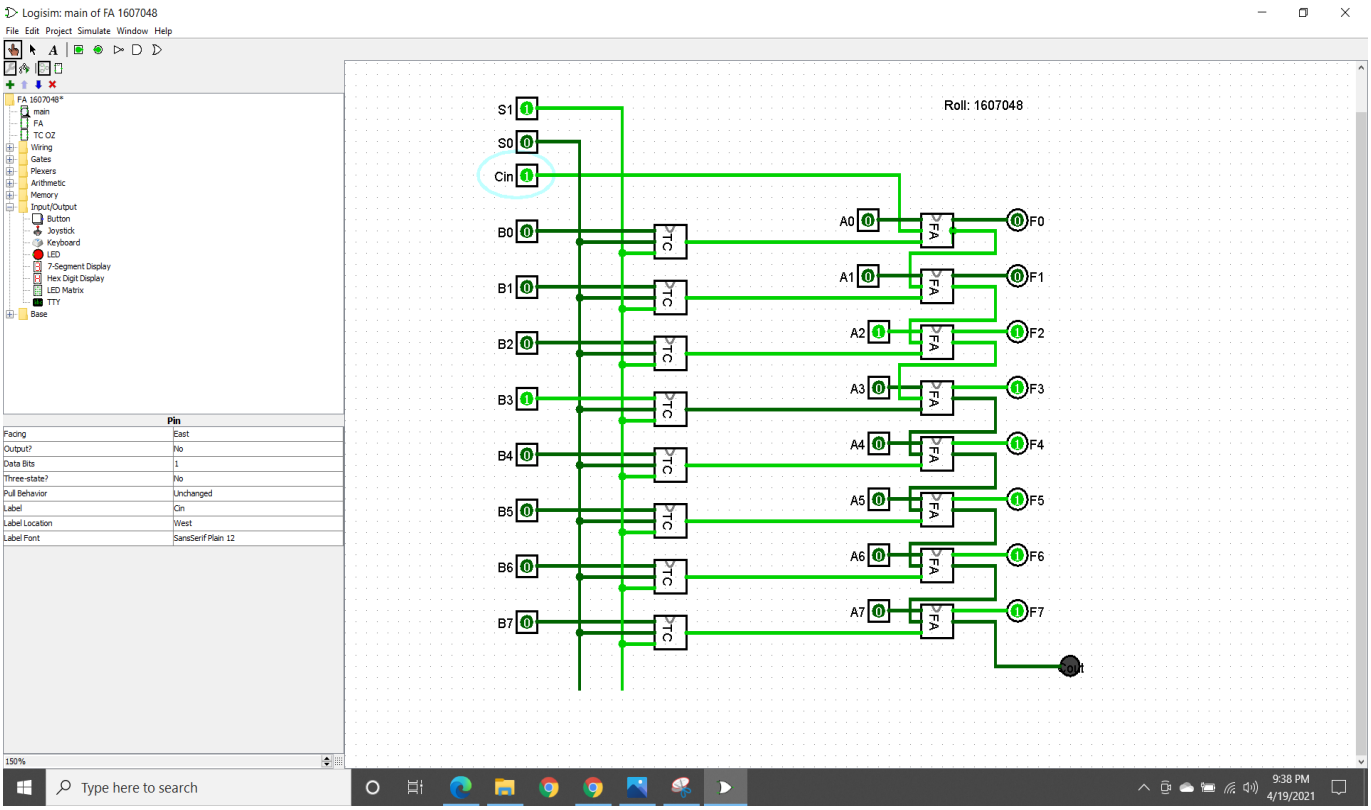
Step 3: S1=0, S0=1, Cin=1



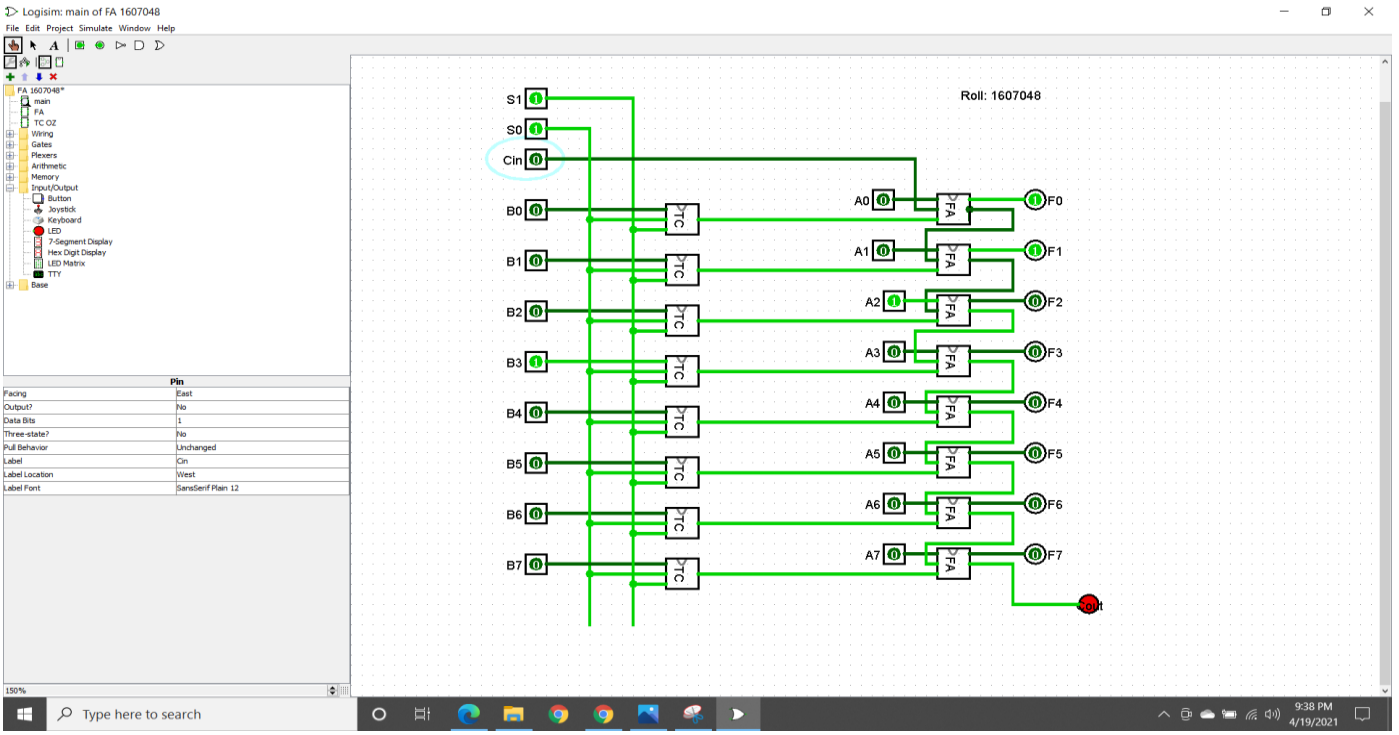
Step 4: S1=1, S0=0, Cin=0



Step 5: S1=1, S0=0, Cin=1



Step 6: S1=1, S0=1, Cin=0



Step 7: S1=1, S0=1, Cin=1