EE204 – COMPUTER ARCHITECTURE

Spring 2017 - FAST-NU, LAHORE

Course Instructor: Dr. Haroon Mahmood

Lectures: Section A: Monday and Wednesday 15:30 - 16:50 (room CS-3)
Section B: Monday and Wednesday 12:30 - 13:50 (room CS-3)

Office hours: Tuesday and Wednesday 10:00 – 12:00

COURSE BOOKS

1. M. Morris Mano, *Computer System Architecture* 3rd Edition 1993, Prentice Hall
2. David A. Patterson, John L. Hennessy, *Computer Organization and Design: The hardware/software interface*, 4th Edition
3. Modern Processor Design: Fundamentals of Superscalar Processors by John Paul Shen and Mikko H. Lipasti

COURSE OBJECTIVE

- The main objective of this course is to provide a profound understanding of the architectural design and internal working of a microprocessor which will allow computer science students to appreciate concepts like optimization and hardware level performance issues.
- This course also introduces advanced concepts like pipelining and superscalar architecture and techniques like microprogramming.
- Multi-Core processors and issues related to multicore processors are introduced.

MARKS BREAKUP

• Quiz	4/5	15%
• Assignments	3/4	10%
• Midterms	2	30%
• Final	1	45%

MISCELLANEOUS

- Academic integrity is expected of all the students. Plagiarism or cheating in any assessment will result in at least an F grade in the course, and possibly more severe penalties.
- There will be no makeup for a missed quiz.

TOPICS TO BE COVERED	BOOK	LECTURE #
Introduction to basic hardware components and devices a) Digital Logic Design Review i) Boolean Algebra ii) Combinational Circuits iii) Sequential Circuits	Text1 Chapter 1 (Excluding 1.4)	1

Frequently used components in computers a) Adders b) Decoders c) Multiplexers d) Registers (Parallel load with shifts) e) Counters	Text1 Chapter 2	2
Number Systems and Binary Representations a) Integer Representations b) Floating point representation Arithmetic Operations (Combined Circuit)	Text1 Chapter 3 (Excluding 3.5) Text2 Chapter 3 (Section 3.1 - 3.3, Section 3.6: IEEE 754) Text1 Chapter 4 (Section 4.4)	3
Logic Operations Shift Operations Combined Arithmetic, Logic and Shift Unit.	Text1 Chapter 4 (Section 4.5 – 4.7)	4
Additional Arithmetic Operations: a) Integer Multiplication, Division b) Floating Point Operations (Addition)	Text2 Chapter 3 (Section 3.4 – 3.6)	5
Complete ALU and FPU design Introduction to Machine Language	Text2 Chapter 3 (Section 3.6)	6
Register File RTL: Register Transfer Language Description of Operations in RTL Register Transfer Register, bus and memory transfers	Text1 Chapter 4 (Section 4.1 – 4.3)	7
Computer Instructions and instruction codes Introduction to the MIPS Assembly Language Instruction Types 1) Arithmetic Instructions 2) Memory Reference 3) Branch Instructions Design of a Single Cycle Machine 1) Register File	Text2 Chapter 5 (Section 5.1 – 5.4) Text2 Chapter 2 (Figure 2.25, 2.47)	8

2) ALU 3) Instruction and Data Memory 4) Control Unit 5) Integration of Units		
Revision for Mid 1		9
Single Cycle Machine Design Continued Control Unit (As a hardwired combinational circuit) Exceptions and Interrupts	Text2 Chapter 5 (Section 5.1 – 5.4, 5.6)	10
Central processing unit in detail a) General register organization b) Program control c) System stack d) Addressing modes e) CISC Vs RISC	Text1 Chapter 8 (Excluding 8.4, 8.6,8.7) Text2 Chapter 2	11
Multi-cycle implementation Motivation and Hardware Differences	Text2 Chapter 5 (Section 5.5)	12
Multi-cycle Continued Control Unit State for each instruction type	Text2 Chapter 5 (Section 5.5)	13
Multi-cycle Continued Control Unit State Machine combined Exception Handling in Multi-Cycle machine	Text2 Chapter 5 (Section 5.5, 5.6)	14
Microprogrammed Control	Text1 Chapter 7	15
Understanding Performance a) CPU Performance b) Benchmarks c) Evaluating Performance	Text2 Chapter 4	16
Enhancing Performance with Pipelining a) Introduction to pipelining b) A pipelined data-path c) Pipelined Control d) Shallow and deep pipelining	Text2 Chapter 6 (Section 6.1 – 6.3)	17
Pipelined Machine: Hardware and Control Unit	Text2 Chapter 6 (Section 6.1 – 6.3)	18
Data Hazards a) RAW (covered in detail) b) WAR	Text2 Chapter 6 Section (6.4 - 6.5)	19

c) WAW		
Control Hazards a) Branch Prediction Performance of pipelined systems	Text2 Chapter 6 Section (6.6)	20
Revision for Mid 2		21
Cache Design: Memory Hierarchy basic concepts Basics and Direct mapped caches	Text 2 Chapter 7	22
Cache Design: Associative Caches and Miss Rates	Text 2 Chapter 7	23
Cache Design: Processor performance evaluation with cache / Multi-level Caches.	Text 2 Chapter 7	24
Superscalar Processors. Basic concepts of superscalar processors and instruction independence		25
Step by step execution of instructions in superscalar processors.		26
Multi-processor Systems basics. Multi-processor system types Into to memory sharing models and cache coherence problem	Text 3 Chapter 7	27
Revision for Final		28