Secure Code Lock System Using CD4017 with Wrong Code Alert

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***Abstract*—This paper presents the detailed design, construction, and analysis of a secure, sequential code lock system built entirely from discrete digital logic integrated circuits. The system utilizes cascaded CD4017 decade counters to manage the code sequence, a CD4081 AND gate for robust error detection, and an NE555 timer to ensure a reliable system-wide reset. The primary objective is to demonstrate a highly reliable security mechanism that unlocks upon the entry of a correct, multi-stage code and triggers an immediate alert and reset for any incorrect input. In an era dominated by microcontroller-based solutions, this project highlights the educational value and inherent security of a hardware-based approach, which is immune to software vulnerabilities. The design proves to be 100% effective in catching erroneous inputs, providing a practical and insightful exploration of sequential logic design for security applications.**

***Index Terms*—code lock, CD4017, NE555, CD4081, sequential logic, digital electronics, security system**

I. Introduction

Security systems are an integral part of modern living, ranging from simple mechanical locks to advanced biometric recognition. This project focuses on the fundamental principles of digital electronics to construct a secure code lock system using basic integrated circuits (ICs). In contrast to contemporary microcontroller-based systems, which abstract away the core logic into software, this design offers a transparent, hardware-level view of sequential logic, state management, and error handling.

The core idea is to create a multi-stage lock that requires a specific sequence of key presses to unlock, for which the code *A-BB-C-D-E* is used as the primary example. The system provides an immediate alert and system reset upon any incorrect entry. This approach leverages the sequential counting capabilities of the CD4017 IC, the logical decision-making of the CD4081 AND gate, and the timing stability of the NE555 timer to establish a reliable and secure access control mechanism. The system's design emphasizes both functionality and the clear indication of operational states, using LEDs to visualize correct and incorrect inputs, making it an excellent educational tool for demonstrating complex digital logic concepts in a practical application.

II. System Components and Theory

The secure code lock system is built upon the principles of sequential logic and digital counting. Its robustness stems from the specific roles and interactions of its key components.

A. CD4017 Decade Counter

The CD4017 IC is a 5-stage Johnson decade counter with ten decoded outputs (Q0-Q9) and serves as the heart of our multi-stage code lock [1]. For this 5-digit code lock, five CD4017 chips are cascaded. Its key pins are:

- **Q0–Q9 (Outputs):** At any time, only one of these ten pins is HIGH, representing the current count. All other output pins are LOW.
- **CLK (Clock Input):** A positive-going pulse on this pin increments the counter.
- **RES (Reset Input):** A HIGH signal on this pin asynchronously resets the counter to its initial state (Q0 HIGH).
- **CI (Clock Inhibit):** When this pin is held HIGH, the counter ignores all clock pulses, effectively freezing its state. When LOW, the counter functions normally. This pin is fundamental to ensuring the code is entered sequentially, as one stage must be unlocked to enable the next.

B. NE555 Timer

The NE555 timer, a highly versatile IC, is configured here in a monostable multivibrator mode to generate a clean, fixed-duration reset pulse [2]. When a brief trigger is received from a wrong key press, the NE555 outputs a stable HIGH signal for a duration of approximately 70ms, determined by an external resistor (R20) and capacitor (C15). This is superior to a direct trigger because it ensures the reset signal is long and stable enough for all five CD4017 counters to reset reliably, preventing the system from entering an undefined or partially-reset state.

C. CD4081 Quad 2-Input AND Gate

This IC, which contains four independent 2-input AND gates, is vital for implementing the intelligent wrong-code detection feature [3]. An AND gate's output is HIGH only if all of its inputs are HIGH. In this circuit, the AND gates are wired to detect when an incorrect key is pressed at a specific stage. If a key corresponding to a future stage is pressed while that stage is still disabled (its CI pin is HIGH), the AND gate receives two HIGH inputs and triggers a system reset.

D. 1N4148 Diodes

These small-signal diodes serve two distinct and critical functions in the circuit:

1) **Wired-OR Logic:** For stages requiring multiple key presses (e.g., 'BB'), diodes are used to create a simple OR gate. They combine the outputs of the counter so that the next stage remains inhibited until the correct number of presses has been registered.
2) **Protection Diodes:** Multiple IC outputs are connected to a common "reset trigger" rail. To prevent a HIGH signal from one output from feeding back into another and potentially causing damage, diodes are placed to act as one-way valves, allowing current to flow out to the reset rail but not back into the ICs.

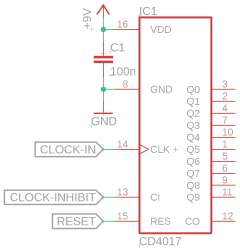

Fig. 1. CD4017 IC: Pinout and Package

III. Circuit Operation and Analysis

The circuit's logic is best understood by tracing the flow of operations for both correct and incorrect code entries. The schematic is shown in Fig. 2.

A. Correct Code Entry Sequence (A-BB-C-D-E)

1) **Initial State:** Upon power-up, the NE555 circuit generates a reset pulse, setting all counters to zero (Q0 HIGH). The Clock Inhibit (CI) pin of IC1 is grounded, making it the only active stage. All other stages are disabled as their CI pins are held HIGH by the Q0 output of the preceding stage.
2) **Stage 1 (Code A):** Pressing key 'A' sends a clock pulse to IC1. The counter advances, Q1 goes HIGH, and LED9 turns on. The Q1 output of IC1 is not used, but its Q0 going LOW is what enables Stage 2 by pulling the CI pin of IC2 LOW.
3) **Stage 2 (Code BB):** With Stage 2 active, the code requires two presses of key 'B'. The first press advances IC2 from Q0 to Q1. The second press advances it from Q1 to Q2. Diodes D9 and D10, along with resistor R19, form a wired-OR gate that keeps Stage 3 locked until IC2's output is Q2. Once Q2 is HIGH, LED10 turns on, Stage 2 is complete, and Stage 3 is enabled.
4) **Stage 3 (Code C):** Pressing 'C' advances IC3 from Q0 to Q1. LED11 turns on, and Stage 4 is activated.
5) **Stage 4 (Code D):** Pressing 'D' advances IC4 from Q0 to Q1. LED12 turns on, and Stage 5 is activated.
6) **Stage 5 (Code E):** Finally, pressing 'E' advances IC5 from Q0 to Q1, which turns on the green "unlocked" LED (LED13). The code lock is now successfully unlocked.

B. Wrong Code Detection Scenarios

The circuit is designed to be 100% secure against incorrect entries through three primary mechanisms.

- **Scenario 1: Unused Key Press.** If a key not part of the code (e.g., F, G, or H) is pressed at any time, it directly triggers the NE555 reset circuit via diodes D1-D3, immediately resetting the system and flashing the alarm LED.
- **Scenario 2: Out-of-Sequence Press.** Suppose the user correctly enters A-BB-C but then presses 'E' instead of 'D'. At this moment, Stage 4 is active, but Stage 5 is not. The AND gate IC6B has its inputs connected to the clock signal for key 'E' and the Q0 output of IC4. Since Stage 5 is not yet active, Q0 of IC4 is HIGH. When 'E' is pressed, its clock line also goes HIGH. With both inputs HIGH, the AND gate triggers, firing the reset circuit. This logic applies to all out-of-sequence key presses.
- **Scenario 3: Repeated Key Press.** If a stage is complete and its key is pressed again (e.g., pressing 'C' after Stage 3 is already unlocked), the corresponding counter (IC3) advances from Q1 to Q2. The Q2 pin of this counter is wired directly to the reset trigger rail via a protection diode (D6). This immediately triggers a system reset.

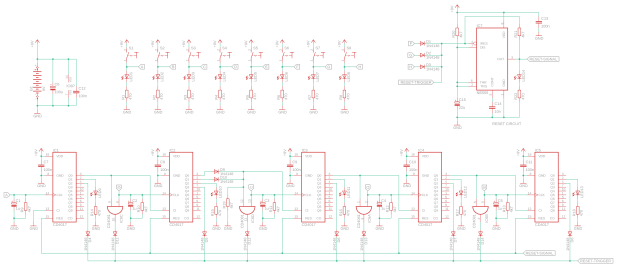

Fig. 2. Schematic Diagram of the Circuit

IV. Construction and Practical Challenges

The circuit was constructed on two 830-pin breadboards, as shown in Fig. 3. The layout strategically utilizes the breadboard's power rails not just for VDD and ground, but also for the "reset trigger" and "reset signal" lines to minimize wiring complexity.

Several practical challenges were encountered and solved during implementation:

- **Switch Debouncing:** Mechanical pushbuttons generate noisy electrical signals ("bouncing") when pressed. This was a critical issue, as a single press could be registered

as multiple clock pulses, invalidating the code. Small 100nF capacitors (C1-C5) were placed in parallel with the switches to act as low-pass filters, smoothing the signal and ensuring each press is registered as one clean pulse.

- **System Reset Integrity:** As noted, a simple, direct reset signal proved inconsistent. The implementation of the NE555 monostable circuit was a crucial design decision that solved this by generating a wider, more stable 70ms pulse, guaranteeing that all five ICs reset simultaneously and reliably.
- **Wiring Complexity and Troubleshooting:** The density of interconnections, particularly for the CD4081 AND gates and the numerous diodes, posed a significant challenge. This was mitigated by adopting a structured wiring approach, using color-coded wires for power, ground, clock, and reset signals. This discipline was invaluable during troubleshooting, as it made tracing signals and identifying incorrect connections significantly easier.

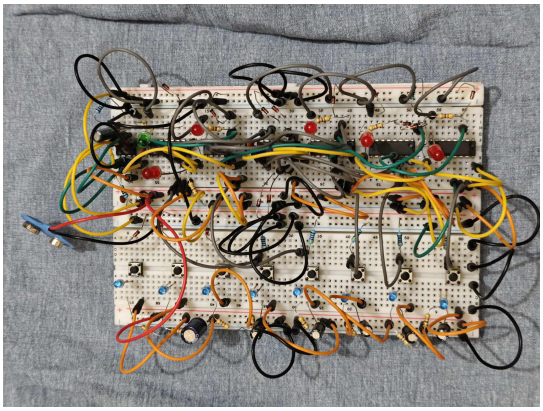

Fig. 3. Picture of the Assembled Circuit

V. Conclusion

This project successfully demonstrates the design and construction of a secure, sequential code lock using fundamental digital logic ICs. The system reliably accepts a predefined code, unlocks a designated output, and effectively detects all forms of incorrect entry by triggering a robust reset mechanism. The project serves as an excellent practical study in sequential logic, state management, and the creative use of common electronic components to build a functional and secure application.

For future improvements, several extensions are possible:

- **Enhanced Security:** The intermediate status LEDs (LED9-LED12), which indicate stage completion, could be removed in a real-world application to prevent an attacker from gaining feedback on partially correct codes.
- **Lockout Mechanism:** An additional counter could be added to track the number of incorrect attempts. After a set number of failed tries (e.g., three), the system could enter a timed lockout mode, further deterring brute-force attacks.
- **Increased Complexity and Customization:** The design can be expanded to accommodate longer or more complex codes by cascading additional CD4017 stages. Furthermore, DIP switches could be integrated to allow the user to change the code without re-wiring the circuit.

Acknowledgment

The authors would like to acknowledge the inspiration and detailed guidance provided by the ”Friendly Wire” website [4], which worked as a huge inspiration for this project.

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