FAISAL SAEED

DIGITAL DESIGN ENGINEER

PROFESSIONAL SUMMARY

Digital Design Engineer specialized in RTL design and verification methodologies. Actively contributes to advanced System-on-Chip (SoC) designs, integrating technologies like AMBA protocols, with a future orientation toward DDR memory, controller, and DDR PHY. Meticulous attention to detail and commitment to excellence ensure high-performance designs.

CONTACT INFO

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https://faisalawan11.github.io/Portfolio/

https://www.linkedin.com/in/faisal-saeed-02334bab/

EXPERTISE

- Verilog/System verilog
- Universal Verification Methodology(UVM)
- Shell scripting
- Git

SOFTWARE SKILLS

- Verilator
- QuestaSim

CERTIFICATION

- Chip Design Verification Essentials training certification from NUST University

EXPERIENCE

TRAINEE ENGINEER
CoMIRA SOLUTIONS — OCT 2022- MAR 2023

- Developed strong experties in Verilog HDL for effiecient hardware design and verification, employing best practices with industry standards
- Developed a UVM testbench for integrating an ALU and synchronous FIFO modules

Design Engineer
CoMIRA SOLUTIONS — APR 2023- PRESENT

- Collaborating with CoMira team on SoC development
- Working on LaTex for the documentation of SoC
- Writing C++ testbench for SoC development. This includes generating test cases, applying stimuli, and checking the expected outputs

EDUCATION

BACHELOR IN INDUSTRIAL ELECTRONICS ENGINEERING

NED UNIVERSITY | 2011-2015

APPRENTICESHIP IN B2/AVIONICS

PAKISTAN INTERNATIONAL AIRLINES | 2016-2018

MASTERS IN ELECTRONICS ENGINEERING

GHULAM ISHAQ KHAN INSTITUTE OF ENGINEERING SCIENCES AND TECHNOLOGY | 2020-2023