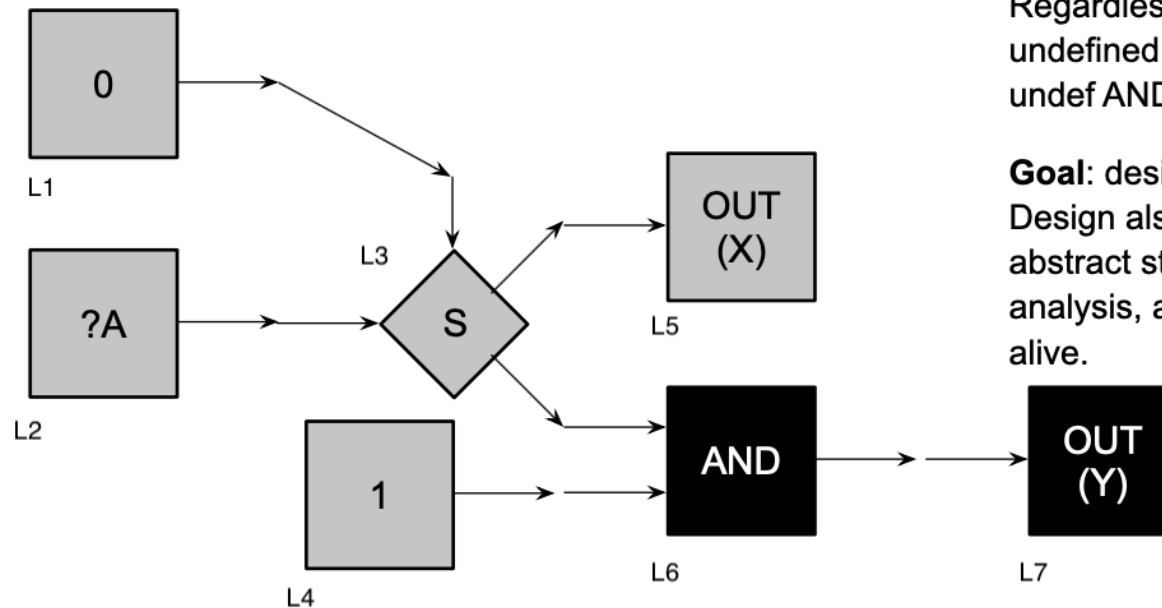


ather, Midsem 2022 dcc888

Question 1

Initial working q1

Question 1 [5 Points] Programs might contain dead code. To see why, consider the program below:



Regardless of the value of `A`, the output `Y` will be always undefined. The `AND` function is also undefined, because `undef AND 1` is always `undef`.

Goal: design a static analysis that marks gates as **DEAD**. Design also a query `IS_DEAD(A)`, which receives the abstract state of a variable `A`, as computed by your static analysis, and reports if `A` **MUST** be dead or if it **MIGHT** be alive.

Forward analysis. Must analysis.

The lattice is of $Scope = INPUTS \cup \{0, 1, \perp\}$ with these operations for evaluation $State = Vars \rightarrow Scope$,

- $eval(\sigma, op(Y, X)) = op(eval(\sigma, Y), eval(\sigma, X))$
- $eval(\sigma, S(Y, X)) = (snd|fst)(S(eval(\sigma, Y), eval(\sigma, X)))$
- $eval(\sigma, op(X)) = op(eval(\sigma, X))$
- $eval(\sigma, INPUT(X)) = X$
- $eval(\sigma, INPUT(N, X)) = (N > 0 \implies X) \vee (N \leq 0 \implies \perp)$
- $eval(\sigma, OUTPUT(X)) = X$

op:

- $AND(Y, X)$
 - $AND(0, X) = 0$
 - $AND(1, X) = X$
- $OR(Y, X)$
 - $OR(0, X) = X$
 - $OR(1, X) = 1$
- $S(X, CONTROL) = \{\neg CONTROL \implies [X, \perp], CONTROL \implies [\perp, X]\}$
 - $S(X, 0) = [X, \perp]$
 - $S(X, 1) = [\perp, X]$
- $NOT(X) = \neg X$

Functions :

- $JOIN(v) = \sqcap_{w \in pred(v)} \llbracket w \rrbracket$
- $op(Y, X) : \llbracket v \rrbracket = JOIN(v)[eval(JOIN(v), op(Y, X))]$
- $op(X) : \llbracket v \rrbracket = JOIN(v)[(eval(JOIN(v), op(X)))]$

Workthrough q1

$$\llbracket L7 \rrbracket = \llbracket L6 \rrbracket = \perp$$

$$\llbracket L6 \rrbracket = \text{snd}(\text{AND}(\llbracket L4 \rrbracket, \llbracket L3 \rrbracket)) = \text{snd}(\text{AND}(1, \llbracket L3 \rrbracket)) = \text{snd}(\llbracket L3 \rrbracket) = \text{snd}([A, \perp]) = \perp$$

$$\llbracket L4 \rrbracket = \text{INP UT}(1) = 1$$

$$\llbracket L3 \rrbracket = S(\llbracket L2 \rrbracket, \llbracket L1 \rrbracket) = S(A, \llbracket L1 \rrbracket) = S(A, 0) = [A, \perp]$$

$$\llbracket L2 \rrbracket = \text{INP UT}(A) = A$$

$$\llbracket L1 \rrbracket = 0$$

$$\llbracket L5 \rrbracket = \text{fst}(\llbracket L3 \rrbracket) = \text{fst}([A, \perp]) = A$$

IS_DEAD(V) q1

$$\text{IS_DEAD}(V) = \text{if}(\llbracket V \rrbracket == \perp) \text{ then } \text{TRUE} \text{ else } \text{FALSE}$$

Time & Space q1

IS_DEAD is just time: O(1) & space: O(1) if constructed abstrace states.

Time q1

O(E) for E nodes, must visit each once.

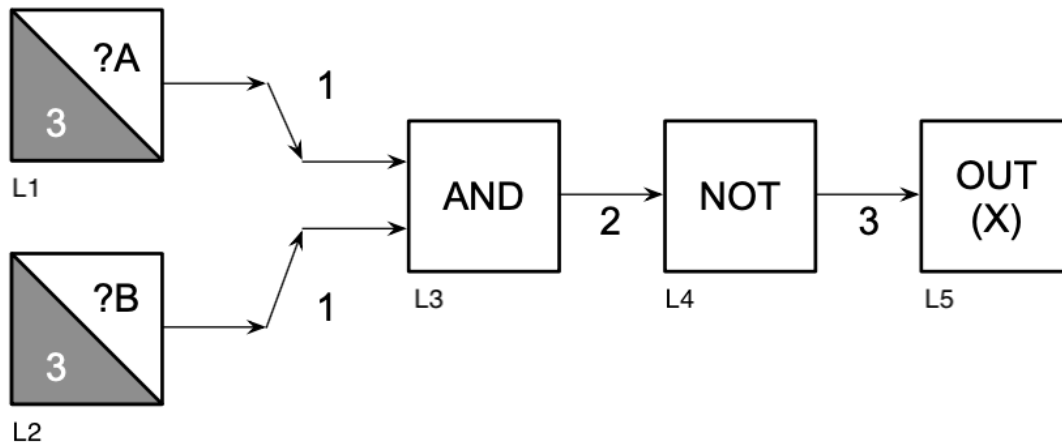
Space q1

Just contains the abstract value of the Node, so O(1) for each Node hence O(E) for E nodes.

Question 2

Initial working q2

Question 2 [5 Points] Edges are *undefined* if they receive an undef value. Edges that hold either zero or one are said to be *well-defined*. Circuits might start with undefined edges, which eventually become well-defined. For instance, in the program below, we show, associated with each edge, the first tick when that edge becomes well-defined.



Goal: design a static analysis to predict the moment when each edge becomes well-defined. If your analysis says that the edge will never become well defined, you must bind that edge to the abstract state INFTY. Otherwise, you must bind that edge to the abstract state [N], whereas N is the first tick when the edge becomes well defined. Design a query WAKE_UP(A), that receives the abstract state of a variable A, and informs the moment when the variable A first became well-defined.

Forward analysis. Must analysis.

$(StartT, MaxT)$, means starts being well-defined at $StartT$ till $StartT + MaxT$ clock tick.

The lattice is of $Scope = (flat(N) \times INPUTS_START_N)$ with these operations for evaluation $State = Vars \rightarrow Scope$,

- $eval(\sigma, op(Y, X)) = op(eval(\sigma, Y), eval(\sigma, X))$
- $eval(\sigma, S(Y, X)) = (snd|fst)(S(eval(\sigma, Y), eval(\sigma, X)))$
- $eval(\sigma, op(X)) = op(eval(\sigma, X))$
- $eval(\sigma, INPUT(X)) = (0, \infty)$
- $eval(\sigma, INPUT(N, X)) = (N > 0 \Rightarrow (0, N)) \vee (N \leq 0 \Rightarrow (\infty, 0))$

- $eval(\sigma, OUTPUT(XS, XM)) = (XS + 1, XM)$

op :

```
CALC_RANGE((YS, YM), (XS, XM)) = let range = ([YS .. (YS + YM)] `intersect` [XS .. (XS + XM)])
                                in if (length(range) `equal` 0) then return (INFINITY, 0)
                                   else return (min(range) + 1, length(range))
```

- $AND((YS, YM), (XS, XM)) = CALC_{RANGE}((YS, YM), (XS, XM))$
- $OR((YS, YM), (XS, XM)) = CALC_{RANGE}((YS, YM), (XS, XM))$
- $S(X, C) = \{$
 - $\neg C \Rightarrow [CALC_{RANGE}(X, C), [\infty, 0]]$,
 - $C \Rightarrow [[\infty, 0], CALC_{RANGE}(X, C)]$
- $NOT((XS, XM)) = (XS + 1, XM)$

Functions :

- $JOIN(v) = \prod_{w \in pred(v)} \llbracket w \rrbracket$
- $op(Y, X) : \llbracket v \rrbracket = JOIN(v)[eval(JOIN(v), op(Y, X))]$
- $op(X) : \llbracket v \rrbracket = JOIN(v)[(eval(JOIN(v), op(X)))]$

Workthrough q2

$$\llbracket L1 \rrbracket = INPUT(3, A) = (0, 3)$$

$$\llbracket L2 \rrbracket = INPUT(3, B) = (0, 3)$$

$$\llbracket L3 \rrbracket = AND(\llbracket L1 \rrbracket, \llbracket L1 \rrbracket) = AND((0, 3), (0, 3)) = (1, 3)$$

$$\llbracket L4 \rrbracket = NOT(\llbracket L3 \rrbracket) = NOT((1, 3)) = (2, 3)$$

$$\llbracket L5 \rrbracket = OUT(\llbracket L4 \rrbracket) = OUT((2, 3)) = (3, 3)$$

WAKE_UP(V) q2

$WAKE_UP(V) = \text{if}(\text{fst}(\llbracket V \rrbracket) == \infty) \text{ then } TRUE \text{ else } FALSE$

Time & Space q2

WAKE_UP is just time: $O(1)$ & space: $O(1)$ if constructed abstrace states.

Time q2

$O(E)$ for E nodes, must visit each once.

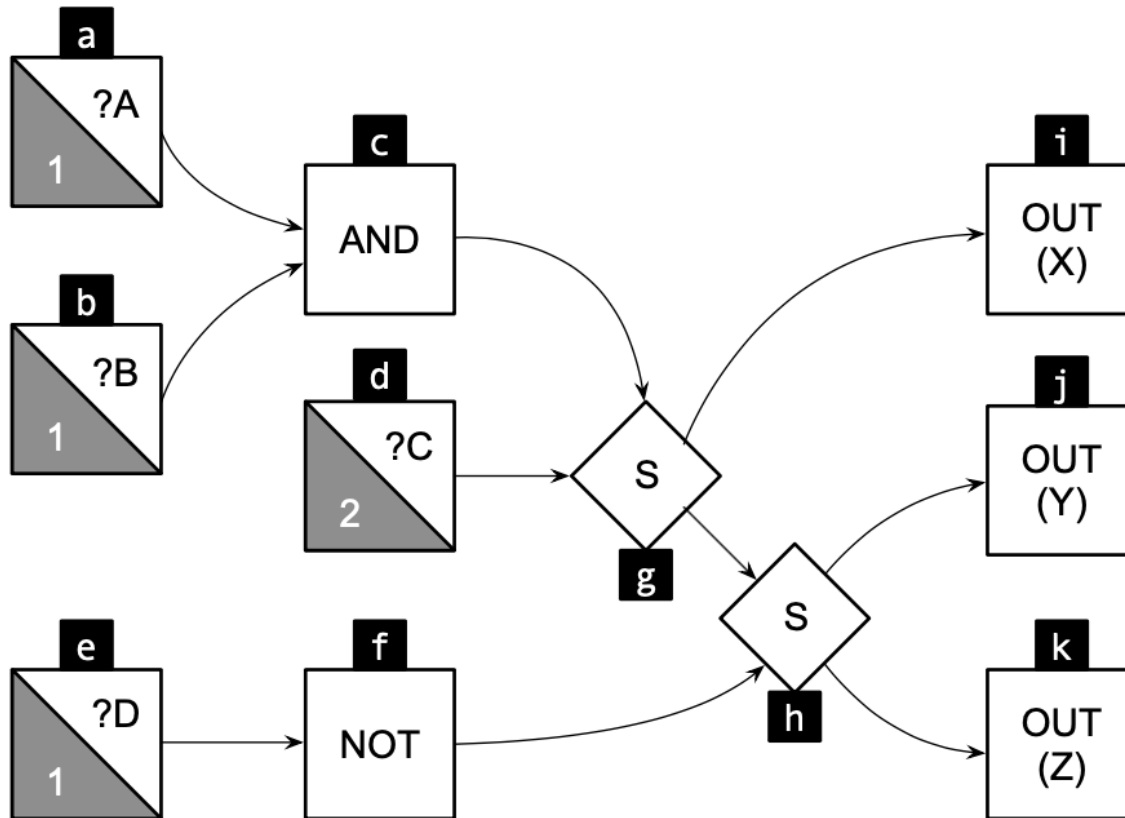
Space q2

Just contains the abstract value of the Node, so $O(1)$ for each Node hence $O(E)$ for E nodes.

Question 3

Initial working q3

Question 3 [5 Points] Some gates can be interpreted in parallel. In other words, whenever there are no dependencies between two gates, they can run simultaneously, because the result of a gate will not influence the result of another one. For an example, see the program below:



In this program, Gate 'a' can influence gates 'c', 'g', 'i', 'h', 'j' and 'k', but gate 'a' cannot influence gate 'f', for instance.

Goal: In this exercise, you must design a static analysis that determines if a gate A can influence the outcome of another gate B. Design your analysis so that, once it runs, the result of the query $M_INF(A, B)$ is true if A can influence the result of B. M_INF must consult the abstract states of A and B, and based on this query, return an answer.

Forward analysis. Must analysis.

The lattice is of $Scope = \wp(Vars)$ with these operations for evaluation $State = \{Vars, \subseteq\}$,

- $eval(\sigma, op(Y, X)) = op(eval(\sigma, Y), eval(\sigma, X))$
- $eval(\sigma, S(Y, X)) = (snd|fst)(S(eval(\sigma, Y), eval(\sigma, X)))$
- $eval(\sigma, op(X)) = op(eval(\sigma, X))$

- $eval(\sigma, INPUT(X)) = X$
- $eval(\sigma, INPUT(N, X)) = (N > 0 \implies X) \vee (N \leq 0 \implies \perp)$
- $eval(\sigma, OUTPUT(X)) = X$

op:

- $AND(Y, X)$
 - $AND(0, X) = \emptyset$
 - $AND(1, X) = X$
- $OR(Y, X)$
 - $OR(0, X) = X$
 - $OR(1, X) = \emptyset$
- $S(X, CONTROL) = \{\neg CONTROL \implies [X, \perp], CONTROL \implies [\perp, X]\}$
 - $S(X, 0) = [X, \emptyset]$
 - $S(X, 1) = [\emptyset, X]$
 - $S(X, Y) = [\{X, Y\}, \{X, Y\}]$
- $NOT(X) = X$

Functions :

- $JOIN(v) = \sqcup_{w \in pred(v)} \llbracket w \rrbracket$
- $op(Y, X) : \llbracket v \rrbracket = JOIN(v)[eval(JOIN(v), op(Y, X))]$
- $op(X) : \llbracket v \rrbracket = JOIN(v)[(eval(JOIN(v), op(X)))]$

Workthrough q3

$$\llbracket i \rrbracket = \{i\} \cup \llbracket g \rrbracket = \{i, g, c, b, a, d\}$$

$$\llbracket j \rrbracket = \{j\} \cup \llbracket h \rrbracket = \{j, h, g, c, b, a, d, f, e\}$$

$$\llbracket k \rrbracket = \{k\} \cup \llbracket h \rrbracket = \{k, h, g, c, b, a, d, f, e\}$$

$$\llbracket h \rrbracket = \{h\} \cup \llbracket g \rrbracket \cup \llbracket f \rrbracket = \{h, g, c, b, a, d, f, e\}$$

$$\llbracket f \rrbracket = \{f\} \cup \llbracket e \rrbracket = \{f, e\}$$

$$\llbracket e \rrbracket = \{e\}$$

$$\llbracket g \rrbracket = \{g\} \cup \llbracket c \rrbracket \cup \llbracket d \rrbracket = \{g, c, b, a, d\}$$

$$\llbracket d \rrbracket = \{d\}$$

$$\llbracket c \rrbracket = \{c\} \cup \llbracket b \rrbracket \cup \llbracket a \rrbracket = \{c, b, a\}$$

$$\llbracket b \rrbracket = \{b\}$$

$$\llbracket a \rrbracket = \{a\}$$

M_INF(V,W) q3

$M_INF(V, W) = \text{if}(\{V\} \subset \llbracket W \rrbracket) \text{ then } TRUE \text{ else } FALSE$

Time & Space q3

M_INF is just time: $O(|\llbracket W \rrbracket|)$ & space: $O(1)$ if constructed abstrace states.

Time q3

$O(E)$ for E nodes, must visit each once.

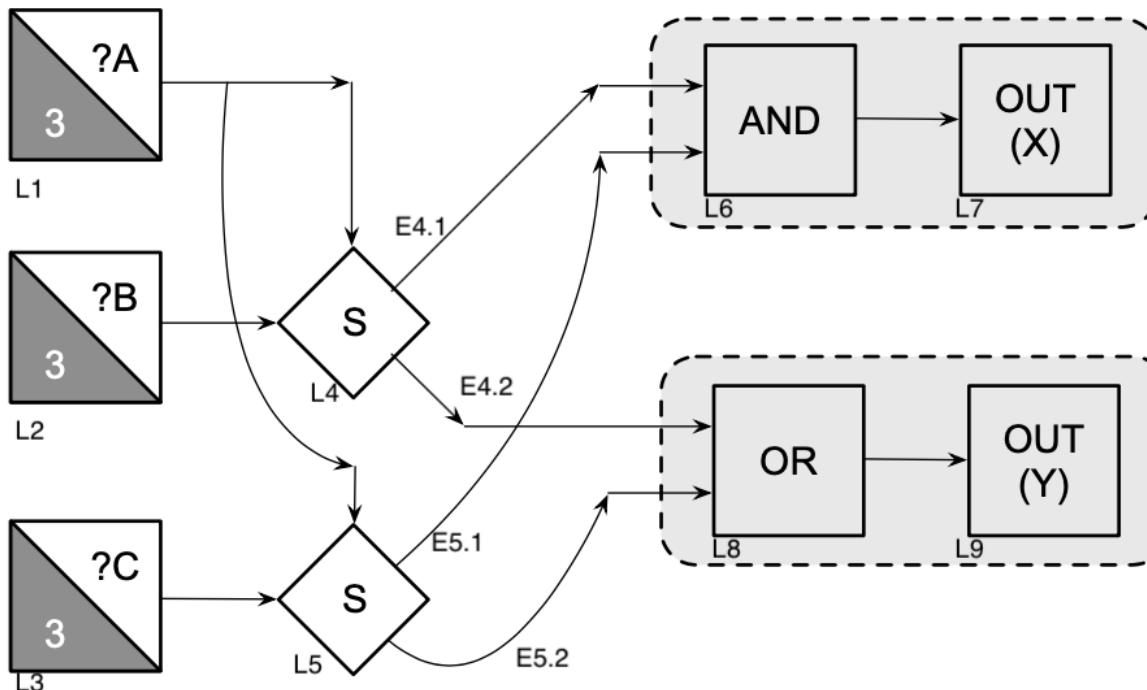
Space q3

Just contains the abstract value of the Node, so $O(1)$ for each Node hence $O(E)$ for E nodes.

Question 4

Initial thoughts q4

Question 4 [5 Points] When porting our hardware description language to an actual hardware, it is necessary to implement the gates using resources, like flip-flops and memory. Some gates can be implemented onto the same resources, because they can never execute together. For instance, consider the program below:



This program computes $X = B \text{ AND } C$ if A is zero, and $Y = B \text{ OR } C$, if A is one. What is interesting about this program is that the gates in the gray regions will never be simultaneously defined. Therefore, these gates can be implemented using the same resources. Or, in other words, there is no problem in allocating these gates onto the same flip-flops, or simulating them in the same memory.

Goal: design an analysis that tells if two gates will never receive well-defined inputs simultaneously. Notice that this is the hardest exercise. You do not need to find the most precise answer to this analysis.

An approximation is fine. Try to think about what would be the abstract state associated with each gate, and try to give at least one example where your analysis produces a non-trivial result, e.g., given two gates, A and B , it tells that they might, indeed, overlap. The product of this exercise is a function $\text{MIGHT_OVERLAP}(A, B)$ which is true if A and B might be allocated to the same resources, e.g., they are never well-defined at the same clock tick.

- E4.1: selector at L4 bound with $\neg \llbracket L1 \rrbracket$
- E4.2: selector at L4 bound with $\llbracket L1 \rrbracket$
- E5.1: selector at L4 bound with $\neg \llbracket L1 \rrbracket$
- E5.2: selector at L4 bound with $\llbracket L1 \rrbracket$

Product lattice of selectors and variables, Set Union.

Reject inconsistent state e.g $s_{l4} @ \llbracket L1 \rrbracket \wedge s_{l4} @ \neg \llbracket L1 \rrbracket$.

Simplify the gates using the previous question 1 technique.

Bundle nodes with same abstract states together.

For each bundle switch on the variables needed to power this current bundle, identify other bundles that light up. These will be the bundles that overlap with this one lets call them activeCurr. Remove them from the set of all bundles to get the bundles that do not overlap.

Initial working q4

Forward analysis. Must analysis.

The lattice is of $States = \{SELECTORS \times VARIABLES, \subseteq\}$.

- $eval(\sigma, op(Y, X)) = op(eval(\sigma, Y), eval(\sigma, X))$
- $eval(\sigma, S(Y, X)) = (snd|fst)(S(eval(\sigma, Y), eval(\sigma, X)))$
- $eval(\sigma, op(X)) = op(eval(\sigma, X))$
- $eval(\sigma, INPUT(X)) = X$
- $eval(\sigma, INPUT(N, X)) = (N > 0 \implies X) \vee (N \leq 0 \implies \emptyset)$
- $eval(\sigma, OUTPUT(X)) = \emptyset$

op :

- $AND(Y, X)$
 - $AND(0, X) = \emptyset$
 - $AND(1, X) = X$
 - $AND(Y, X) = X \cup Y$
- $OR(Y, X)$
 - $OR(0, X) = X$
 - $OR(1, X) = \emptyset$

- $OR(Y, X) = X \cup Y$
- $S_{label}(X, CONTROL) = \{\neg CONTROL \Rightarrow (S_{label}, \neg CONTROL), CONTROL \Rightarrow (S_{label}, CONTROL)\}$
 - $S_{label}(X, 0) = [(S_{label}, \neg CONTROL), \perp]$
 - $S_{label}(X, 1) = [\perp, (S_{label}, CONTROL)]$
- $NOT(X) = \neg X$ (apply inside on to vars, i.e. snd)

Functions :

- $JOIN(v) = \sqcap_{w \in pred(v)} \llbracket w \rrbracket$
- $op(Y, X) : \llbracket v \rrbracket = JOIN(v)[eval(JOIN(v), op(Y, X))]$
- $op(X) : \llbracket v \rrbracket = JOIN(v)[(eval(JOIN(v), op(X)))]$

Workthrough q4

Not given.

MIGHT_OVERLAP(V, W) q4

$MIGHT_OVERLAP(V, W) = if(\llbracket V \rrbracket \cap \llbracket W \rrbracket) == \emptyset \text{ then } FALSE \text{ else } TRUE$