Arithmetic Logic Unit (ALU) Design:
A Core Digital System Development

Submitted to:
Supervisor Name: Assistant Prof Dr. Muhammad Kamran Khan
Email: Kamranmu@uop.edu.pk

Phone: (+92)3339154241

Arithmetic Logic Unit (ALU) Design: A Core Digital System Development

As part of my Digital Logic Design (DLD) semester project, I successfully designed and implemented an Arithmetic Logic Unit (ALU)—a fundamental component of computing systems. This project provided hands-on experience in designing digital circuits and deepened my understanding of combinational and sequential logic.

Project Insights & Technical Outcomes:

- **Multi-Function Computation:** Developed an ALU capable of performing arithmetic operations (addition, subtraction) and logical functions (AND, OR, XOR, NOT).
- **Hardware Implementation:** Designed the circuit using logic gates, multiplexers, and adders, ensuring efficient data processing.
- **Boolean Optimization & Efficiency:** Applied Karnaugh Map (K-map) simplifications to optimize logic expressions and reduce hardware complexity.
- **Real-World Applications:** Explored applications in microprocessors, embedded systems, and programmable logic devices.

This project enhanced my expertise in digital system design, logic circuit optimization, and hardware debugging, strengthening my problem-solving abilities. It was an exciting step toward mastering computer architecture and FPGA-based digital systems!