2014

(First Semester)

MASTER OF COMPUTER APPLICATIONS

Paper No: MCA 105

(Computer Organization & Architecture)

Full Marks : 60

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer Question No 1 and **any four** from the rest

1. Answer the following questions briefly: 2X6 = 12

a) What is a structural hazards?

b) What is the disadvantage of direct addressing modes?

c) Explain LRU algorithm used in set-associative cache mapping?

d) Differentiate memory mapped I/O and Isolated I/O.

e) Distinguish between Synchronous and Asynchronous data transfer.

f) If A=+13, B=-7, Compute: A+B.

2. a) Define Microoperation. Explain Bus and Memory transfer using Bus system for 4 registers. **(6)**

2. b) Write the difference between RISC and CISC architecture. **(6)**

3. a) Write addition- subtraction algorithm with detail hardware implementation. **(6)**

   b) Explain the paging technique in virtual memory with diagram **(6)**

4. a) Consider a 5 stage pipeline (Fetch, Decode, Execute, Memory Access and write back). Each stage takes one clock cycle. How many clock cycles are required to execute 10 independent instructions using above mentioned 5 stage pipeline. Draw the pipeline diagram and show the calculation. **(6)**

   b) Explain the three different types of memory mapping. **(6)**

5. a) Explain array multiplier with 2-bit by 2-bit array multiplier. **(6)**

   b) Write a short note on the following: **(2X3=6)**
      i) RISC pipeline
      ii) Delayed Branch
      iii) Delayed Load

6. a) Write a brief notes on handshaking in asynchronous data transfer. **(6)**

   b) What is interrupt? Expalin the different types of interrupt. **(6)**

7. a) Define data transparency? Explain I/O processor (IOP) with block diagram. **(1+6=7)**

b) Explain Direct Memory Controller (DMA) with diagram. **(5)**

8. a) Expain in brief the MIMD architecture. **(6)**

b) Define logic microoperation and shift microoperation by giving a suitable diagram. **(3+3=6)**

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