Asboosh soil X-ot- 2014 Lanizenuza an

(First Semester)

MASTER OF COMPUTER APPLICATIONS

Paper No: MCA 104

(Digital Fundamentals)

Full Marks: 60

Time: 3 hours

The figures in the margin indicate full marks for the questions

Answer Question No 1 and any four from the rest

1. (a) Define:

(4)

10)

- (i) Registers
 - (ii) RAM
 - (b) Design a half subtractor with truth table.

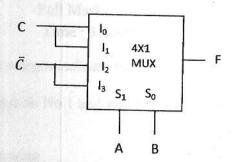
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- (c) Give the comparison between BJT and FET.
- (d) Simplify the logical expression $f(A,B,C) = \overline{ABC} + \overline{ABC} + \overline{ABC} + AB\overline{C}$.
- (e) What are comparators? Write down the truth table for one bit magnitude comparator.
- (f) What do you mean by doping? Explain the types of semiconductors. (6X2=12)

MCA/104/1

2.	(a)	What is a decoder? Draw the logic diagram, truth t	
			(1+5=6)
	(b)	Draw and explain the functional block diagram of 555	
		Timer. 101 AOM MCA 104 Timer. 104 MCA 104 (Digital Fundamentals)	(6)
3.	(a)	Explain in detail J-K flip-flop.	(4)
	(b)	with the state of	
		both common base and common emitter BJT.	
		see and meaning and amount to have able to \$24.08% 20%.	(4)
	(c)	Explain the free-running Multivibrator.	
			(4)
4.	(a)	Implement $F=\sum m (0,1,2,3,4,10,11,14,15)$ using 8x	1
) (T ISZ	
		(ii) RAM	(6)
	(b)	Explain in detail the 4-bit binary ripple counter.	
			(6)
	. 1	(c) Give the comparison between BJT and FE	
5.	(a)	Explain the Enhancement mode MOSFET in detail	
	=	(d) Simplify the logical expression f(A.B.C)	(6)
		ĀBC + ĀBC + ĀBC + ABC	
	(b)	Implement carry look ahead adder with logic diagra	am
	d selas da	and logical expression.	(6)
		bit magnitude comparator	(0)
6.	(a)	What are combinational circuits and sequential circ	uits?
	=57.0) -	semiconductors.	(2)
	1		
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- (b) Explain the forward and reverse bias of a pn junction diode with circuit diagram. (6)
- (c) Find the output F of the 4x1 MUX (4)



- 7. Differentiate between:
 - (a) Monostable Multivibrator and Astable Multivibrator.
 - (b) Synchronous Counter and Asynchronous Counter.
- (6)
- 8. (a) Explain in detail the Master-Slave J-K flip-flop. (6)
 - (b) Calculate the upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}) in a Schmitt Trigger circuit if $V_{sat} = 13 \text{ V}$, $R_1 = 100 \text{k}\Omega$ and $R_2 = 100 \Omega$.
 - (c) Draw the circuit diagram of a 3-bit parallel comparator A/D converter. (2)