

1. b, c

2. A

\$zero 只读不可写, 能被任何数整除.
\$sp 可以加 1, 加 2, 不一定只加 4.

3. a.

4. a, b, c

b, c 包含在 a 里面

5. cause overflow?

D

zero extension & ones extension 包含在 sign extension 里.
进位不一定代表 overflow, (c): $1111 + 0001 = 0000$
 $-1 + 1 = 0$
b) = -8 c) = 0 a) ok. d) = 8 (-8 ~ 7)

6. 16

7. B

2^{16} 个 instruction $\Rightarrow 2^{18}$ bytes.

opcode 6 - rs 5 - rt 5 - imm 16

signed 16 bit $[-2^{15} \sim 2^{15}-1]$ 2^{16} 个数 $\Rightarrow 2^{16}$ instruction $\Rightarrow 2^{18}$ byte

★ branch 都是 i-type

8. D 2^{28}

9. high-z

10. 256 B

6 address $\Rightarrow 2^6$ 个 instruction \Rightarrow Memory = $2^6 \cdot 4B$
32 bit $\Rightarrow 4$ Bytes $\Rightarrow 2^8 B$
 $= 256 B$

11. 8 bits

memory = 1024 B. \Rightarrow instruction = $\frac{1024 B}{4 B} = 256 \Rightarrow \log_2(256) = 8$
32-bit = 4 B.

12. x: 16

y: 1

if n bits number \rightarrow shift register take n clock cycles
load register take 1 clock cycles.

13. 对 bge

#slt d s t \Rightarrow if $s < t$:
d = 1

a b
c d

a) \checkmark


b) \times

c) \times

d) \checkmark

#bne 和 beq 条件相反.

14. b.

15. 

$$15 = 8 + 4 + 2 + 1$$

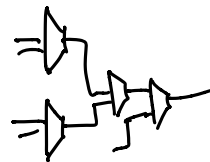
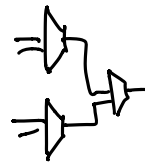
2-1 Mux 用 4

3-1 Mux 用 2 : $3 = 2 + 1$

4-1 Mux 用 : $4 = 2 + 2$

5-1 Mux : $5 = 2 + 2 + 1$
 $= 4 + 1$

6-1 Mux : $6 = 4 + 2$



16 B. D

$$b) = x\bar{y}z + x\bar{y}\bar{z} = x\bar{y}$$

17.

Matal 1

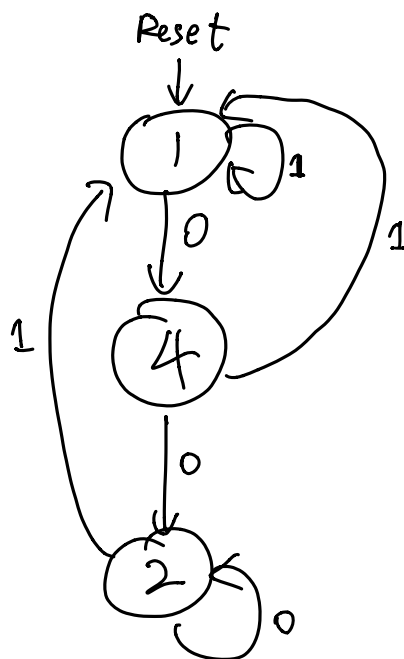
Oxide 3

Semi 2

18. 略

19. package 同

20. i) moore machine
输出不能状态有关



ii) 写 2 个 模块.



iii) 4.

iv) (6)

part C: 1. Booth's alg

$$A = -5 \quad B = -7$$

$$1. \quad A' = 10 \Rightarrow \text{minus.}$$

$$\begin{array}{r} 0000 \ 0000 \\ + \ 0011 \\ \hline P = 0111 \ 0000 \end{array}$$

$$P \gg 1 \Rightarrow 0011 \ 1000$$

$$A' = 11011$$

$$2. \quad A' = 11 \Rightarrow \text{shift}$$

$$P \gg 1 = 0001 \ 1100$$

$$A' \gg 1 = 11100$$

$$3. \quad A' = 01 \text{ add}$$

$$\begin{array}{r} 0001 \ 1100 \\ + \ 1001 \\ \hline P = 1010 \ 1100 \end{array}$$

$$P \gg 1 = 1101 \ 0110$$

$$A' \gg 1 = 11110$$

$$4. \quad A' = 10 \text{ minus}$$

$$\begin{array}{r} 1101 \ 0110 \\ - \ 0111 \\ \hline P = 1101 \ 0110 \end{array}$$

$$P \gg 1 = 0010 \ 0011_{(2)} = 35_{(10)}$$

$$2. \quad a) \quad PC := \$ra + \$zero$$

$$b) \quad \$ra := PC$$

c)

$$1) \quad D \quad \boxed{100011} \quad \begin{array}{c} rs \\ 11101 \\ \hline 29 \end{array} \quad \begin{array}{c} t \\ 00010 \\ \hline 2 \end{array} \quad \left| \quad \begin{array}{c} imm \\ 1111 \dots 1111 \\ \hline 16 \end{array} \right.$$

lw, \$0, -((\$sp)

$$vi) \quad C \quad \begin{array}{l} 30 = 000 \dots 011110 \\ -30 = 111 \dots 100010 \end{array}$$

$$\boxed{100/00} \overset{8}{0/000} \overset{9}{0/001} \mid 111 \dots 111000/0$$

-30

1bu $\$t_1$, -30($\t_0)

iii)

F

6143

2 | 6143

2 | 3071

2 | 1535

2 | 767

2 | 383

2 | 191

2 | 95

2 | 47

2 | 23

2 | 11

2 | 5

2 | 2

2 | 1

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

0

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

00000

v.)

B

$$\overset{2}{00010} \mid \dots$$

iv)

A

$$\begin{array}{ccc} d & s & t \\ \$t_8 & \$t_0 & \$t_1 \\ 0/000 & 0/001 & \dots \end{array}$$

ii)

E

2. a) $\$sp := \$sp + 4(\text{imm})$

0	0	x	0	0
0	0	xx	001	
1	10	1	0	

b) $\$ra := PC + 100$

0	0	x	0	0
0	0	xx	001	1011
0	10	1	0	

↑
从PC来的
所以是"0"

c)

0	0	0	1	0
x	1	xx	xxx	
x	xx	0	x	

Fetch 读-个东西

Part 1:

32-bit instruction register which can decode the input message into opcode, rs, rt, rd, and imm

1. i: imm
0: opcode

3. reg [3:0] M [255:0]
⇒ 53-个RAM

Input [7:0] a ; \rightarrow address

answer :

create a $256 * 4$ bit RAM
with synchronous enable
with one-bit wire signal w that control
write or read

4. e = enable
w = write/read'

part F

1. a) sra \$s0, \$s0, 3

b) xori \$a0, \$a0, -1

c) # ~~is~~ load 指令
lb \$t0, 0(\$sp)

★ d) # ~~is~~ pc = 0

jr \$zero
r-type

better

j 0
j-type

\Rightarrow 只影响后 26 位
高 6 位无法改