UNIVERSITY OF TORONTO

Fall 2012 Midterm

CSC258: Computer Organization

Duration: 2 hours

November 1st, 2012

Last Name: _____

First Name: _____

Student Number: _____

Instructor: **Steve Engels**

Instructions:

- **Write your name on the back of this exam paper.**
- **Do not open this exam until you hear the signal to start.**
- Have your student ID on your desk.
- No aids permitted other than writing tools. Keep all bags and notes far from your desk before the exam begins.
- There are 3 questions on 8 pages. When you hear the signal to start, make sure that your exam is complete before you begin.
- Read over the entire exam before starting.
- If you use any space for rough work or have to user the overflow page, clearly indicate the section(s) that you want marked.

Mark Breakdown

Part A:	**/22**
Part B:	**/22**
Part C:	**/ 6**
Total:	**/ 50**

Part A: Short Answer (22 marks)

Answer the following questions in the space provided. When providing a written answer, write **as clearly and legibly as possible**. Marks will not be awarded to unreadable answers.

1. Given inputs `A`, `B` and `C`, which of the following are valid maxterms? Circle all that apply. **(2 marks)**

a) $\overline{C} + \overline{B} + \overline{A}$

b) $A \cdot B \cdot \overline{C}$

c) $C \cdot B + A$

d) $A + \overline{C} + B$

e) $B + C$

f) $A + B + A$

2. True or False? JK flip-flops behave like RS flip-flops as long as at least one input is high. **(1 mark)**

True **False**

3. What is the most negative value possible for a 8-bit signed binary number? Write your answer in both binary and decimal in the space below. **(2 marks)**

4. Which of the following Verilog statements doesn't belong in an `always` block? **(1 mark)**

a) `case`

b) `assign`

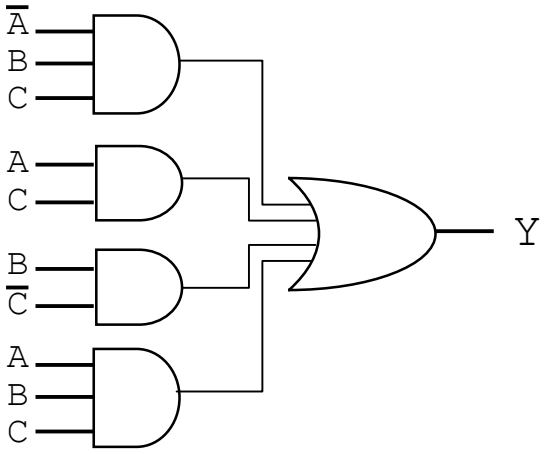
c) `if`

d) `for`

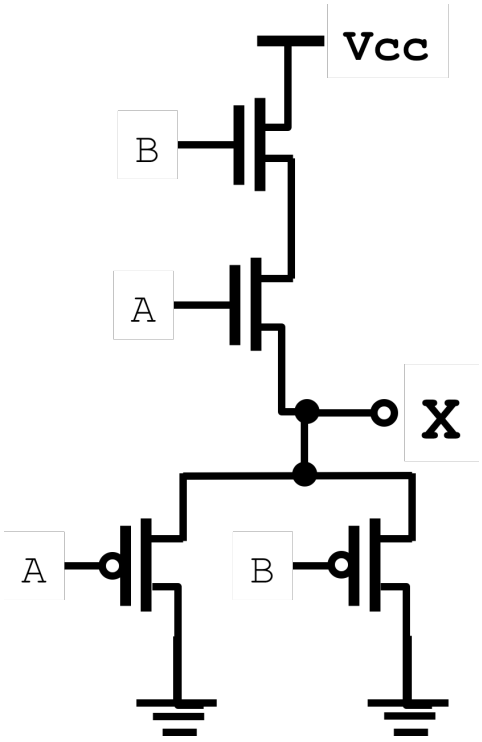
5. What is the name of the current caused by the combination of holes and electrons at a pn junction? **(1 mark)**

6. In the space below, assuming you have 18 switches as inputs and 18 red LEDs as outputs, write a Verilog statement that writes the values of the switches onto the LEDs. **(2 marks)**

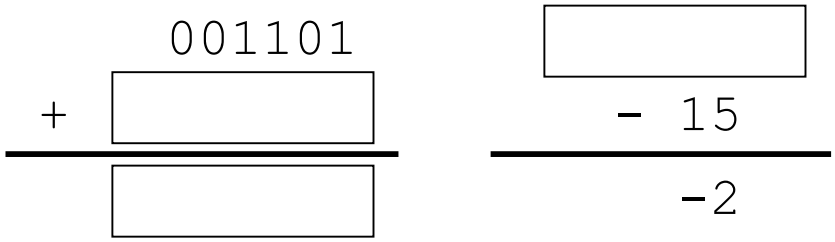
7. Consider the circuit below. What is the boolean expression for Y, in terms of A, B & C? For full marks, provide the most reduced expression possible, and show your work. **(3 marks)**



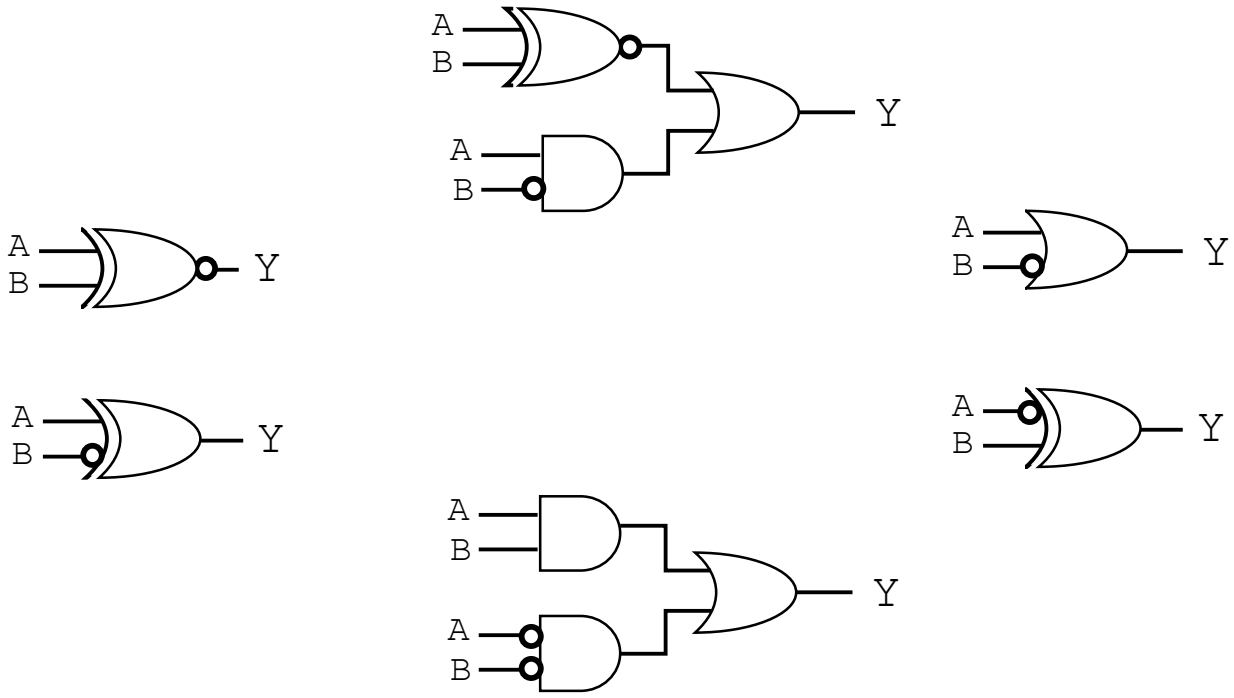
8. Consider the following circuit. What logic gate is represented by this circuit? **(2 marks)**



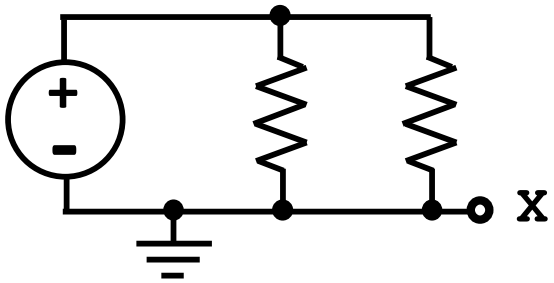
9. The signed binary and decimal operations below are the same. Fill in the blanks. **(3 marks)**



10. Which of the circuits below have equivalent behaviour? Draw lines to connect any circuits that match. **(4 marks)**

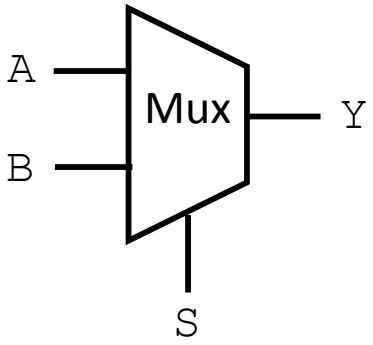


11. Assuming the voltage source on the left is 5V, what is the logic value of X? **(1 mark)**

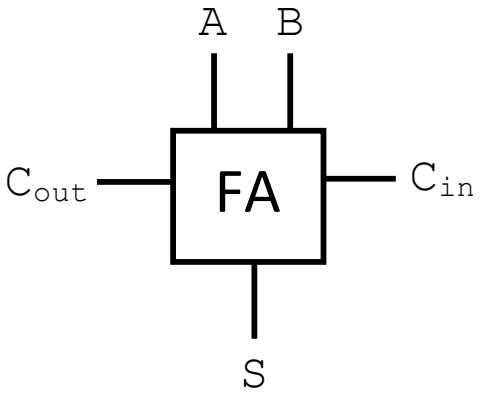


Part B: Circuit Design and Analysis (22 marks)

1. Consider the two-input multiplexer device on the right. In the space below, show how a **three-input multiplexer** can be implemented as a combination of two-input mux units. For full marks, no other gates or devices should be used in your solution. **(4 marks)**



2. Consider the full adder unit on the right. In the space below, draw a circuit that would implement a 4-bit adder circuit, implemented only using these 1-bit full adder units. **(4 marks)**



3. In the space below, use T flip-flops to implement a 3-bit counter that counts **down**, not up. That is, the counter values on [Q_2, Q_1, Q_0] will be `111` on the first clock cycle, then `110` on the second, then `101` on the third, all the way down to `000`. The counter will then reset back to `111`. For full marks, no other gates or logic devices should be used. **(4 marks)**

4. Given the minterms [m_o, m_1, m_2, m_4, m_5, m_8, m_{10}, m_{12}], fill in the Karnaugh map below. Make the minterm groupings that will result in a circuit with the lowest gate cost. **(3 marks)**

	$\overline{C} \cdot \overline{D}$	$\overline{C} \cdot D$	$C \cdot D$	$C \cdot \overline{D}$
$\overline{A} \cdot \overline{B}$				
$\overline{A} \cdot B$				
$A \cdot B$				
$A \cdot \overline{B}$				

5. Given the Karnaugh map groupings in the previous question, write the minimal equivalent boolean expression in the space below. **(1 mark)**

6. For this question, implement a FSM that takes in an input called `X`, and returns an output called `SAME`. `SAME` is high if the current value of `X` is the same as the previous value of `X`.

Draw a state diagram for this circuit in the space below. **(5 marks)**

7. How many flip-flops would you need to implement the state machine from Part 6? **(1 mark)**

Part C: Verilog (6 marks)

Consider the piece of Verilog code on the right.

1. What does this piece of code do? **(2 marks)**

2. What does the z signal represent here? **(1 mark)**

```
module part1 (V, z, M);
   input [3:0] V;
   output z;
   output [3:0] M;

   wire[2:0] B;

   // circuit A
   assign z = (V[3] & V[2]) |
           (V[3] & V[1]);

   // circuit B
   assign B[2] = V[2] & V[1];
   assign B[1] = V[2] & ~V[1];
   assign B[0] = (V[1] & V[0]) |
           (V[2] & V[0]);

   // multiplexers
   assign M[3] = ~z & V[3];
   assign M[2] = (~z & V[2]) |
           (z & B[2]);
   assign M[1] = (~z & V[1]) |
           (z & B[1]);
   assign M[0] = (~z & V[0]) |
           (z & B[0]);

endmodule
```

```
module part2 (out, enable, clk, reset);

output [7:0] out;
input [7:0] data;
input enable, clk, reset;
reg [7:0] out;

always @(posedge clk)
if (reset) begin
  out <= 8'b0;
end
else begin
  out <= {out[6],out[5],
          out[4],out[3],
          out[2],out[1],
          out[0], enable};
end

endmodule
```

Consider the piece of Verilog code on the left.

3. What device does this piece of code represent? **(3 marks)**

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Please enter your first and last name in the space below. Do NOT write your student number here.