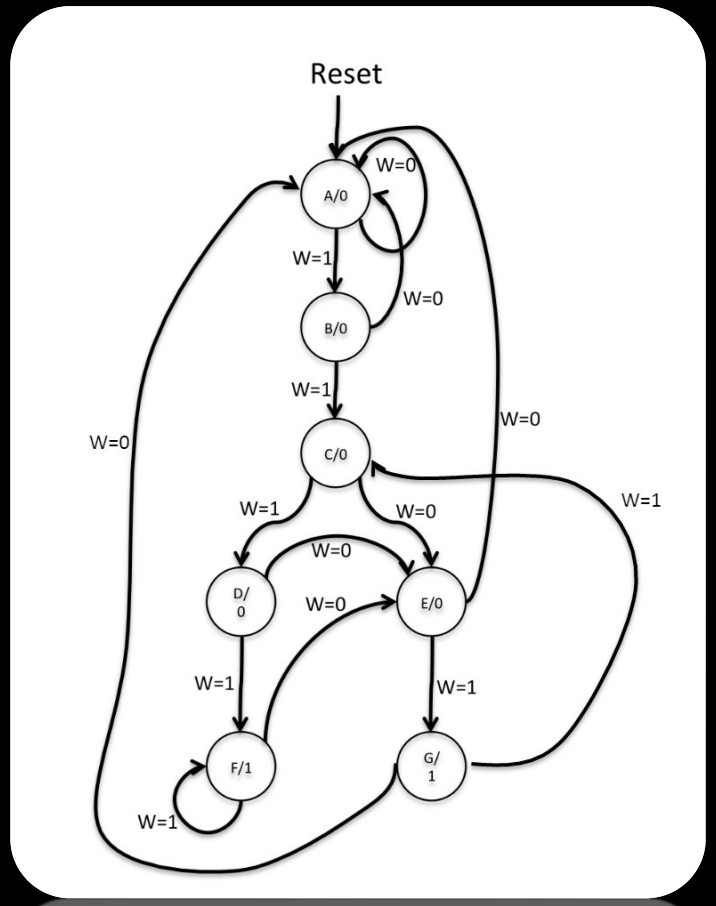
Lab 6 Preparation

Lab 6 Components

- Part I: Create a Finite State Machine
  - Make a clocked sequence recognizer.
- Part II: Control a datapath
  - Combine datapath + FSM to perform ALU functions.
- Part III: Divider circuit

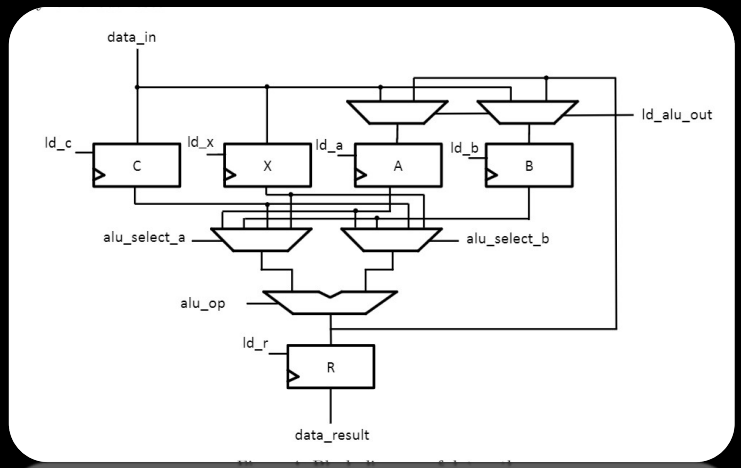
Part I: Finite State Machine

- Recognize 1111 or 1101 sequence.
- Starter code provided.
  - Case statement that updates flip-flop values (stored in a 3-bit register).
  - You fill in the missing case conditions.



Part II: Controlling datapath

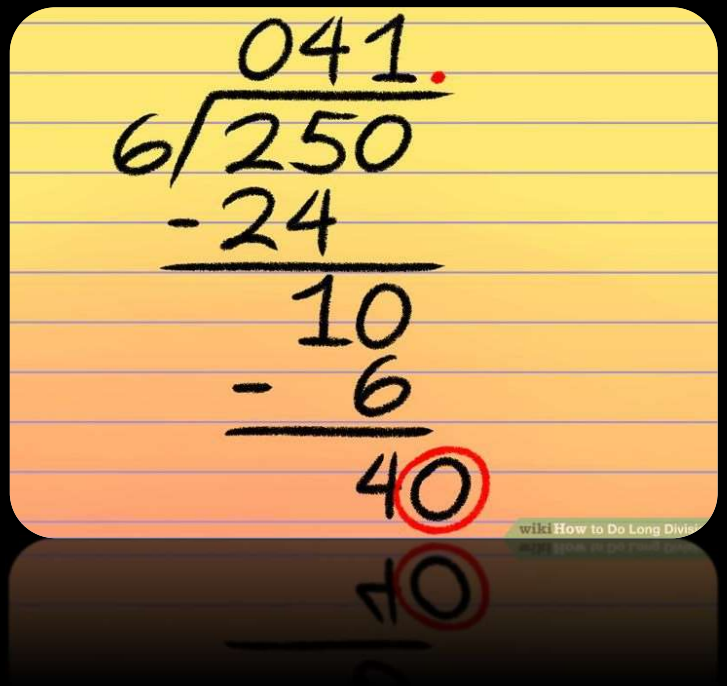
- Remember the ALU datapath example we did in class?
  - This is another! ☺
- We provide the code for the datapath, you provide the controller FSM.



  - Send signals to the datapath components to move the data around, and make the computation happen.
  - Provide state diagram in prelab, and compare with Quartus-generated one.

Part III: Divider Circuit

- Note: This part is optional, but can be done for bonus marks in the course.
- Basic idea from decimal long division:
  - From left to right, find where the divisor can be subtracted from the dividend.
  - Doing this in binary is simpler, except that we keep the divisor static, and move everything else!



New Verilog Syntax

- The `localparam` keyword:

```
localparam A = 3'b000;
```

  - Defines values that are replaced at compile time.