



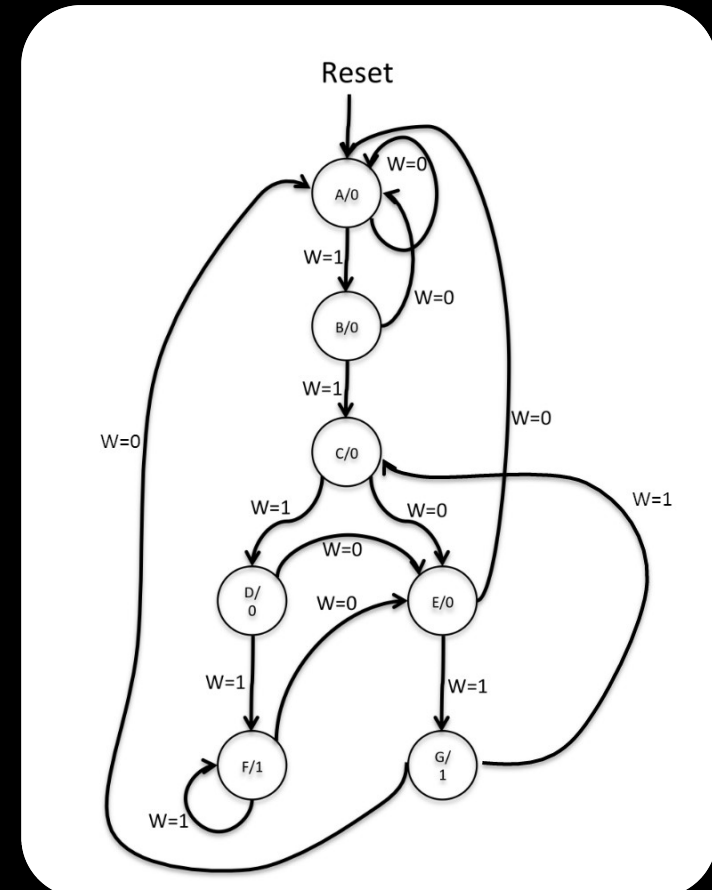
Lab 6 Preparation

Lab 6 Components

- **Part I:** Create a Finite State Machine
 - Make a clocked sequence recognizer.
- **Part II:** Control a datapath
 - Combine datapath + FSM to perform ALU functions.
- **Part III:** Divider circuit

Part I: Finite State Machine

- Recognize 1111 or 1101 sequence.
- Starter code provided.
 - Case statement that updates flip-flop values (stored in a 3-bit register).
 - You fill in the missing case conditions.



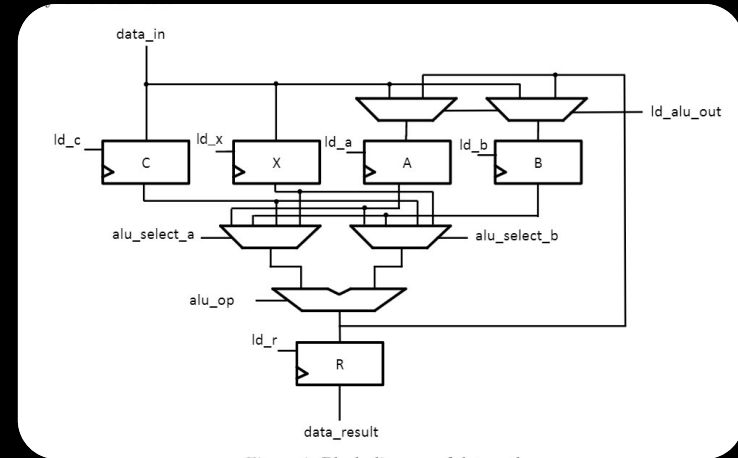
Part II: Controlling datapath

- Remember the ALU datapath example we did in class?

- This is another! 😊

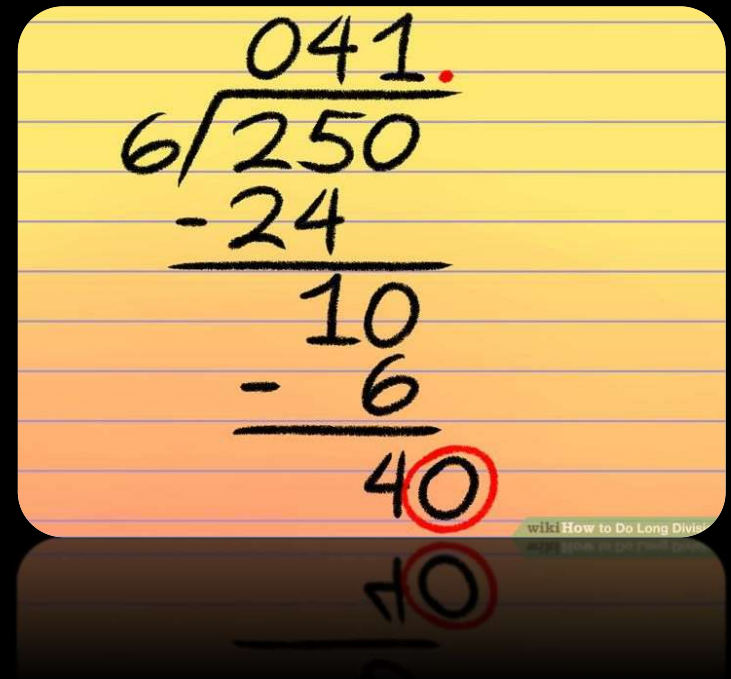
- We provide the code for the datapath, you provide the controller FSM.

- Send signals to the datapath components to move the data around, and make the computation happen.
 - Provide state diagram in prelab, and compare with Quartus-generated one.



Part III: Divider Circuit

- Note: This part is optional, but can be done for bonus marks in the course.
- Basic idea from decimal long division:
 - From left to right, find where the divisor can be subtracted from the dividend.
 - Doing this in binary is simpler, except that we keep the divisor static, and move everything else!



A handwritten long division problem on lined paper. The divisor is 6, and the dividend is 250. The quotient is 41 with a decimal point. The steps shown are: 6 goes into 25 four times (24), leaving a remainder of 10. Then, 6 goes into 10 one time (6), leaving a remainder of 40. The final result is 41.0. The number 40 is circled in red.

$$\begin{array}{r} 041. \\ 6 \overline{) 250} \\ \underline{-24} \\ 10 \\ \underline{-6} \\ 40 \end{array}$$

New Verilog Syntax

- The `localparam` keyword:

```
localparam A = 3'b000;
```

- Defines values that are replaced at compile time.