8

top.v

OpCodes

(Opcodes

Processor)

processor

spare symbols

mmc\_opcodes

8

Initialize

Processor

init\_x7

arb8

spi\_arbiter

SPI

I/O

Intf

spiwr

SPI

Proc

????

spiwr\_fifo

spidata\_fifo

SPI CLK

12.5MHz

freq\_fifo

8

set\_freq

Frequency

Processor

set\_power

Power

Processor

power\_fifo

8

pulse\_fifo

8

pulse\_processor

Pulse

Processor

bias\_processor

Bias

Processor

bias\_fifo

8

8

8

spi\_fifo\_mux

8

8

8

i0

i1

i2

i3

i4

8

clkgen

main\_clocks

50MHz

MMC Transactor

(initial block:

array oplist)

initial block

pulse.v (top.pulse\_processor)

OpCodes

(Opcodes

Processor)

pattern\_processor

freq\_fifo

power\_fifo

bias\_fifo

ptn\_opcodes

8