B38DF **Lab 1 Report Template**

**PRINT NAME: ……………………………..…………………………... Matriculation No:………………………….**

Complete the following sections:

1. Section 7 Checking the Simulation Result

|  |
| --- |
| *Does the actual truth table found from simulation match the intended truth table on page 5?* |

1. Section 8 Modifying the Logic Function

|  |
| --- |
| *Your K-map and your derived logic expression derived should be shown below* |

1. Modified Verilog Source file

|  |
| --- |
| *(i)Give verilog code for the correct logic expression. (ii)Is this structural or behavioural representation?*  *(iii)Give your modified source file.* |

1. Simulator Waveforms for 3 above.

|  |
| --- |
|  |

1. Verilog code for Section 10.

|  |
| --- |
|  |

1. Simulator Waveforms for 5 above.

|  |
| --- |
|  |