

## SYDNEY MOTORSPORT, FORMULA STUDENT - OVERVIEW

### What is Sydney Motorsport and Formula Student?

Sydney Motorsport is a student-run engineering team at the University of Sydney. Each year, we design, build, and race an open-wheel electric vehicle to compete at the Formula Student Australasia competition, held annually in December in Melbourne. The project mechanical, electrical, and software disciplines under tight deadlines, budgets, and performance goals.

As part of the team, I have contributed to both the design and implementation of the electrical systems, applying engineering principles to solve real-world challenges in performance, reliability, and safety.

### My Role and Contributions

#### *Position Progression:*

- Electrical Department Head - Jan - Present 2025
- High Voltage Lead Engineer - Aug - Dec
- Low Voltage Member - Jan 2023 - Aug 2024

#### *Contributions and Projects*

##### Electrical Department Head

As Department Head, I oversee the design, development, and integration of the entire electrical system for the team's first track-tested EV, covering both high and low-voltage subsystems.

- Manage a team of over 15 electrical engineers and ensure all project deadlines and safety requirements are met.
- Coordinate system level design reviews and testing schedules.
- Lead recruitment, onboarding, and technical upskilling of new team members.
- Oversee design for manufacturability (DFM) and rule compliance for competition readiness.
- Pioneered the design of the electrical system of the EV.



2024 Competition - Calder Park, Melbourne

##### High Voltage Lead Engineer

As High Voltage Lead, I was responsible for the design and implementation of all high-voltage systems for the team's first electric vehicle.

- Led a 10-person subsystem in developing the battery pack (accumulator) and associated control and safety circuitry.
- Designed the precharge and discharge circuits, and validated inverter-motor configurations for performance and reliability.
- Managed component selection, integration testing, and documentation for scrutineering compliance.
- Achieved a key milestone: successful accumulator scrutineering at competition, meeting all safety and performance requirements within a two-month development window.

##### Low Voltage Engineer

As a Low Voltage member, I contributed to the design and development of vehicle support and control electronics.

- Designed and built the Tractive System Active Light (TSAL) circuit, a safety system that indicates when the vehicle operates above 60V.
- In 2025 (while electrical department head), redesigned the TSAL into the integrated TSAL-DISCHARGE board, combining the tractive light functionality with the discharge circuit.
- Assisted with PCB design, system debugging, and wiring loom manufacture

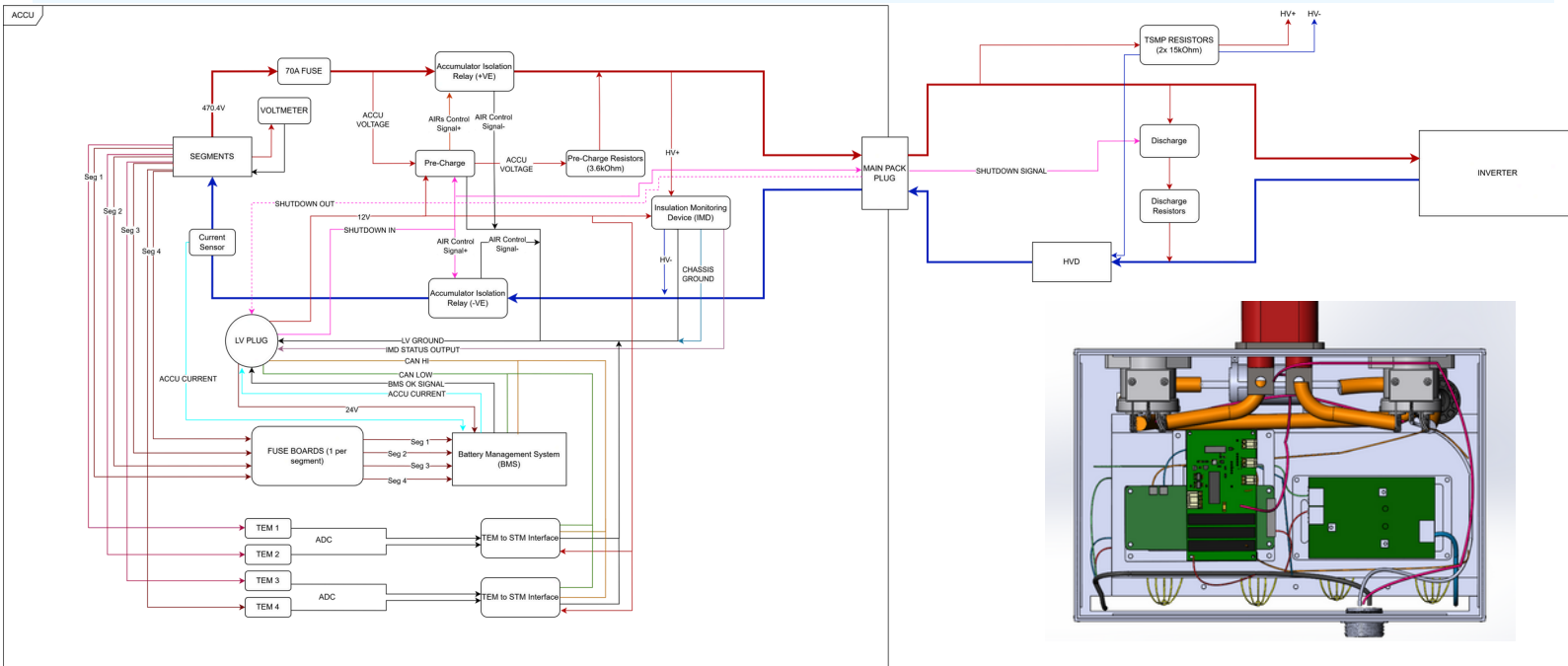


The team making its way to the static tests at competition (2024)

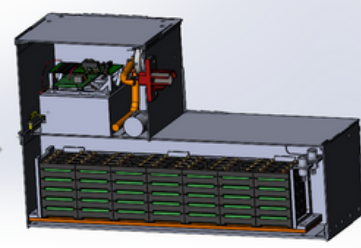
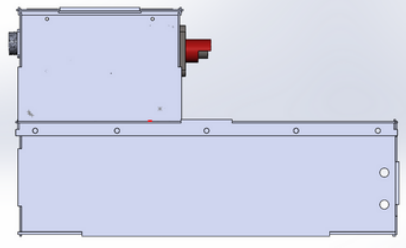
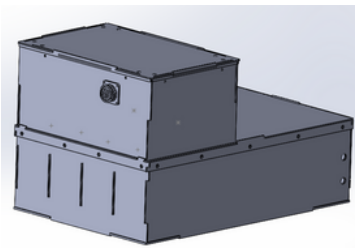
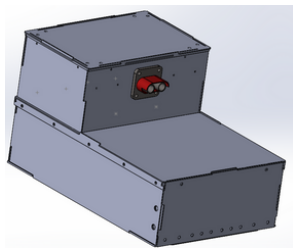


Getting the accumulator fully ready for Accumulator Scrutineering (2024)

## HIGH VOLTAGE ELECTRICAL SYSTEM DESIGN - TEAM'S FIRST EV



System Block Diagram of the High Voltage System: Consists of Accumulator (ACCUM) and Tractive System. Bottom right image is LV control electronics box of ACCUM

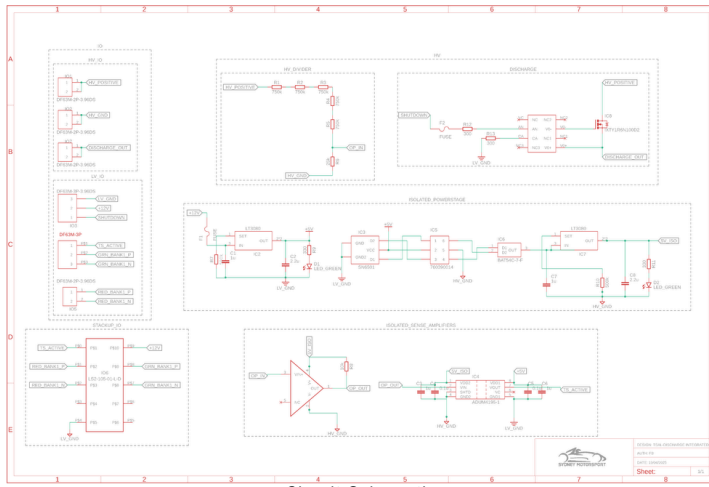


Current Accumulator Design: - Rightmost image is a section-view showing the inside (segment of battery modules (117.6V) on the bottom and all control circuitry, BMS, and Isolation Relays in the top box) (2025): Max Voltage = 470.4V

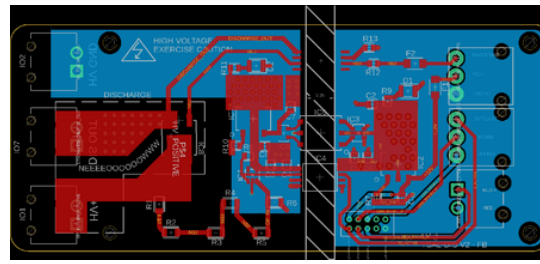
As former High Voltage Lead and current Electrical Department Head of Sydney Motorsports, my focus has been more on the high voltage subsystem of the vehicle, this includes the accumulator, inverter, motors and integration of all of this with the low voltage system as well as packaging it all together.

- Accumulator consists of the main following components
  - 470.4V battery pack, using 112 ENEPAQ 18650VCT5A modules in a configuration of 1s5p (each module consisting of 1 cell in series, and 5 cells in parallel)
  - AIRs or IRs (Accumulator Isolation Relays / Isolation Relays): These isolate the battery from the rest of the system outside the accumulator until the vehicle is ready.
  - BMS (Battery Management System): Off the shelf component which measures the cells state of charge and temperatures as well as passively balance the cells.
  - IMD (Insulation Monitoring Device): Off the shelf component (as per rules) which measures the isolation between high voltage and low voltage ground, will send a fault signal if isolation has been tripped
  - Precharge Circuit: When the vehicle is ready, the precharge safely powers up the system gradually until the tractive system is ready to receive full power, in which case it will close the positive AIR.
  - TEMs (Thermistor Expansion Modules): These measure the temperatures of the cells within the modules, and relay these to the BMS through CAN communication using an STM32.
  - High Voltage Indicator Light: This board is a safety system that is purely powered by High Voltage and is a device that will indicate if the tractive system is at a high voltage (>60V) despite the vehicle supposedly being shut off.

## TSAL-DISCHARGE CIRCUIT

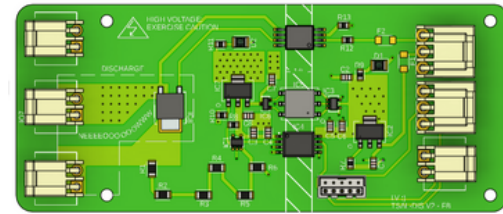


Circuit Schematic



PCB Layout

3D Render of PCB



### What?

The TSAL-DISCHARGE circuit is a combined TSAL and Discharge circuit. Its purpose is twofold:

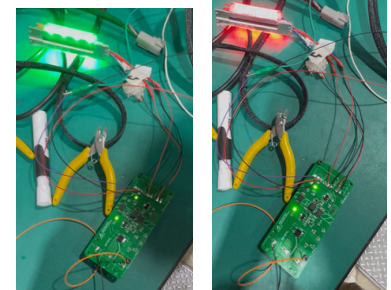
- To indicate when the vehicle's tractive system (inverters) is  $>60V$  via a visible indicator light mounted on the vehicle's roll-hoop.
- Safely discharge the tractive system.

This board replaces two separate circuits, simplifying wiring and improving maintainability.

### How?

- Schematic and Layout designed in Fusion360, simulated in LTspice
- Utilises a voltage sensing network to monitor the tractive system voltage, utilising an op-amp with an internal reference to detect if  $>60V$ .
- When the shutdown signal is LOW, the discharge circuit creates a closed RC circuit between the inverter capacitors (150uF) and a 4.2kOhm resistor, hence discharging a 470.4V tractive system in 3.15 seconds.

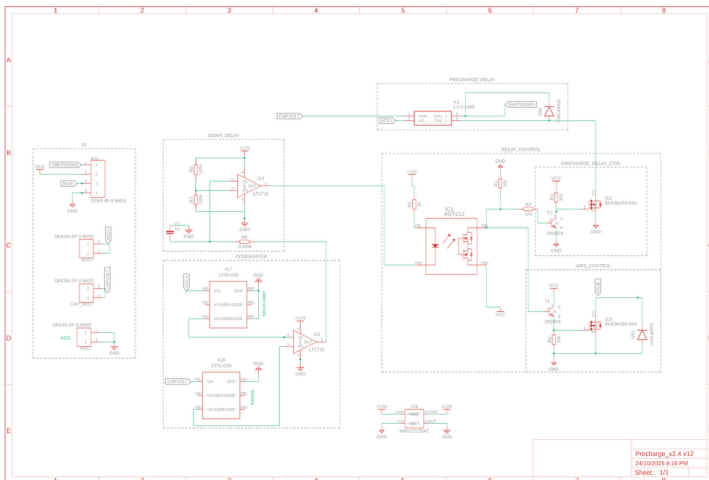
### Results



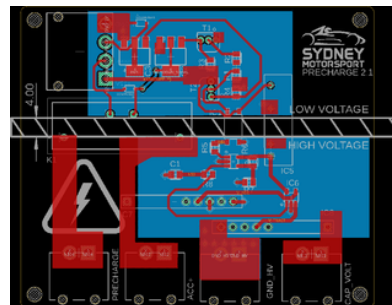
Left:  $V < 60$ , Right:  $V > 60$

- Successfully Validated and tested in electrical system

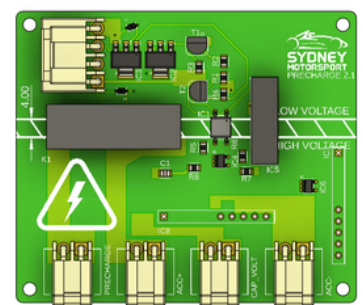
## PRECHARGE CIRCUIT



Circuit Schematic



PCB Layout



3D Render of PCB

### How?

- The circuit and layout was designed in Fusion360, simulated in LTspice
- When the shutdown signal is HIGH, the precharge relay on the board closes, connecting the accumulator directly to the tractive system through a resistor.
- A voltage sensing network detects when the tractive system is  $>95\%$  of the max voltage, and closes the PIR, passing full power through to the tractive system while preventing inrush current.

### Results

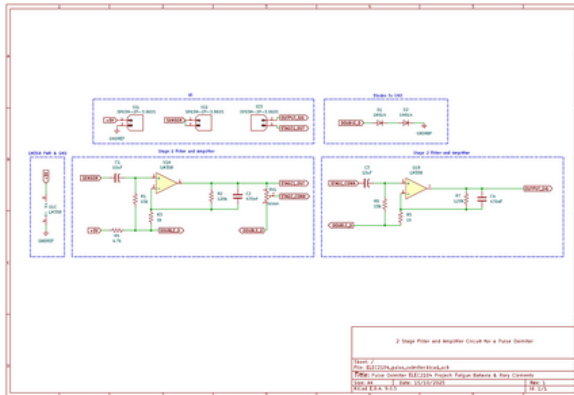
- Precharge circuit was successfully designed and tested, passing the regulation requiring the vehicle to be safely charged to 95% max voltage in  $<5$  seconds. Circuit is currently used in 2025 EV build.

### What?

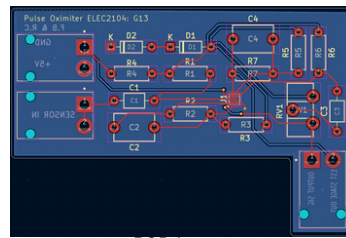
The Precharge Circuit is a safety-critical subsystem responsible for managing the initial connection between the accumulator and inverter in an electric vehicle. It limits inrush current during startup and ensures the tractive system voltage rises smoothly to over 95% of the accumulator voltage before the positive isolation relay closes, bypassing the precharge resistor and passing full power to the tractive system.



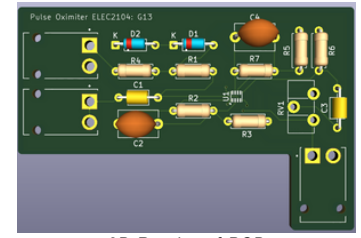
## PULSE OXIMETER CIRCUIT



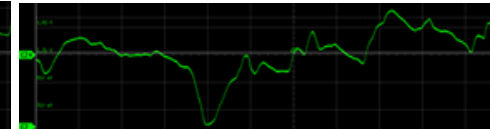
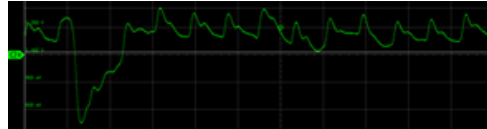
Circuit Schematic



PCB Layout



3D Render of PCB



Oscilloscope readings of output - Left: Red LED On and IR Off, Right: IR LED On and Red Off

### What?

This Pulse Oximeter circuit is a fully analog circuit which was designed and developed for ELEC2104: Electronic Devices and Circuits. It measures the heartbeat and the SPO2 using IR and Red LED's passing light through to a BJT phototransistor gate input.

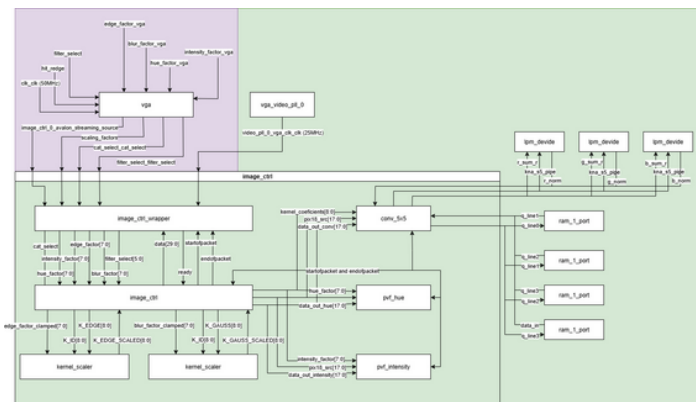
### How?

- Schematic and Layout designed in KiCad
- The circuit uses a BJT phototransistor sensor that detects infrared (IR) and red LED light transmitted through a fingertip. The sensor output is taken from the node between the collector of the phototransistor and a 22 kΩ load resistor, producing a small voltage signal proportional to the varying light intensity caused by blood flow.
- This signal is then passed through a two-stage cascading RC filter network, designed to isolate the 1–3 Hz frequency range corresponding to the human heart rate. The filtering stages attenuate noise from ambient light and high-frequency interference, leaving a clean pulse waveform.
- The conditioned signal is then observed and verified using an oscilloscope, confirming proper frequency response and amplitude variation in sync with the user's heartbeat.

### Results

The circuit successfully detected and displayed pulse waveforms between 1–2 Hz on the oscilloscope. The two-stage RC filter effectively suppressed noise, producing a stable and repeatable signal. Testing across users confirmed consistent response, validating the circuit's analog filtering design and sensor accuracy.

## BEAT-SYNC VFX (FPGA)



System Block Diagram

### What?

This project is an FPGA-based system that was completed as a group assignment for a core unit (MTRX3700: Mechatronics 3). This project processes live audio input through a microphone stream, and maps the BPM, beat detection and high, mid, low frequency bands to image filtering operations on a VGA output display. My contribution to this group project was the VGA controller, image rendering pipeline, 5x5 convolution filter, weighted sum based convolution kernel scaling, as well as the intensity and hue pixelwise image filters.



Image 1: Original, Image 2: Edge Detection, Image 3: Intensity, Image 4: Hue

### How?

- Implemented a VGA display controller in Verilog/SystemVerilog with pixel synchronization, frame timing, and memory buffering, simulated using custom testbenches.
- Designed a parameterised 5×5 convolution filter using separable kernels for 1px per cycle at 25MHz throughput with weighted sum kernel scaling according the audio signals input

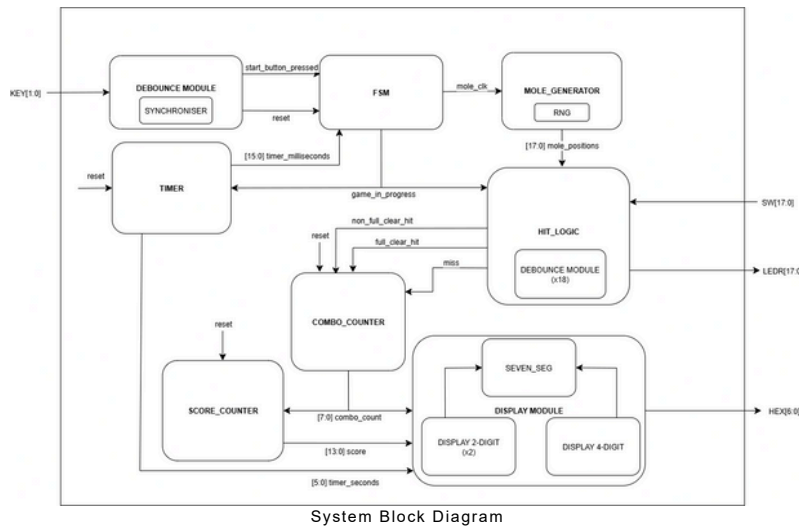


VIDEO OF PROJ

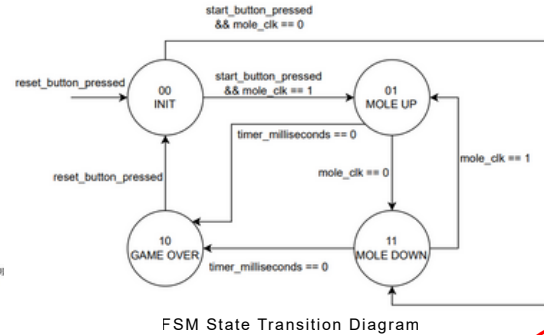
### Results

- The system successfully performed real-time image filtering and display, controlled by the live audio input.
- Audio signal BPM and frequency bands were used to modulate the convolution kernel and pixelwise filters, producing visible changes in the filtered image on the VGA monitor.
- This project demonstrated complete FPGA-based data path integration from analog input to visual output, combining DSP, video, and hardware architecture in one design.

## WHACK A MOLE (FPGA)



System Block Diagram



FSM State Transition Diagram



VIDEO OF PROJ

### What?

This FPGA-based group project was completed as the first assignment for a core unit (MTRX3700: Mechatronics 3). The project involved designing and implementing a Whack-A-Mole game on an FPGA board (DE2-115) using Verilog. The system replicates the classic arcade game by lighting LEDs as moles and detecting user inputs through toggle switches to register hits and misses. The game logic, timing, and scoring were handled entirely in hardware to achieve low-latency and deterministic performance.

My contribution in the project was the FSM design, which coordinated all gameplay states, timing signals, and control outputs.

### Results

- The system achieved stable and predictable gameplay with correct mole timing and score updates.
- During the live demo, the full game performed seamlessly, with responsive LED updates and scoring, confirming successful integration between control logic, RNG-driven mole generation, and user input.
- This project demonstrated the practical application of hardware-based state machines and modular FPGA design, reinforcing my understanding of digital control systems, timing analysis, and Verilog synthesis workflow.

### How?

- I developed a custom Moore-style FSM to manage transitions between the core game states: INIT, MOLE\_UP, MOLE\_DOWN, and GAMEOVER.
- The FSM received button inputs and timing signals from the TIMER module.
- Based on these inputs, control signals such as mole\_clk (to toggle mole visibility) and game\_in\_progress are generated.
- A Gray-coded state encoding was chosen to minimize transition errors and reduce combinational logic complexity.
- FSM was tested using custom made testbenches in ModelSim.
- The design was integrated into a larger modular system with components to create the functioning game.