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Note：
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

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Version	Date	Author	Change Note	Approved
V00	20170925	LZZ	First edictor	

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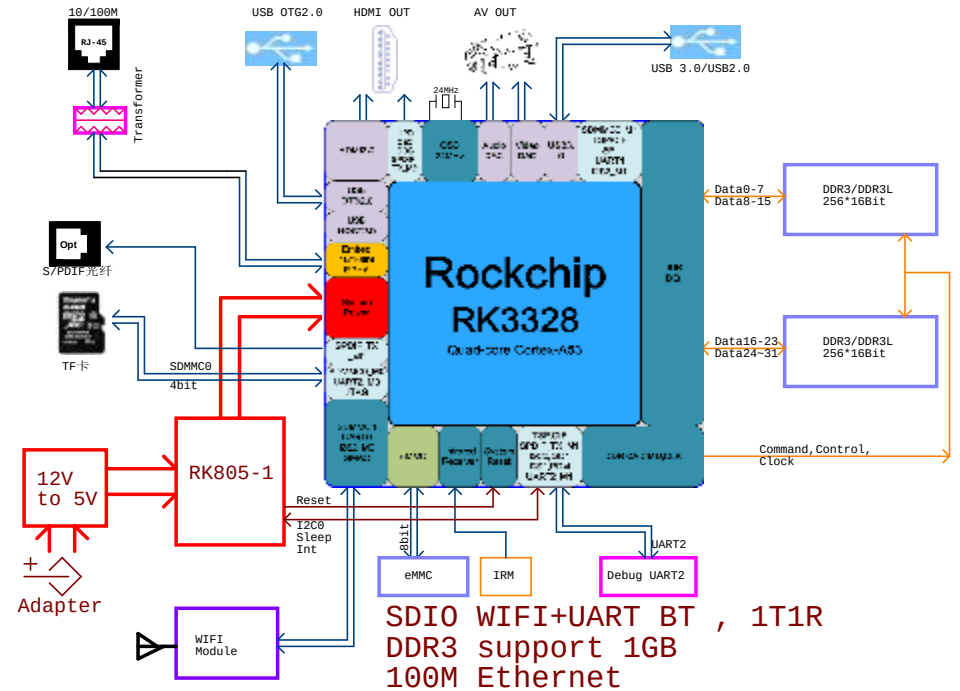
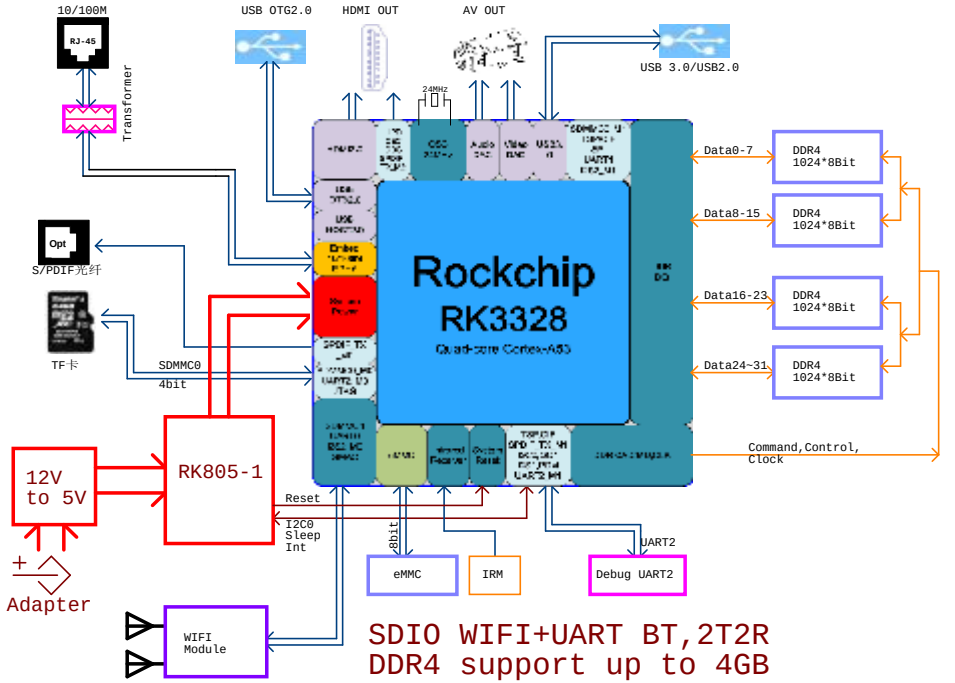


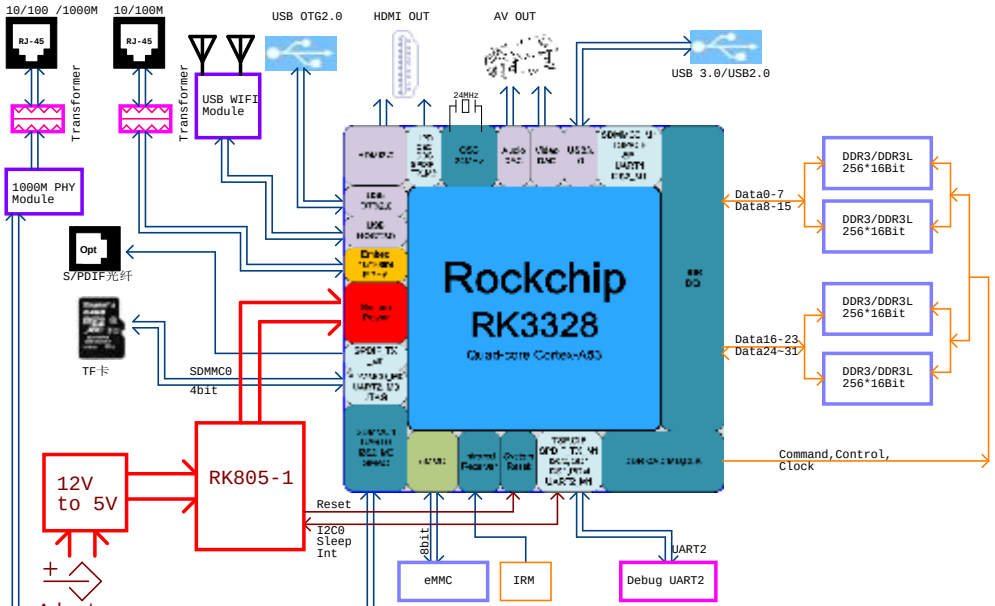
SDIO WIFI+UART BT , 1T1R
DDR3 support 1GB
100M Ethernet

Default config



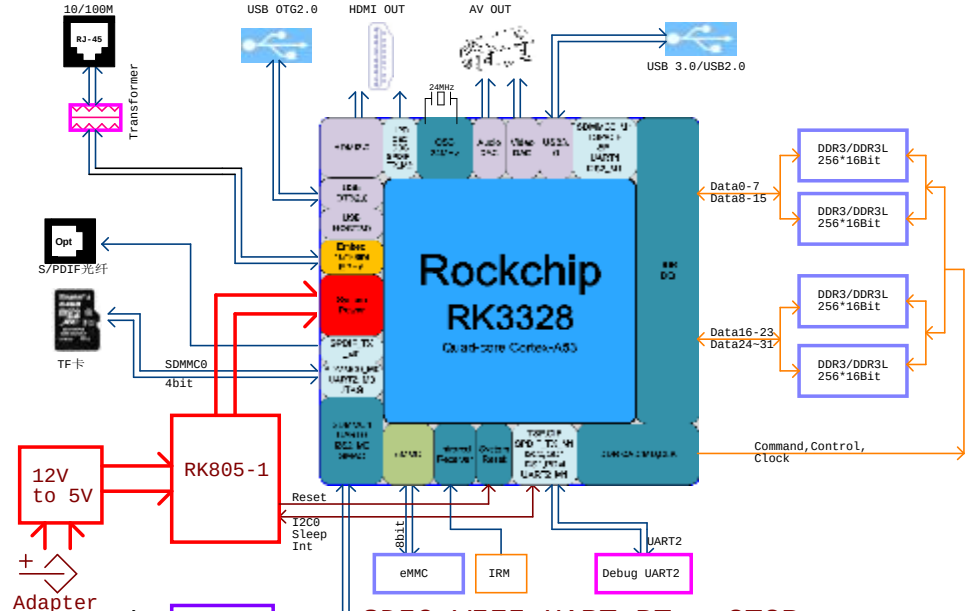
SDIO WIFI+UART BT,2T2R
DDR4 support up to 4GB
100M Ethernet

Config4



USB WIFI/BT ,
DDR3 support up to 2GB
100M+1000M Ethernet

Config2



SDIO WIFI+UART BT , 2T2R
DDR3 support up to 2GB
100M Ethernet

Config3

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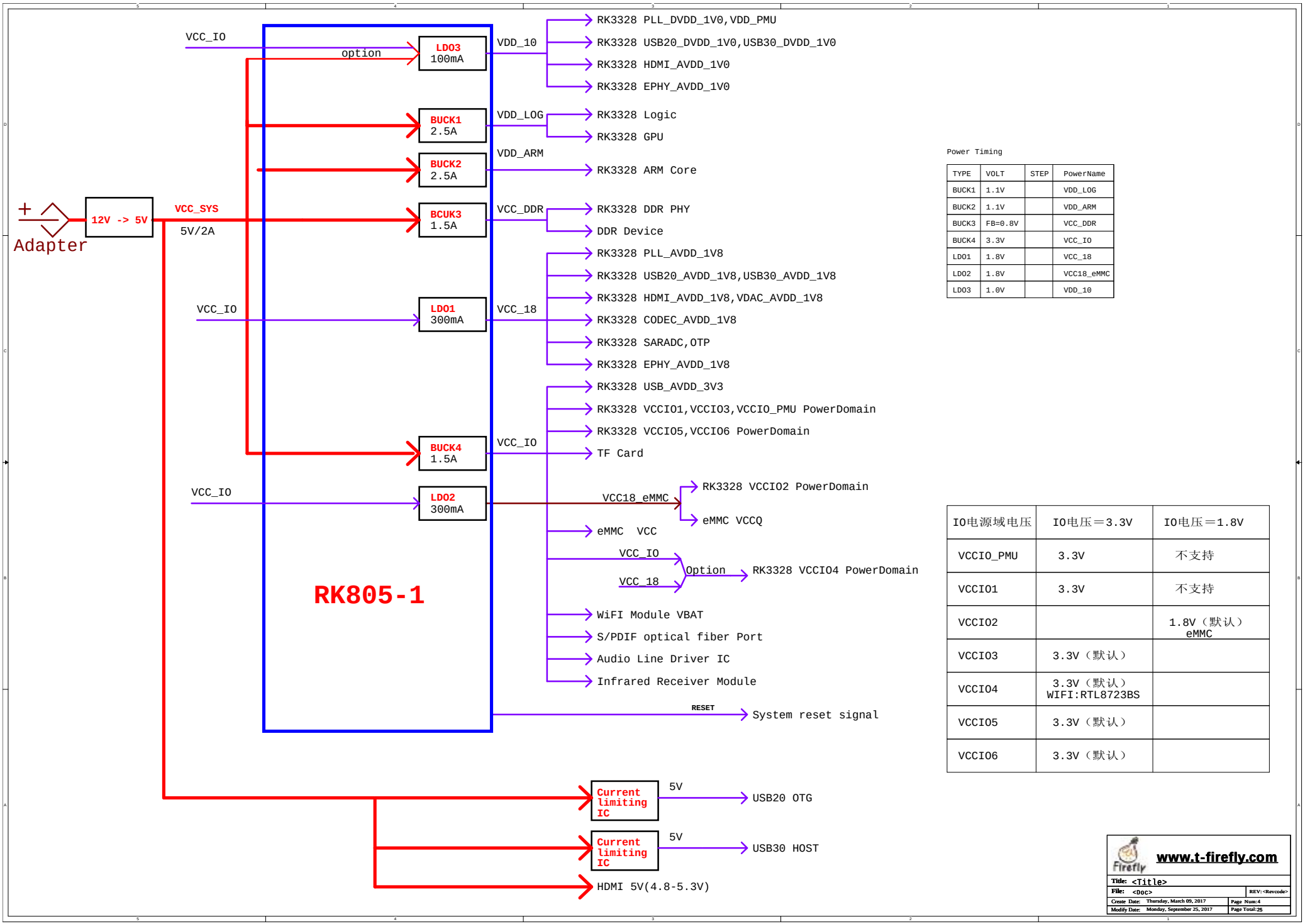

Power Timing

TYPE	VOLT	STEP	PowerName
BUCK1	1.1V		VDD_LOG
BUCK2	1.1V		VDD_ARM
BUCK3	FB=0.8V		VCC_DDR
BUCK4	3.3V		VCC_IO
LDO1	1.8V		VCC_18
LDO2	1.8V		VCC18_eMMC
LDO3	1.0V		VDD_10

IO电源域电压	IO电压＝3.3V	IO电压＝1.8V
VCCIO_PMU	3.3V	不支持
VCCIO1	3.3V	不支持
VCCIO2		1.8V（默认） eMMC
VCCIO3	3.3V（默认）	
VCCIO4	3.3V（默认） WIFI:RTL8723BS	
VCCIO5	3.3V（默认）	
VCCIO6	3.3V（默认）	

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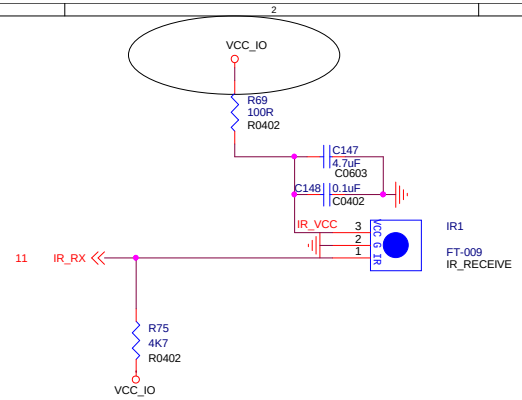
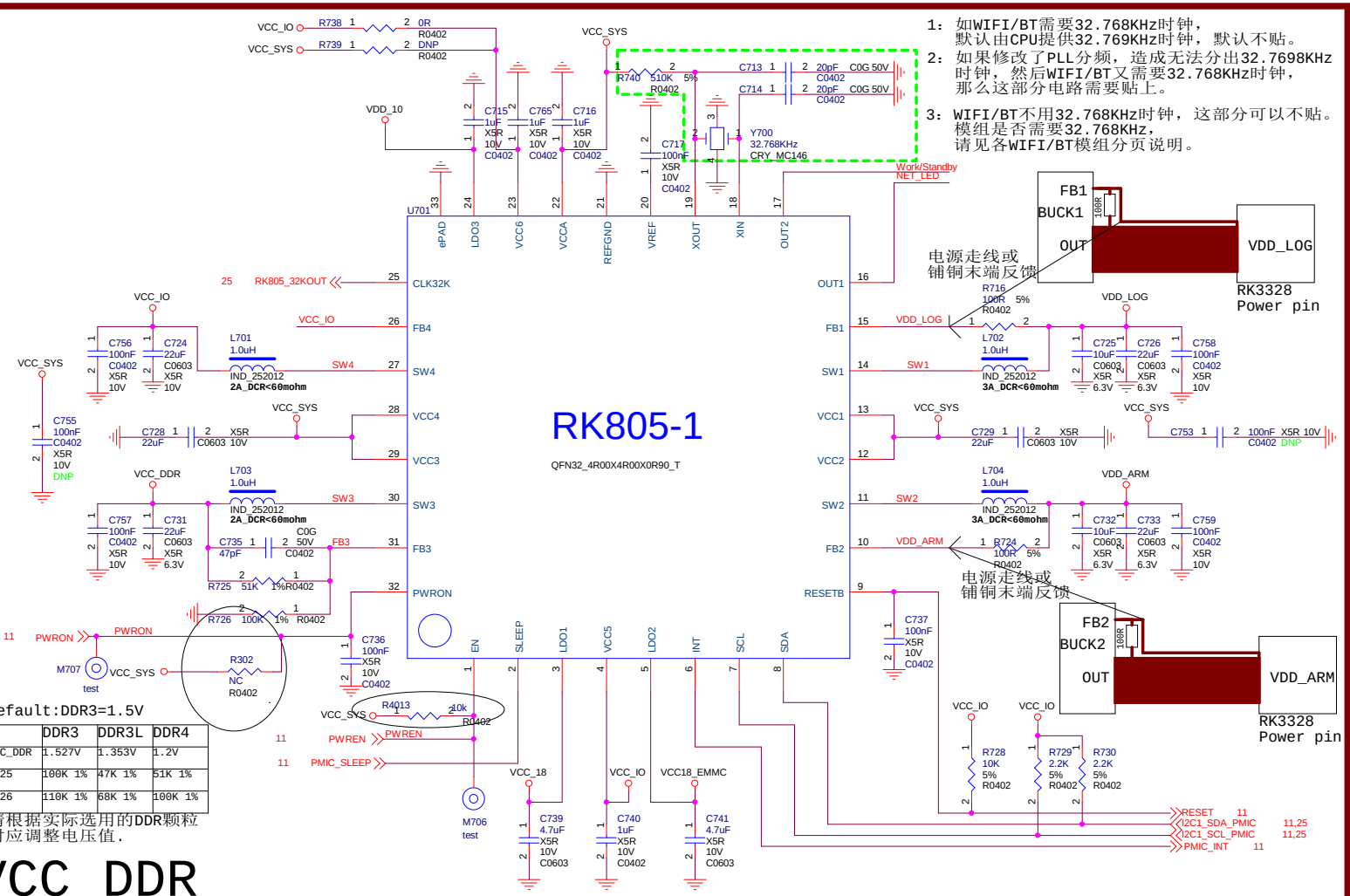


1: 如WIFI/BT需要32.768KHz时钟，
默认由CPU提供32.769KHz时钟，默认不贴。
2: 如果修改了PLL分频，造成无法分出32.7698KHz
时钟，然后WIFI/BT又需要32.768KHz时钟，
那么这部分电路需要贴上。
3: WIFI/BT不用32.768KHz时钟，这部分可以不贴。
模组是否需要32.768KHz，
请见各WIFI/BT模组分页说明。



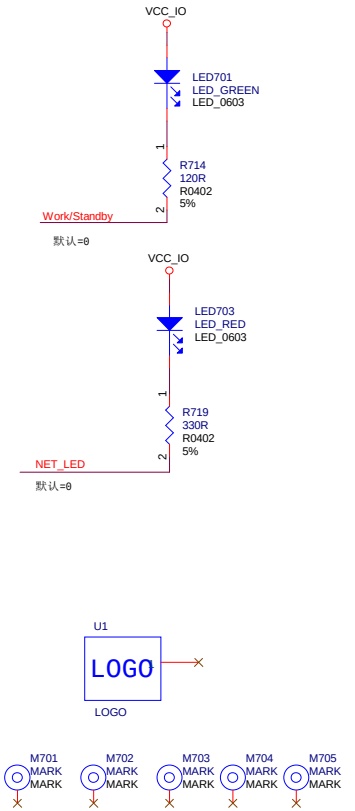
Default:DDR3=1.5V

	DDR3	DDR3L	DDR4
VCC_DDR	1.527V	1.353V	1.2V
R725	100K 1%	47K 1%	51K 1%
R726	110K 1%	68K 1%	100K 1%

请根据实际选用的DDR颗粒
对应调整电压值.

VCC_DDR

LED DISPLAY



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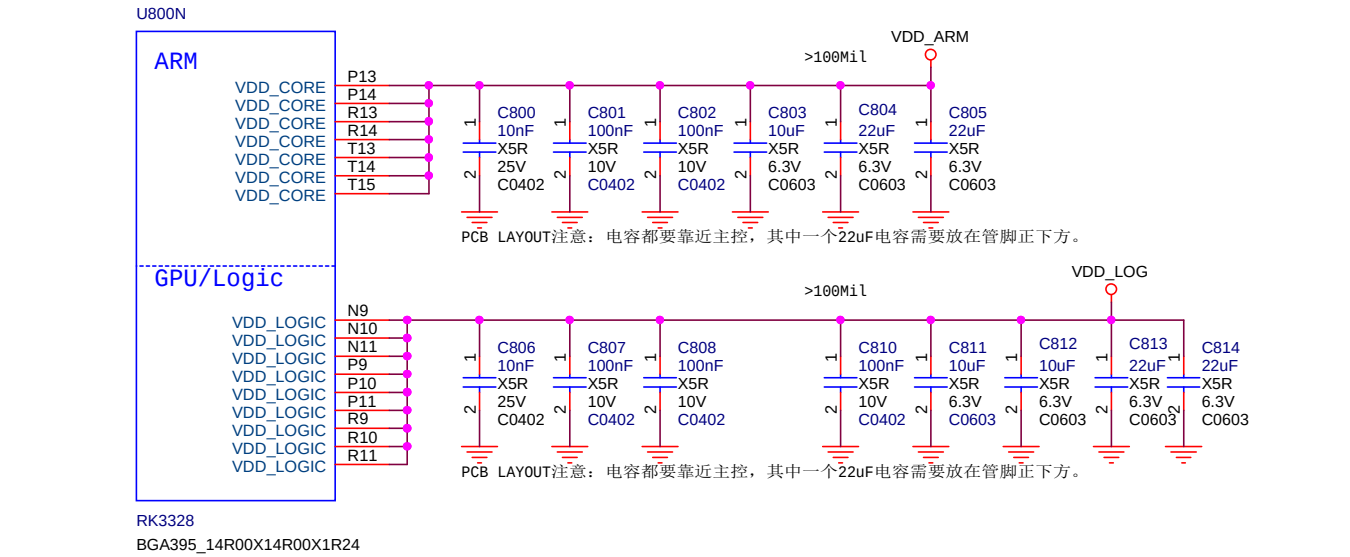

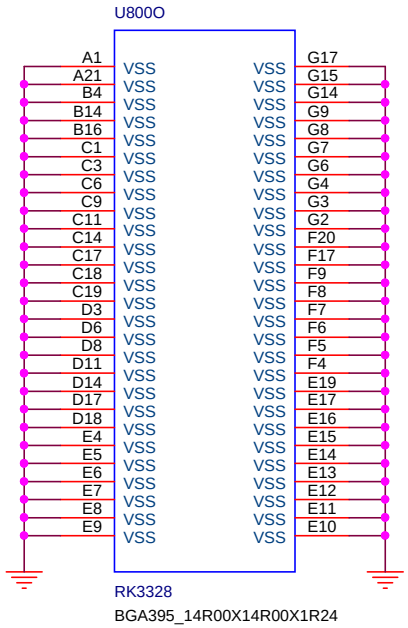

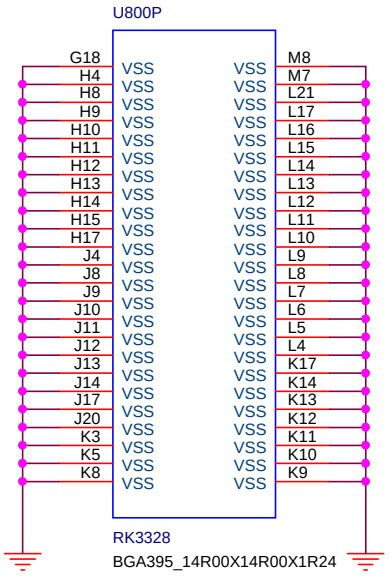

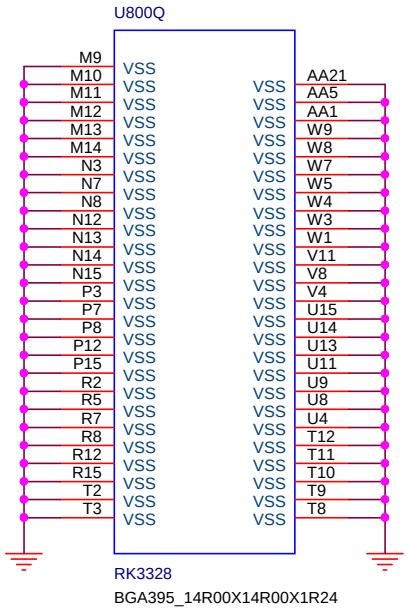

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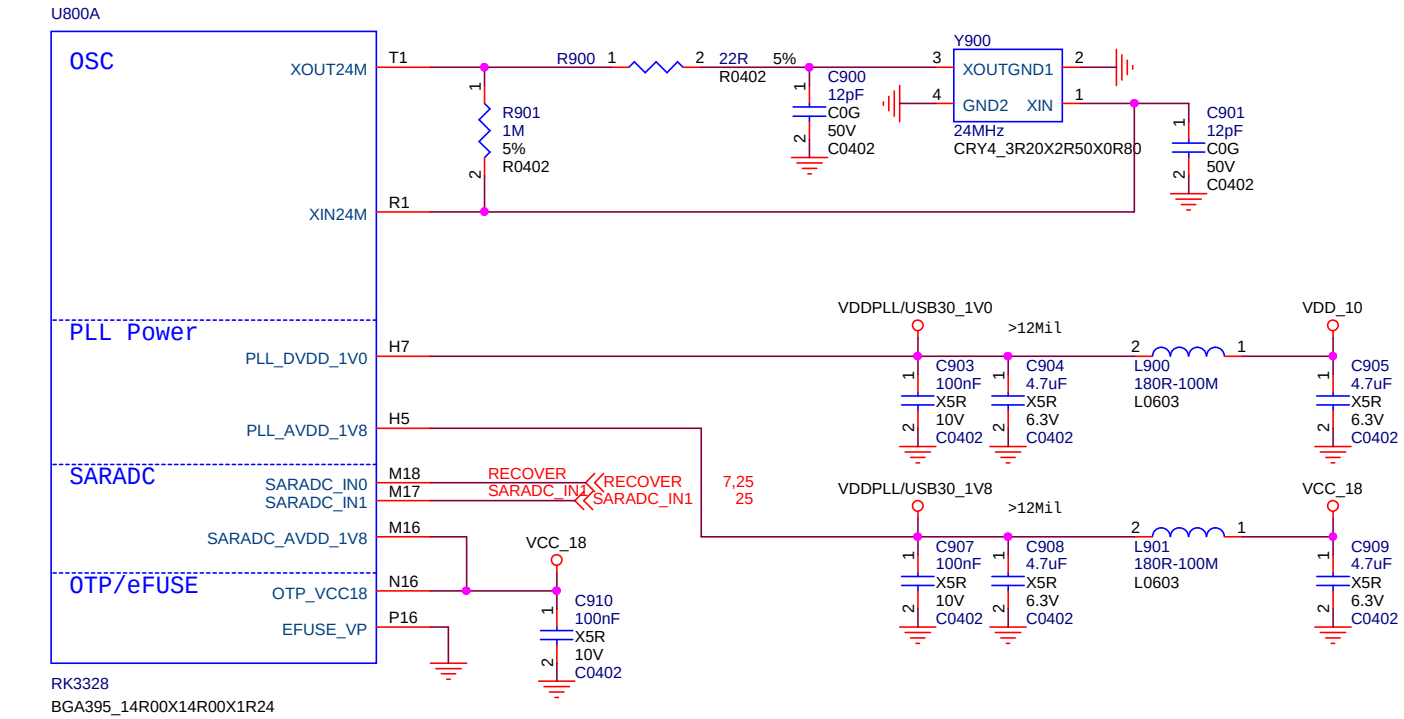

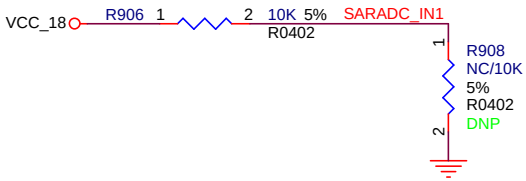

SARADC_IN0 BOM版本	SARADC_IN1 PCB版本	Up阻值	Down阻值	
Recover		DNP	10K	
BOM1		110K	10K	
BOM2		100K	20K	
BOM3		100K	33K	
BOM4		36K	18K	
BOM5		51K	36K	
BOM6		51K	51K	
BOM7		36K	51K	
BOM8		18K	36K	
BOM9		33K	100K	
BOM10		20K	100K	
BOM11		10K	110K	
BOM12		10K	DNP	

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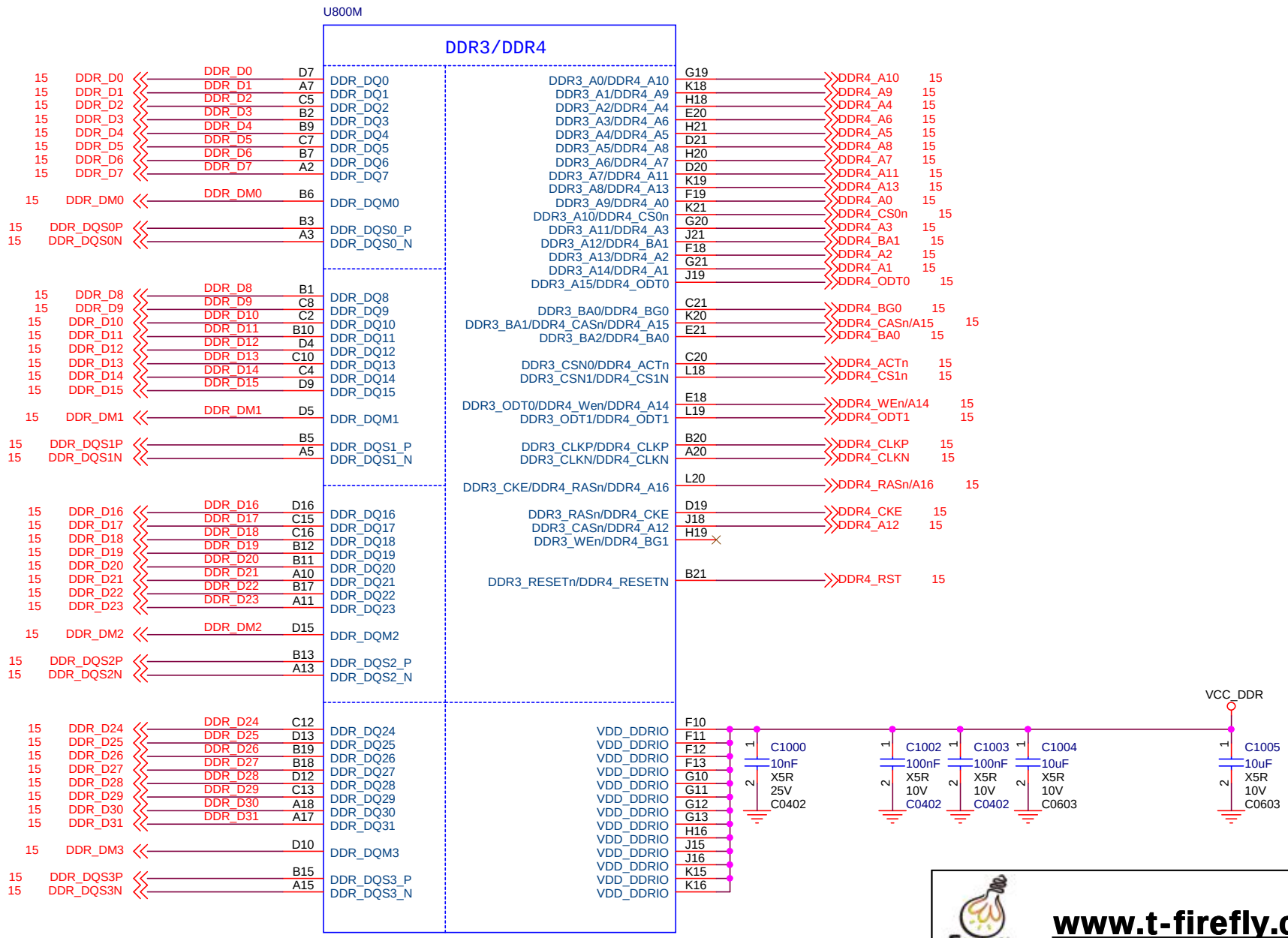

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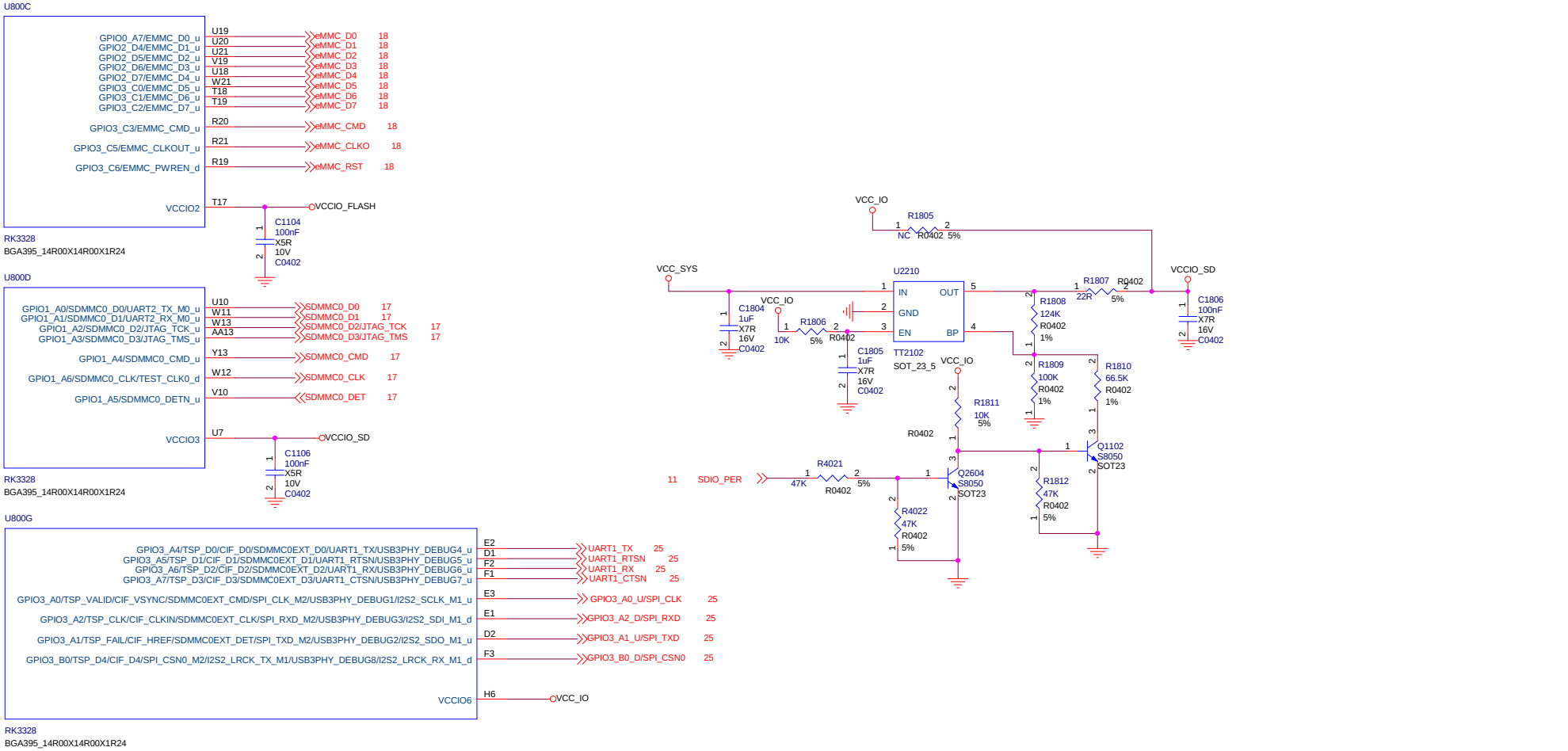

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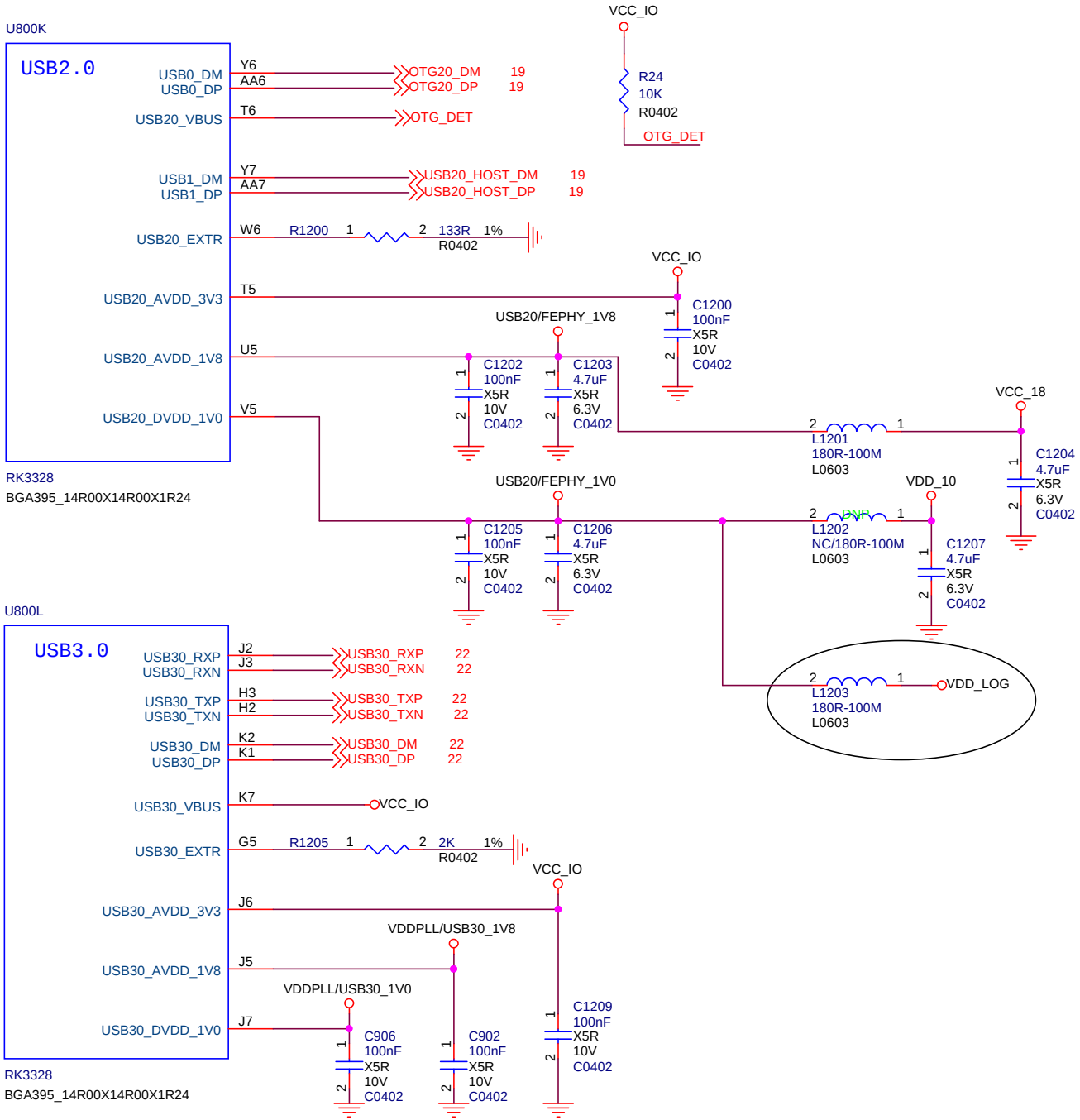

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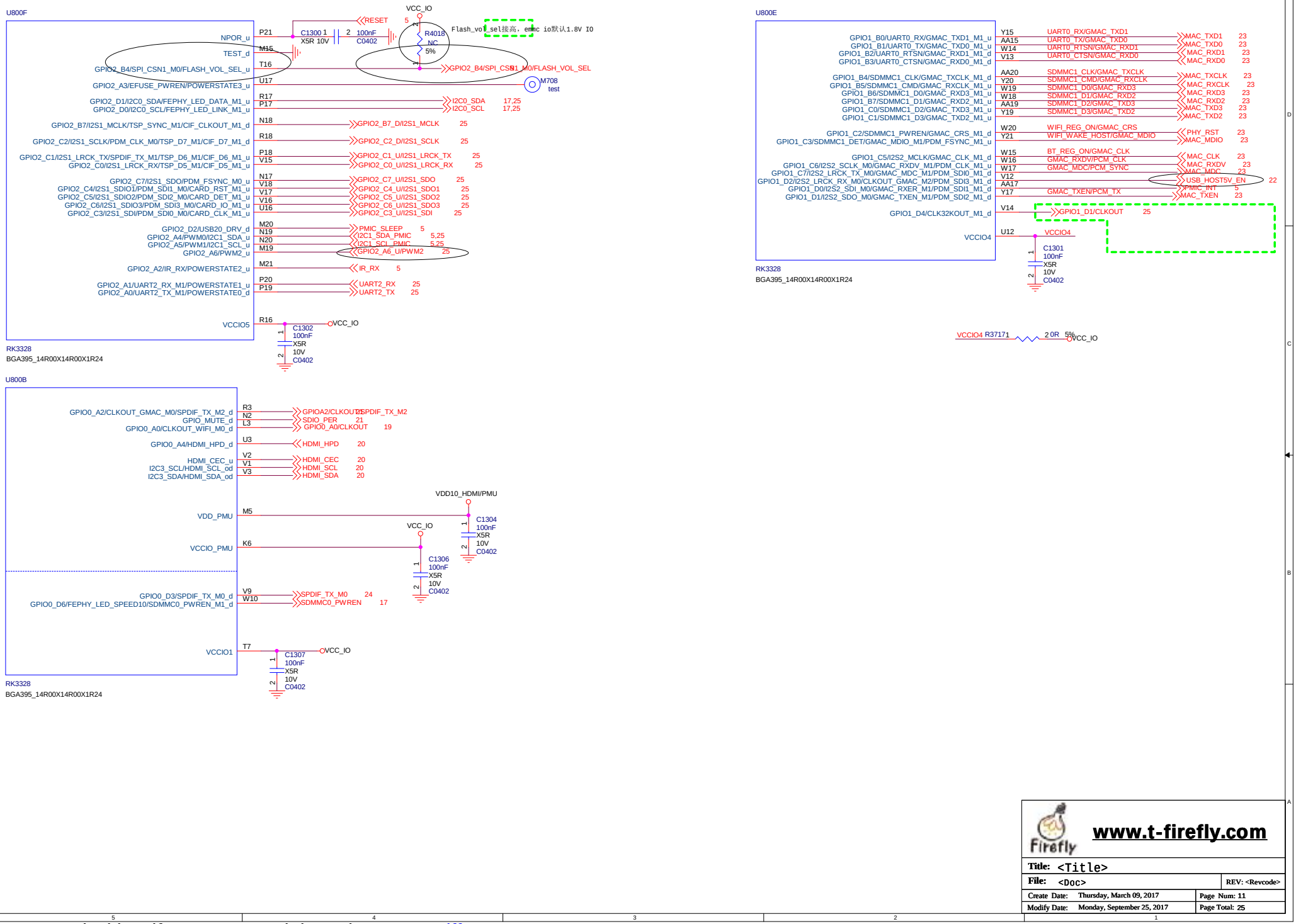

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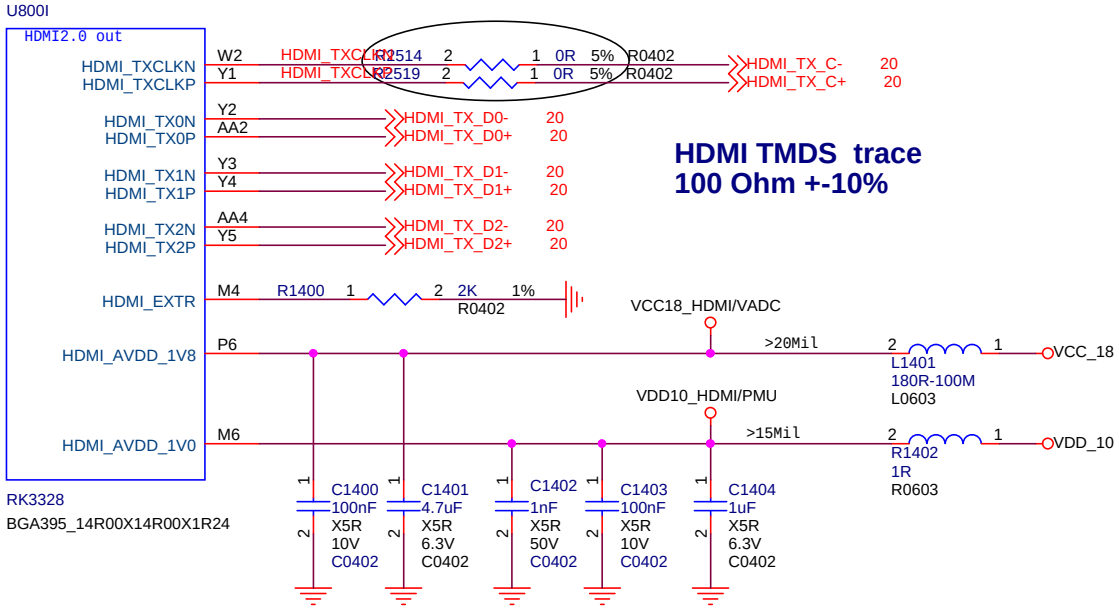

HDMI TMDS trace
100 Ohm +-10%

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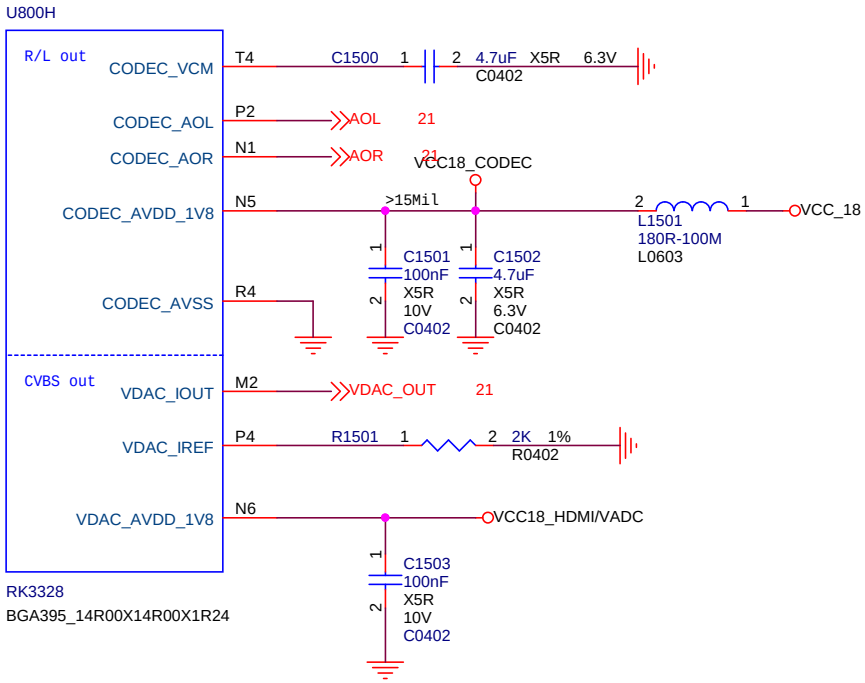

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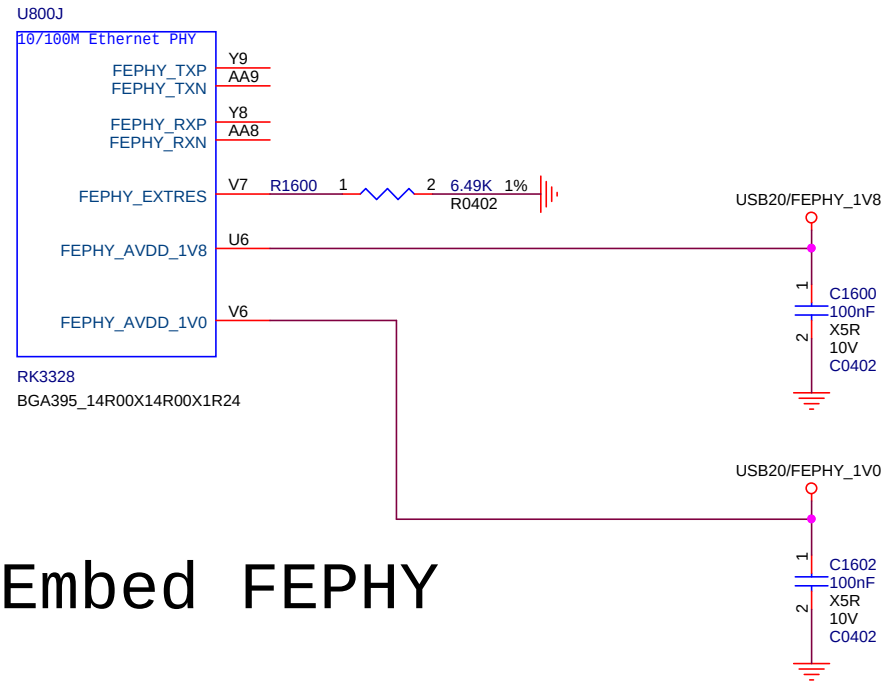

Embed FEPHY

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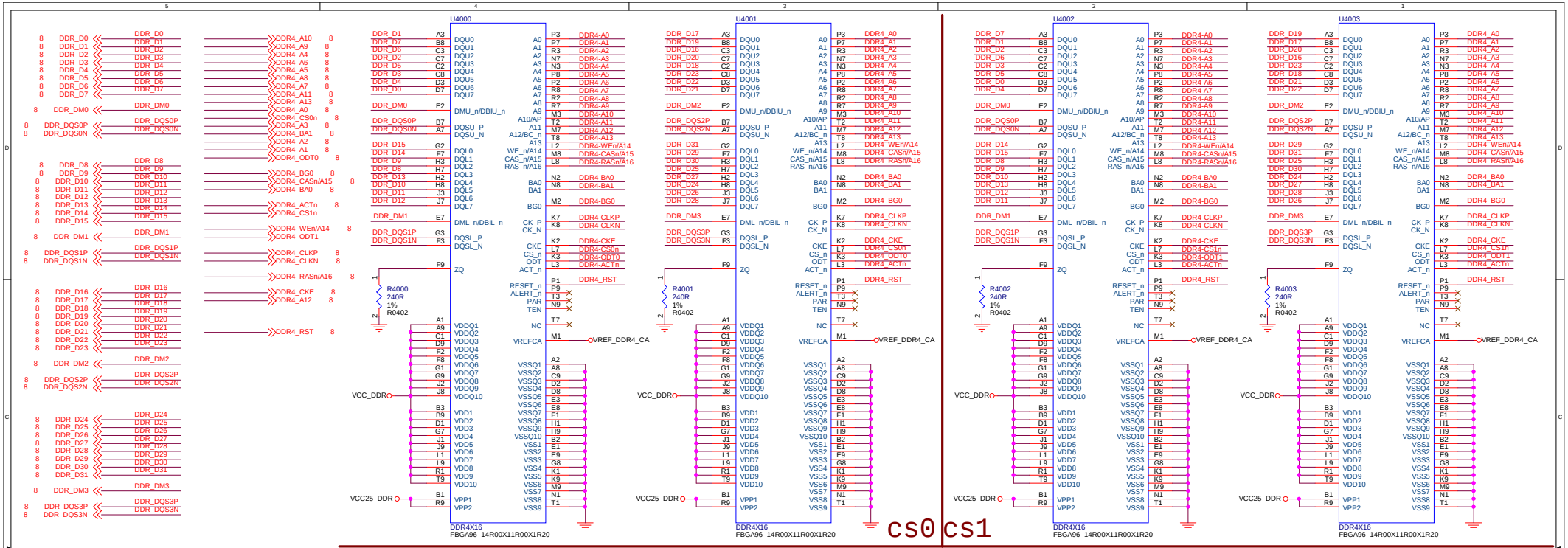
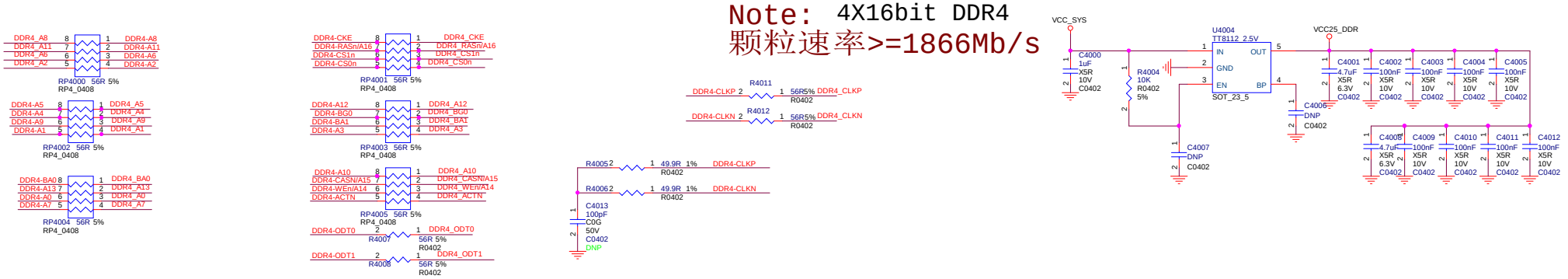
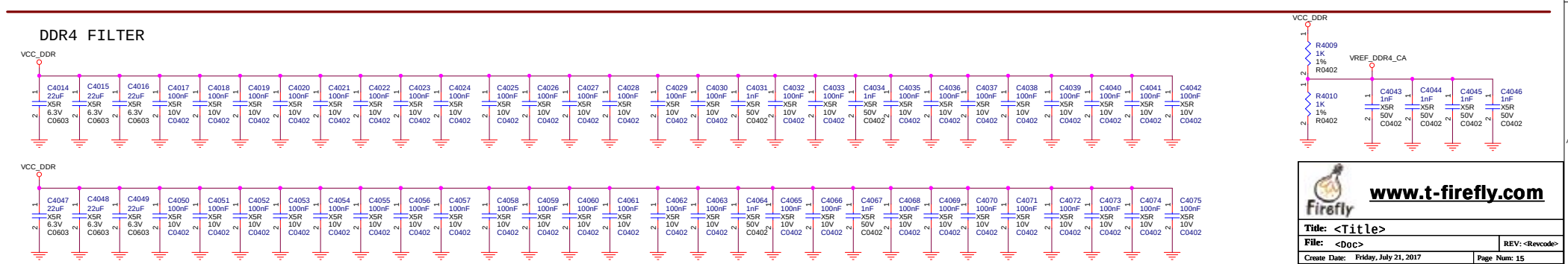


Note: 4X16bit DDR4
颗粒速率>=1866Mb/s





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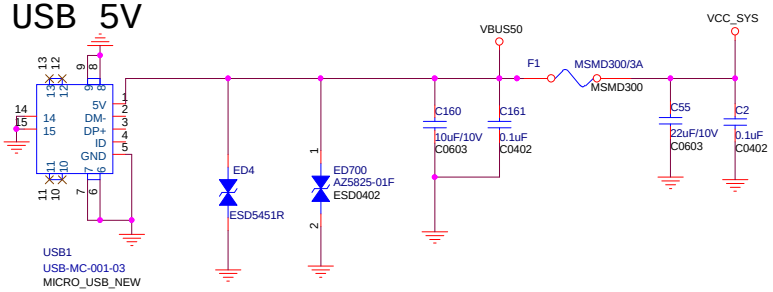
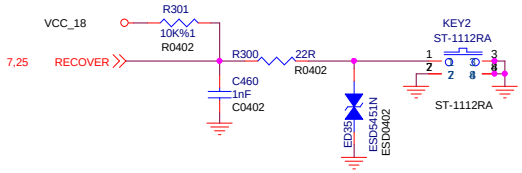
USB 5V





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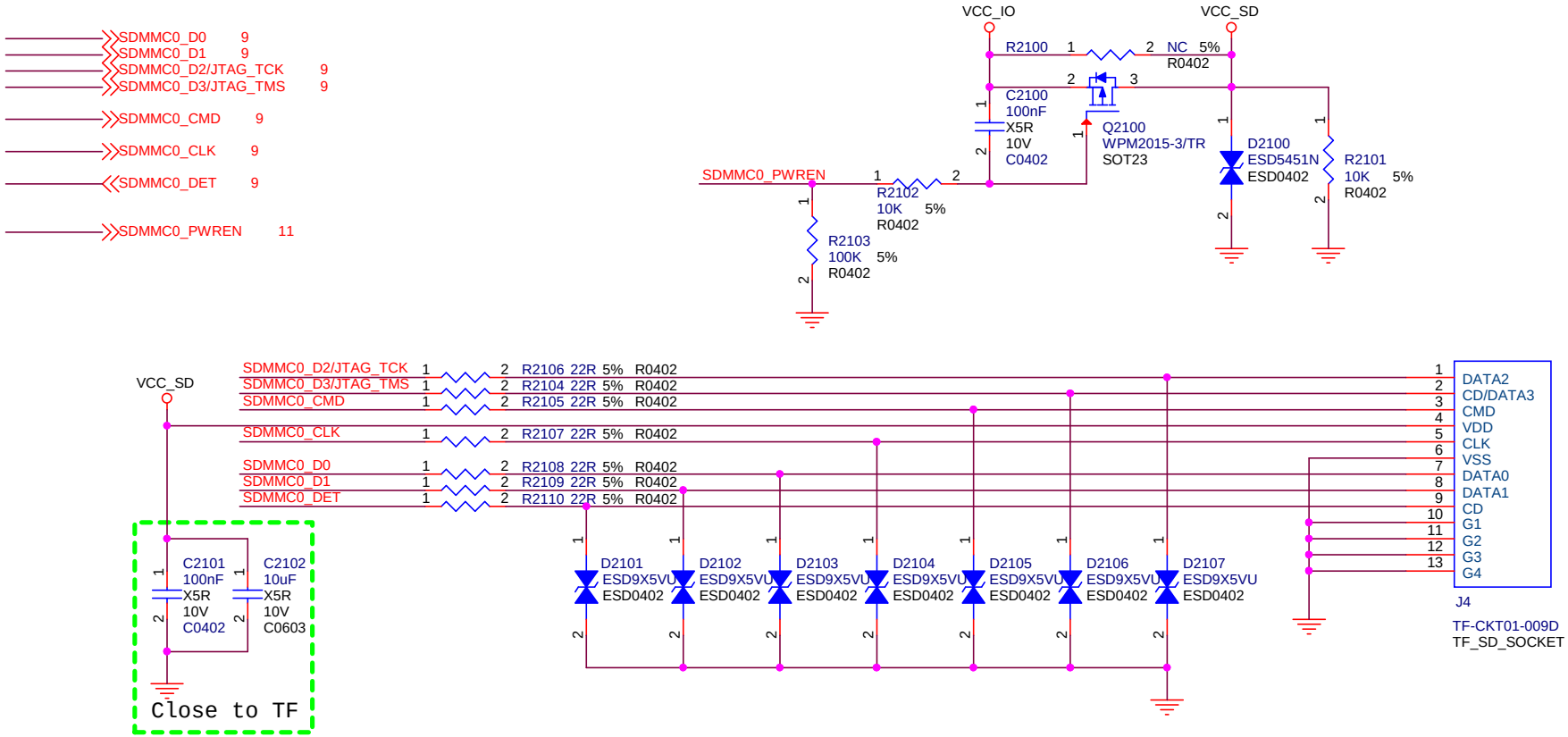

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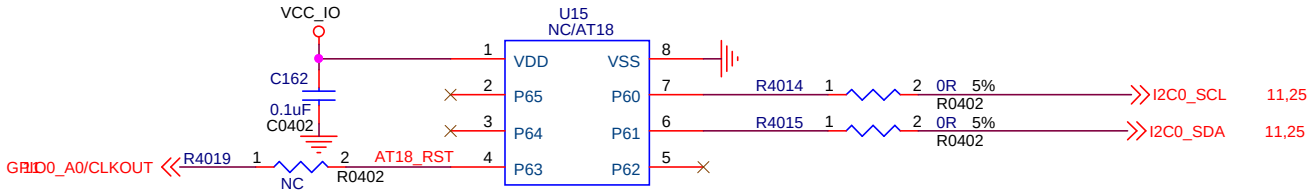

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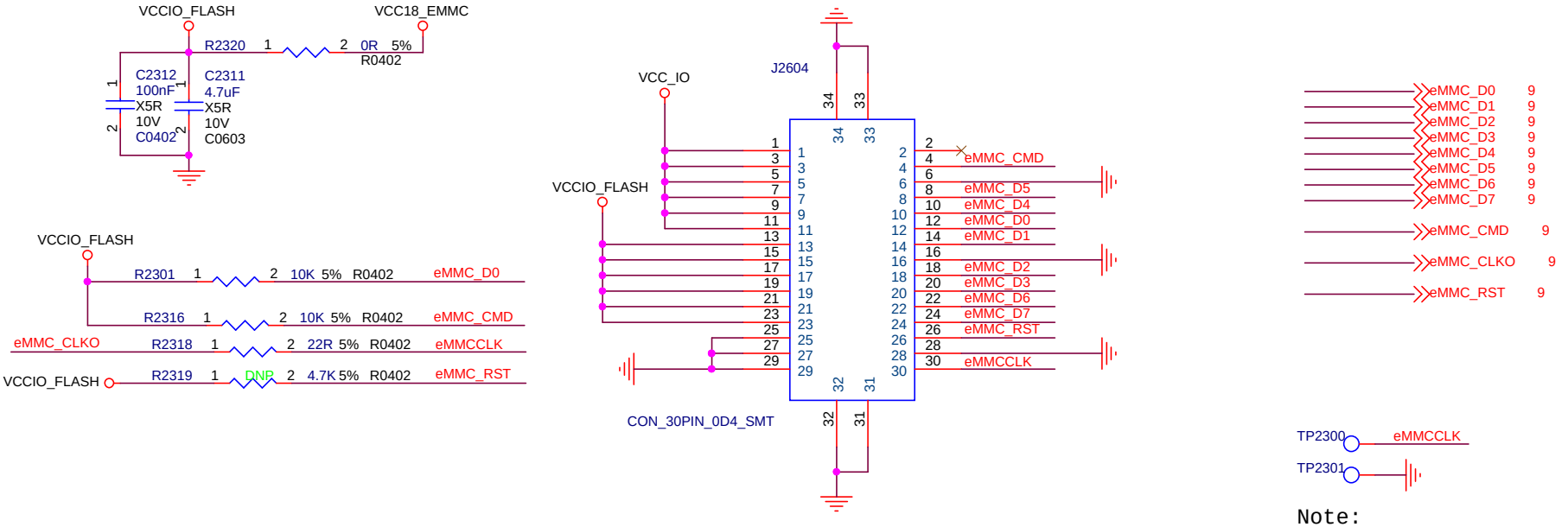

Note:
eMMC Update.

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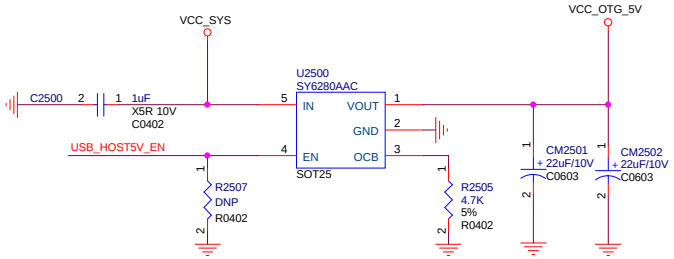

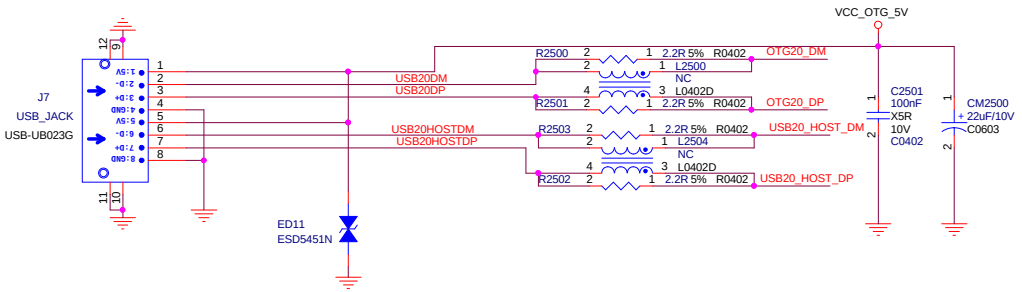

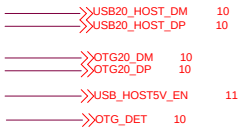

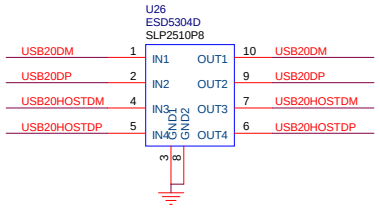

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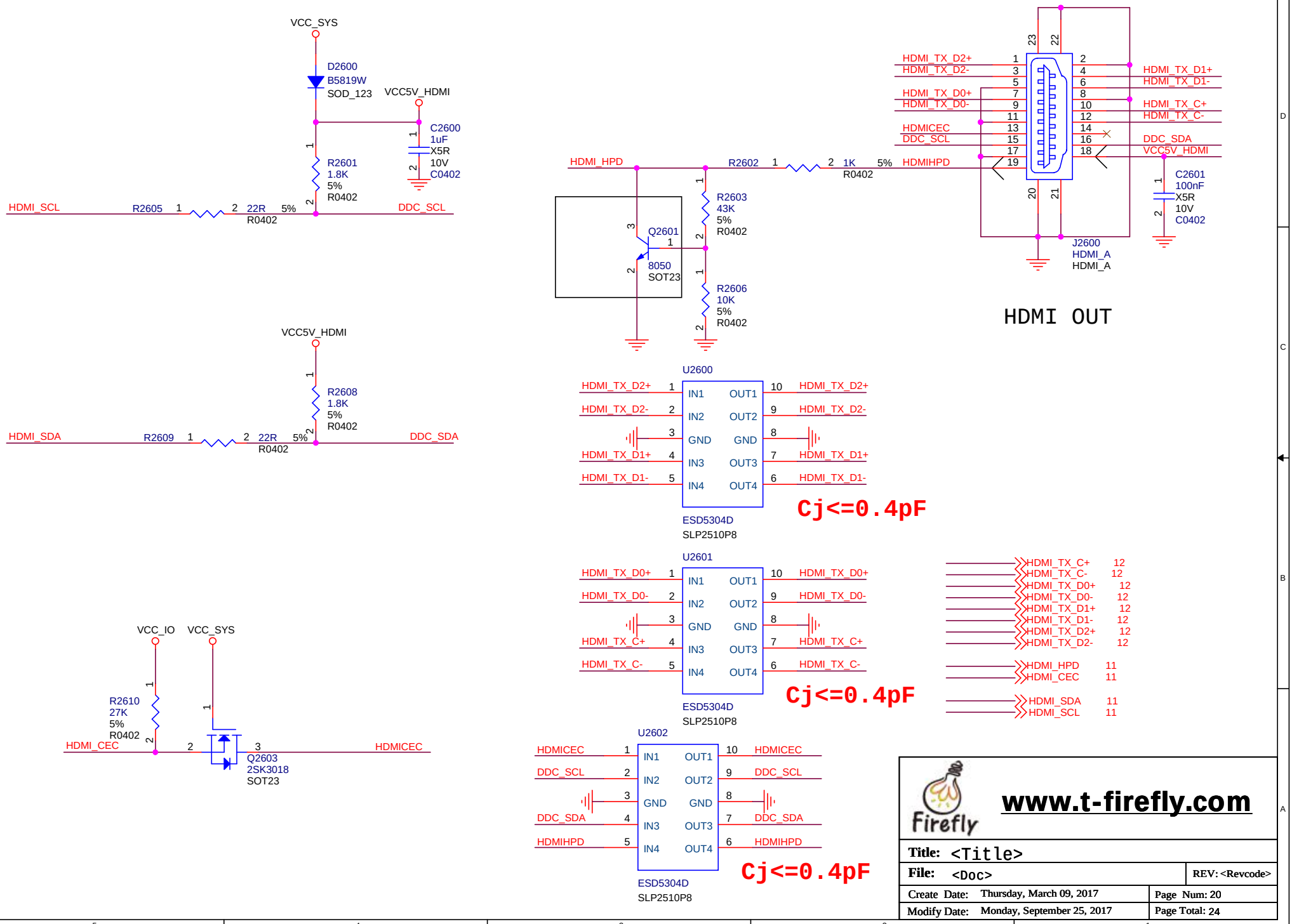

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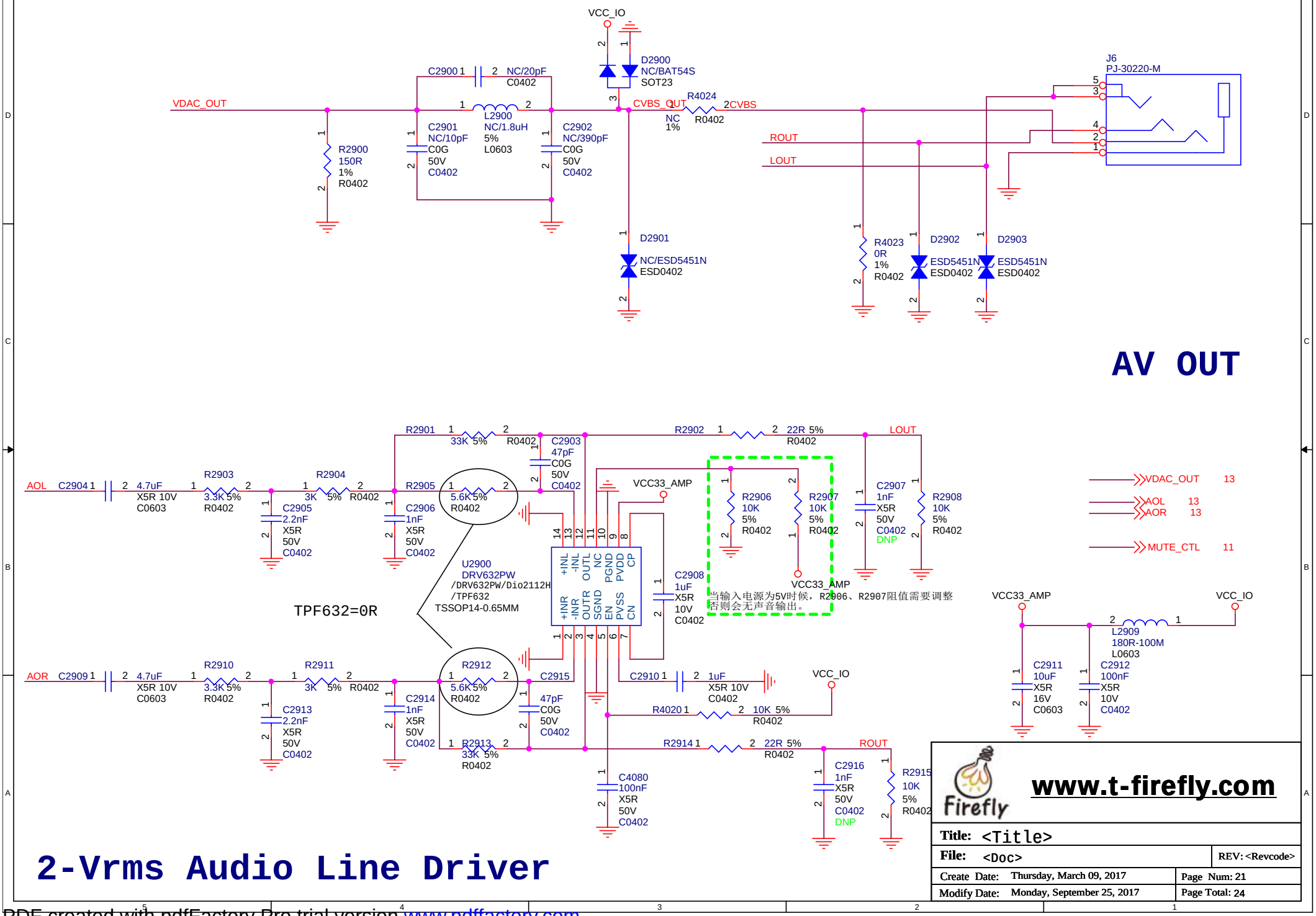

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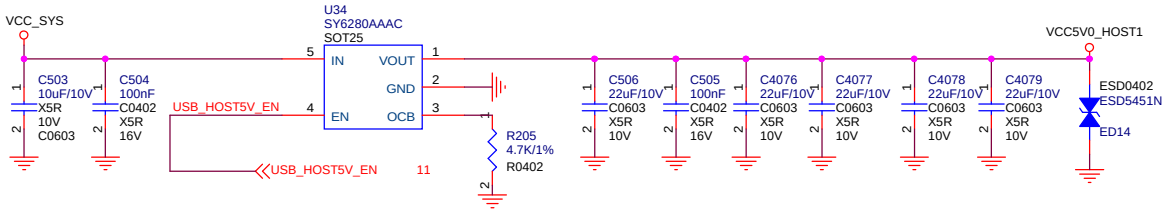

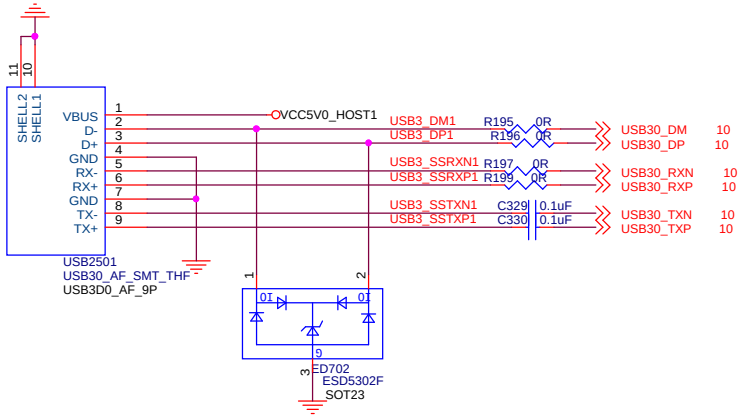

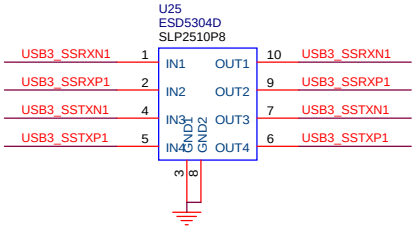

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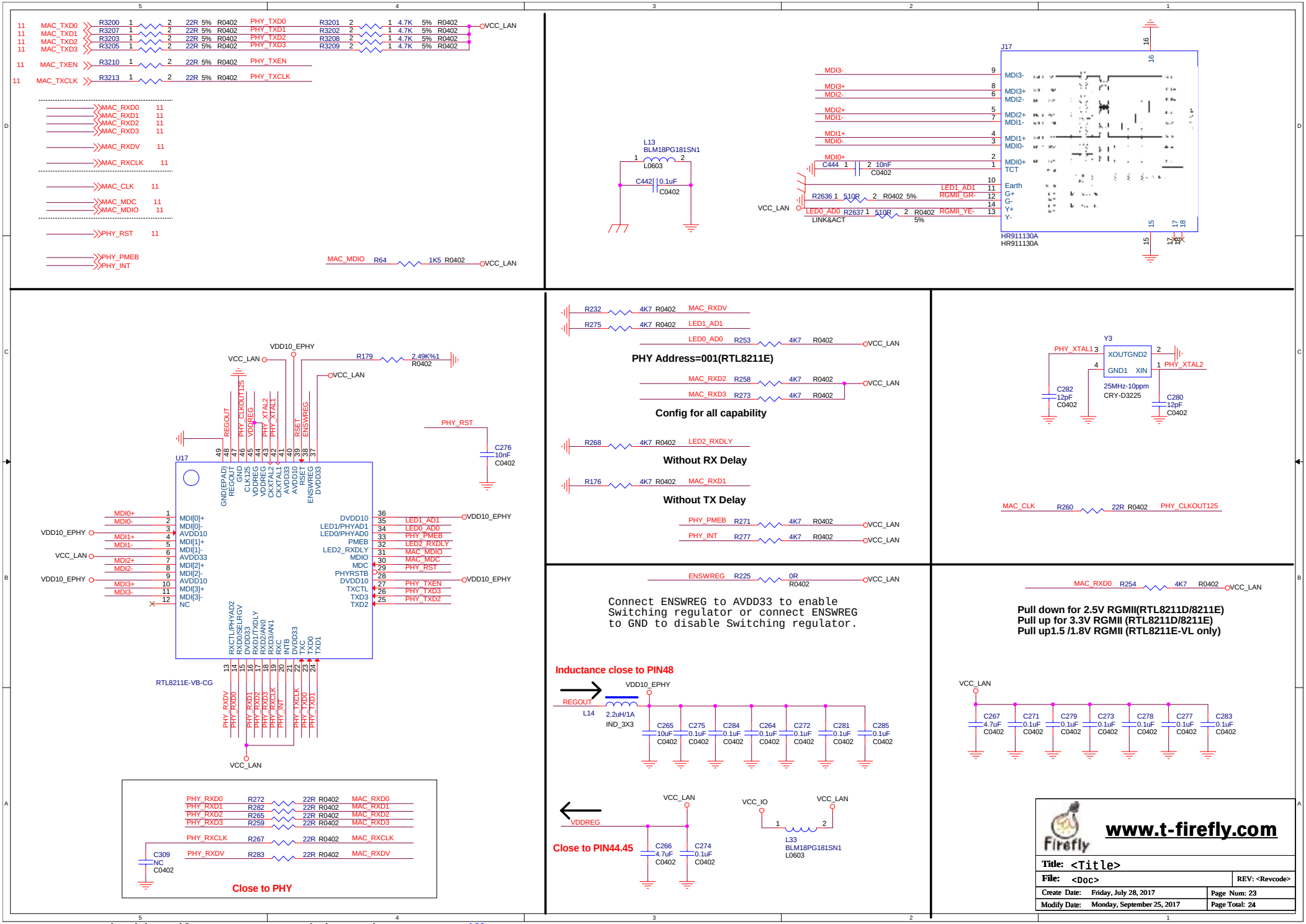

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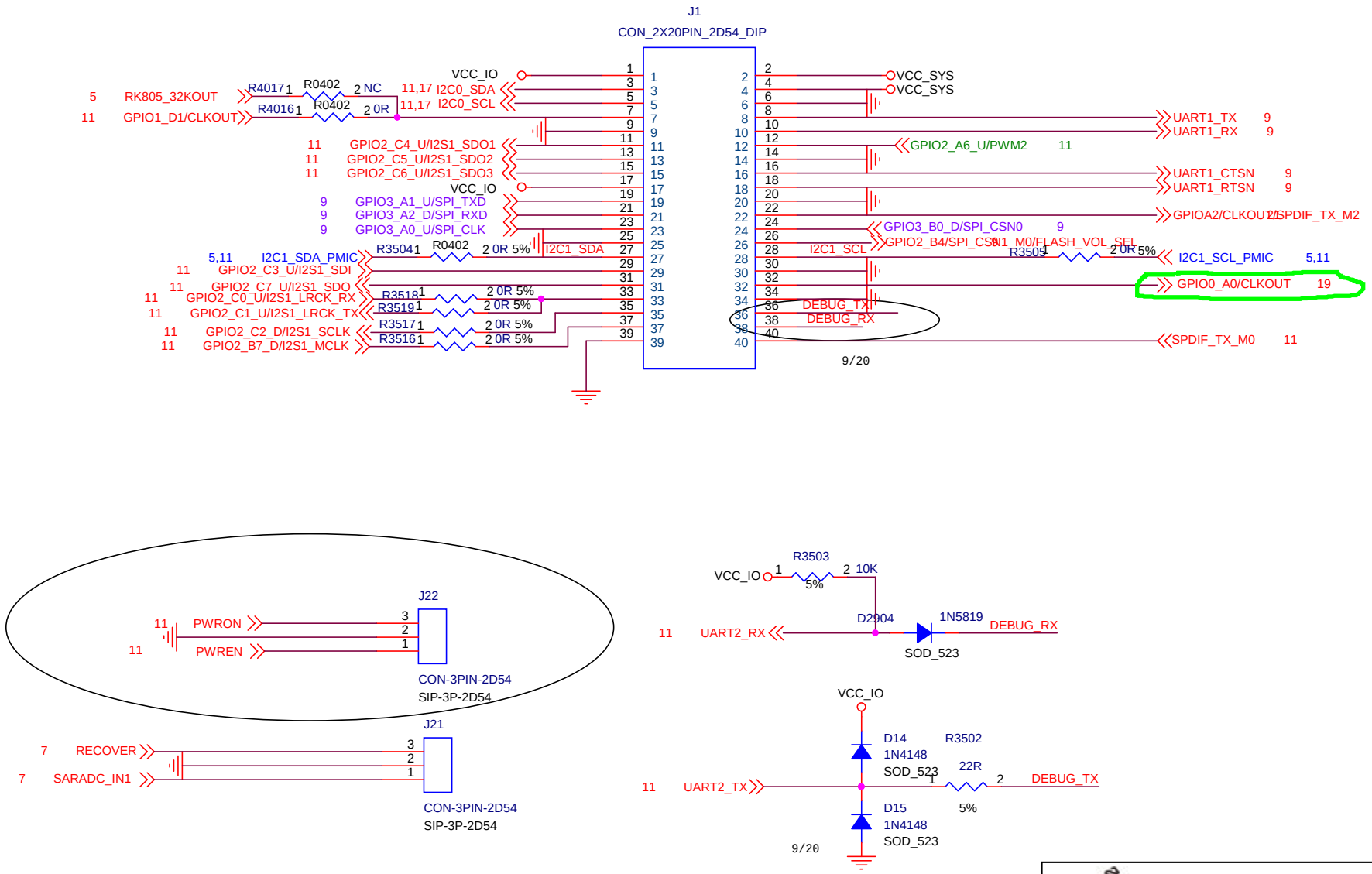

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