實用數位系統設計

HW3 Traffic Light

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一、 設計原理 ：

我想要設計一個十字路口的紅綠燈，此紅綠燈有左轉燈，次要道路上要有車才會轉綠燈(控制訊號為 sel)，否則主要道路持續綠燈。

State0： 主要道路綠燈(次要道路紅燈)

State1： 主要道路左轉燈亮(主要道路直行為紅燈，次要道路紅燈)

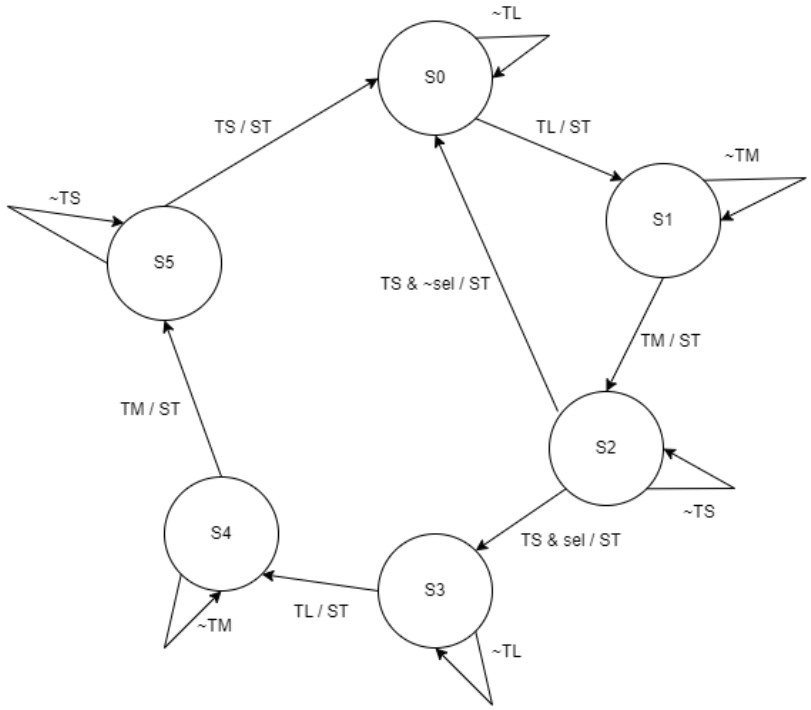
State2： 主要道路黃燈(次要道路紅燈)

State3： 次要道路綠燈(主要道路紅燈)

State4： 次要道路左轉燈亮(主要道路紅燈，次要道路直行紅燈)

State5： 次要道路黃燈(主要道路紅燈)

利用以上邏輯繪製出下圖



- 訊號解釋 ：

(1) TL： 代表綠燈時間(不管是次要或主要道路)，此時間我設定成 10 個正緣的時間，如果綠燈的時間到，TL 為 1，則為 0。

(2) TM： 代表左轉燈時間(不管是次要或主要道路)，此時間我設定成 5 個正緣的時間，如果左轉燈的時間到，TM 為 1，則為 0。

(3) TS： 代表黃燈時間(不管是次要或主要道路)，此時間我設定成 2 個正緣的時間，如果黃燈的時間到，TS 為 1，則為 0。

(4) ST： 代表控制 counter 的訊號，狀態轉換期間會送出 ST = 1 給 counter 告訴它要歸零並重新開始計數，否則會送出 ST = 0 告訴它繼續計數就好。

(5) sel： 代表次要道路上有車的訊號，如過在主要道路轉紅燈時 sel = 1，

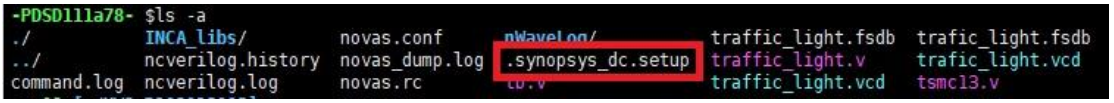
那接下來次要道路會為綠燈，而主要道路為紅燈，否則主要道路持續綠燈。

- 此電路有 9 個輸出訊號，和三個輸入訊號。

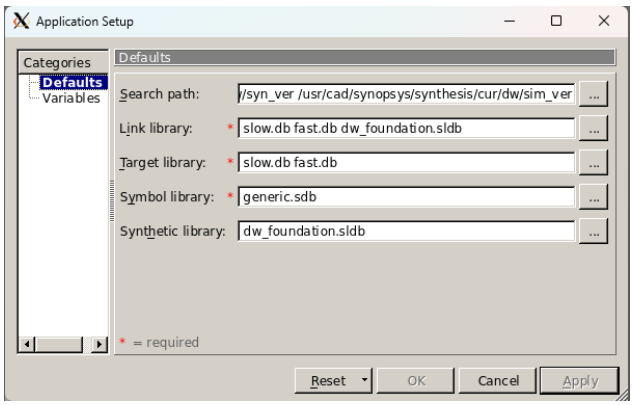
1. 輸出訊號 ：
   (1) HG： 代表主要道路綠燈。
   (2) HY： 代表主要道路黃燈。
   (3) HR： 代表主要道路紅燈。
   (4) HL： 代表主要道路左轉。
   (5) FG： 代表次要道路綠燈。
   (6) FY： 代表次要道路黃燈。
   (7) FR： 代表次要道路紅燈。
   (8) FL： 代表次要道路左轉。
   (9) _ST： 為了方便分析才顯示出來，代表狀態切換時，也代表 counter 歸零重新開始計數。
2. 輸入訊號 ：
   (1) clk : clock。
   (2) reset： 初始化狀態(state 變成 S0，counter 歸零重新開始計數)。
   (3) sel： 代表次要道路上有車的訊號，如過在主要道路轉紅燈時 sel = 1，那接下來次要道路會為綠燈，而主要道路為紅燈，否則主要道路持續綠燈。

二、 邏輯合成步驟 ：

1. 基礎步驟 ：
   (1) 在 Xshell 中輸入指令 ls -a 確認資料夾中是否有隱藏檔。



   (2) 輸入指令 dv 開啟邏輯合成軟體，並確認檔案是否正確被載入。



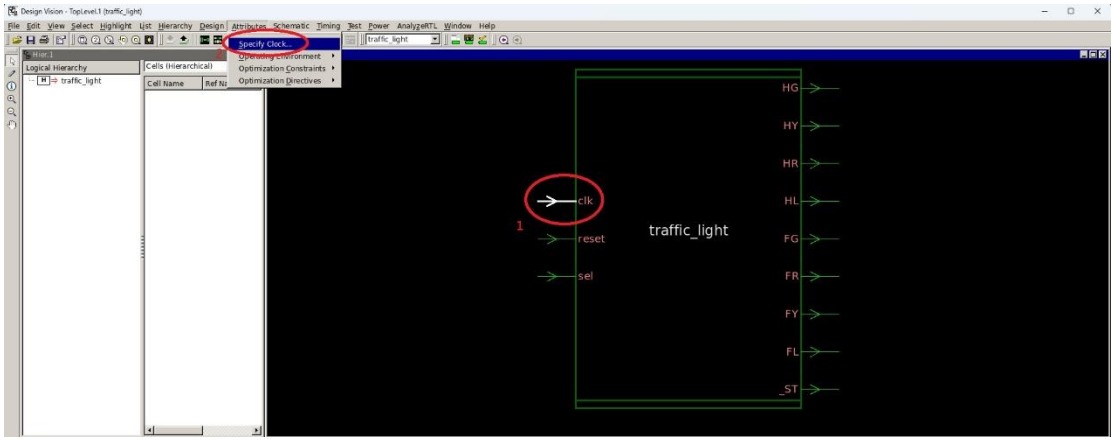
   (3) 透過左上快捷鍵開啟檔案，並確認是否有錯誤或警告。

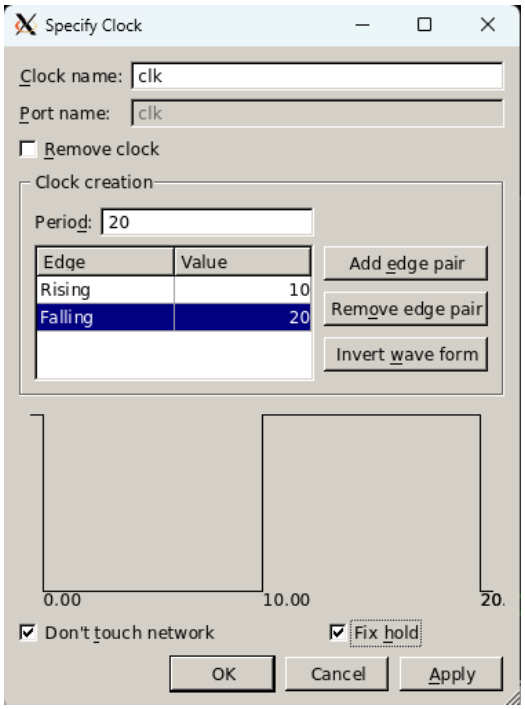
```
Presto compilation completed successfully.
Current design is now '/home/PDSD111/PDSD111a78/HW3_B103012002/traffic_light.db:traffic_light'
Loaded 1 design.
Current design is 'traffic_light'.
```

(4) 輸入指令 set_fix_multiple_port_nets -all -buffer_constants 來預防 assign 錯誤

```
design_vision> set_fix_multiple_port_nets -all -buffer_constant
```

(5) Specify clock





(6) Compile design，並確認是否有錯誤或警告

```
  Optimization Complete
  ---------------------
1
design_vision>
```

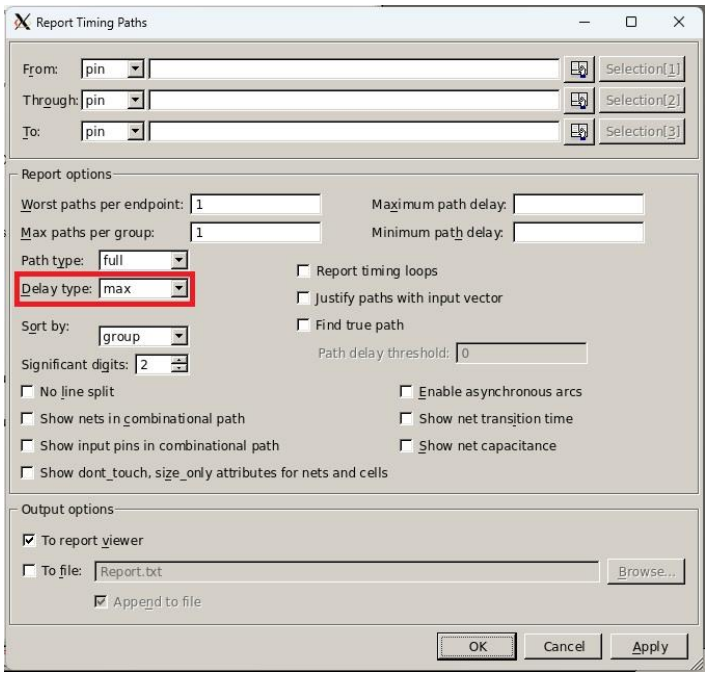
(7) Area report

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Tue May  9 00:51:31 2023
****************************************

Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          12
Number of nets:                           54
Number of cells:                          46
Number of combinational cells:            38
Number of sequential cells:                8
Number of macros/black boxes:              0
Number of buf/inv:                         9
Number of references:                     17

Combinational area:               259.702197
Buf/Inv area:                      30.553200
Noncombinational area:            258.004791
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  517.706988
Total area:                 undefined

***** End Of Report *****
```

Gate count = 517.706 / 5 = 104

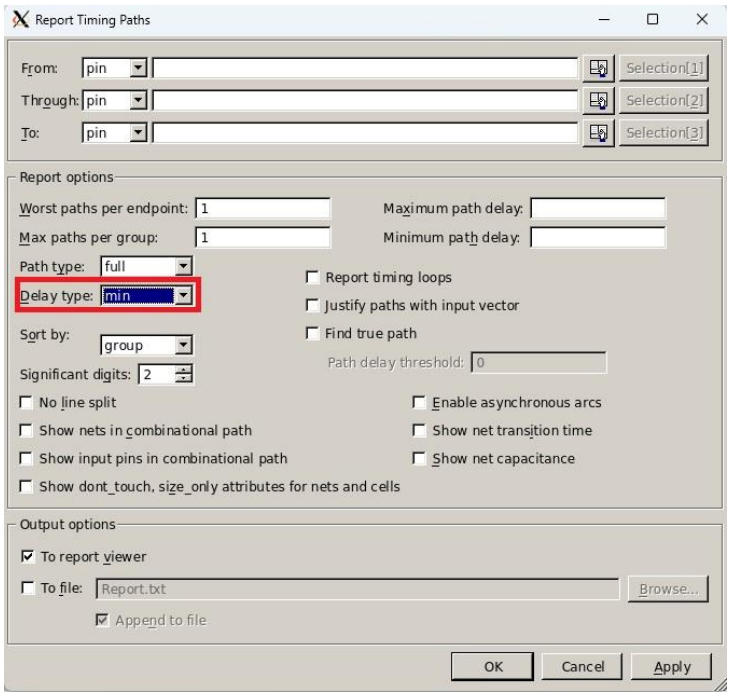
(8) Timing report

- 檢查 setup-time



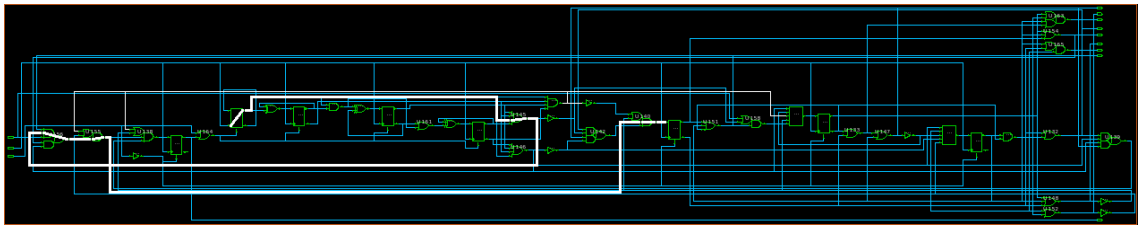
```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 12:34:15 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[3]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/Q (DFFRX1)                  0.56      10.56 f
  U74/Y (NAND2X1)                          0.13      10.69 r
  U76/Y (NOR2BX1)                          0.07      10.76 f
  U75/Y (XOR2X1)                           0.13      10.89 r
  count_reg[3]/D (DFFRX1)                  0.00      10.89 r
  data arrival time                                  10.89

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  count_reg[3]/CK (DFFRX1)                 0.00      30.00 r
  library setup time                      -0.24      29.76
  data required time                                 29.76
  -----------------------------------------------------------
  data required time                                 29.76
  data arrival time                                 -10.89
  -----------------------------------------------------------
  slack (MET)                                        18.87
```

- 檢查 hold-time



```
****************************************
Report : timing
         -path full
         -delay min
         -max_paths 1
         -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 12:37:54 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/QN (DFFRX1)                 0.25      10.25 f
  count_reg[0]/D (DFFRX1)                  0.00      10.25 f
  data arrival time                                  10.25

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  library hold time                       -0.03       9.97
  data required time                                  9.97
  -----------------------------------------------------------
  data required time                                  9.97
  data arrival time                                 -10.25
  -----------------------------------------------------------
  slack (MET)                                         0.27


***** End Of Report *****
```

(9) Critical path



(10) Power report

```
****************************************
Report : power
       -analysis_effort low
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 12:50:54 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.3694 uW   (93%)
  Net Switching Power  = 756.1635 nW    (7%)
                         ---------
Total Dynamic Power    =  10.1256 uW  (100%)

Cell Leakage Power     = 474.4306 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register       8.8456e-03       3.7808e-04          2.3747e+05         9.4612e-03  (  89.26%)
sequential     7.1143e-05       4.9058e-06          7.2161e+04         1.4821e-04  (   1.40%)
combinational  4.5267e-04       3.7318e-04          1.6480e+05         9.9065e-04  (   9.35%)
--------------------------------------------------------------------------------------------------
Total          9.3694e-03 mW     7.5616e-04 mW     4.7443e+05 pW      1.0600e-02 mW

***** End Of Report *****
```

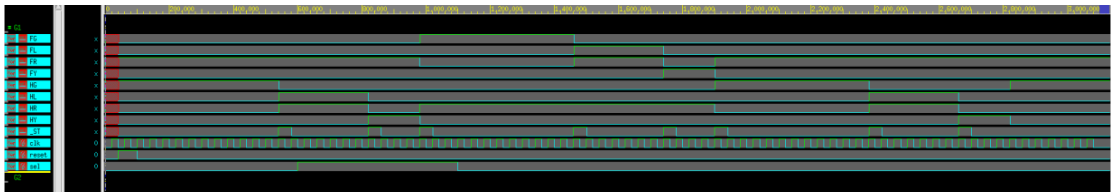
(11) 存檔

```
Information: Annotated 'cell' delays are assumed to include load delay(UID-282)
Information: Writing timing information to file '/home/PDSD111/PDSD111a78/HW3_B103012002/traffic_light.sdf(WT-3)
```

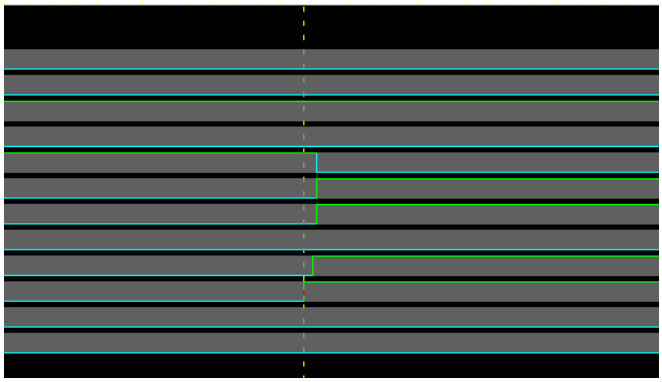
(12) 修改 testbench 並進行模擬

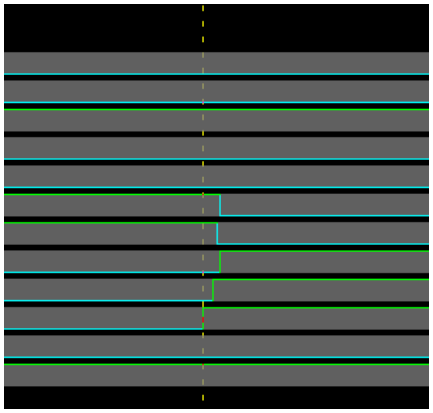
```
Reading SDF file from location "traffic_light.sdf"
Writing compiled SDF file to "traffic_light.sdf.X".
Annotating SDF timing data:
        Compiled SDF file:     traffic_light.sdf.X
        Log file:
        Backannotation scope:  tb.t0
        Configuration file:
        MTM control:
        Scale factors:
        Scale type:
Annotation completed successfully...
```

(13) 波形模擬



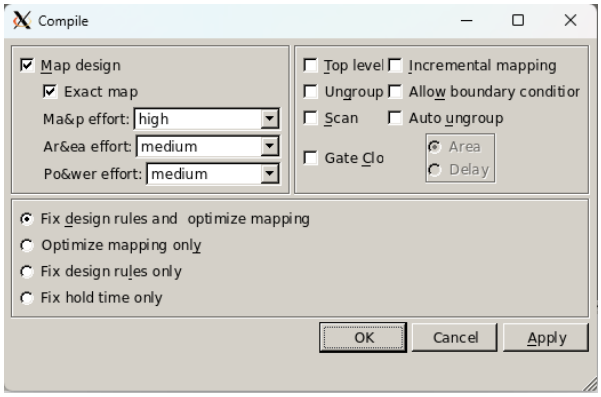
將波形某部分放大後，可以觀察到延遲的影響，如下面兩張圖





2. 進階步驟 ：

(1) 將 map effort 調整至 high



- Timing report :

  修改 map effort 前，Setup time 為 29.79 ns，Hold time 為 9.79 ns ；修改 map effort 後，setup time 為 29.78 ns，hold time 為 9.96 ns，如下面兩張圖所示。比較後發現 setup time 減少一點點，hold time 增加一點點。

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 19:11:16 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[2]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[3]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[2]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[2]/Q (DFFRX1)                  0.56      10.56 f
  U122/Y (NAND2X1)                         0.11      10.67 r
  U121/Y (XOR2X1)                          0.14      10.81 f
  count_reg[3]/D (DFFRX1)                  0.00      10.81 f
  data arrival time                                  10.81

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  count_reg[3]/CK (DFFRX1)                 0.00      30.00 r
  library setup time                      -0.22      29.78
  data required time                                 29.78
  -----------------------------------------------------------
  data required time                                 29.78
  data arrival time                                 -10.81
  -----------------------------------------------------------
  slack (MET)                                        18.98
```

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 19:15:02 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/QN (DFFRX1)                 0.30      10.30 f
  count_reg[0]/D (DFFRX1)                  0.00      10.30 f
  data arrival time                                  10.30

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  library hold time                       -0.04       9.96
  data required time                                  9.96
  -----------------------------------------------------------
  data required time                                  9.96
  data arrival time                                 -10.30
  -----------------------------------------------------------
  slack (MET)                                         0.33


***** End Of Report *****
```

- Area report :

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Tue May  9 00:53:16 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           12
Number of nets:                            53
Number of cells:                           46
Number of combinational cells:             38
Number of sequential cells:                 8
Number of macros/black boxes:               0
Number of buf/inv:                          8
Number of references:                      17

Combinational area:               256.307396
Buf/Inv area:                      27.158400
Noncombinational area:            258.004791
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  514.312187
Total area:                 undefined

***** End Of Report *****
```

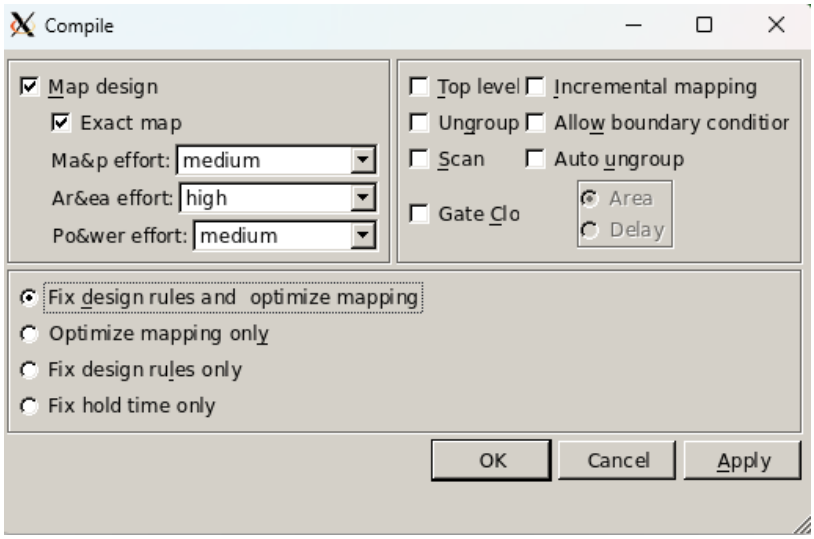
修改 map effort 前，total cell area 為 517.706 um × um
修改 map effort 後，total cell area 為 514.312187 um × um，比修改前小一點。

- Power report :

```
****************************************
Report : power
        -analysis_effort low
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 19:12:05 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.3223 uW   (92%)
  Net Switching Power  = 761.3987 nW    (8%)
                         ---------
Total Dynamic Power    =  10.0837 uW  (100%)

Cell Leakage Power     = 468.8183 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register       8.8411e-03       3.8027e-04        2.3747e+05        9.4588e-03  (  89.64%)
sequential     7.0952e-05       4.8928e-06        7.2161e+04        1.4801e-04  (   1.40%)
combinational  4.1034e-04       3.7623e-04        1.5919e+05        9.4576e-04  (   8.96%)
--------------------------------------------------------------------------------------------------
Total          9.3223e-03 mW     7.6140e-04 mW     4.6882e+05 pW     1.0553e-02 mW

***** End Of Report *****
```

修改 map effort 前，Total dynamic power = 10.1256 uW，Cell leakage power = 242.4306 nW；修改 map effort 後，total dynamic power = 10.0827 uW，cell leakage power = 468.8183 nW。比較後發現 total dynamic power 減少一點，cell leakage power 增加一點。

(2) 將 area effort 調整至 high



- Timing report :

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 19:33:12 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[3]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/Q (DFFRX1)                  0.56      10.56 f
  U74/Y (NAND2X1)                          0.13      10.69 r
  U76/Y (NOR2BX1)                          0.07      10.76 f
  U75/Y (XOR2X1)                           0.13      10.89 r
  count_reg[3]/D (DFFRX1)                  0.00      10.89 r
  data arrival time                                  10.89

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  count_reg[3]/CK (DFFRX1)                 0.00      30.00 r
  library setup time                      -0.24      29.76
  data required time                                 29.76
  -----------------------------------------------------------
  data required time                                 29.76
  data arrival time                                 -10.89
  -----------------------------------------------------------
  slack (MET)                                        18.87


***** End Of Report *****
```

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 19:33:52 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/QN (DFFRX1)                 0.25      10.25 f
  count_reg[0]/D (DFFRX1)                  0.00      10.25 f
  data arrival time                                  10.25

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  library hold time                       -0.03       9.97
  data required time                                  9.97
  -----------------------------------------------------------
  data required time                                  9.97
  data arrival time                                 -10.25
  -----------------------------------------------------------
  slack (MET)                                         0.27
```

修改 area effort 前，Setup time 為 29.79 ns，Hold time 為 9.79 ns ；修改 area effort 後，setup time 為 29.76 ns，hold time 為 9.97 ns，如下面兩張圖所示。比較後發現 setup time 減少一點點，hold time 增加一點點。

- Area report:

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Tue May  9 00:55:32 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           12
Number of nets:                            52
Number of cells:                           43
Number of combinational cells:             35
Number of sequential cells:                 8
Number of macros/black boxes:               0
Number of buf/inv:                          7
Number of references:                      16

Combinational area:               251.215198
Buf/Inv area:                      23.763600
Noncombinational area:            258.004791
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  509.219990
Total area:                 undefined

***** End Of Report *****
```

修改 area effort 前，total cell area 為 517.706 um × um
修改 area effort 後，total cell area 為 509.21999 um × um，比修改前小一點。

- Power report :

```
****************************************
Report : power
         -analysis_effort low
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 19:35:33 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.3694 uW   (93%)
  Net Switching Power  = 756.1635 nW    (7%)
                         ---------
Total Dynamic Power    =  10.1256 uW  (100%)

Cell Leakage Power     = 474.4306 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000           0.0000  (   0.00%)
register       8.8456e-03       3.7808e-04        2.3747e+05       9.4612e-03  (  89.26%)
sequential     7.1143e-05       4.9058e-06        7.2161e+04       1.4821e-04  (   1.40%)
combinational  4.5267e-04       3.7318e-04        1.6480e+05       9.9065e-04  (   9.35%)
--------------------------------------------------------------------------------------------------
Total          9.3694e-03 mW     7.5616e-04 mW     4.7443e+05 pW     1.0600e-02 mW

***** End Of Report *****
```

修改 area effort 前，Total dynamic power = 10.1256 uW，Cell leakage power = 242.4306 nW；修改 area effort 後，total dynamic power = 10.1256 uW，cell leakage power = 474.7306 nW。比較後發現 total dynamic power 減少一點，cell leakage power 增加一點。

三、 結果分析 ：

1. Area report :

```
****************************************
Report : area
Design : traffic_light
Version: P-2019.03
Date   : Tue May  9 00:55:32 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           12
Number of nets:                            52
Number of cells:                           43
Number of combinational cells:             35
Number of sequential cells:                 8
Number of macros/black boxes:               0
Number of buf/inv:                          7
Number of references:                      16

Combinational area:               251.215198
Buf/Inv area:                      23.763600
Noncombinational area:            258.004791
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  509.219990
Total area:                 undefined

***** End Of Report *****
```

Gate count = total cell area / NAND2 gate area = 102

2. Timing report :
   - Setup time :

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 12:34:15 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[3]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/Q (DFFRX1)                  0.56      10.56 f
  U74/Y (NAND2X1)                          0.13      10.69 r
  U76/Y (NOR2BX1)                          0.07      10.76 f
  U75/Y (XOR2X1)                           0.13      10.89 r
  count_reg[3]/D (DFFRX1)                  0.00      10.89 r
  data arrival time                                  10.89

  clock clk (rise edge)                   30.00      30.00
  clock network delay (ideal)              0.00      30.00
  count_reg[3]/CK (DFFRX1)                 0.00      30.00 r
  library setup time                      -0.24      29.76
  data required time                                 29.76
  -----------------------------------------------------------
  data required time                                 29.76
  data arrival time                                 -10.89
  -----------------------------------------------------------
  slack (MET)                                        18.87
```

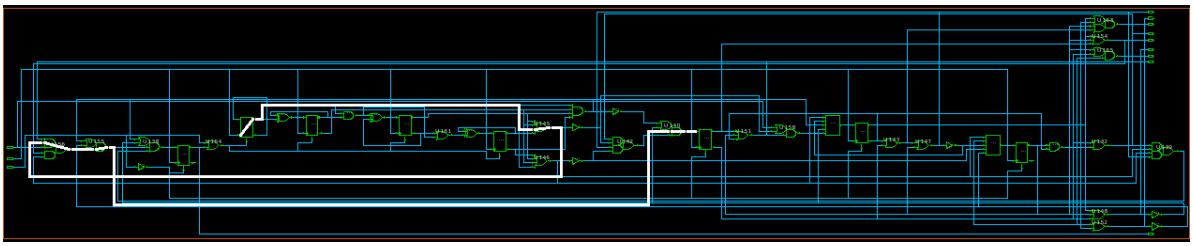
Setup time 為 29.79 ns ，slack 為正代表沒有 setup time violation

- Hold time :

```
****************************************
Report : timing
         -path full
         -delay min
         -max_paths 1
         -sort_by group
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 12:37:54 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: count_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: count_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  count_reg[0]/QN (DFFRX1)                 0.25      10.25 f
  count_reg[0]/D (DFFRX1)                  0.00      10.25 f
  data arrival time                                  10.25

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  count_reg[0]/CK (DFFRX1)                 0.00      10.00 r
  library hold time                       -0.03       9.97
  data required time                                  9.97
  -----------------------------------------------------------
  data required time                                  9.97
  data arrival time                                 -10.25
  -----------------------------------------------------------
  slack (MET)                                         0.27


***** End Of Report *****
```

Hold time 為 9.79 ns ，slack 為正代表沒有 hold time violation

3. Critical path :



這一段路徑為 counter 的計算過程到 FSM。

4. Power report :

```
****************************************
Report : power
         -analysis_effort low
Design : traffic_light
Version: P-2019.03
Date   : Sun Apr 30 12:50:54 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   9.3694 uW   (93%)
  Net Switching Power  = 756.1635 nW    (7%)
                         ---------
Total Dynamic Power    =  10.1256 uW  (100%)

Cell Leakage Power     = 474.4306 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register       8.8456e-03        3.7808e-04        2.3747e+05         9.4612e-03  (  89.26%)
sequential     7.1143e-05        4.9058e-06        7.2161e+04         1.4821e-04  (   1.40%)
combinational  4.5267e-04        3.7318e-04        1.6480e+05         9.9065e-04  (   9.35%)
--------------------------------------------------------------------------------------------------
Total          9.3694e-03 mW     7.5616e-04 mW     4.7443e+05 pW      1.0600e-02 mW

***** End Of Report *****
```

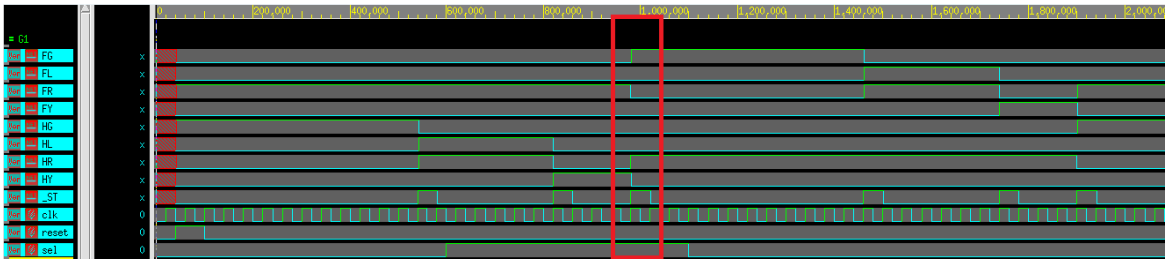
Total dynamic power = 10.1256 uW

Cell leakage power = 242.4306 nW

5. 波形 ：

我 testbench 的設計是分成兩個階段，第一階段為主要道路轉紅燈時，次要道路上有車，此時下一個壯代應該為次要道路綠燈，主要道路紅燈；第二階段為主要道路轉紅燈時，次要道路上沒車，此時下一個狀態應該為次要道路紅燈，主要道路綠燈。

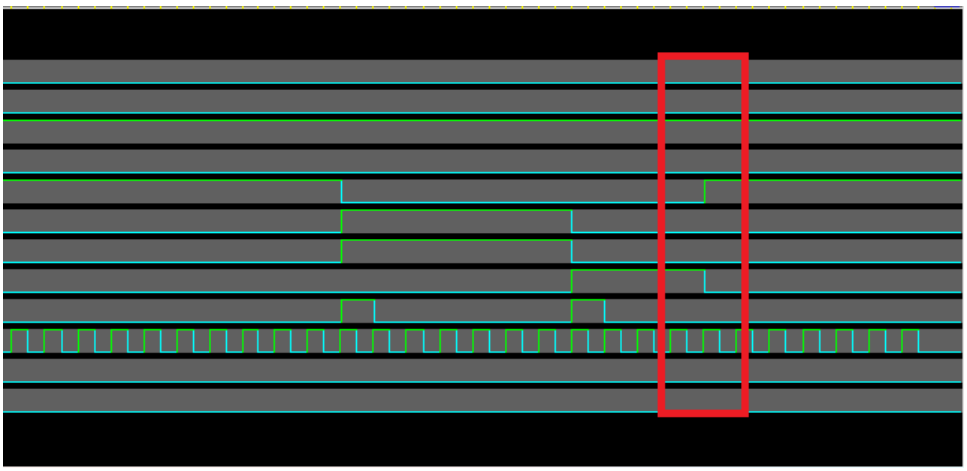
先看第一階段的波形，如下圖



紅色圈起來的部分為主要道路轉紅燈時的地方，此時 sel = 1，也就是次要道路上有車，而主要道路確實有變紅燈，次要道路也確實有轉綠

燈。

接著看第二階段，如下圖

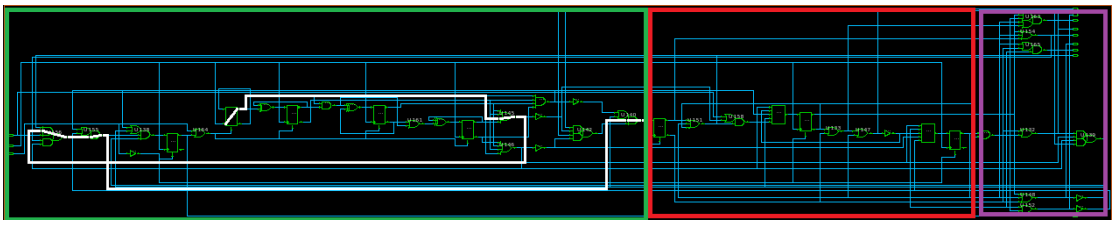


紅色框起來的部分為主要道路轉紅燈時的地方，此時 sel = 0，也就是次要道路上沒車，而主要道路確實繼續維持綠燈，次要道路繼續維持紅燈。

四、 電路分析 ：

critical path 應該會出現在 flipflop 和 flipflop 之間，對於此電路來說，最長的路經會發生在 counter 上，與合成軟體判斷的相同。

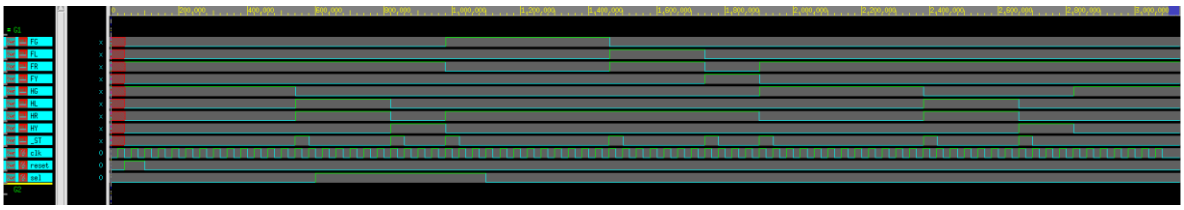
此電路分成三個部分，第一為 FSM 的部分(下圖紅色框起來的部分)，FSM 會送出 ST 訊號給 counter，然後開始 counter 的計數(下圖綠色框起來的部分)。下圖紫色框起來的部分為判斷輸出結果的部分。



五、 問題討論 ：

1. 一開始在做邏輯合成時有錯誤訊息說 always 的部分無法合成，經過檢查後發現有兩個問題 ：
   (1) always 裡有一個控制訊號為 reset | _ST，但是 always@(　)裡的訊號只有 posedge reset or posedge _ST，所以才導致合成錯誤。
   (2) ST 訊號的 assignment 有 nonblocking 和 blocking 兩種，這也導致邏輯合成無法順利執行。

2. 為什麼邏輯合成後的波形圖沒有 delay？
   一開始做波形模擬時得到下圖結果



此圖看起來沒有延遲，但是其實有，只是因為延遲的時間不大，所以將波形圖縮小後看起來沒有延遲，但是放大後就能夠觀察到延遲的狀況了。

3. 要怎麼讓 FSM 和 counter 之間可以順利溝通?
   一開始我設定了一堆訊號來控制，例如：當主要道路綠燈時間過了之後，TL = 1 並回傳一個訊號 ST1 告訴 counter 可以開始 S1 狀態的計數，在此狀態時，當經過五個正緣時，再傳一個訊號 TM 給 FSM 告訴它左轉時間結束，可以進到 S2.....以此類推。但是這樣的話會有一大堆 if-else 迴圈，變成實際電路後會很多多工器，電路面積會變很大，所以不太可行。我想到另外的方法是先設定訊號 TL = (count == 10)，然後讓計數器一直數。當經過 10 個正緣，TL = 1，代表 FSM 可以進入下一個狀態，此時 FSM 再產生一個訊號 ST 給 counter，讓 counter 歸零重新開始計數.....以此類推。這樣就能大幅減少多工器的使用，進而減少面積。
4. 合成結果的 timing report 沒有 slack。
   合成後電路跑不動的時候我發現合成出來的電路裡有 latch，檢查 code 後發現是 case 沒有寫滿，修正過後電路就正常運作了。在修正前 area report 的面積是 600 多，將 latch 修正後面積變成 500 出頭，從中也驗證了電路中出現 latch 的話電路面積會變大。

六、 心得 ：

這次作業主要是練習 finite state machine 的運用，然後額外的加分項就是透過 counter 來達到自動控制紅綠燈的效果。在這次作業中，雖然有花上比較多的時間來思考如何實現電路，但是我覺得如果只是要實現電路功能的話，那其實不難，這次作業有挑戰性的地方主要是 debug 和如何分析合成後的電路以及優化電路的部分，特別是 debug，像是我遇到最大的問題就是合成後的波形圖沒有 delay，雖然最後發現其實是有延遲的，但是過程中也是花了不少時間在尋找問題。從這次作業中，我了解到了自己對邏輯合成還不是很熟悉，也對於未來要進步的事情有了更明確的目標。