實用數位系統設計

HW2 Logic Synthesis

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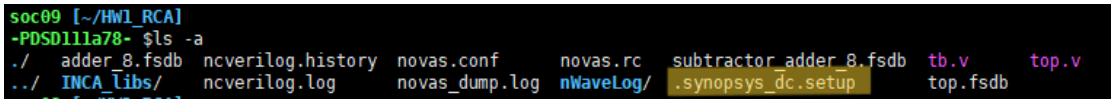
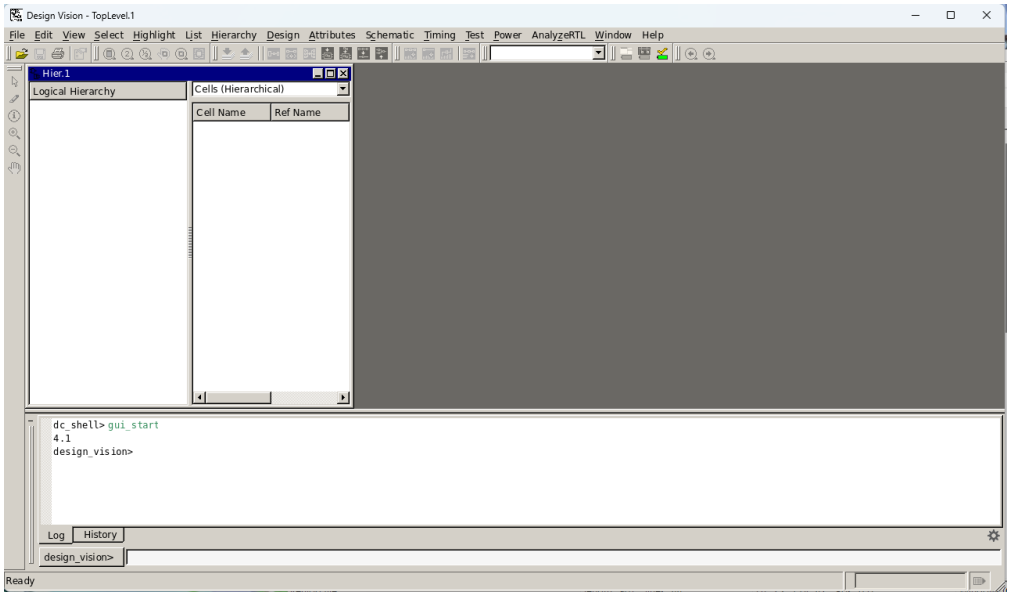
一、 合成流程 ：

I. Ripple carry adder :

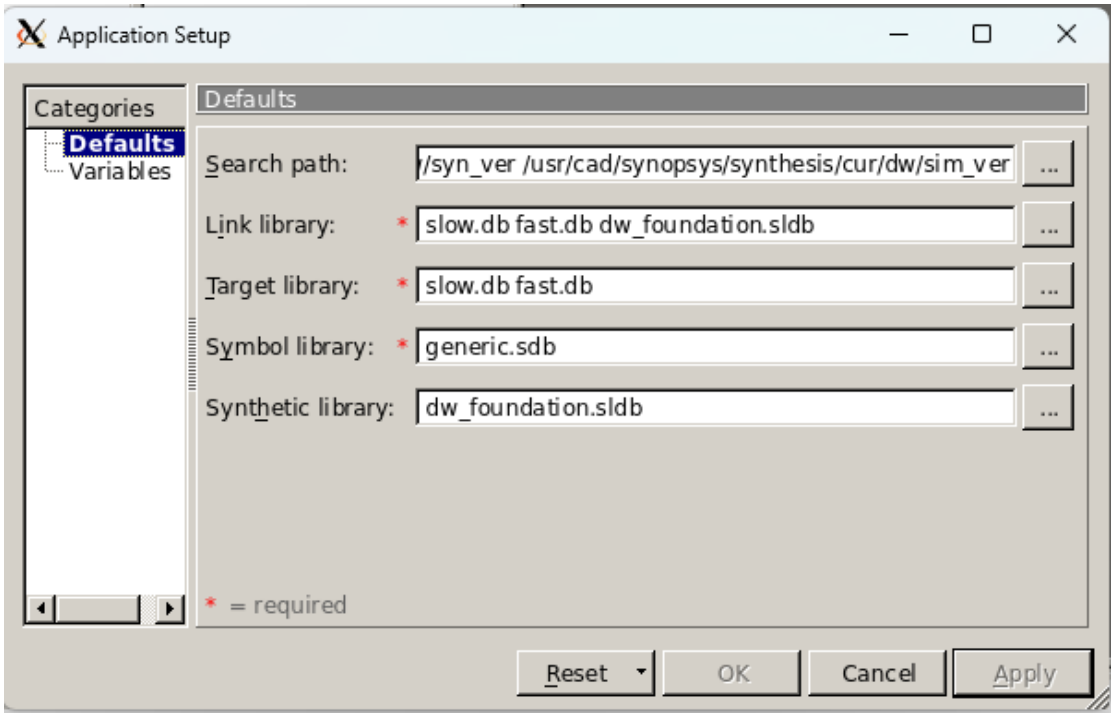
1. 在 Xshell 中輸入指令 ls -a 確認使否有.synopsys_dc.setup



2. 在 Xshell 中輸入 dv 開啟邏輯合成軟體

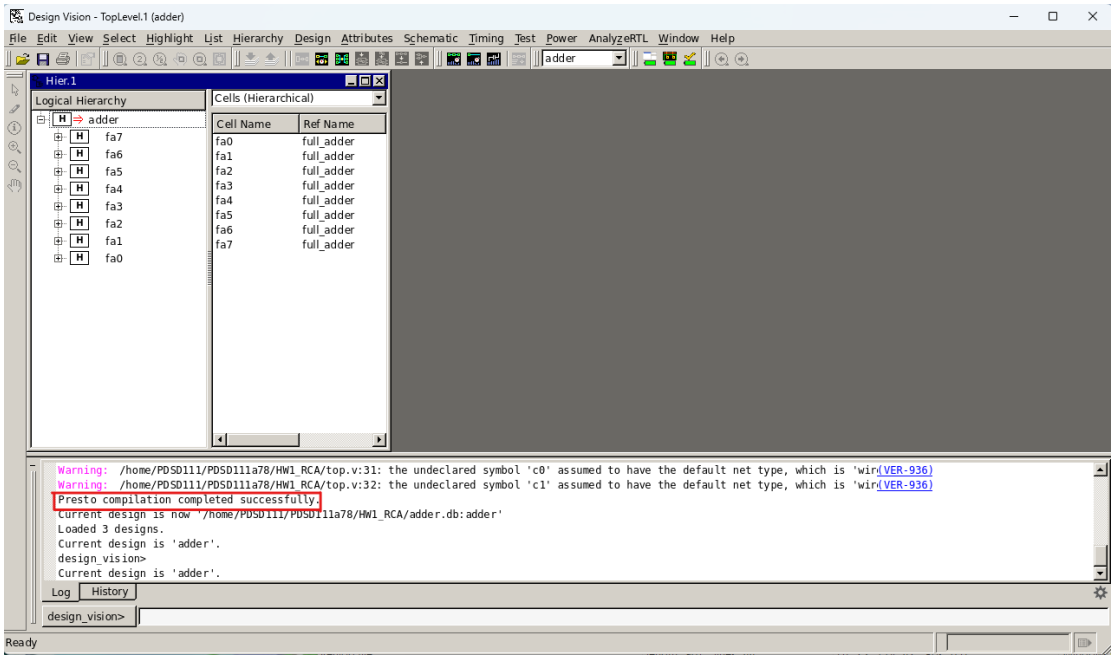


3. 在合成軟體中點擊 File>>Setup 確認檔案是否正確被引入

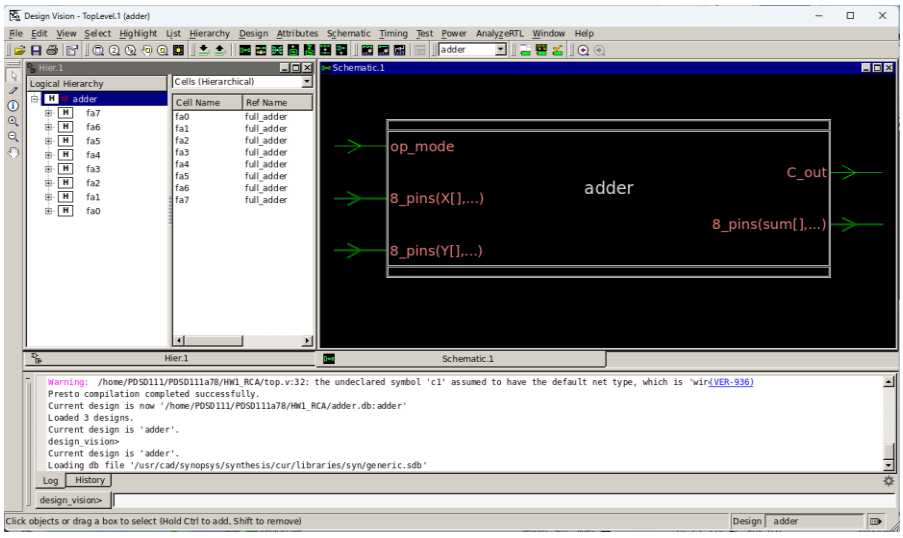


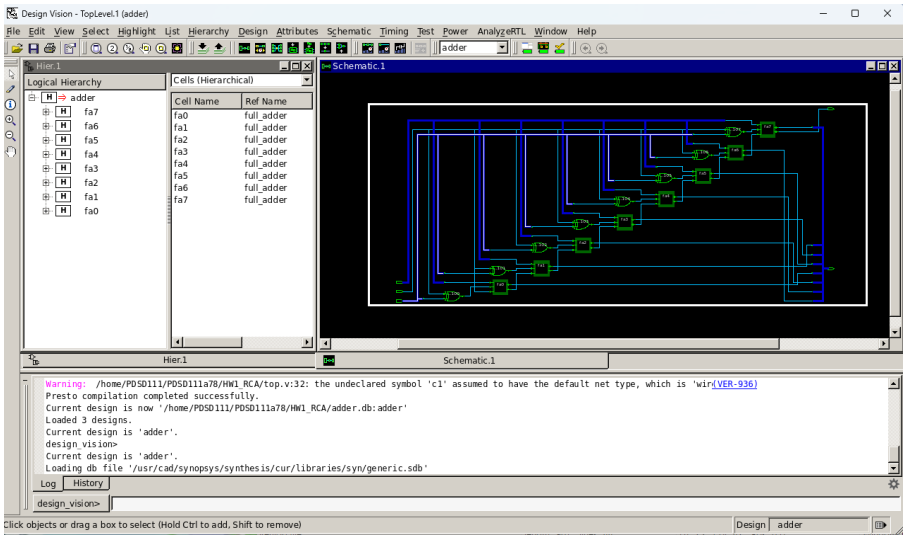
4. 利用左上角的快捷鍵讀取檔案並確認下面是否有出現 Presto

compilation completed successfully



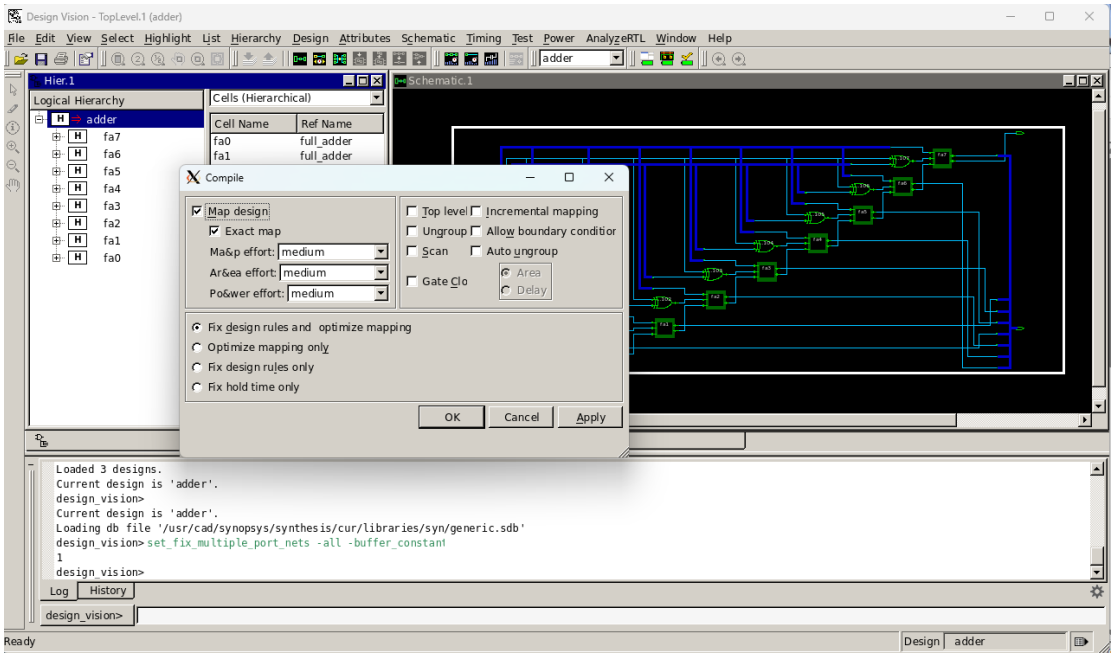
5. Symbol view 和 schematic view



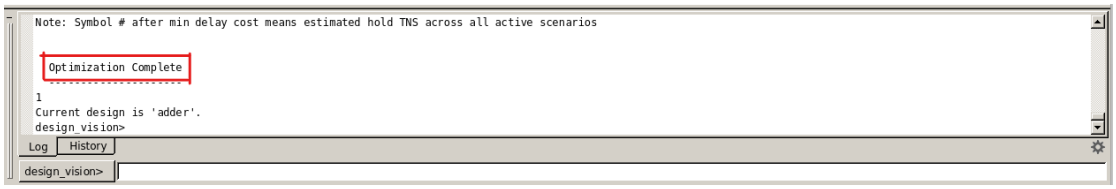


6. 在底下輸入 set_fix_multiple_port_nets -all -buffer_constants 來避免合成後電路出現 latch

7. Compile design



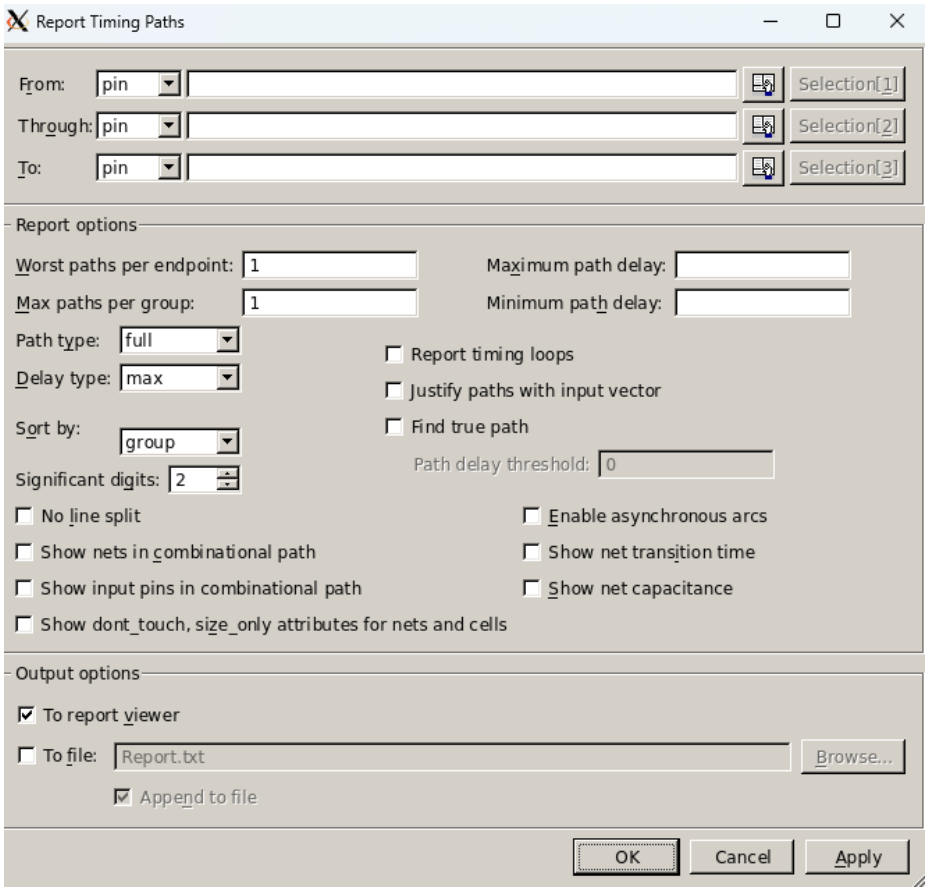
確認有沒有錯誤或警告



8. 利用 Design>>Report Area 來查看合成後電路的面積

```
****************************************
Report : area
Design : adder
Version: P-2019.03
Date   : Sat Apr 15 22:34:08 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          130
Number of nets:                           169
Number of cells:                           72
Number of combinational cells:             48
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       9

Combinational area:               448.113590
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  448.113590
Total area:                 undefined

***** End Of Report *****
```

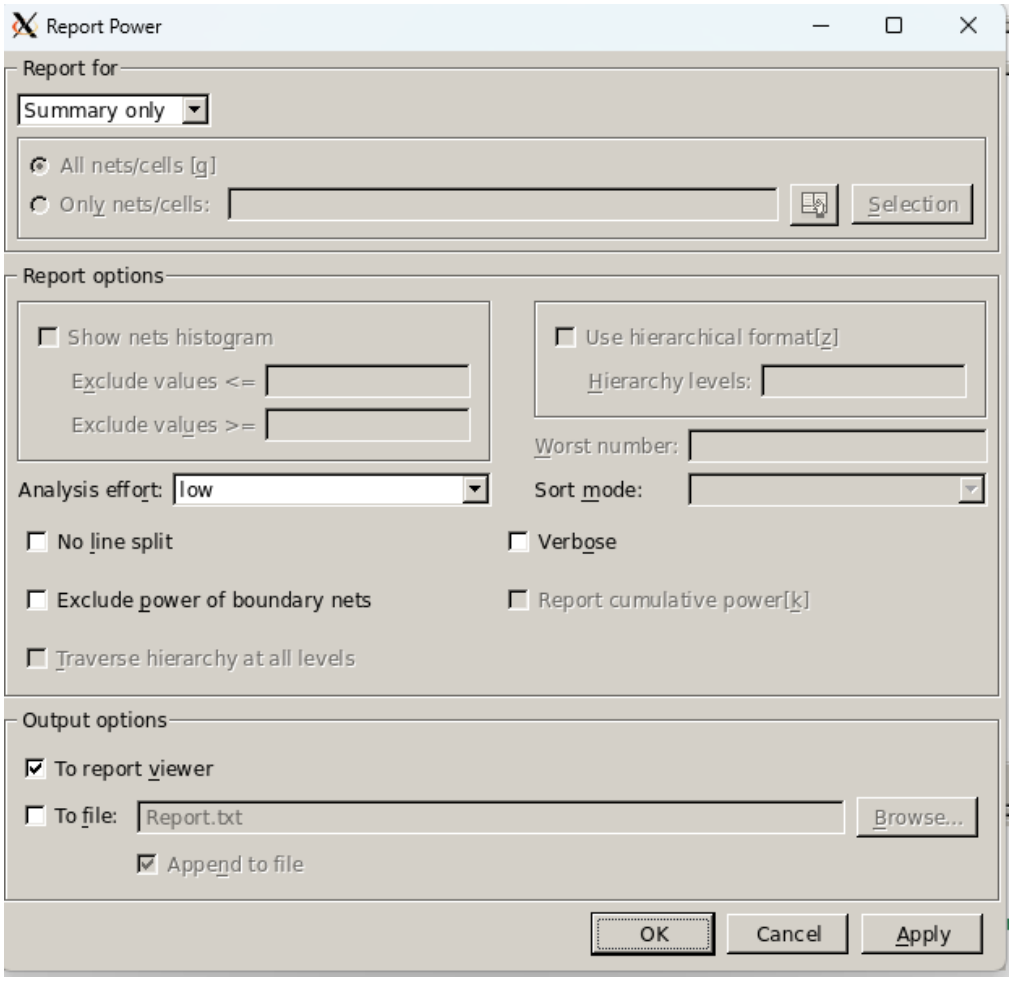
9. 利用 Timing>>Report Timing Path 來查看 critical path delay 等




```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : adder
Version: P-2019.03
Date   : Sat Apr 15 22:39:56 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: Y[0] (input port)
  Endpoint: C_out (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  Y[0] (in)                                0.00       0.00 r
  U16/Y (XOR2X1)                           0.14       0.14 r
  fa0/y (full_adder_0)                     0.00       0.14 r
  fa0/ha1/y (half_adder_0)                 0.00       0.14 r
  fa0/ha1/U1/Y (XOR2X1)                    0.20       0.34 f
  fa0/ha1/s (half_adder_0)                 0.00       0.34 f
  fa0/ha2/x (half_adder_15)                0.00       0.34 f
  fa0/ha2/U2/Y (AND2X1)                    0.20       0.54 f
  fa0/ha2/c (half_adder_15)                0.00       0.54 f
  fa0/U1/Y (OR2X1)                         0.25       0.79 f
  fa0/c (full_adder_0)                     0.00       0.79 f
  fa1/z (full_adder_7)                     0.00       0.79 f
  fa1/ha2/y (half_adder_13)                0.00       0.79 f
  fa1/ha2/U2/Y (AND2X1)                    0.17       0.96 f
  fa1/ha2/c (half_adder_13)                0.00       0.96 f
  fa1/U1/Y (OR2X1)                         0.25       1.21 f
  fa1/c (full_adder_7)                     0.00       1.21 f
  fa2/z (full_adder_6)                     0.00       1.21 f
  fa2/ha2/y (half_adder_11)                0.00       1.21 f
  fa2/ha2/U2/Y (AND2X1)                    0.17       1.39 f
  fa2/ha2/c (half_adder_11)                0.00       1.39 f
  fa2/U1/Y (OR2X1)                         0.25       1.64 f
  fa2/c (full_adder_6)                     0.00       1.64 f
  fa3/z (full_adder_5)                     0.00       1.64 f
  fa3/ha2/y (half_adder_9)                 0.00       1.64 f
  fa3/ha2/U2/Y (AND2X1)                    0.17       1.81 f
  fa3/ha2/c (half_adder_9)                 0.00       1.81 f
  fa3/U1/Y (OR2X1)                         0.25       2.06 f
  fa3/c (full_adder_5)                     0.00       2.06 f
  fa4/z (full_adder_4)                     0.00       2.06 f
  fa4/ha2/y (half_adder_7)                 0.00       2.06 f
  fa4/ha2/U2/Y (AND2X1)                    0.17       2.23 f
  fa4/ha2/c (half_adder_7)                 0.00       2.23 f
  fa4/U1/Y (OR2X1)                         0.25       2.48 f
  fa4/c (full_adder_4)                     0.00       2.48 f
  fa5/z (full_adder_3)                     0.00       2.48 f
```

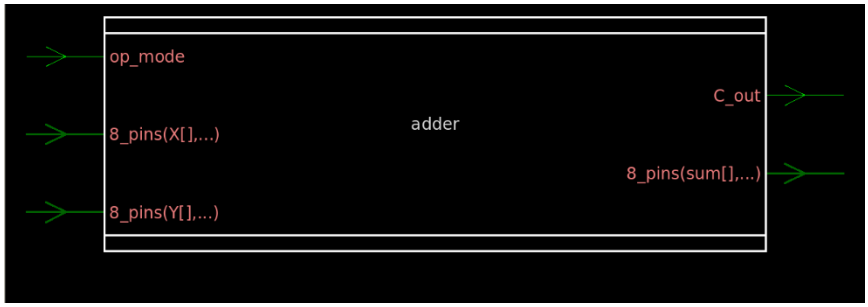
```
  fa4/c (full_adder_4)                    0.00       2.48 f
  fa5/z (full_adder_3)                    0.00       2.48 f
  fa5/ha2/y (half_adder_5)                0.00       2.48 f
  fa5/ha2/U2/Y (AND2X1)                   0.17       2.65 f
  fa5/ha2/c (half_adder_5)                0.00       2.65 f
  fa5/U1/Y (OR2X1)                        0.25       2.90 f
  fa5/c (full_adder_3)                    0.00       2.90 f
  fa6/z (full_adder_2)                    0.00       2.90 f
  fa6/ha2/y (half_adder_3)                0.00       2.90 f
  fa6/ha2/U2/Y (AND2X1)                   0.17       3.07 f
  fa6/ha2/c (half_adder_3)                0.00       3.07 f
  fa6/U1/Y (OR2X1)                        0.25       3.32 f
  fa6/c (full_adder_2)                    0.00       3.32 f
  fa7/z (full_adder_1)                    0.00       3.32 f
  fa7/ha2/y (half_adder_1)                0.00       3.32 f
  fa7/ha2/U2/Y (AND2X1)                   0.17       3.49 f
  fa7/ha2/c (half_adder_1)                0.00       3.49 f
  fa7/U1/Y (OR2X1)                        0.21       3.70 f
  fa7/c (full_adder_1)                    0.00       3.70 f
  C_out (out)                             0.00       3.70 f
  data arrival time                                  3.70
  ---------------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

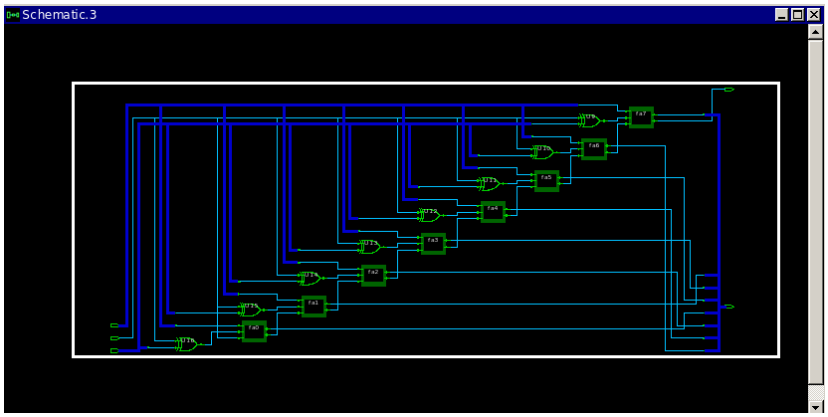
10. 利用 Design>>Report Power 來查看電路的功率表現



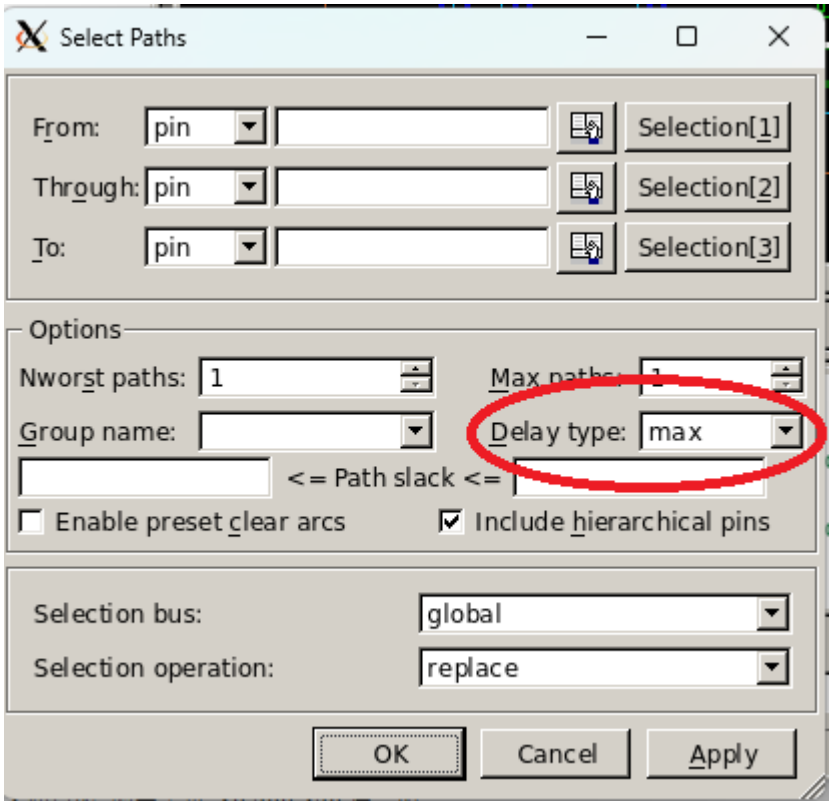
```
****************************************
Report : power
        -analysis_effort low
Design : adder
Version: P-2019.03
Date   : Sat Apr 15 22:47:08 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  60.6764 uW   (80%)
  Net Switching Power  =  15.2832 uW   (20%)
                         ---------
Total Dynamic Power    =  75.9596 uW  (100%)

Cell Leakage Power     = 614.1201 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.0676e-02        1.5283e-02        6.1412e+05         7.6574e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.0676e-02 mW     1.5283e-02 mW     6.1412e+05 pW      7.6574e-02 mW

***** End Of Report *****
```

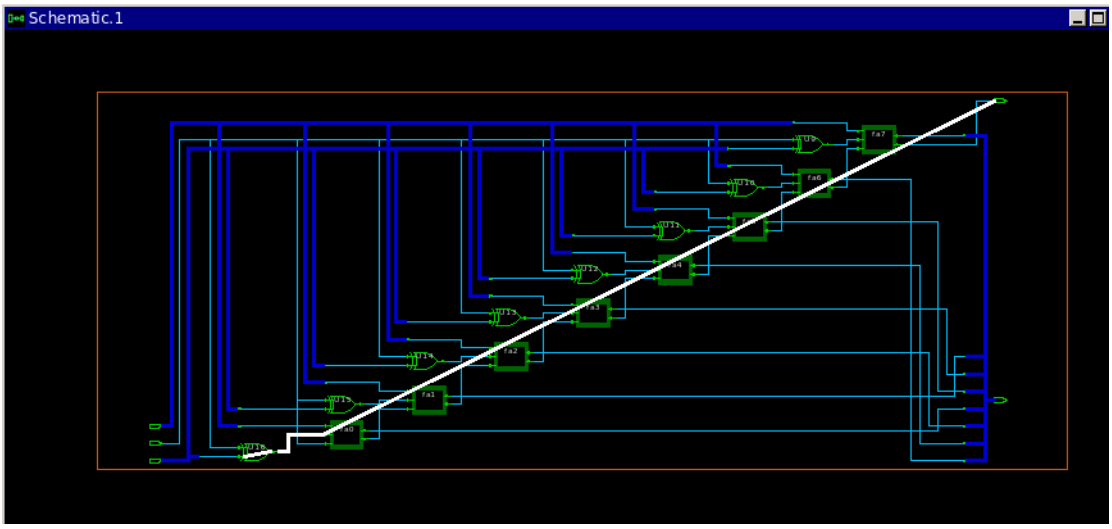
11. 利用 Hierarchy>>New Logical View 來查看合成後的電路



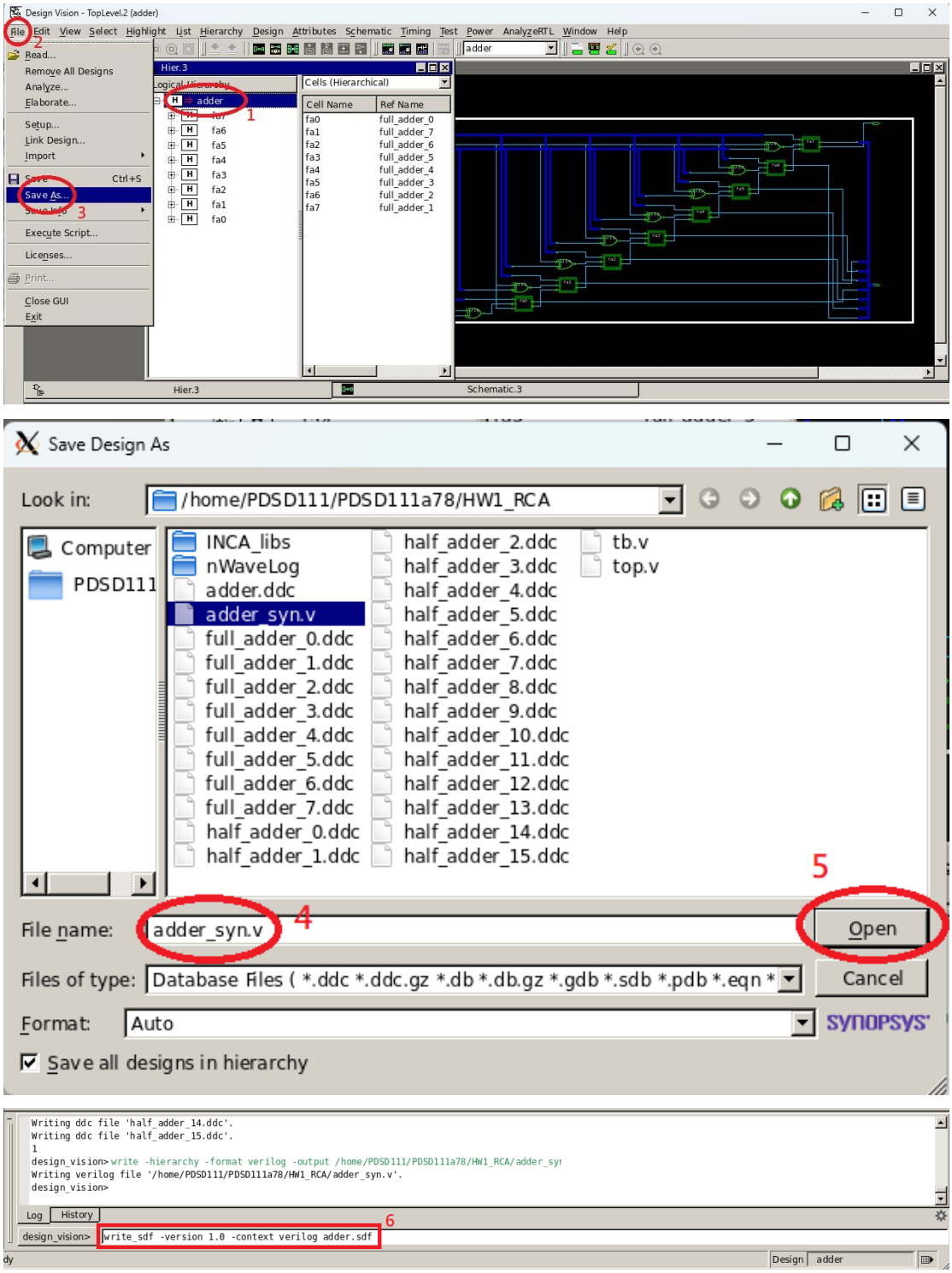


12. 利用 Select>>Paths From/Through/to 來查看 critical path

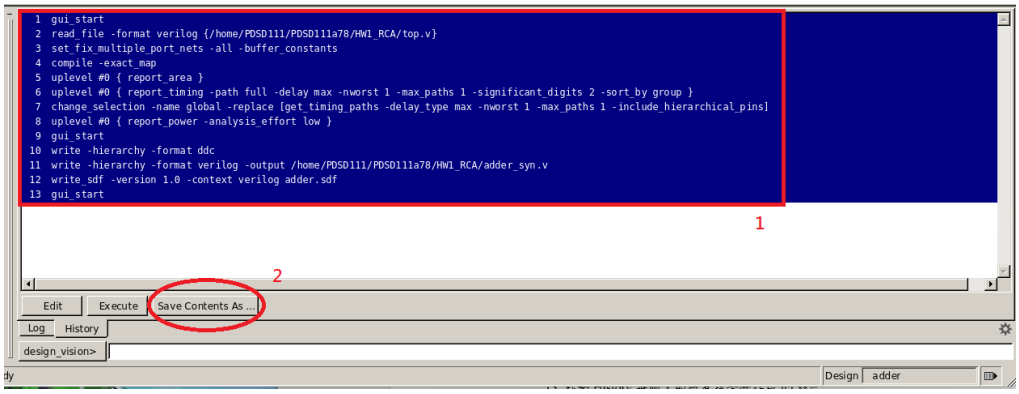


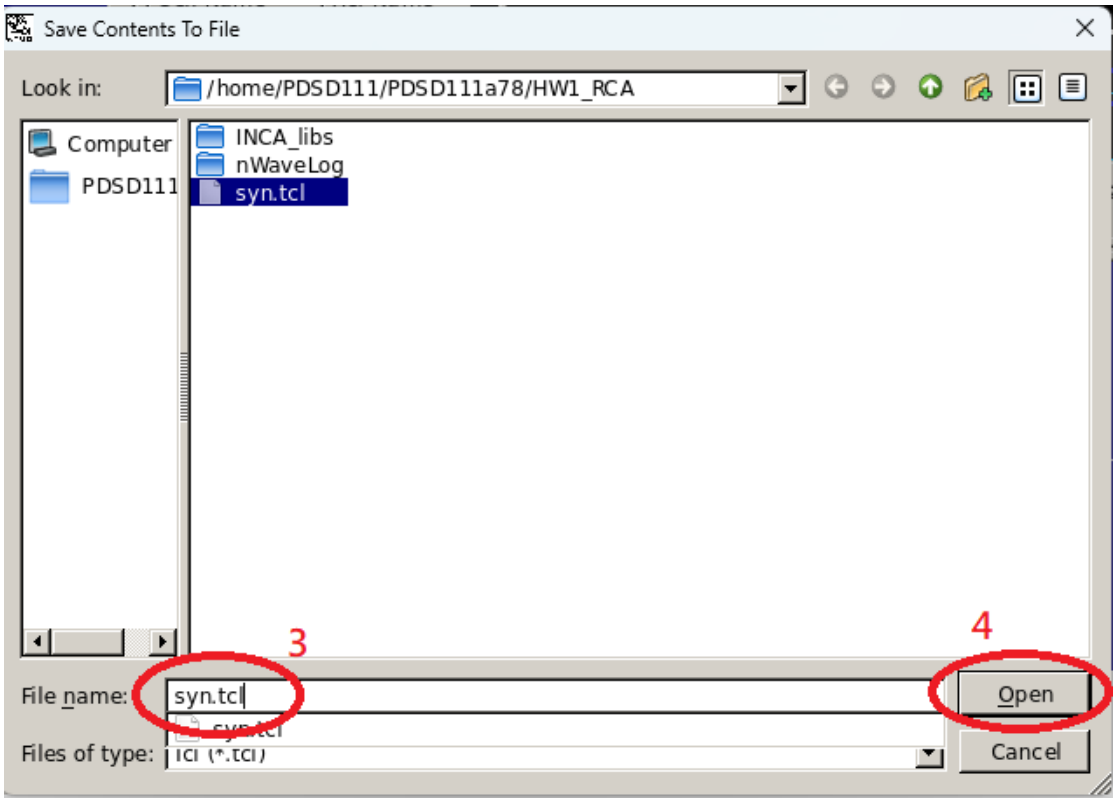


13. 將剛才合成後的結果以及各種回報儲存起來



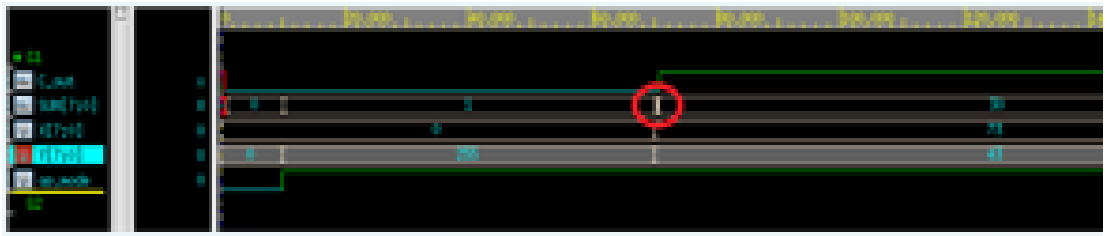
14. 點擊 History 將剛才的所有指令儲存成 tcl 檔

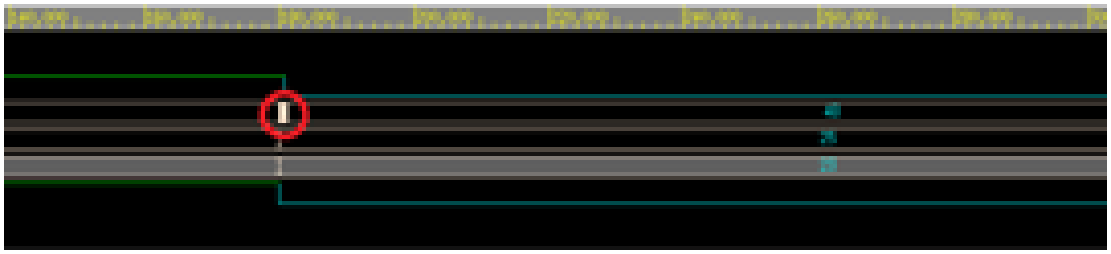




15. 修改 testbench 後回到 Xshell 輸入指令進行模擬並確認是否正確執行

```
                errors: 0, warnings: 0
        primitive worklib.udp_dff:v
                errors: 0, warnings: 0
        primitive worklib.udp_tlat:v
                errors: 0, warnings: 0
        primitive worklib.udp_edff:v
                errors: 0, warnings: 0
        primitive worklib.udp_bmx:v
                errors: 0, warnings: 0
        module worklib.tb:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Reading SDF file from location "adder.sdf"
        Writing compiled SDF file to "adder.sdf.X".
        Annotating SDF timing data:
                Compiled SDF file:     adder.sdf.X
                Log file:
                Backannotation scope:  tb.adder1
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF statistics: No. of Pathdelays = 3053  Annotated = 4.72% -- No. of Tchecks = 1206  Annotated = 0
.00%
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.ACCSHCINX2:v <0x74864a97>
                        streams:   0, words:     0
                worklib.ACCSHCINX4:v <0x7e515698>
```





紅色圈起來的部分即代表延遲的影響

II. Carry Lookahead Adder :

1. 如同 ripple carry adder 的步驟 1~10，執行邏輯合成和各種回報

   Area report :

```
****************************************
Report : area
Design : adder
Version: P-2019.03
Date   : Sun Apr 16 10:25:06 2023
****************************************

Information: Updating design information...(UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           54
Number of nets:                            79
Number of cells:                           36
Number of combinational cells:             34
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       3

Combinational area:               363.243591
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  363.243591
Total area:                 undefined
```

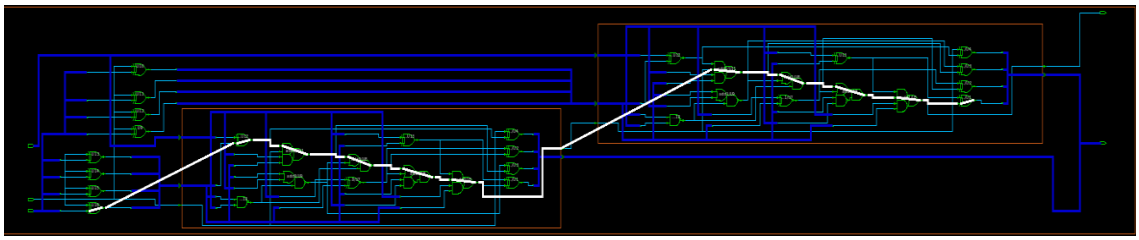
   Timing report :

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : adder
Version: P-2019.03
Date   : Sun Apr 16 10:25:06 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: Y[0] (input port)
  Endpoint: sum[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  Y[0] (in)                                0.00       0.00 r
  U16/Y (XOR2X1)                           0.15       0.15 r
  add0/b[0] (CLadder_4_0)                  0.00       0.15 r
  add0/U12/Y (XOR2X1)                      0.22       0.37 f
  add0/U11/Y (AOI22X1)                     0.15       0.53 r
  add0/U8/Y (OA21XL)                       0.22       0.75 r
  add0/U6/Y (OAI2BB2XL)                    0.08       0.83 f
  add0/U5/Y (AO22X1)                       0.39       1.22 f
  add0/cout (CLadder_4_0)                  0.00       1.22 f
  add1/cin (CLadder_4_1)                   0.00       1.22 f
  add1/U11/Y (AOI22X1)                     0.17       1.39 r
  add1/U8/Y (OA21XL)                       0.22       1.61 r
  add1/U6/Y (OAI2BB2XL)                    0.08       1.69 f
  add1/U5/Y (AO22X1)                       0.34       2.03 f
  add1/U1/Y (XOR2X1)                       0.14       2.17 f
  add1/sum[3] (CLadder_4_1)                0.00       2.17 f
  sum[7] (out)                             0.00       2.17 f
  data arrival time                                   2.17
  -----------------------------------------------------------
  (Path is unconstrained)
```

Power report :

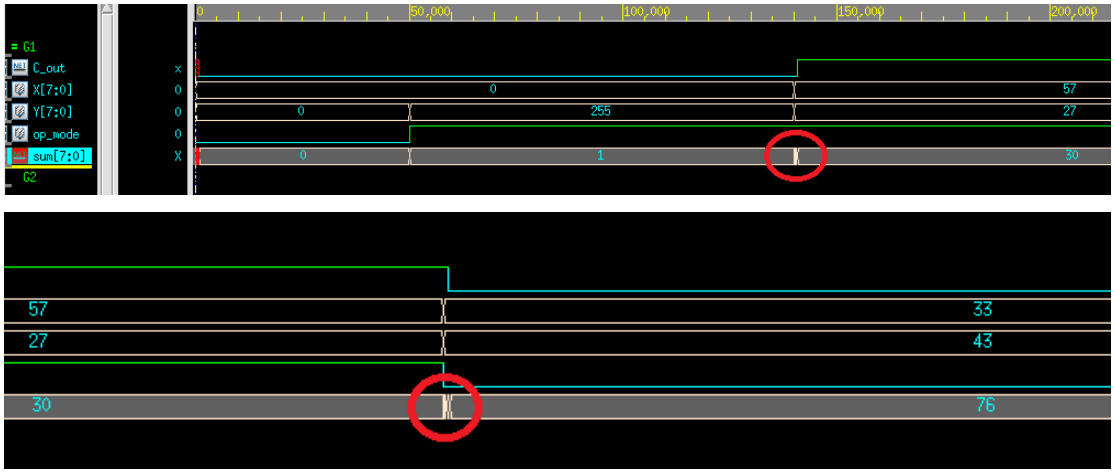
```
Report : power
        -analysis_effort low
Design : adder
Version: P-2019.03
Date   : Sun Apr 16 10:25:06 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  47.3617 uW   (76%)
  Net Switching Power  =  14.7320 uW   (24%)
                         ---------
Total Dynamic Power    =  62.0937 uW  (100%)

Cell Leakage Power     = 438.0449 nW

Information: report_power power group summary does not include estimated clock tree power(PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  4.7362e-02        1.4732e-02        4.3804e+05         6.2532e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          4.7362e-02 mW     1.4732e-02 mW     4.3804e+05 pW      6.2532e-02 mW
```

2. 如同 ripple carry adder 的步驟 12，將 critical path 顯示出來



3. 如同 ripple carry adder 的步驟 13，將檔案儲存起來
4. 如同 ripple carry adder 的步驟 15，執行模擬

```
        errors: 0, warnings: 0
    primitive worklib.udp_outrf:v
        errors: 0, warnings: 0
    primitive worklib.udp_dff:v
        errors: 0, warnings: 0
    primitive worklib.udp_tlat:v
        errors: 0, warnings: 0
    primitive worklib.udp_edff:v
        errors: 0, warnings: 0
    primitive worklib.udp_bmx:v
        errors: 0, warnings: 0
    module worklib.tb:v
        errors: 0, warnings: 0
        Caching library 'worklib' ....... Done
    Elaborating the design hierarchy:
    Reading SDF file from location "adder.sdf"
    Writing compiled SDF file to "adder.sdf.X".
    Annotating SDF timing data:
        Compiled SDF file:     adder.sdf.X
        Log file:
        Backannotation scope:  tb.add1
        Configuration file:
        MTM control:
        Scale factors:
        Scale type:
    Annotation completed successfully...
    SDF statistics: No. of Pathdelays = 3015  Annotated = 4.25% -- No. of Tchecks = 1206  Annotated = 0
.00%
    Building instance overlay tables: ..................... Done
    Generating native compiled code:
        worklib.ACCSHCINX2:v <0x74864a97>
```



由紅色圈起來的部分我們可以看到延遲的影響

III. Voting :

1. 如同 ripple carry adder 的步驟 1~10，執行邏輯合成和各種回報

   Area report :

```
****************************************
Report : area
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 11:04:20 2023
****************************************

Information: Updating design information...(UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          198
Number of nets:                           267
Number of cells:                          111
Number of combinational cells:             71
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          2
Number of references:                      18

Combinational area:               600.879589
Buf/Inv area:                       6.789600
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  600.879589
Total area:                 undefined
```

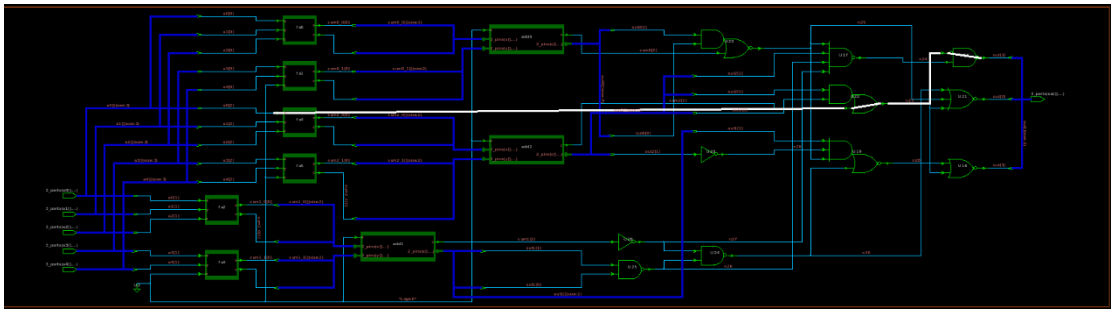
Timing report :

```
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 11:04:20 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[2] (input port)
  Endpoint: out[2] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[2] (in)                               0.00       0.00 f
  fa4/x (full_adder_8)                     0.00       0.00 f
  fa4/ha1/x (half_adder_16)                0.00       0.00 f
  fa4/ha1/U1/Y (XOR2X1)                    0.14       0.14 f
  fa4/ha1/s (half_adder_16)                0.00       0.14 f
  fa4/ha2/x (half_adder_15)                0.00       0.14 f
  fa4/ha2/U2/Y (AND2X1)                    0.20       0.34 f
  fa4/ha2/c (half_adder_15)                0.00       0.34 f
  fa4/U1/Y (OR2X1)                         0.25       0.60 f
  fa4/c (full_adder_8)                     0.00       0.60 f
  add2/x[1] (adder2_1)                     0.00       0.60 f
  add2/f1/x (full_adder_1)                 0.00       0.60 f
  add2/f1/ha1/x (half_adder_2)             0.00       0.60 f
  add2/f1/ha1/U1/Y (XOR2X1)                0.17       0.76 f
  add2/f1/ha1/s (half_adder_2)             0.00       0.76 f
  add2/f1/ha2/x (half_adder_1)             0.00       0.76 f
  add2/f1/ha2/U2/Y (AND2X1)                0.20       0.97 f
  add2/f1/ha2/c (half_adder_1)             0.00       0.97 f
  add2/f1/U1/Y (OR2X1)                     0.22       1.19 f
  add2/f1/c (full_adder_1)                 0.00       1.19 f
  add2/c (adder2_1)                        0.00       1.19 f
  U22/Y (AO21X1)                           0.27       1.46 f
  U16/Y (NAND2BX1)                         0.16       1.62 f
  out[2] (out)                             0.00       1.62 f
  data arrival time                                   1.62
  -----------------------------------------------------------
  (Path is unconstrained)
```

Power report :

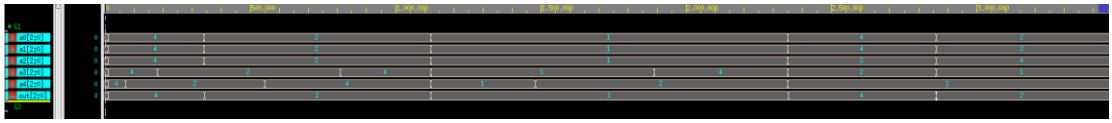
```
Report : power
        -analysis_effort low
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 11:04:20 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  69.1570 uW   (73%)
  Net Switching Power  =  25.2965 uW   (27%)
                         ---------
Total Dynamic Power    =  94.4534 uW  (100%)

Cell Leakage Power     = 755.5283 nW

Information: report_power power group summary does not include estimated clock tree power(PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.9157e-02        2.5296e-02        7.5553e+05         9.5209e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.9157e-02 mW     2.5296e-02 mW     7.5553e+05 pW      9.5209e-02 mW
```

2. 如同 ripple carry adder 的步驟 12，將 critical path 顯示出來



3. 如同 ripple carry adder 的步驟 13，將檔案儲存起來
4. 如同 ripple carry adder 的步驟 15，執行模擬

```
Recompiling... reason: file './tb_median.v' is newer than expected.
        expected: Wed Apr 12 16:28:57 2023
        actual:   Sun Apr 16 11:16:23 2023
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Reading SDF file from location "voting.sdf"
        Writing compiled SDF file to "voting.sdf.X".
        Annotating SDF timing data:
                Compiled SDF file:     voting.sdf.X
                Log file:
                Backannotation scope:  tb.v0
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF Statistics: No. of Pathdelays = 3080  Annotated = 6.33% -- No. of Tchecks = 1206  Annotated = 0
.00%
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.ACCSHCINX2:v <0x74864a97>
                        streams:   0, words:     0
                worklib.ACCSHCINX4:v <0x7e515698>
                        streams:   0, words:     0
                worklib.ACCSHCONX2:v <0x4bd2e171>
                        streams:   0, words:     0
                worklib.ACCSHCONX4:v <0x4105fd7e>
                        streams:   0, words:     0
                worklib.ACHCINX2:v <0x6fc8ef3b>
                        streams:   0, words:     0
                worklib.ACHCINX4:v <0x3da5360c>
```



IV. Median :

1. 如同 ripple carry adder 的步驟 1~10，執行邏輯合成和各種回報

   Area report :

```
****************************************
Report : area
Design : median
Version: P-2019.03
Date   : Sun Apr 16 12:21:14 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           32
Number of nets:                            87
Number of cells:                           63
Number of combinational cells:             63
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         24
Number of references:                      12

Combinational area:               490.548591
Buf/Inv area:                      81.475199
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  490.548591
Total area:                 undefined

***** End Of Report *****
```

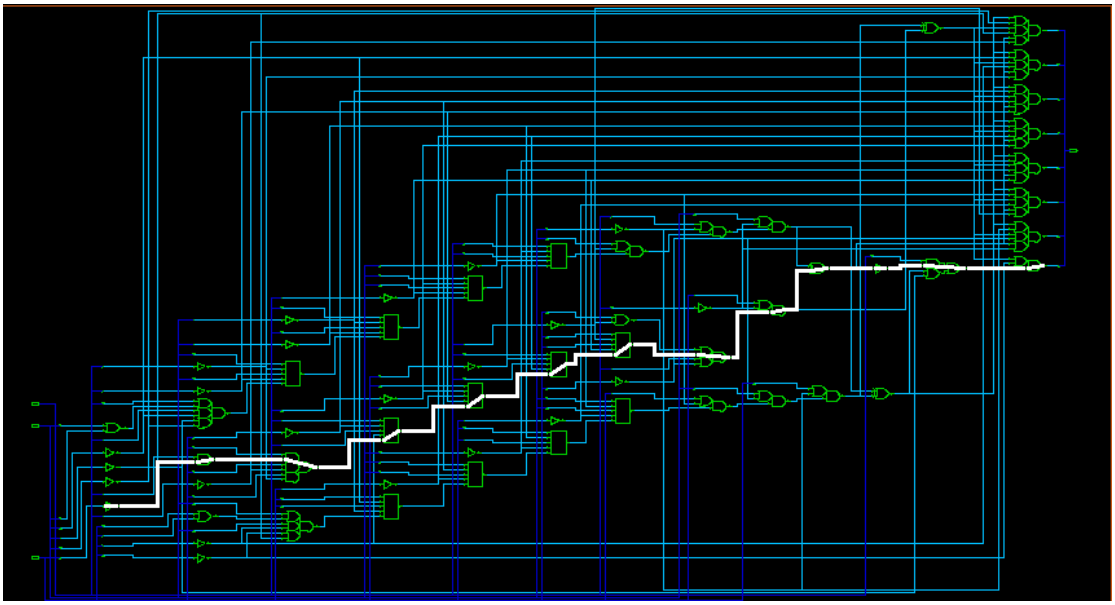
Timing report :

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : median
Version: P-2019.03
Date   : Sun Apr 16 12:22:27 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[1] (input port)
  Endpoint: out[0] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[1] (in)                               0.00       0.00 f
  U56/Y (CLKINVX1)                         0.05       0.05 r
  U38/Y (NAND2X1)                          0.05       0.10 f
  U36/Y (AOI222XL)                         0.33       0.43 r
  U35/Y (AOI221XL)                         0.10       0.53 f
  U34/Y (AOI221XL)                         0.20       0.74 r
  U33/Y (AOI221XL)                         0.10       0.83 f
  U32/Y (AOI221XL)                         0.20       1.04 r
  U31/Y (OAI22XL)                          0.12       1.16 f
  U30/Y (OA21XL)                           0.21       1.36 f
  U17/Y (XOR2X1)                           0.28       1.64 r
  U16/Y (CLKINVX1)                         0.10       1.75 f
  U14/Y (AOI2BB2X1)                        0.14       1.89 r
  U13/Y (OAI21XL)                          0.06       1.95 f
  out[0] (out)                             0.00       1.95 f
  data arrival time                                   1.95
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

Power report :

```
****************************************
Report : power
        -analysis_effort low
Design : median
Version: P-2019.03
Date   : Sun Apr 16 12:23:31 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  32.3743 uW   (60%)
  Net Switching Power  =  21.9078 uW   (40%)
                         ---------
Total Dynamic Power    =  54.2821 uW  (100%)

Cell Leakage Power     = 166.1685 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  3.2374e-02        2.1908e-02        1.6617e+05         5.4448e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          3.2374e-02 mW     2.1908e-02 mW     1.6617e+05 pW      5.4448e-02 mW

***** End Of Report *****
```

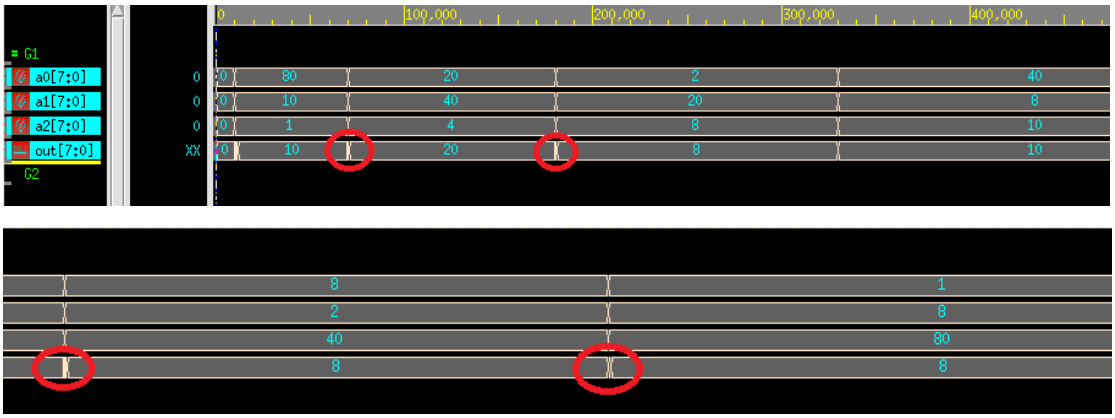
2. 如同 ripple carry adder 的步驟 12，將 critical path 顯示出來



3. 如同 ripple carry adder 的步驟 13，將檔案儲存起來

4. 如同 ripple carry adder 的步驟 15，執行模擬

```
        Writing compiled SDF file to "median.sdf.X".
        Annotating SDF timing data:
                Compiled SDF file:     median.sdf.X
                Log file:
                Backannotation scope:  tb.m0
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
                SDF Statistics: No. of Pathdelays    3068  Annotated = 6.39% -- No. of Tchecks = 1206  Annotated = 0
.00%
        Building instance overlay tables: ..................... Done
        Generating native compiled code:
                worklib.ACCSHCINX2:v <0x74864a97>
                        streams:   0, words:     0
                worklib.ACCSHCINX4:v <0x7e515698>
                        streams:   0, words:     0
                worklib.ACCSHCONX2:v <0x4bd2e171>
                        streams:   0, words:     0
                worklib.ACCSHCONX4:v <0x4105fd7e>
                        streams:   0, words:     0
                worklib.ACHCINX2:v <0x6fc8ef3b>
                        streams:   0, words:     0
                worklib.ACHCINX4:v <0x3da5360c>
                        streams:   0, words:     0
                worklib.ACHCONX2:v <0x404cc974>
                        streams:   0, words:     0
                worklib.ACHCONX4:v <0x12211043>
                        streams:   0, words:     0
                worklib.ADDFHX1:v <0x18dec4ad>
```



由紅色圈起來的部分可以看出延遲的影響

二、 電路分析 ：

1. Ripple Carry Adder :

(1) Area report 分析 ：

```
****************************************
Report : area
Design : adder
Version: P-2019.03
Date   : Sat Apr 15 22:34:08 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          130
Number of nets:                           169
Number of cells:                           72
Number of combinational cells:             48
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       9

Combinational area:               448.113590
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  448.113590
Total area:                 undefined

***** End Of Report *****
```

要計算 gate count 要將 report area 除以 NAND2 的面積 448.113599 / 5 = 89.62 。

(2) Timing report 分析 ：

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : adder
Version: P-2019.03
Date   : Sat Apr 15 22:39:56 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: Y[0] (input port)
  Endpoint: C_out (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  Y[0] (in)                                0.00       0.00 r
  U16/Y (XOR2X1)                           0.14       0.14 r
  fa0/y (full_adder_0)                     0.00       0.14 r
  fa0/ha1/y (half_adder_0)                 0.00       0.14 r
  fa0/ha1/U1/Y (XOR2X1)                    0.20       0.34 f
  fa0/ha1/s (half_adder_0)                 0.00       0.34 f
  fa0/ha2/x (half_adder_15)                0.00       0.34 f
  fa0/ha2/U2/Y (AND2X1)                    0.20       0.54 f
  fa0/ha2/c (half_adder_15)                0.00       0.54 f
  fa0/U1/Y (OR2X1)                         0.25       0.79 f
  fa0/c (full_adder_0)                     0.00       0.79 f
  fa1/z (full_adder_7)                     0.00       0.79 f
  fa1/ha2/y (half_adder_13)                0.00       0.79 f
  fa1/ha2/U2/Y (AND2X1)                    0.17       0.96 f
  fa1/ha2/c (half_adder_13)                0.00       0.96 f
  fa1/U1/Y (OR2X1)                         0.25       1.21 f
  fa1/c (full_adder_7)                     0.00       1.21 f
  fa2/z (full_adder_6)                     0.00       1.21 f
  fa2/ha2/y (half_adder_11)                0.00       1.21 f
  fa2/ha2/U2/Y (AND2X1)                    0.17       1.39 f
  fa2/ha2/c (half_adder_11)                0.00       1.39 f
  fa2/U1/Y (OR2X1)                         0.25       1.64 f
  fa2/c (full_adder_6)                     0.00       1.64 f
  fa3/z (full_adder_5)                     0.00       1.64 f
  fa3/ha2/y (half_adder_9)                 0.00       1.64 f
  fa3/ha2/U2/Y (AND2X1)                    0.17       1.81 f
  fa3/ha2/c (half_adder_9)                 0.00       1.81 f
  fa3/U1/Y (OR2X1)                         0.25       2.06 f
  fa3/c (full_adder_5)                     0.00       2.06 f
  fa4/z (full_adder_4)                     0.00       2.06 f
  fa4/ha2/y (half_adder_7)                 0.00       2.06 f
  fa4/ha2/U2/Y (AND2X1)                    0.17       2.23 f
  fa4/ha2/c (half_adder_7)                 0.00       2.23 f
  fa4/U1/Y (OR2X1)                         0.25       2.48 f
  fa4/c (full_adder_4)                     0.00       2.48 f
  fa5/z (full_adder_3)                     0.00       2.48 f
```

```
  fa4/c (full_adder_4)                    0.00       2.48 f
  fa5/z (full_adder_3)                    0.00       2.48 f
  fa5/ha2/y (half_adder_5)                0.00       2.48 f
  fa5/ha2/U2/Y (AND2X1)                   0.17       2.65 f
  fa5/ha2/c (half_adder_5)                0.00       2.65 f
  fa5/U1/Y (OR2X1)                        0.25       2.90 f
  fa5/c (full_adder_3)                    0.00       2.90 f
  fa6/z (full_adder_2)                    0.00       2.90 f
  fa6/ha2/y (half_adder_3)                0.00       2.90 f
  fa6/ha2/U2/Y (AND2X1)                   0.17       3.07 f
  fa6/ha2/c (half_adder_3)                0.00       3.07 f
  fa6/U1/Y (OR2X1)                        0.25       3.32 f
  fa6/c (full_adder_2)                    0.00       3.32 f
  fa7/z (full_adder_1)                    0.00       3.32 f
  fa7/ha2/y (half_adder_1)                0.00       3.32 f
  fa7/ha2/U2/Y (AND2X1)                   0.17       3.49 f
  fa7/ha2/c (half_adder_1)                0.00       3.49 f
  fa7/U1/Y (OR2X1)                        0.21       3.70 f
  fa7/c (full_adder_1)                    0.00       3.70 f
  C_out (out)                             0.00       3.70 f
  data arrival time                                  3.70
  ---------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

由於此電路為 combinational 電路，所以最後會有一行 path is unconstrained。藍色的部分代表 critical path 所經過的邏輯閘，data arrival time 代表 critical path 的 delay 時間，此電路的 data arrival time 為 3.79 ns。

(3) Power report 分析 ：

```
****************************************
Report : power
        -analysis_effort low
Design : adder
Version: P-2019.03
Date   : Sat Apr 15 22:47:08 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  60.6764 uW   (80%)
  Net Switching Power  =  15.2832 uW   (20%)
                         ---------
Total Dynamic Power    =  75.9596 uW  (100%)

Cell Leakage Power     = 614.1201 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.0676e-02        1.5283e-02        6.1412e+05         7.6574e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.0676e-02 mW     1.5283e-02 mW     6.1412e+05 pW      7.6574e-02 mW

***** End Of Report *****
```

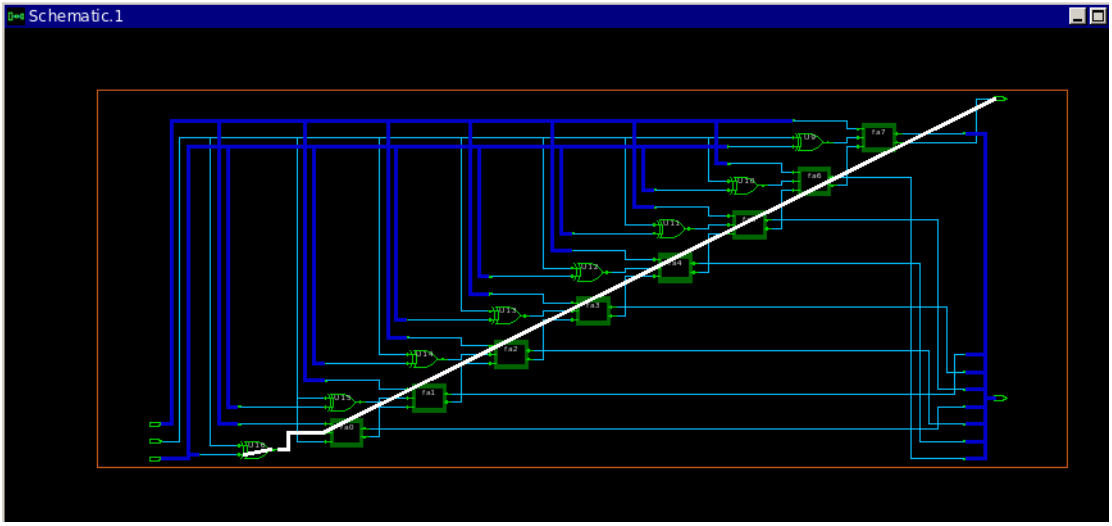
Total dynamic power 代表訊號在 0 跟 1 之間轉換時所消耗的功

率，此電路消耗的功率為 75.9596 uW。

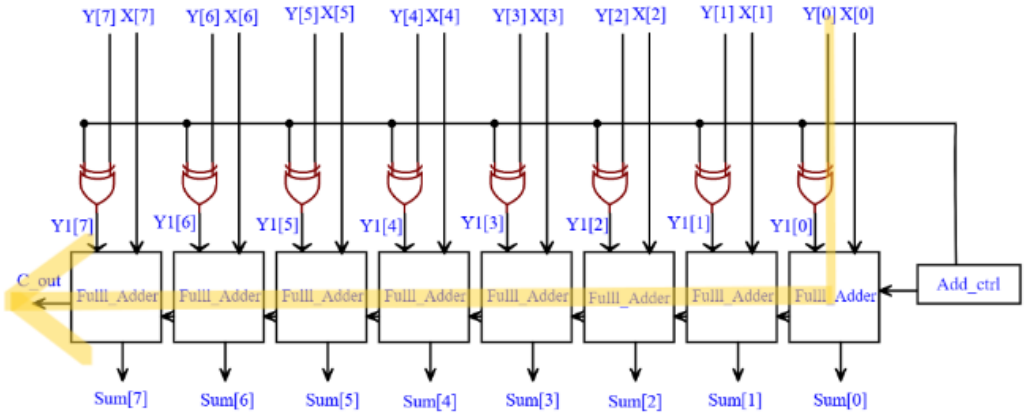
Cell leakage power 代表電路靜止時的漏電，此電路為 614.1201 nW。

通常 total dynamic power 會比 cell leakage power 大。

(4) Critical path 分析 ：



上圖為邏輯合成後邏輯合成軟體判斷的 critical path。

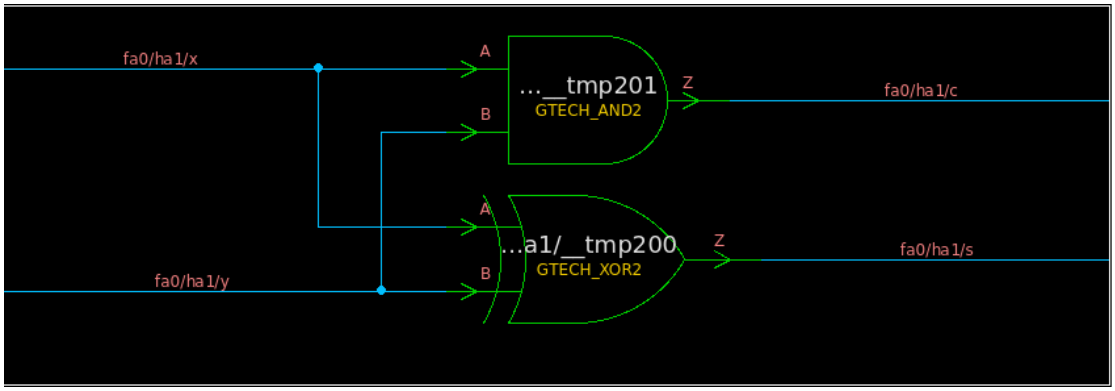


上圖為第一次作業中，自己分析的 critical path。

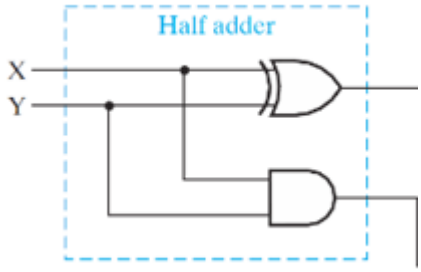
由這兩張圖我們可以發現兩者判斷的 critical path 相同。

(5) 電路分析 ：

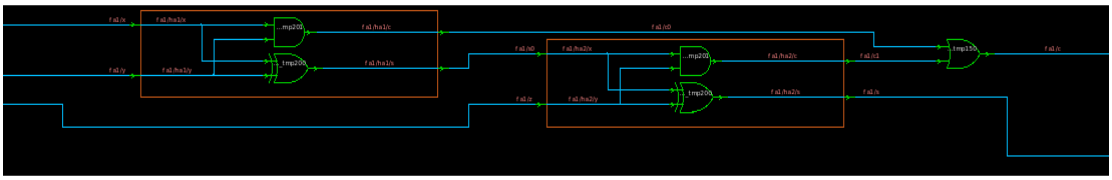
先看 half adder 合成後的電路，如下圖



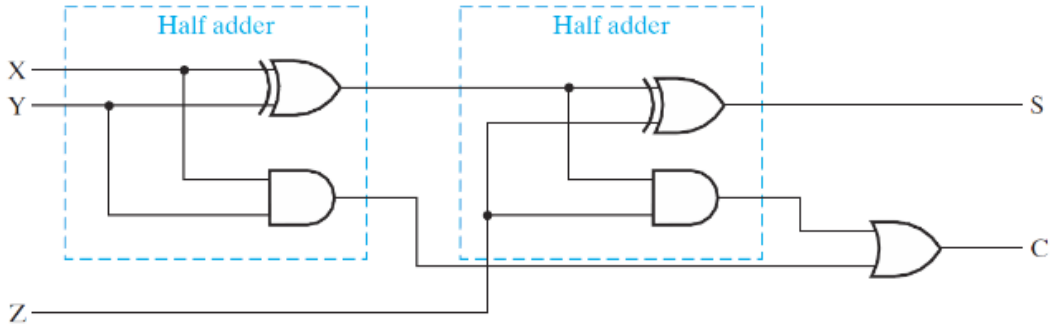
拿此電路與作業一中自己畫的電路(下圖)做比較，我們可以發現兩者相同



接著看 full adder 合成後的電路，如下圖



拿此電路與作業一中自己畫的電路(下圖)做比較，我們可以發現兩者相同



利用 critical path 分析的結果以及上面分析的結果我們可以得知，此電路合成後的結果與我們預期的相同。

2. Carry Lookahead Adder :

(1) Area report 分析 ：

```
****************************************
Report : area
Design : adder
Version: P-2019.03
Date   : Sun Apr 16 10:25:06 2023
****************************************

Information: Updating design information...(UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           54
Number of nets:                            79
Number of cells:                           36
Number of combinational cells:             34
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       3

Combinational area:               363.243591
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  363.243591
Total area:                 undefined
```

Gate count = 363.243591 / 5 = 72.64

(2) Timing report 分析 ：

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : adder
Version: P-2019.03
Date   : Sun Apr 16 13:31:42 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: Y[0] (input port)
  Endpoint: sum[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  Y[0] (in)                                0.00       0.00 r
  U16/Y (XOR2X1)                           0.15       0.15 r
  add0/b[0] (CLadder_4_0)                  0.00       0.15 r
  add0/U12/Y (XOR2X1)                      0.22       0.37 f
  add0/U11/Y (AOI22X1)                     0.15       0.53 r
  add0/U8/Y (OA21XL)                       0.22       0.75 r
  add0/U6/Y (OAI2BB2XL)                    0.08       0.83 f
  add0/U5/Y (AO22X1)                       0.39       1.22 f
  add0/cout (CLadder_4_0)                  0.00       1.22 f
  add1/cin (CLadder_4_1)                   0.00       1.22 f
  add1/U11/Y (AOI22X1)                     0.17       1.39 r
  add1/U8/Y (OA21XL)                       0.22       1.61 r
  add1/U6/Y (OAI2BB2XL)                    0.08       1.69 f
  add1/U5/Y (AO22X1)                       0.34       2.03 f
  add1/U1/Y (XOR2X1)                       0.14       2.17 f
  add1/sum[3] (CLadder_4_1)                0.00       2.17 f
  sum[7] (out)                             0.00       2.17 f
  data arrival time                                   2.17
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

由於此電路為 combinational 電路，所以最後會有一行 path is unconstrained。藍色的部分代表 critical path 所經過的邏輯閘，data arrival time 代表 critical path 的 delay 時間，此電路的 data arrival time 為 2.17 ns。

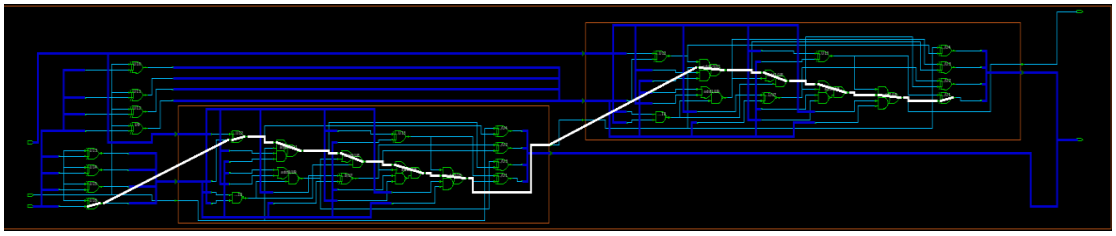
(3) Power report 分析 ：

```
****************************************
Report : power
        -analysis_effort low
Design : adder
Version: P-2019.03
Date   : Sun Apr 16 13:32:53 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  47.3617 uW   (76%)
  Net Switching Power  =  14.7320 uW   (24%)
                         ---------
Total Dynamic Power    =  62.0937 uW  (100%)

Cell Leakage Power     = 438.0449 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  4.7362e-02       1.4732e-02        4.3804e+05         6.2532e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          4.7362e-02 mW     1.4732e-02 mW     4.3804e+05 pW      6.2532e-02 mW

***** End Of Report *****
```

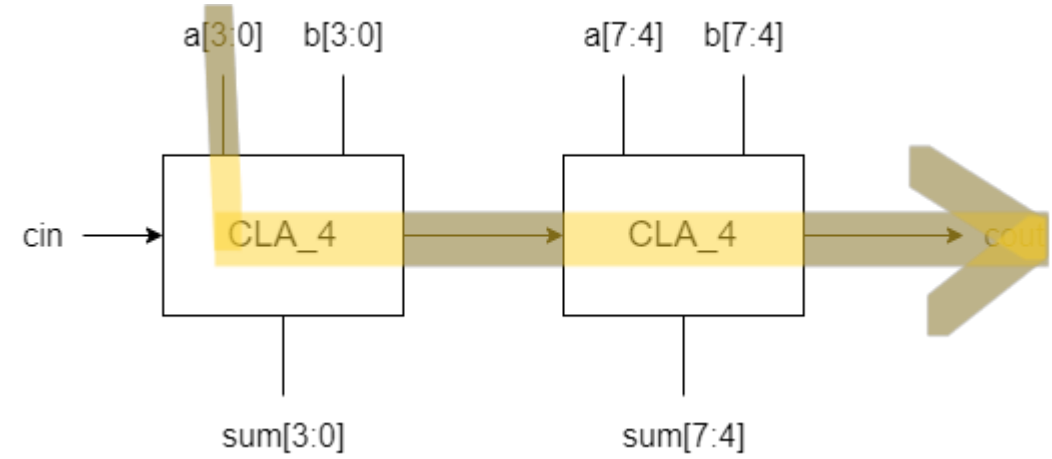
Total dynamic power 代表訊號在 0 跟 1 之間轉換時所消耗的功率，此電路消耗的功率為 62.0937 uW。

Cell leakage power 代表電路靜止時的漏電，此電路為 438.0449 nW。

(4) Critical path 分析 ：



上圖為邏輯合成後邏輯合成軟體判斷的 critical path。

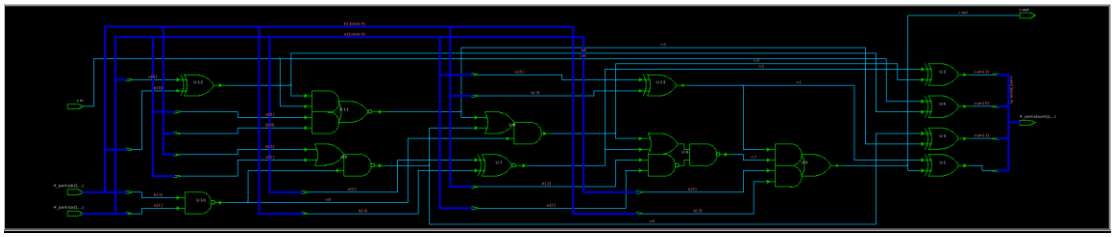


上圖為第一次作業中，自己分析的 critical path。

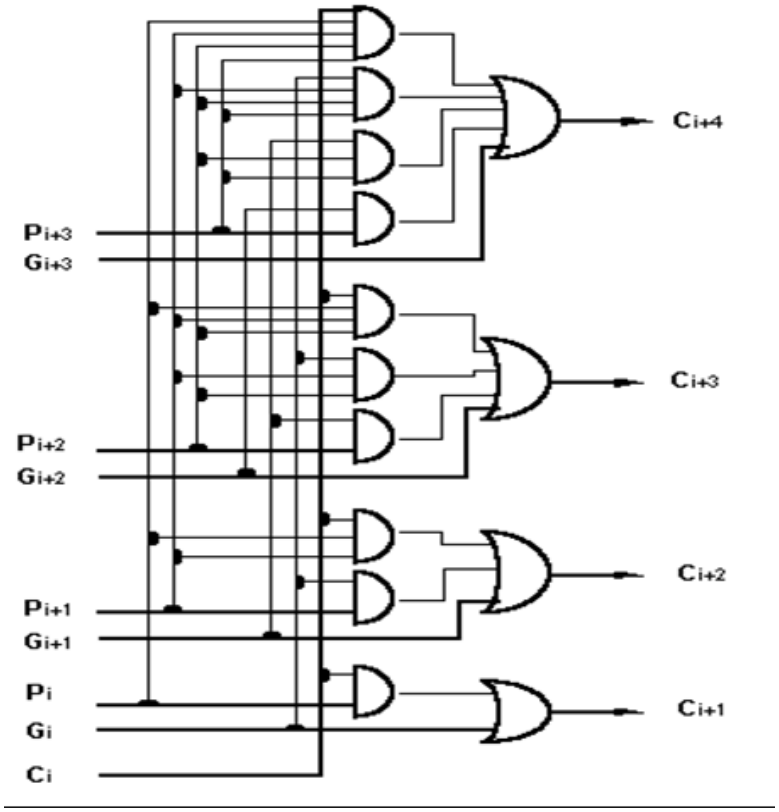
由這兩張圖我們可以發現兩者判斷的 critical path 相同。

(5) 電路分析 ：

觀察 4 bits carry lookahead adder 合成後的電路，如下圖



拿此電路與預期中的電路(下圖)做比較，我們可以發現兩者似乎不太一樣。



由上述結果以及 critical path 分析的結果我們可以得知，合成後電路的結果與預期的結果略有不同。

3. Voting :

(1) Area report 分析 ：

```
****************************************
Report : area
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 11:04:20 2023
****************************************

Information: Updating design information...(UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          198
Number of nets:                           267
Number of cells:                          111
Number of combinational cells:             71
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          2
Number of references:                      18

Combinational area:               600.879589
Buf/Inv area:                       6.789600
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  600.879589
Total area:                 undefined
```

Gate count = 600.979589 / 5 = 120.196

(2) Timing report 分析 ：

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:12:21 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[2] (input port)
  Endpoint: out[2] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[2] (in)                               0.00       0.00 f
  fa4/x (full_adder_8)                     0.00       0.00 f
  fa4/ha1/x (half_adder_16)                0.00       0.00 f
  fa4/ha1/U1/Y (XOR2X1)                    0.14       0.14 f
  fa4/ha1/s (half_adder_16)                0.00       0.14 f
  fa4/ha2/x (half_adder_15)                0.00       0.14 f
  fa4/ha2/U2/Y (AND2X1)                    0.20       0.34 f
  fa4/ha2/c (half_adder_15)                0.00       0.34 f
  fa4/U1/Y (OR2X1)                         0.25       0.60 f
  fa4/c (full_adder_8)                     0.00       0.60 f
  add2/x[1] (adder2_1)                     0.00       0.60 f
  add2/f1/x (full_adder_1)                 0.00       0.60 f
  add2/f1/ha1/x (half_adder_2)             0.00       0.60 f
  add2/f1/ha1/U1/Y (XOR2X1)                0.17       0.76 f
  add2/f1/ha1/s (half_adder_2)             0.00       0.76 f
  add2/f1/ha2/x (half_adder_1)             0.00       0.76 f
  add2/f1/ha2/U2/Y (AND2X1)                0.20       0.97 f
  add2/f1/ha2/c (half_adder_1)             0.00       0.97 f
  add2/f1/U1/Y (OR2X1)                     0.22       1.19 f
  add2/f1/c (full_adder_1)                 0.00       1.19 f
  add2/c (adder2_1)                        0.00       1.19 f
  U22/Y (AO21X1)                           0.27       1.46 f
  U16/Y (NAND2BX1)                         0.16       1.62 f
  out[2] (out)                             0.00       1.62 f
  data arrival time                                   1.62
  -----------------------------------------------------------
  (Path is unconstrained)
```

藍色的部分代表 critical path 所經過的邏輯閘，data arrival time 代表 critical path 的 delay 時間，此電路的 data arrival time 為 1.62 ns。

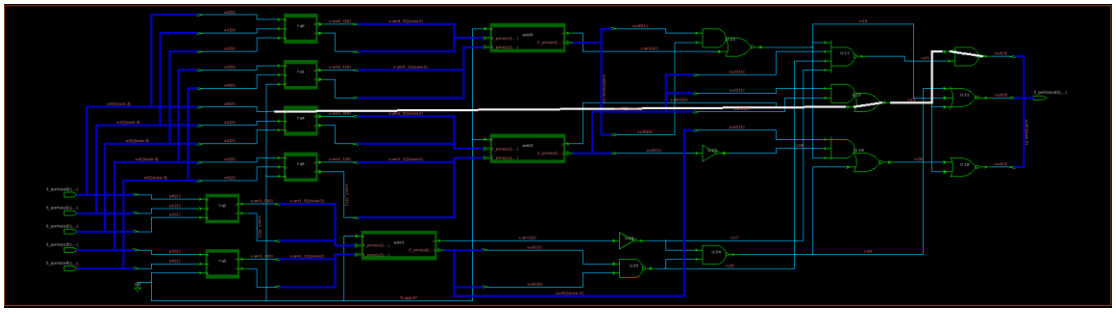
(3) Power report 分析 ：

```
Report : power
        -analysis_effort low
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 11:04:20 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  69.1570 uW   (73%)
  Net Switching Power  =  25.2965 uW   (27%)
                         ---------
Total Dynamic Power    =  94.4534 uW  (100%)

Cell Leakage Power     = 755.5283 nW

Information: report_power power group summary does not include estimated clock tree power(PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.9157e-02        2.5296e-02        7.5553e+05         9.5209e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.9157e-02 mW     2.5296e-02 mW     7.5553e+05 pW      9.5209e-02 mW
```

Total dynamic power 代表訊號在 0 跟 1 之間轉換時所消耗的功率，此電路消耗的功率為 94.4534 uW。

Cell leakage power 代表電路靜止時的漏電，此電路為 755.5283 nW。

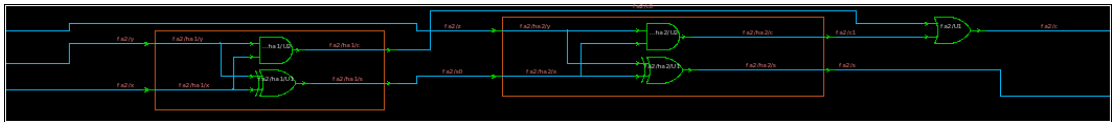
(4) Critical path 分析 ：



上圖為邏輯合成後邏輯合成軟體判斷的 critical path。
第二次作中分析出來的 critical path 為先經過 full adder，在經過二位元家法器，最後進入 if-else loop 來判斷結果。
兩者的 critical path 相同。

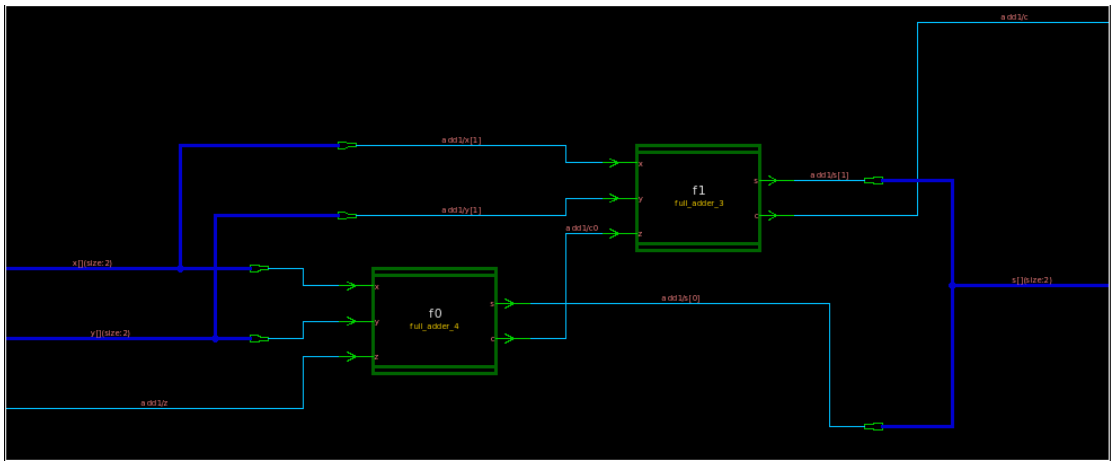
(5) 電路分析 ：

先看合成後的 full adder 電路，如下圖

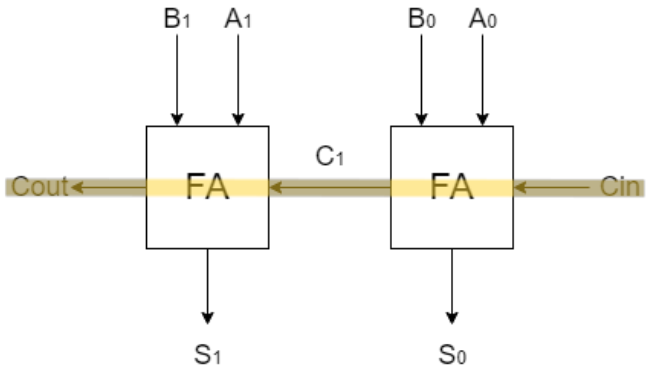


此結果與預期的電路相同

接著看合成後的二位元加法器，如下圖



此結果與第二次作業中自己畫的電路(下圖)相同



由上述結果以及 critical path 分析的結果可以得知，合成後的電路與預期的電路相同。

4. Median :

(1) Area report 分析:

```
****************************************
Report : area
Design : median
Version: P-2019.03
Date   : Sun Apr 16 12:21:14 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           32
Number of nets:                            87
Number of cells:                           63
Number of combinational cells:             63
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         24
Number of references:                      12

Combinational area:               490.548591
Buf/Inv area:                      81.475199
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  490.548591
Total area:                 undefined

***** End Of Report *****
```

Gate count = 490.548591 / 5 = 98.1

(2) Timing report 分析 ：

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : median
Version: P-2019.03
Date   : Sun Apr 16 12:22:27 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[1] (input port)
  Endpoint: out[0] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[1] (in)                               0.00       0.00 f
  U56/Y (CLKINVX1)                         0.05       0.05 r
  U38/Y (NAND2X1)                          0.05       0.10 f
  U36/Y (AOI222XL)                         0.33       0.43 r
  U35/Y (AOI221XL)                         0.10       0.53 f
  U34/Y (AOI221XL)                         0.20       0.74 r
  U33/Y (AOI221XL)                         0.10       0.83 f
  U32/Y (AOI221XL)                         0.20       1.04 r
  U31/Y (OAI22XL)                          0.12       1.16 f
  U30/Y (OA21XL)                           0.21       1.36 f
  U17/Y (XOR2X1)                           0.28       1.64 r
  U16/Y (CLKINVX1)                         0.10       1.75 f
  U14/Y (AOI2BB2X1)                        0.14       1.89 r
  U13/Y (OAI21XL)                          0.06       1.95 f
  out[0] (out)                             0.00       1.95 f
  data arrival time                                   1.95
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

藍色的部分代表 critical path 所經過的邏輯閘，data arrival time 代表 critical path 的 delay 時間，此電路的 data arrival time 為 1.95 ns。

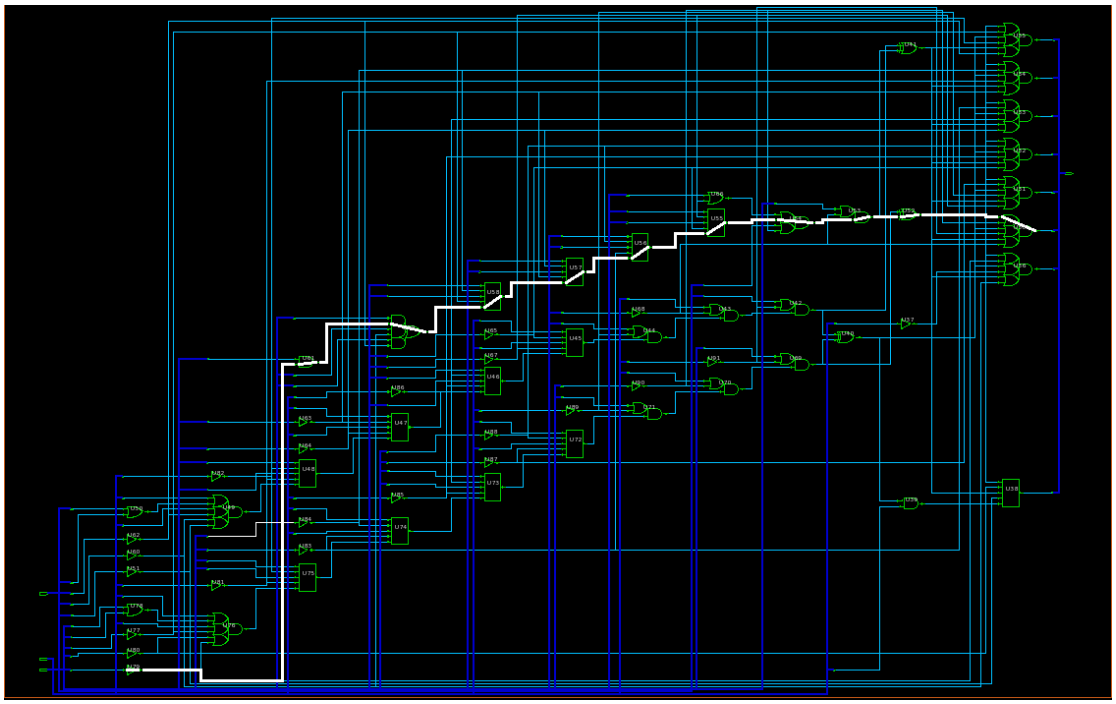
(3) Power report 分析 ：

```
****************************************
Report : power
        -analysis_effort low
Design : median
Version: P-2019.03
Date   : Sun Apr 16 12:23:31 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  32.3743 uW   (60%)
  Net Switching Power  =  21.9078 uW   (40%)
                         ---------
Total Dynamic Power    =  54.2821 uW  (100%)

Cell Leakage Power     = 166.1685 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  3.2374e-02        2.1908e-02        1.6617e+05         5.4448e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          3.2374e-02 mW     2.1908e-02 mW     1.6617e+05 pW      5.4448e-02 mW

***** End Of Report *****
```

Total dynamic power 代表訊號在 0 跟 1 之間轉換時所消耗的功率，此電路消耗的功率為 54.2821 uW。

Cell leakage power 代表電路靜止時的漏電，此電路為 166.1685 nW。

(4) Critical path 分析 ：

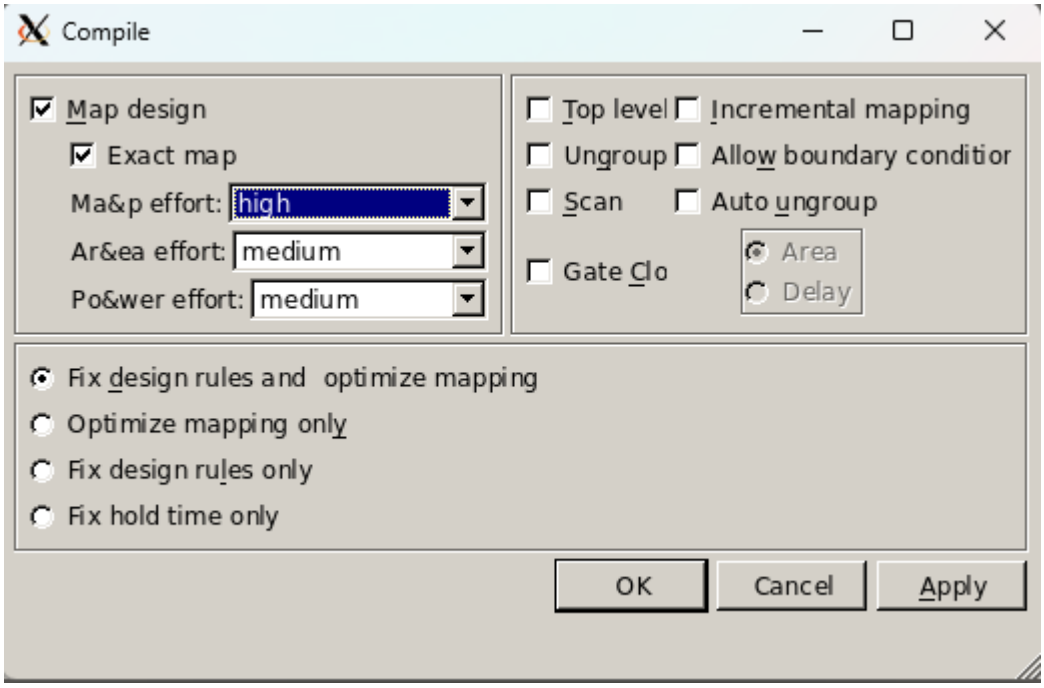


上次作業中分析的 critical path 為經過比較器產生 flag 訊號，接著經過一個大的 mux 來選擇輸出。

三、 進階指令 ：

1. Voting :

(1) 嘗試將 Map effort 調至 high



- Area report :

```
****************************************
Report : area
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:48:59 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          198
Number of nets:                           267
Number of cells:                          111
Number of combinational cells:             71
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          2
Number of references:                      18

Combinational area:               600.879589
Buf/Inv area:                       6.789600
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  600.879589
Total area:                 undefined

***** End Of Report *****
```

Gate count = 600.879589 / 5 = 120.176

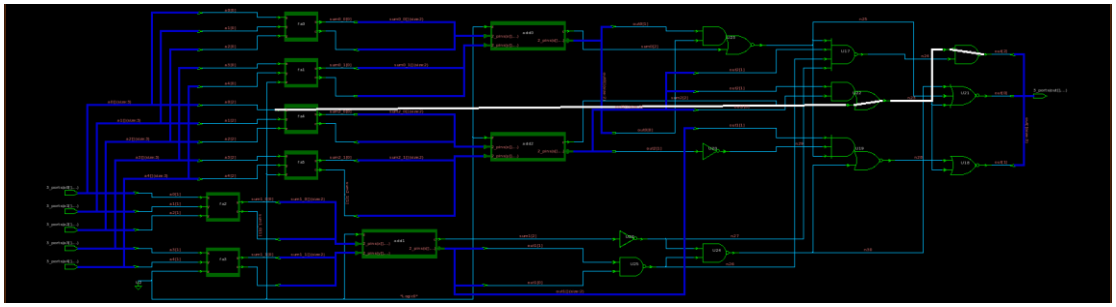
- Timing report :

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:51:15 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[2] (input port)
  Endpoint: out[2] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[2] (in)                               0.00       0.00 f
  fa4/x (full_adder_8)                     0.00       0.00 f
  fa4/ha1/x (half_adder_16)                0.00       0.00 f
  fa4/ha1/U1/Y (XOR2X1)                    0.14       0.14 f
  fa4/ha1/s (half_adder_16)                0.00       0.14 f
  fa4/ha2/x (half_adder_15)                0.00       0.14 f
  fa4/ha2/U2/Y (AND2X1)                    0.20       0.34 f
  fa4/ha2/c (half_adder_15)                0.00       0.34 f
  fa4/U1/Y (OR2X1)                         0.25       0.60 f
  fa4/c (full_adder_8)                     0.00       0.60 f
  add2/x[1] (adder2_1)                     0.00       0.60 f
  add2/f1/x (full_adder_1)                 0.00       0.60 f
  add2/f1/ha1/x (half_adder_2)             0.00       0.60 f
  add2/f1/ha1/U1/Y (XOR2X1)                0.17       0.76 f
  add2/f1/ha1/s (half_adder_2)             0.00       0.76 f
  add2/f1/ha2/x (half_adder_1)             0.00       0.76 f
  add2/f1/ha2/U2/Y (AND2X1)                0.20       0.97 f
  add2/f1/ha2/c (half_adder_1)             0.00       0.97 f
  add2/f1/U1/Y (OR2X1)                     0.22       1.19 f
  add2/f1/c (full_adder_1)                 0.00       1.19 f
  add2/c (adder2_1)                        0.00       1.19 f
  U22/Y (AO21X1)                           0.27       1.46 f
  U16/Y (NAND2BX1)                         0.16       1.62 f
  out[2] (out)                             0.00       1.62 f
  data arrival time                                   1.62
  -----------------------------------------------------------
  (Path is unconstrained)
```

- Power report :

```
****************************************
Report : power
         -analysis_effort low
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:52:12 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  69.1570 uW   (73%)
  Net Switching Power  =  25.2965 uW   (27%)
                         ---------
Total Dynamic Power    =  94.4534 uW  (100%)

Cell Leakage Power     = 755.5283 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.9157e-02        2.5296e-02        7.5553e+05         9.5209e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.9157e-02 mW     2.5296e-02 mW     7.5553e+05 pW      9.5209e-02 mW

***** End Of Report *****
```

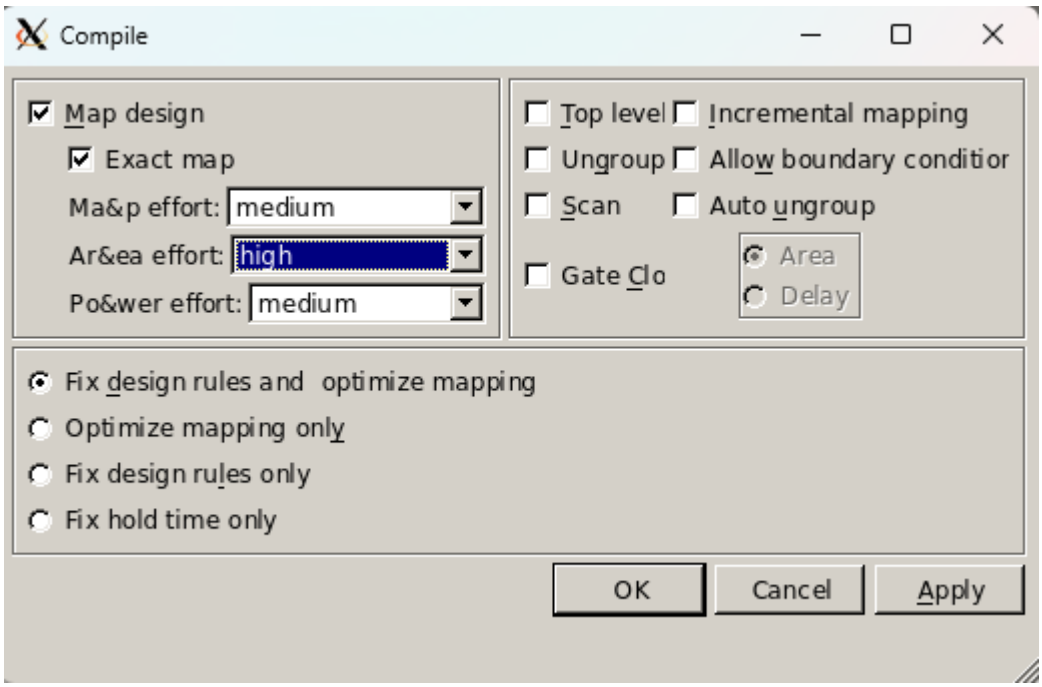
- Critical path :



- 比較 :

  改變 Map effort 後的結果與先前相同。

(2) 嘗試將 Area effort 調至 High



- Area report :

```
****************************************
Report : area
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:58:13 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          198
Number of nets:                           267
Number of cells:                          111
Number of combinational cells:             71
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          2
Number of references:                      18

Combinational area:               600.879589
Buf/Inv area:                       6.789600
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  600.879589
Total area:                 undefined

***** End Of Report *****
```

Gate count = 600.879589 / 5 = 120.176

- Timing report :

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:59:27 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[2] (input port)
  Endpoint: out[2] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[2] (in)                               0.00       0.00 f
  fa4/x (full_adder_8)                     0.00       0.00 f
  fa4/ha1/x (half_adder_16)                0.00       0.00 f
  fa4/ha1/U1/Y (XOR2X1)                    0.14       0.14 f
  fa4/ha1/s (half_adder_16)                0.00       0.14 f
  fa4/ha2/x (half_adder_15)                0.00       0.14 f
  fa4/ha2/U2/Y (AND2X1)                    0.20       0.34 f
  fa4/ha2/c (half_adder_15)                0.00       0.34 f
  fa4/U1/Y (OR2X1)                         0.25       0.60 f
  fa4/c (full_adder_8)                     0.00       0.60 f
  add2/x[1] (adder2_1)                     0.00       0.60 f
  add2/f1/x (full_adder_1)                 0.00       0.60 f
  add2/f1/ha1/x (half_adder_2)             0.00       0.60 f
  add2/f1/ha1/U1/Y (XOR2X1)                0.17       0.76 f
  add2/f1/ha1/s (half_adder_2)             0.00       0.76 f
  add2/f1/ha2/x (half_adder_1)             0.00       0.76 f
  add2/f1/ha2/U2/Y (AND2X1)                0.20       0.97 f
  add2/f1/ha2/c (half_adder_1)             0.00       0.97 f
  add2/f1/U1/Y (OR2X1)                     0.22       1.19 f
  add2/f1/c (full_adder_1)                 0.00       1.19 f
  add2/c (adder2_1)                        0.00       1.19 f
  U22/Y (AO21X1)                           0.27       1.46 f
  U16/Y (NAND2BX1)                         0.16       1.62 f
  out[2] (out)                             0.00       1.62 f
  data arrival time                                   1.62
  -----------------------------------------------------------
  (Path is unconstrained)
```

- Power report :

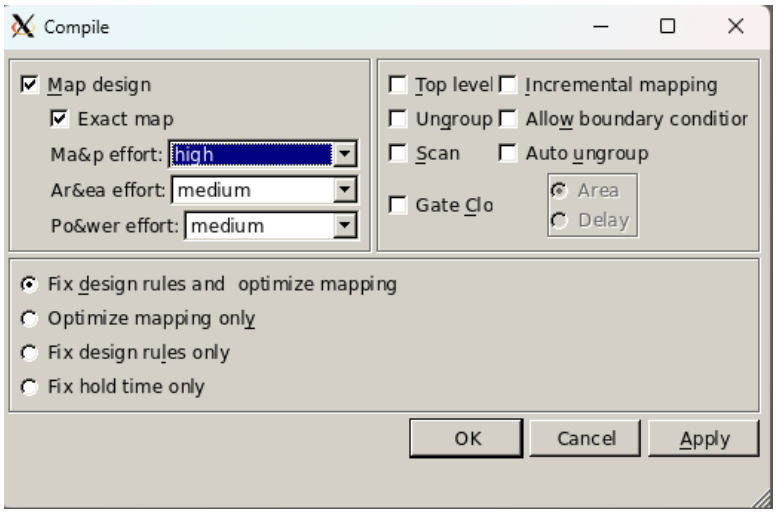
```
****************************************
Report : power
        -analysis_effort low
Design : voting
Version: P-2019.03
Date   : Sun Apr 16 14:59:52 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  69.1570 uW   (73%)
  Net Switching Power  =  25.2965 uW   (27%)
                         ---------
Total Dynamic Power    =  94.4534 uW  (100%)

Cell Leakage Power     = 755.5283 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  6.9157e-02        2.5296e-02        7.5553e+05         9.5209e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          6.9157e-02 mW     2.5296e-02 mW     7.5553e+05 pW      9.5209e-02 mW

***** End Of Report *****
```

- 比較 ：

  將 Area effort 改成 high 後的結果與先前的相同。

2. Median :

(1) 嘗試將 Map effort 調至 high



- Area report :

```
****************************************
Report : area
Design : median
Version: P-2019.03
Date   : Sun Apr 16 15:28:18 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           32
Number of nets:                            86
Number of cells:                           62
Number of combinational cells:             62
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         23
Number of references:                      13

Combinational area:               488.851191
Buf/Inv area:                      78.080399
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  488.851191
Total area:                 undefined

***** End Of Report *****
```

Gate count = 488.851191 / 5 = 97.77

- Timing report :

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : median
Version: P-2019.03
Date   : Sun Apr 16 15:29:31 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[1] (input port)
  Endpoint: out[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[1] (in)                               0.00       0.00 f
  U79/Y (CLKINVX1)                         0.05       0.05 r
  U61/Y (NAND2X1)                          0.05       0.10 f
  U59/Y (AOI222XL)                         0.33       0.43 r
  U58/Y (AOI221XL)                         0.10       0.53 f
  U57/Y (AOI221XL)                         0.20       0.74 r
  U56/Y (AOI221XL)                         0.10       0.83 f
  U55/Y (AOI221XL)                         0.20       1.04 r
  U54/Y (OAI22XL)                          0.12       1.16 f
  U53/Y (OA21XL)                           0.21       1.36 f
  U52/Y (XOR2X1)                           0.25       1.61 f
  U30/Y (OAI222XL)                         0.29       1.90 r
  out[7] (out)                             0.00       1.90 r
  data arrival time                                   1.90
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

- Power report :

```
****************************************
Report : power
        -analysis_effort low
Design : median
Version: P-2019.03
Date   : Sun Apr 16 15:32:01 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  31.7243 uW   (60%)
  Net Switching Power  =  21.3499 uW   (40%)
                         ---------
Total Dynamic Power    =  53.0743 uW  (100%)

Cell Leakage Power     = 160.9021 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           0.0000           0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational  3.1724e-02        2.1350e-02        1.6090e+05        5.3235e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          3.1724e-02 mW     2.1350e-02 mW     1.6090e+05 pW     5.3235e-02 mW

***** End Of Report *****
```

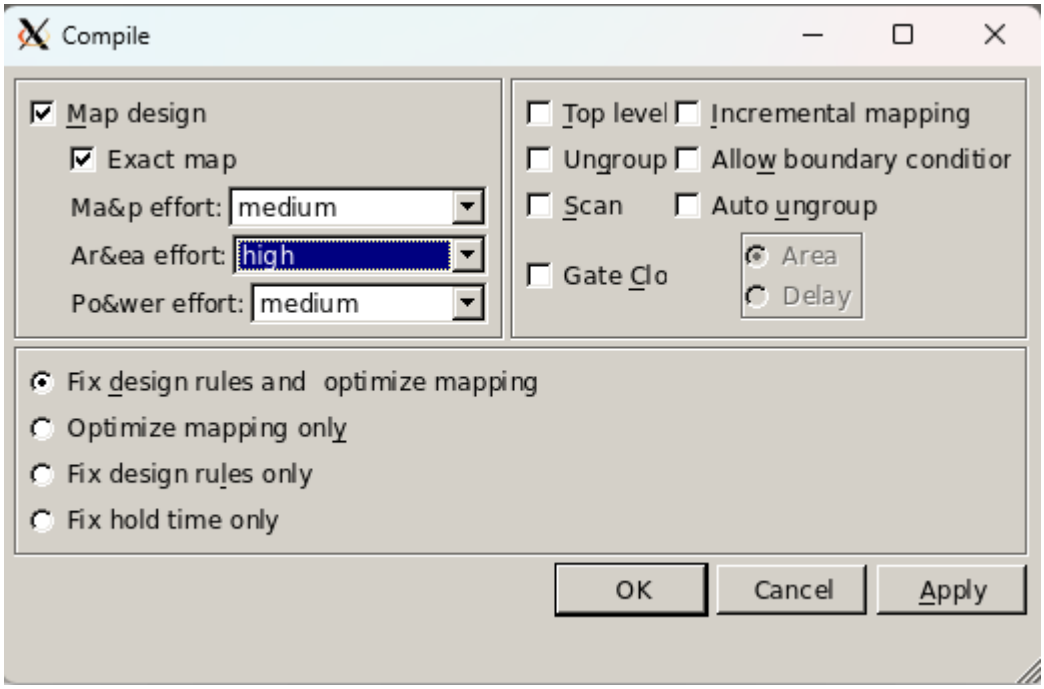
- 比較 :

  先看 area report 的數據，在調整 Map effort 之前，面積為 490.548591 um × um (gate count = 98.1)；調整 Map effort 之後，面積變成 488.851191 um × um (gate count = 97.77)。調整後面積有變小一點。

  再來比較 timing report 的數據，在調整 Map effort 之前。delay 為 1.95 ns；調整後 delay 變成 1.9 ns。調整後 delay 有縮短一點。

  最後比較功率消耗，在調整 Map effort 之前，Total dynamic power 為 54.2821 uW，Cell leakage power 為 166.1685 nW；調整後 total dynamic power 變成 53.0743 uW，cell leakage power 變成 160.9021 nW。total dynamic power 和 cell leakage power 都有變小一點。

(2) 嘗試將 Area effort 調至 High



- Area report :

```
****************************************
Report : area
Design : median
Version: P-2019.03
Date   : Sun Apr 16 15:45:59 2023
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                           32
Number of nets:                            86
Number of cells:                           62
Number of combinational cells:             62
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         23
Number of references:                      13

Combinational area:               488.851191
Buf/Inv area:                      78.080399
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  488.851191
Total area:                 undefined

***** End Of Report *****
```

Gate count = 488.851191 / 5 = 97.77

- Timing report :

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : median
Version: P-2019.03
Date   : Sun Apr 16 15:47:13 2023
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: a0[1] (input port)
  Endpoint: out[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  a0[1] (in)                               0.00       0.00 f
  U79/Y (CLKINVX1)                         0.05       0.05 r
  U61/Y (NAND2X1)                          0.05       0.10 f
  U59/Y (AOI222XL)                         0.33       0.43 r
  U58/Y (AOI221XL)                         0.10       0.53 f
  U57/Y (AOI221XL)                         0.20       0.74 r
  U56/Y (AOI221XL)                         0.10       0.83 f
  U55/Y (AOI221XL)                         0.20       1.04 r
  U54/Y (OAI22XL)                          0.12       1.16 f
  U53/Y (OA21XL)                           0.21       1.36 f
  U52/Y (XOR2X1)                           0.25       1.61 f
  U30/Y (OAI222XL)                         0.29       1.90 r
  out[7] (out)                             0.00       1.90 r
  data arrival time                                   1.90
  -----------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

- Power report :

```
****************************************
Report : power
        -analysis_effort low
Design : median
Version: P-2019.03
Date   : Sun Apr 16 15:47:47 2023
****************************************


Library(s) Used:

    slow (File: /mnt3/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  31.7243 uW   (60%)
  Net Switching Power  =  21.3499 uW   (40%)
                         ---------
Total Dynamic Power    =  53.0743 uW  (100%)

Cell Leakage Power     = 160.9021 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational  3.1724e-02        2.1350e-02        1.6090e+05         5.3235e-02  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total          3.1724e-02 mW     2.1350e-02 mW     1.6090e+05 pW      5.3235e-02 mW

***** End Of Report *****
```

- 比較：

  先看 area report 的數據，在調整 Map effort 之前，面積為 490.548591 um × um (gate count = 98.1)；調整 Map effort 之後，面積變成 488.851191 um × um (gate count = 97.77)。調整後面積有變小一點。

  再來比較 timing report 的數據，在調整 Map effort 之前。delay 為 1.95 ns；調整後 delay 變成 1.9 ns。調整後 delay 有縮短一點。

  最後比較功率消耗，在調整 Map effort 之前，Total dynamic power 為 54.2821 uW，Cell leakage power 為 166.1685 nW；調整後 total dynamic power 變成 53.0743 uW，cell leakage power 變成 160.9021 nW。total dynamic power 和 cell leakage power 都有變小一點。

四、 問題討論：

1. 照理來說 Ripple carry adder 的面積要比 carry lookahead adder 的小，但結果卻相反。我認為會有這樣的狀況是因為當初寫 code 的時候，carry lookahead adder 有用到五個 input 的 OR gate，但是合成後的電路中似乎找不到這麼多 input 的 OR gate，也許是因為合成軟體將這個 OR gate 利用其他方式表現才造成面積比預期的結果小。

2. 調整 map effort 和 area effort 可以讓軟體在進行邏輯合成時花較多的時間在優化速度和面積上。由這次作業的嘗試可以發現，有些時候調整 map effort 和 area effort 確實能讓電路效能提升，但是提升的幅度不大，所以如果希望能夠提升電路效能，最好的辦法還是對電路架構進行調整。
3. 在面積分析時，計算 gate count 的方式為面積除以 NAND gate 的面積，要計算 gate count 而不是直接比較面積的原因為面積的大小會受到製程技術的影響，直接拿來比較不能公平的比較出電路架構的好壞，所以才會選擇使用 gate count 來比較電路在面積上的表現。
4. 為甚麼要做邏輯合成?
   邏輯合成可以讓我們看到自己的 RTL code 變成電路後長怎樣以及合成後是否能正常運作，從中我們也能檢視自己的 coding style 的好壞。除此之外，透過邏輯合成後的各項數據，像是 area report、timing report 等，我們更好分析設計出來的電路的效能是否符合預期，也能夠更好的從中找到自己電路該如何去優化。

五、 心得：

這次作業主要是練習如何正確使用邏輯合成軟體還有透過與同班同學比較的方式來檢視自己的學習狀況以及還能進步的地方。將之前設計的電路做完邏輯合成後，看到自己設計的電路的樣子還蠻有成就感的，也透過分析各項數據來觀察自己電路的效能以及自己的 coding style 是否有足夠的硬體導向。透過這次的作業我發現到自己在 coding 時忽略掉的事情，像是邏輯閘 fan_in 的限制，未來遇到太多輸入的邏輯閘時就要注意是不是要用其他方式來呈現這樣的效果，否則合成後結果會跟預期的不同。