Quiz 1

1. Question on Amdahl's Law
2. Explain buffer overflow vulnerability
3. Explain the stages in a compilation system
4. Question involving two's complement multiplication

Midsem

1. Name 2 AMD processors
2. Address space vs memory space and which is bigger
3. What is the displacement addressing mode

Quiz 2

2) Answer the following.
   a) What is a programmer visible state? (**1.5 marks**)
   b) Please list what constitutes the programmer visible state for a Y86-64 program. (**3.5 marks**)

4) Please answer the following.
   (a) What is a control hazard? (**1 marks**)
   (b) Briefly explain how you will solve the two control hazards in a 5-stage pipeline architecture. (**4 marks**)

5) For a 5-stage pipeline consisting of fetch, decode, execute, memory and writeback stages, please answer the following.
   (a) What is the issue encountered with the following instructions? (**2.5 marks**)

```
mrmovq (%rdx),%rbx
addq %rcx,%rbx
```

   (b) What will happen to the above issue if you change the pipeline architecture to consist of only 4 stages – fetch, decode, execute+memory, writeback? Please explain briefly. (**2.5 marks**)

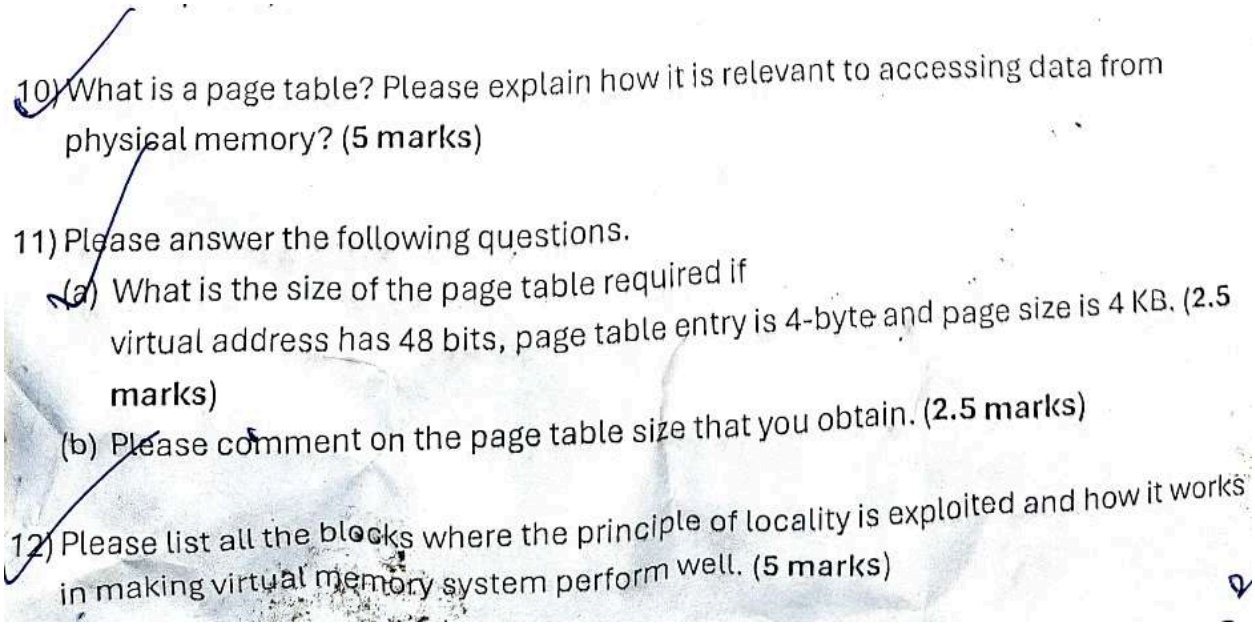
3) A large program with 6 million instructions needs to be executed in a processor with frequency of 2 GHz.
a) If the first 30% of the instructions run in 3 clock cycles, the second 30% instructions run in 5 clock cycles and the remaining 40% instructions run in 8 clock cycles, what is the execution time of the program? (**2.5 marks**)
b) If in the above scenario 3(a), the first 40% of the instruction executions can be optimized to execute in 2 clock cycles, what is the change in the execution time of the program? (**2.5 marks**)

6) Please explain how the push and pop instructions work by describing what actions are taken in each of the 5 stages in the pipelined architecture. (**5 marks**)

7) Suppose there is a processor architecture with an arbitrary number of pipeline stages n and each pipeline stage has a delay of 400/n, please answer the following. (Assume the pipeline register delay is 30 ps)
(a) What is the latency and throughput of the system in terms of n? (**2 marks**)
(b) What is the limit on throughput that can be achieved with increase in pipeline stages? (**3 marks**)

Endsem

1. Write an assembly program in X86 to compute factorial of a number (same question as lab exam)

2. 

3. Explain the 4 types of flags
4. Name the callee-saved registers and examine a code block to determine which callee-saved registers are being used (and why are callee-saved registers required)
5. What is a cache miss and types of cache misses
6. Question involving calculation of number of tag bits, set bits, and offset bits
7. Looking at an inefficient code for matrix multiplication (ie. one that doesn't take advantage of locality), explaining why its inefficient and rewriting the code in the most efficient possible manner
8. Conditions (in terms of flags) for certain setx instructions to be executed (look at slide 13 on the Machine Control ppt)