CMOS II

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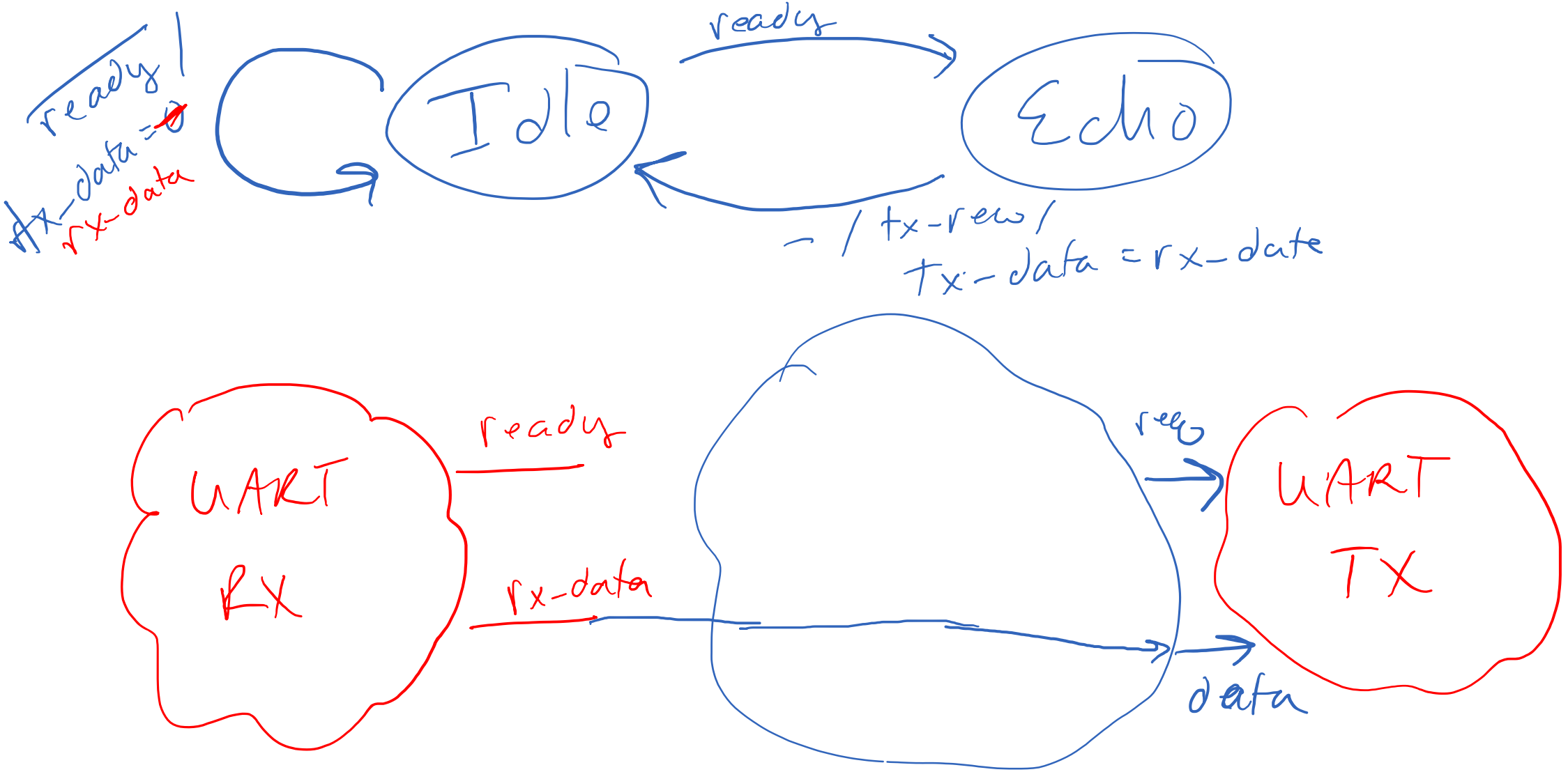

ready
Idle
ready
Echo
ready /
tx_data = 0
rx_data
- / tx_req /
tx_data = rx_data
UART
RX
ready
rx_data
req
UART
TX
data

Calculator.py

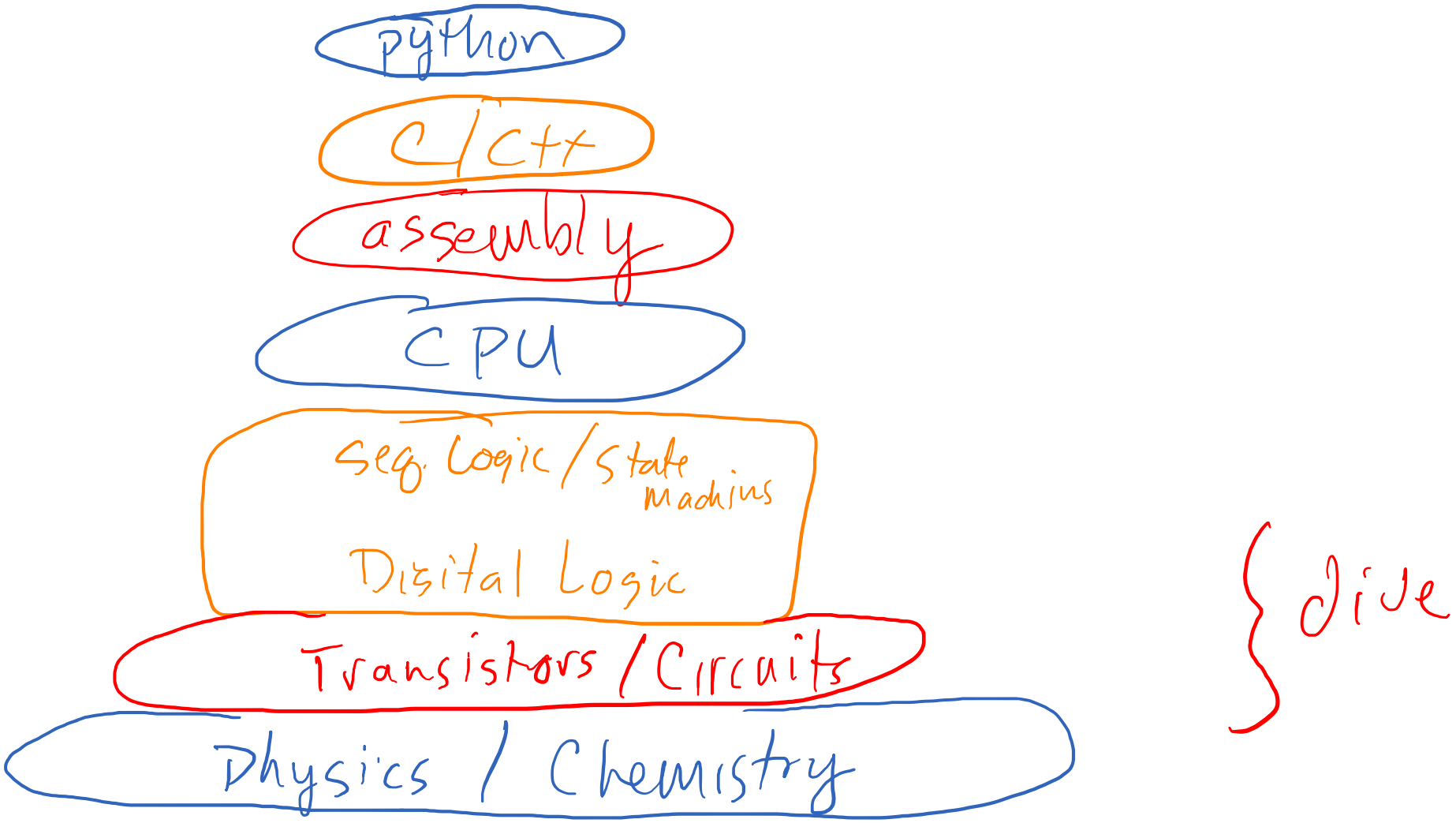
- Lets you interact with the FPGA via the keyboard
  - Translates ASCII <--> Binary for you

```
$ python3 calculator.py –s /dev/ttyUSB1

$ python3 calculator.py –-help
```

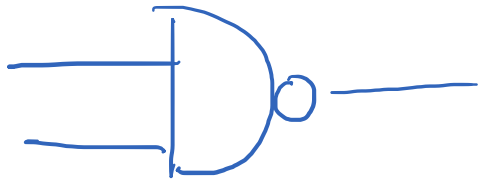
python3 (not “python”)

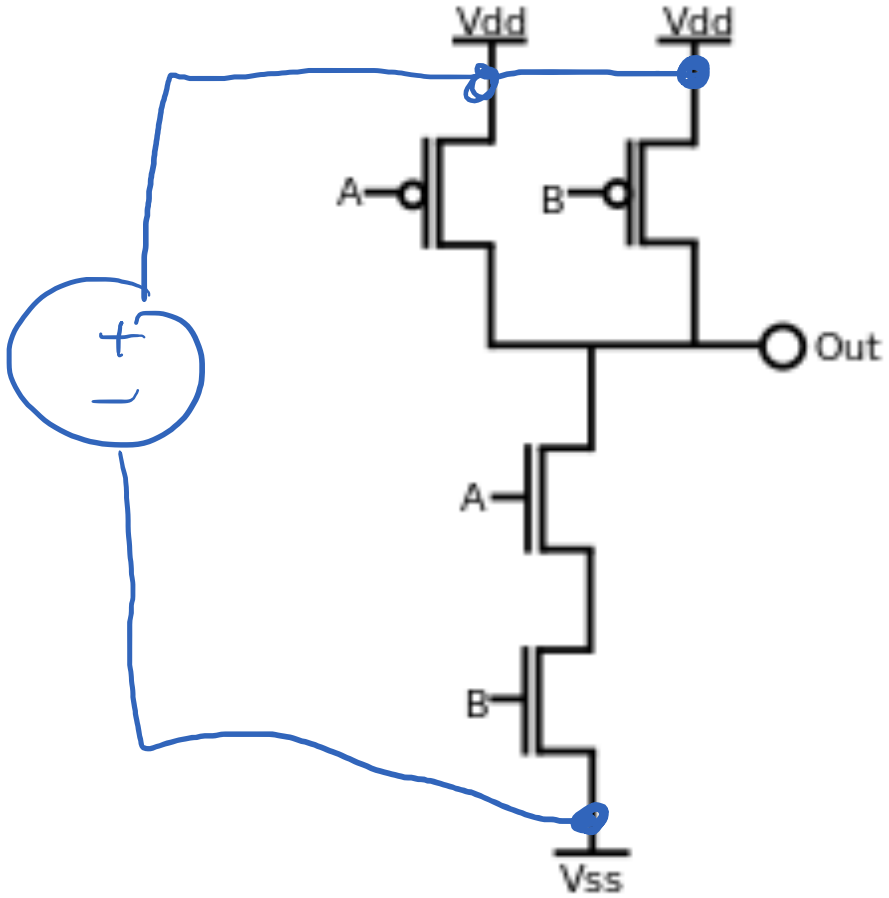
Review: The Compute Stack



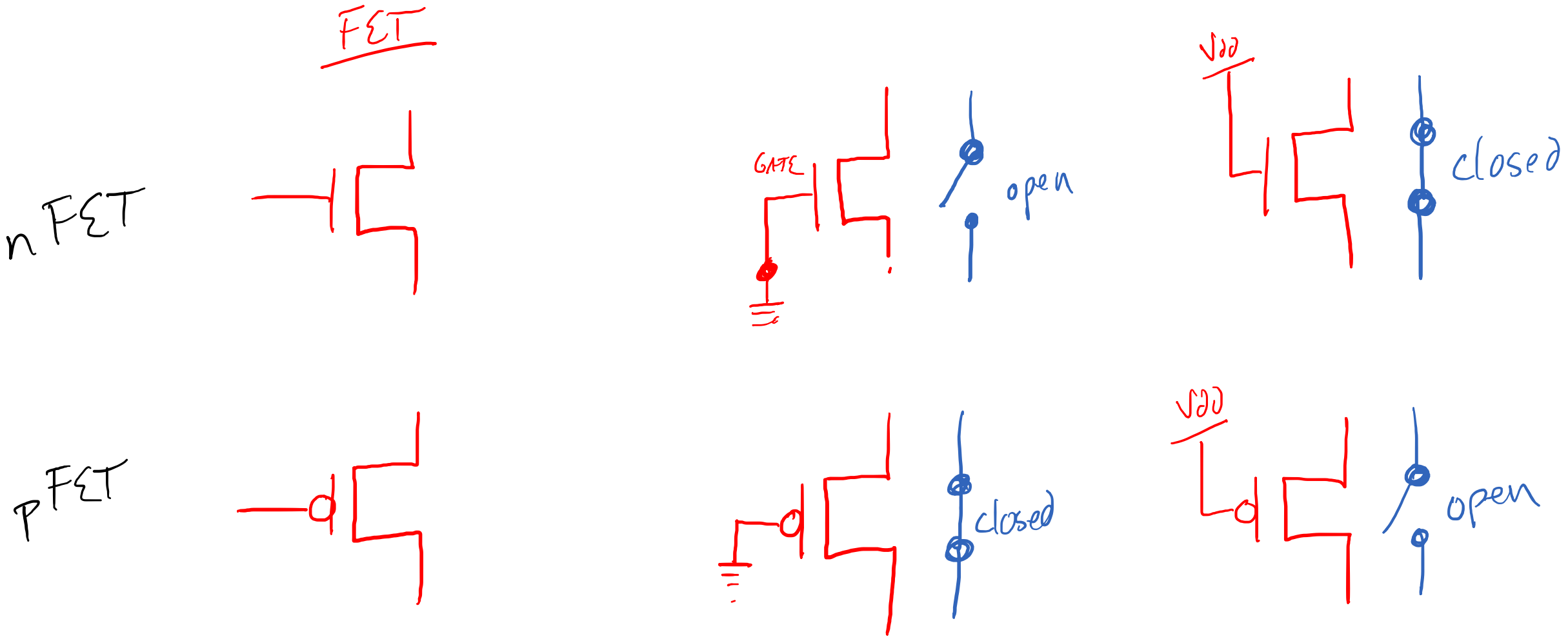
Review: All logic is NAND

- It’s not magic, it’s an electronic circuit

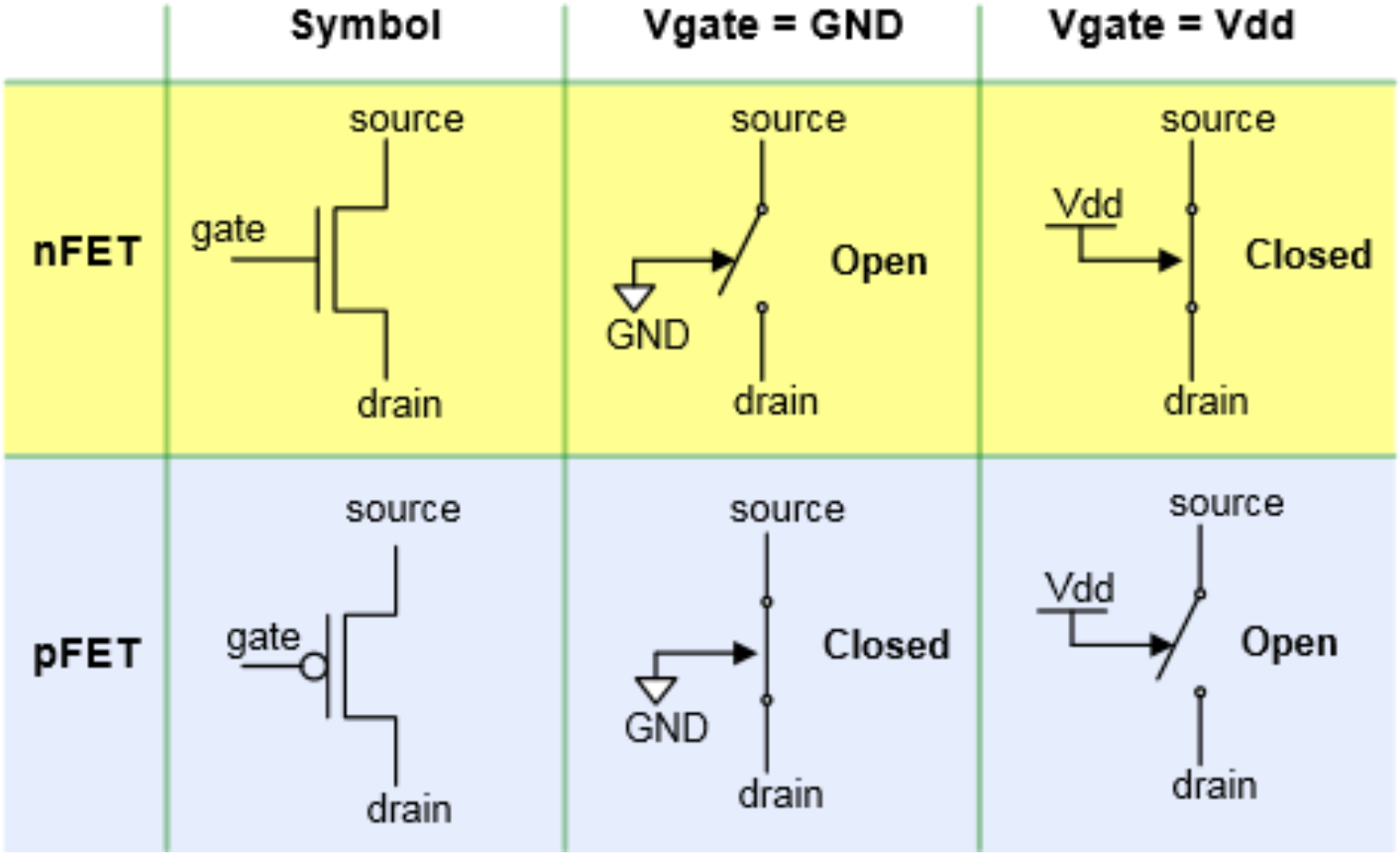




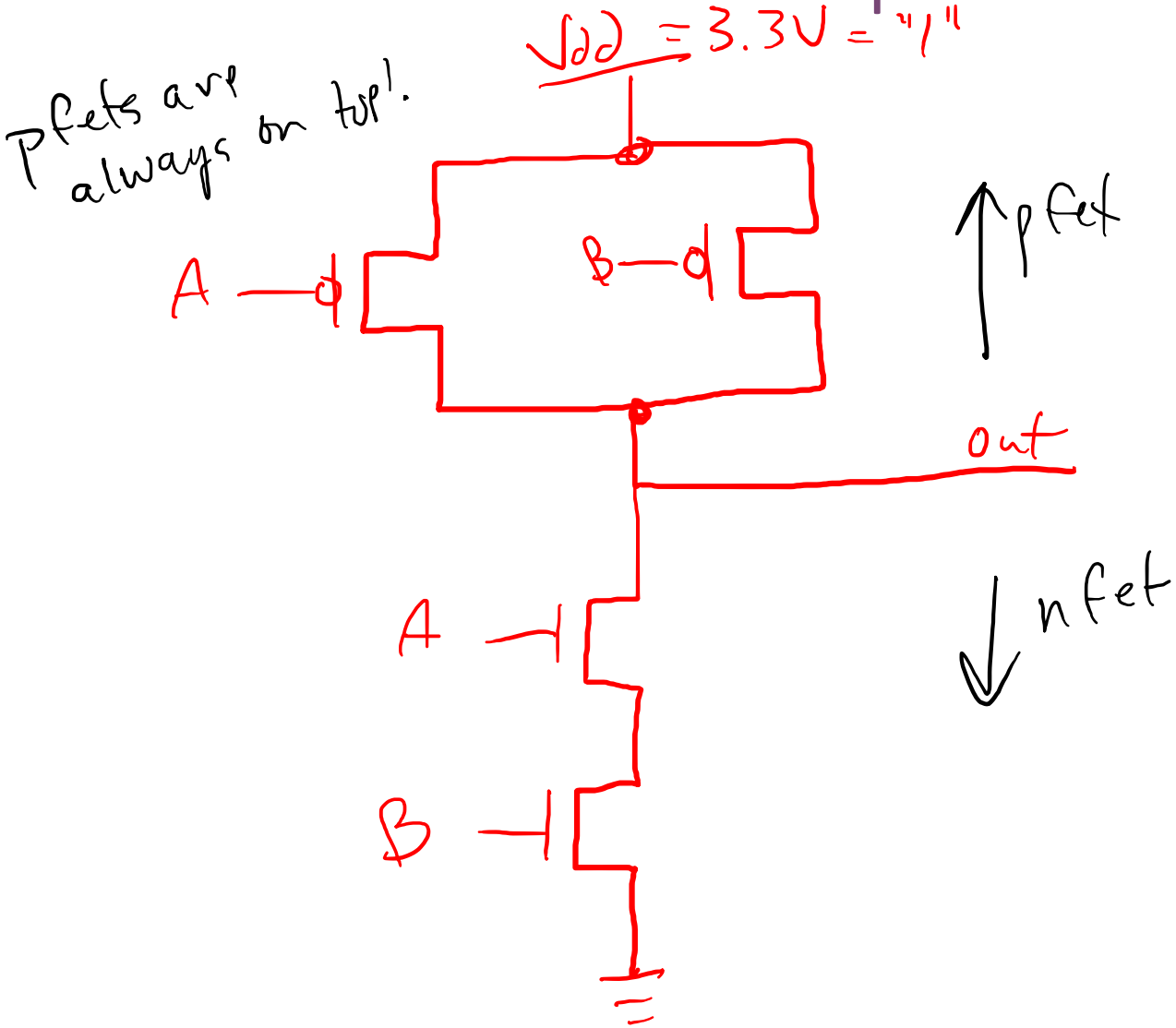
MOSFETS


FET
GND
(3.3V)
Vdd
nFET
GATE
open
Vdd
closed
pFET
closed
Vdd
open

MOSFETS


Symbol
Vgate = GND
Vgate = Vdd
nFET
source
gate
drain
source
GND
Open
drain
source
Vdd
Closed
drain
pFET
source
gate
drain
source
GND
Closed
drain
source
Vdd
Open
drain

NAND with Complimentary MOS (CMOS)



nMos

0 => open

1 => closed

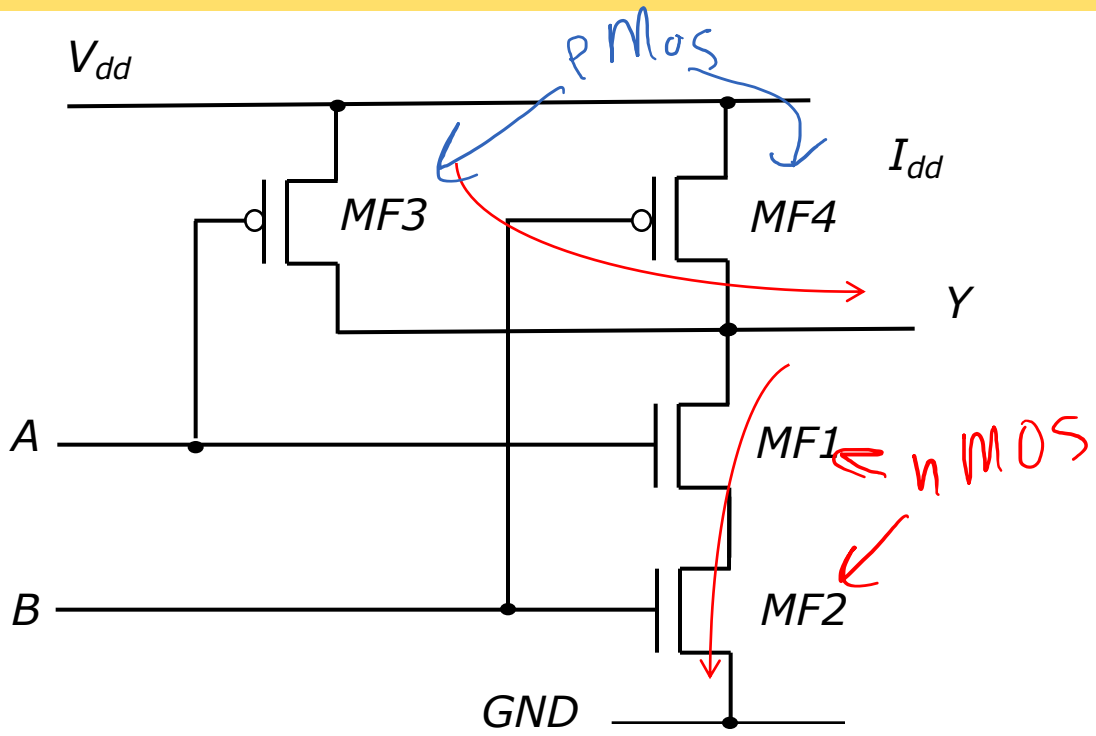
pMos

0 => closed

1 => open

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NAND Gate



Both nFET and pFET transistors are used to implement the gate.

Advantage: no current from V_{dd} to GND in either state, thus extremely low power dissipation.

A	B	MF1	MF2	MF3	MF4	I	Y
LV	LV	off	off	on	on	0	HV
LV	HV	off	on	on	off	0	HV
HV	LV	on	off	off	on	0	HV
HV	HV	on	on	off	off	0	LV

CMOS Power Dissipation

Because there is no current in either state, the CMOS gates have extremely low power dissipation.

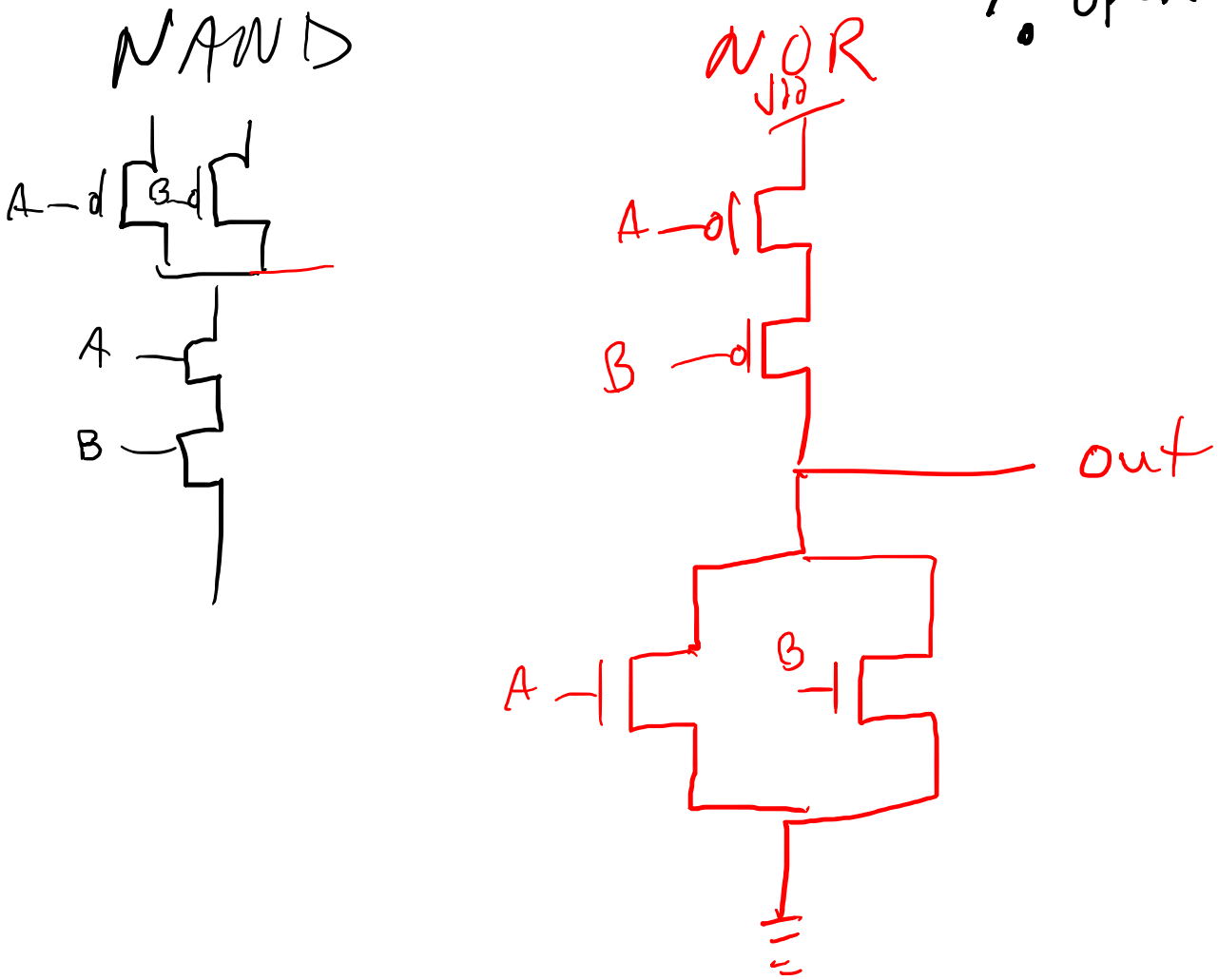
Dissipation is due to following effects:

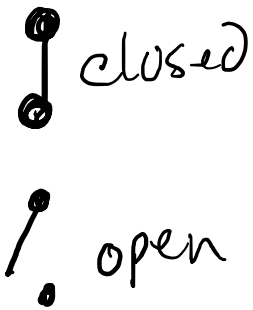
- When the output switches from one logic level to another, there is a short period of time when all output transistors are ON, and the current flows from V_{dd} to GND.

- Gates have some parasitic capacitance, and during the switching of output from one voltage level to another, the output has to charge and discharge gates that are connected to the output.

As the working frequency of CMOS gates increase, so will the power dissipation.

CMOS NOR Gate

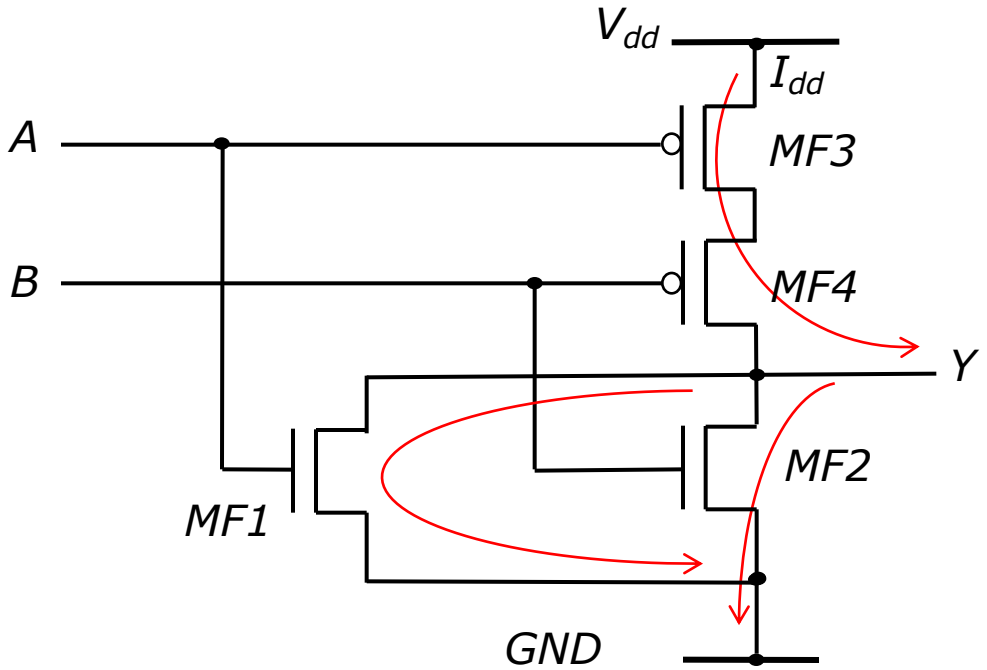




	NFET	P Fet
1	close	open
0	open	closed

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

CMOS NOR Gate

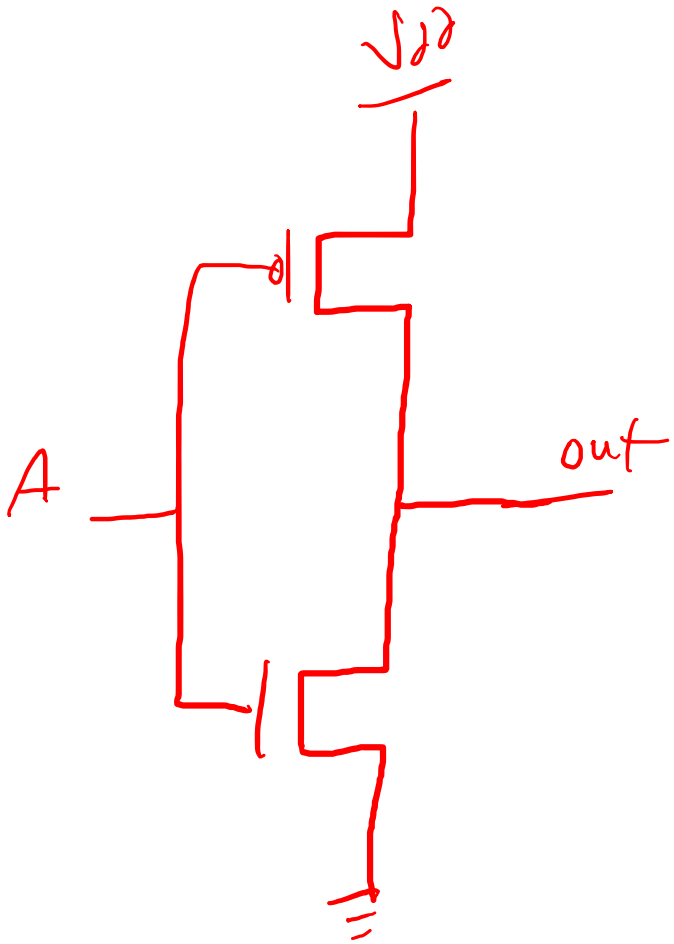


Both *nFET* and *pFET* transistors are used to implement the gate.

Advantage: no current from V_{dd} to *GND* in either state, thus extremely low power dissipation.

A	B	MF1	MF2	MF3	MF4	I	Y
LV 0	LV 0	off	off	on	on	0	HV 1
LV	HV	off	on	on	off	0	LV
HV	LV	on	off	off	on	0	LV
HV	HV	on	on	off	off	0	LV

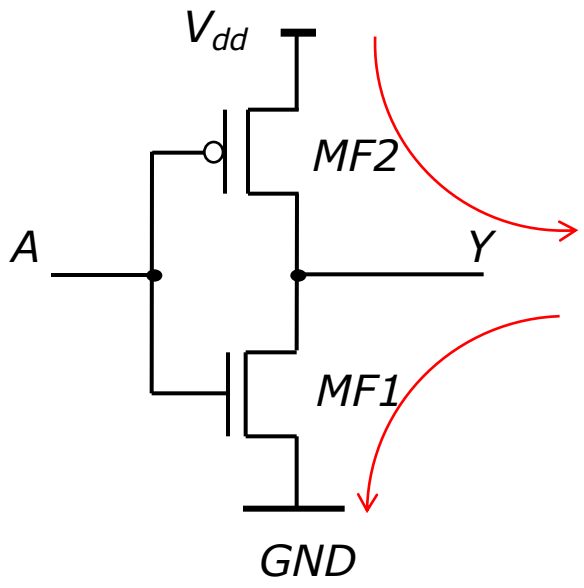
CMOS NOT



	Nmos	Pmos
1	closed	open
0	open	closed

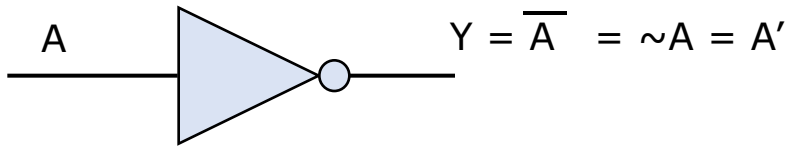
A	Out
0	1
1	0

CMOS inverter:

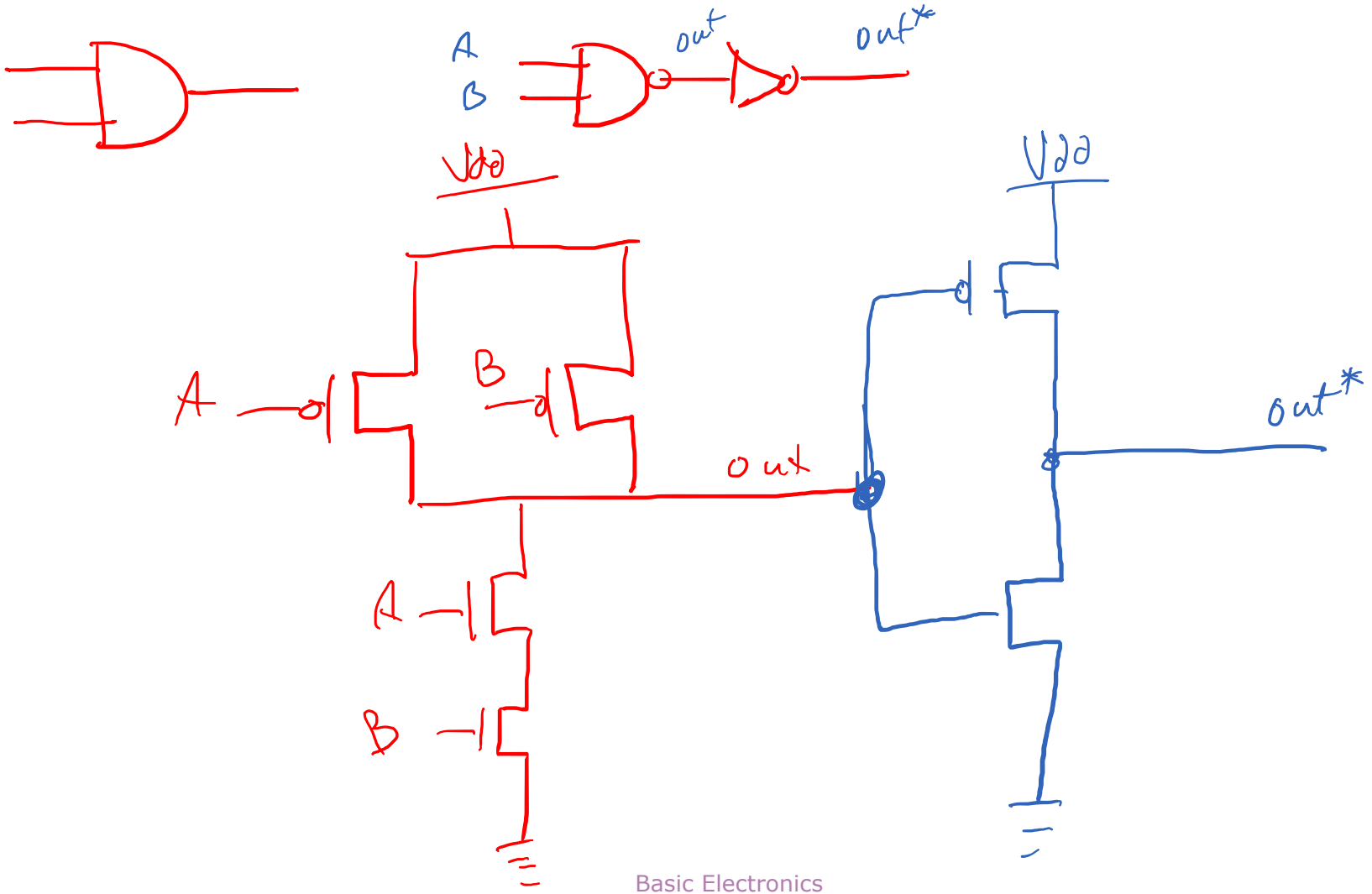


A	MF1	MF2	I_{dd}	Y
LV	off	on	0	HV
HV	on	off	0	LV

A	Y
0	1
1	0



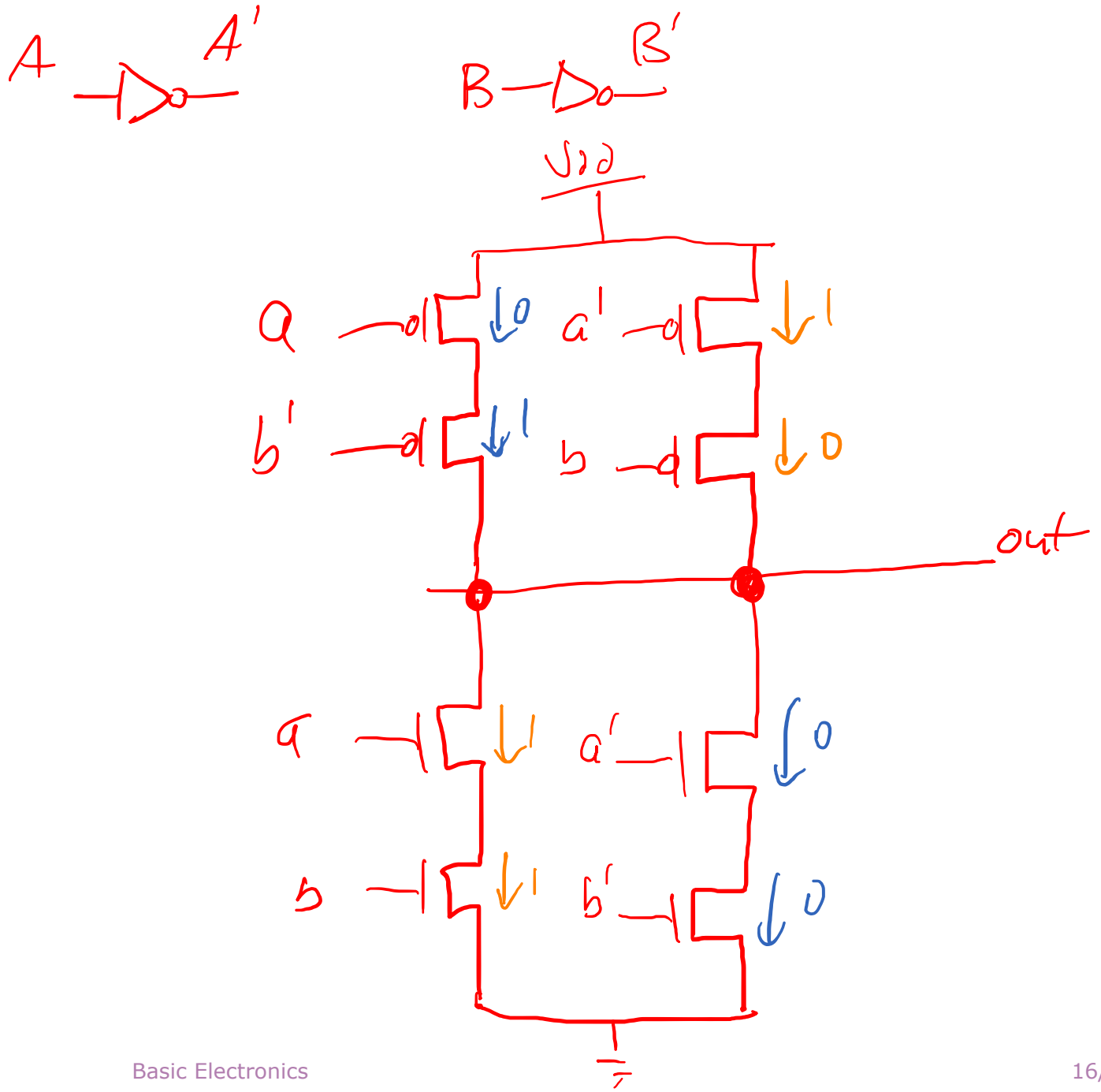
CMOS AND?



CMOS XOR?

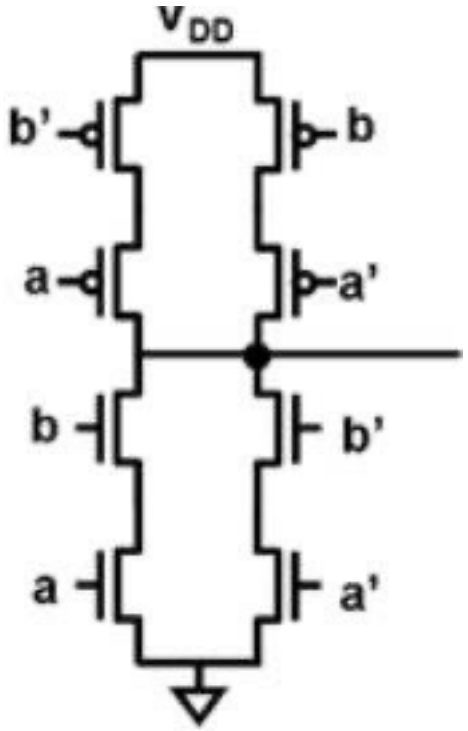
A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

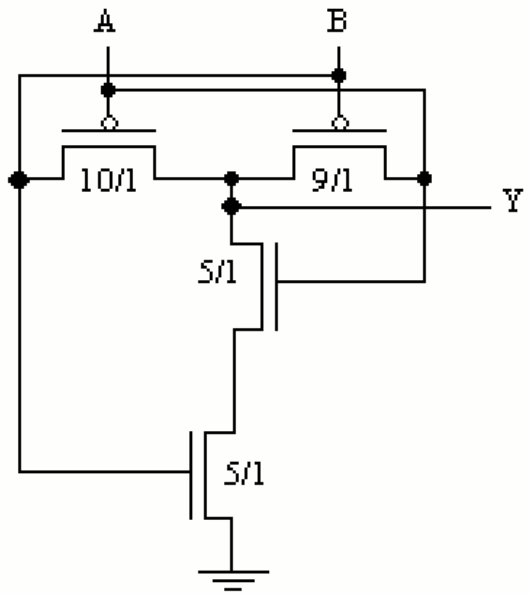
	N	P
0	open	closed
1	closed	open



CMOS XOR?

(NOT ON EXAM)





How a MOSFET works

- Yea, I'm not going to pretend I'm better than this guy…
- https://www.youtube.com/watch?v=IcrBqCFLHIY

Closer to physical reality:

- https://www.youtube.com/watch?v=tz62t-q_KEc
- @0.45

- Add FinFETs
- https://www.youtube.com/watch?v=TXxw1kdF5_Q

Next Time

- Setup + Hold Times
- Pipelining