Timing

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Calculator.py

- Lets you interact with the FPGA via the keyboard
  - Translates ASCII <--> Binary for you

```
$ python3 calculator.py –s /dev/ttyUSB1
```

```
$ python3 calculator.py –-help
```

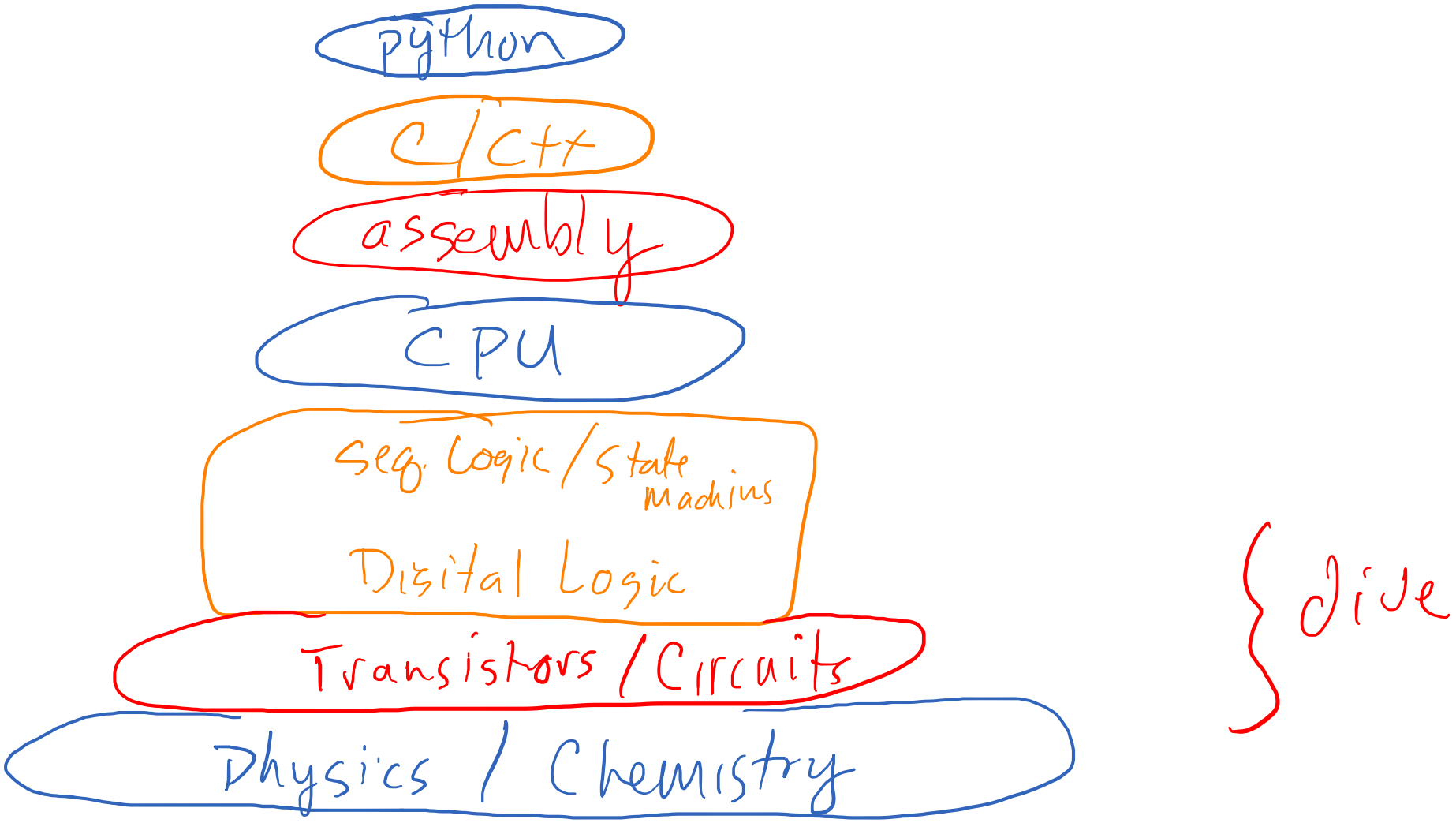
python3 (not “python”)

Overview

- Circuit Timing
- ~~Binary Multiplication~~

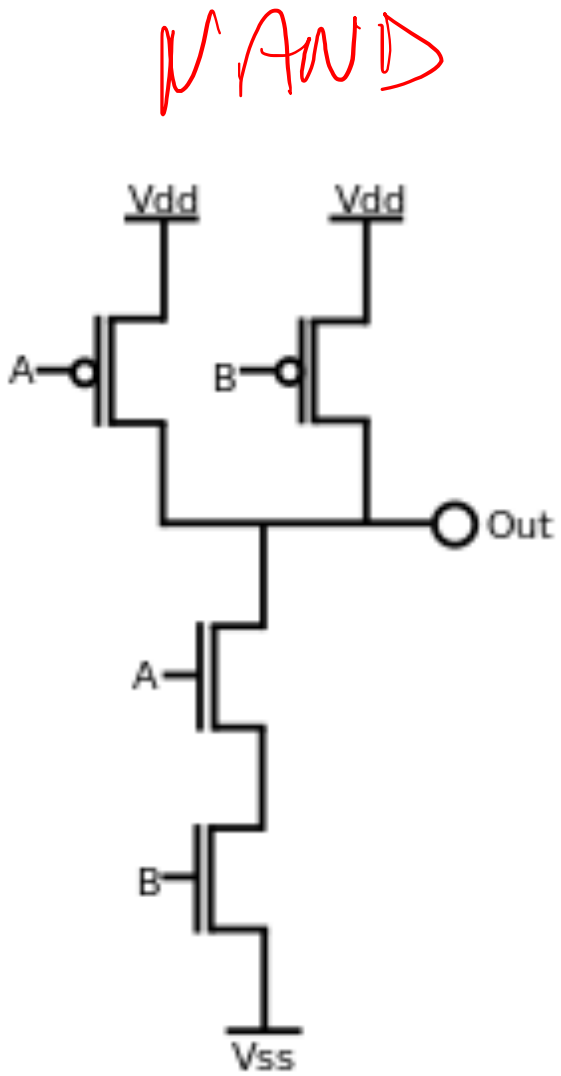
Synchronizers (?)

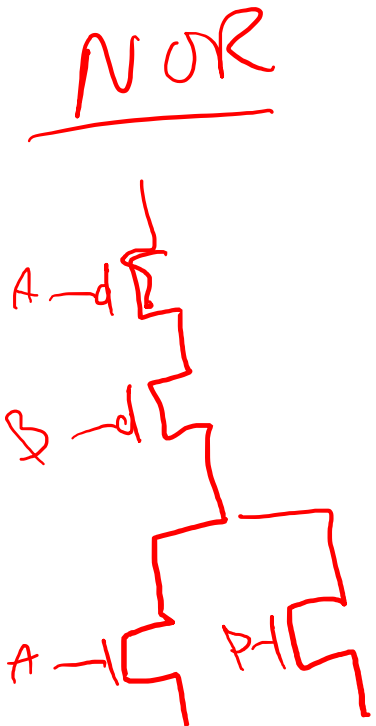
Review: The Compute Stack



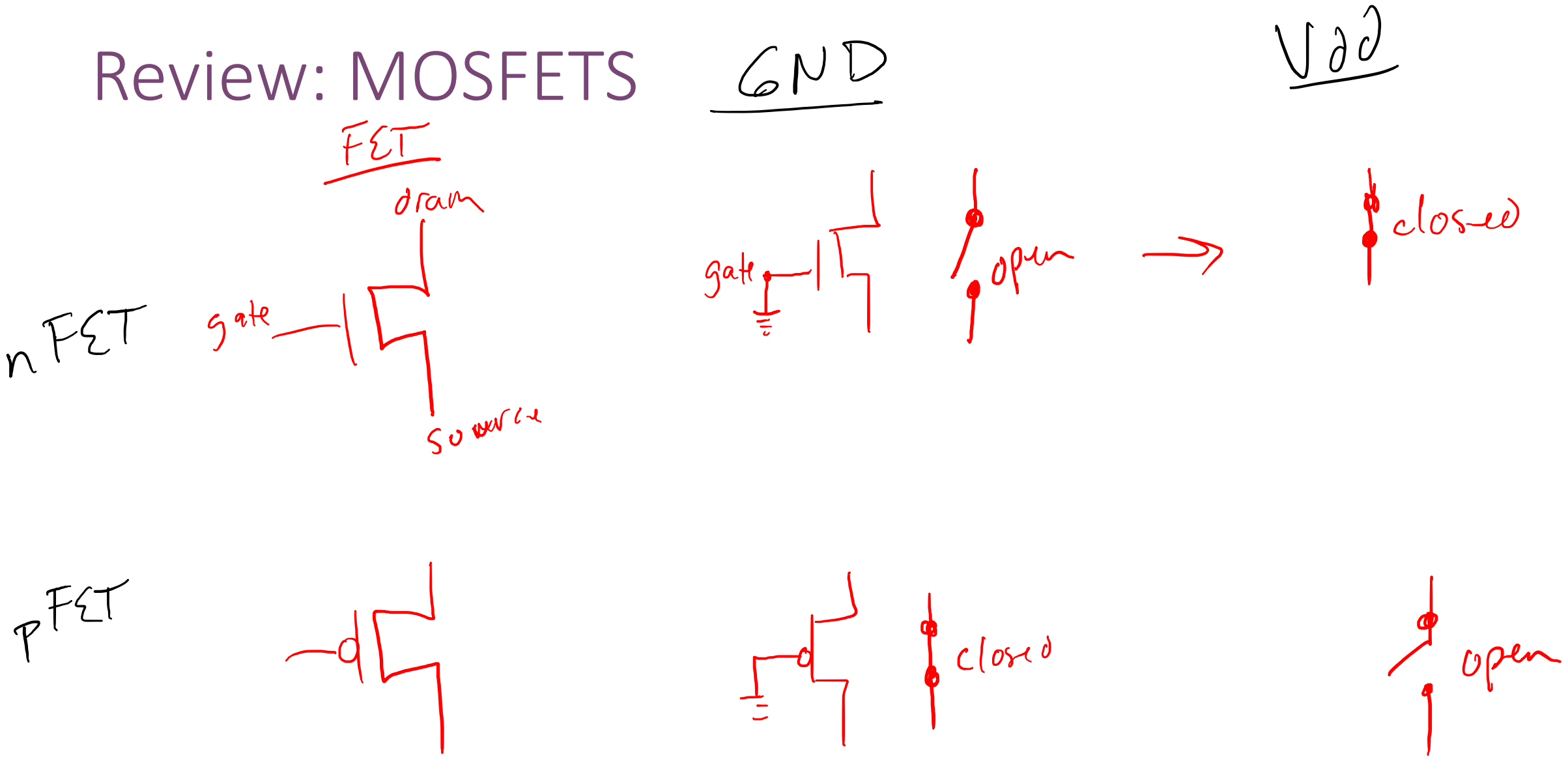
Review: All logic is NAND

- It's not magic, it's an electronic circuit

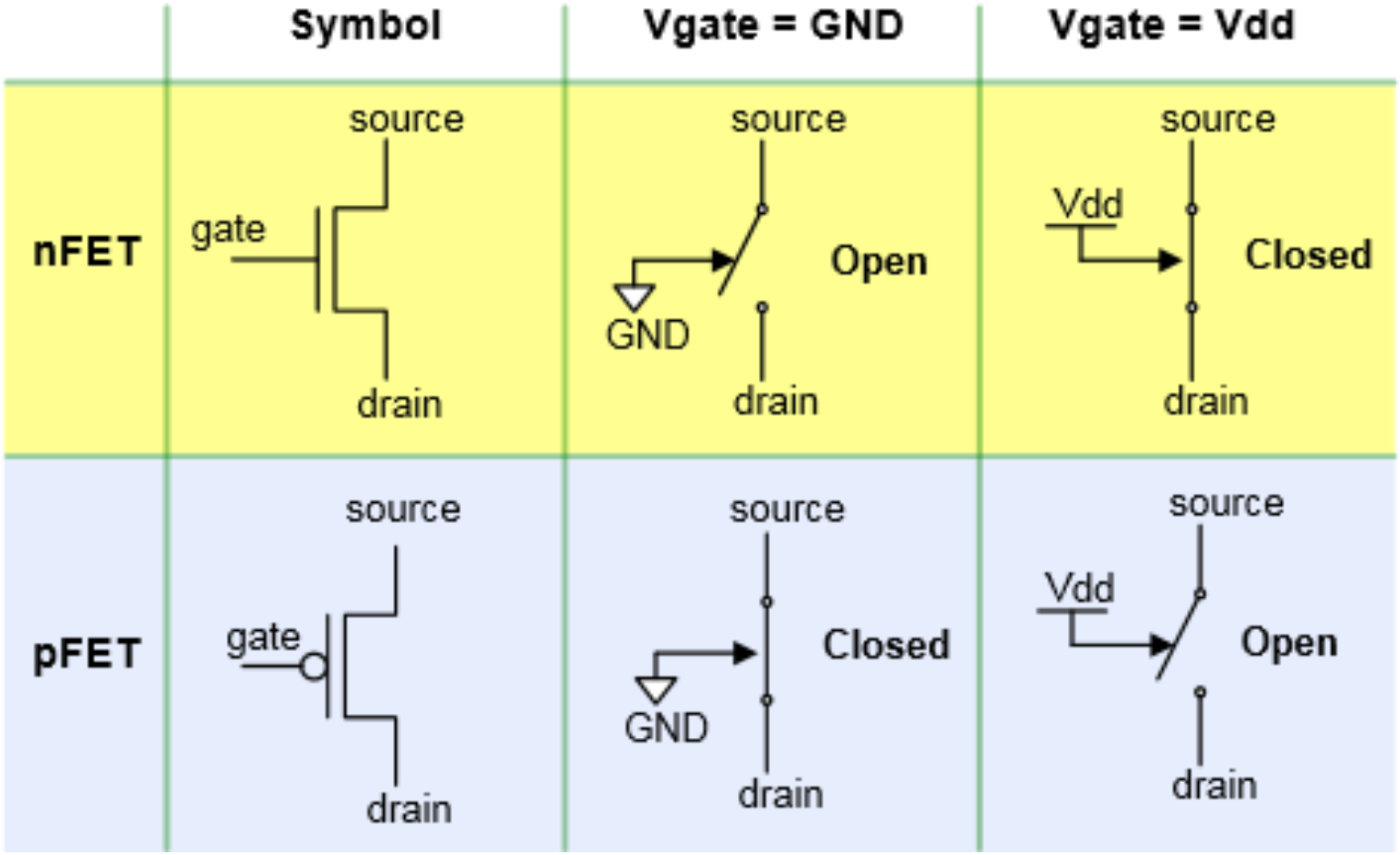




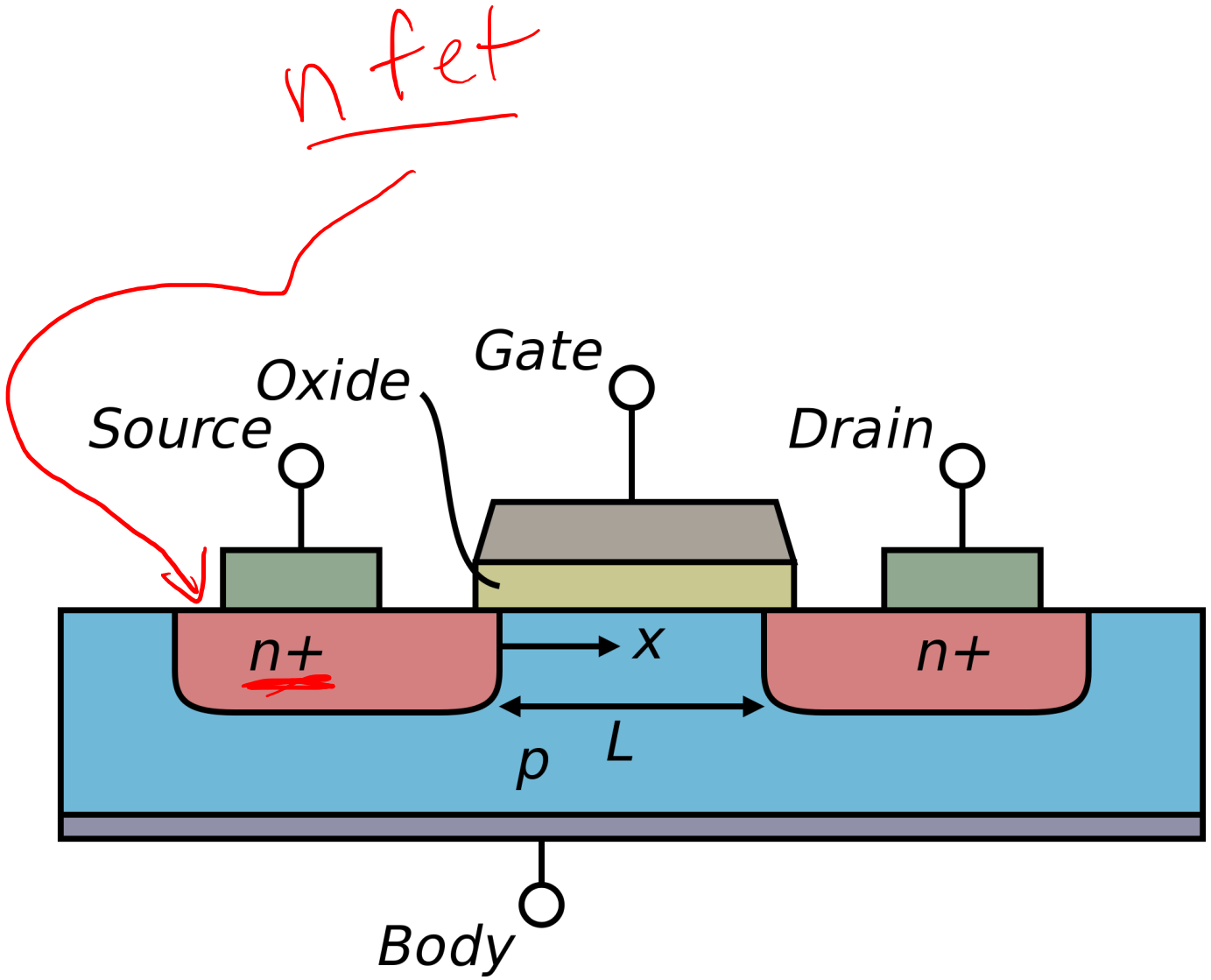
Review: MOSFETS



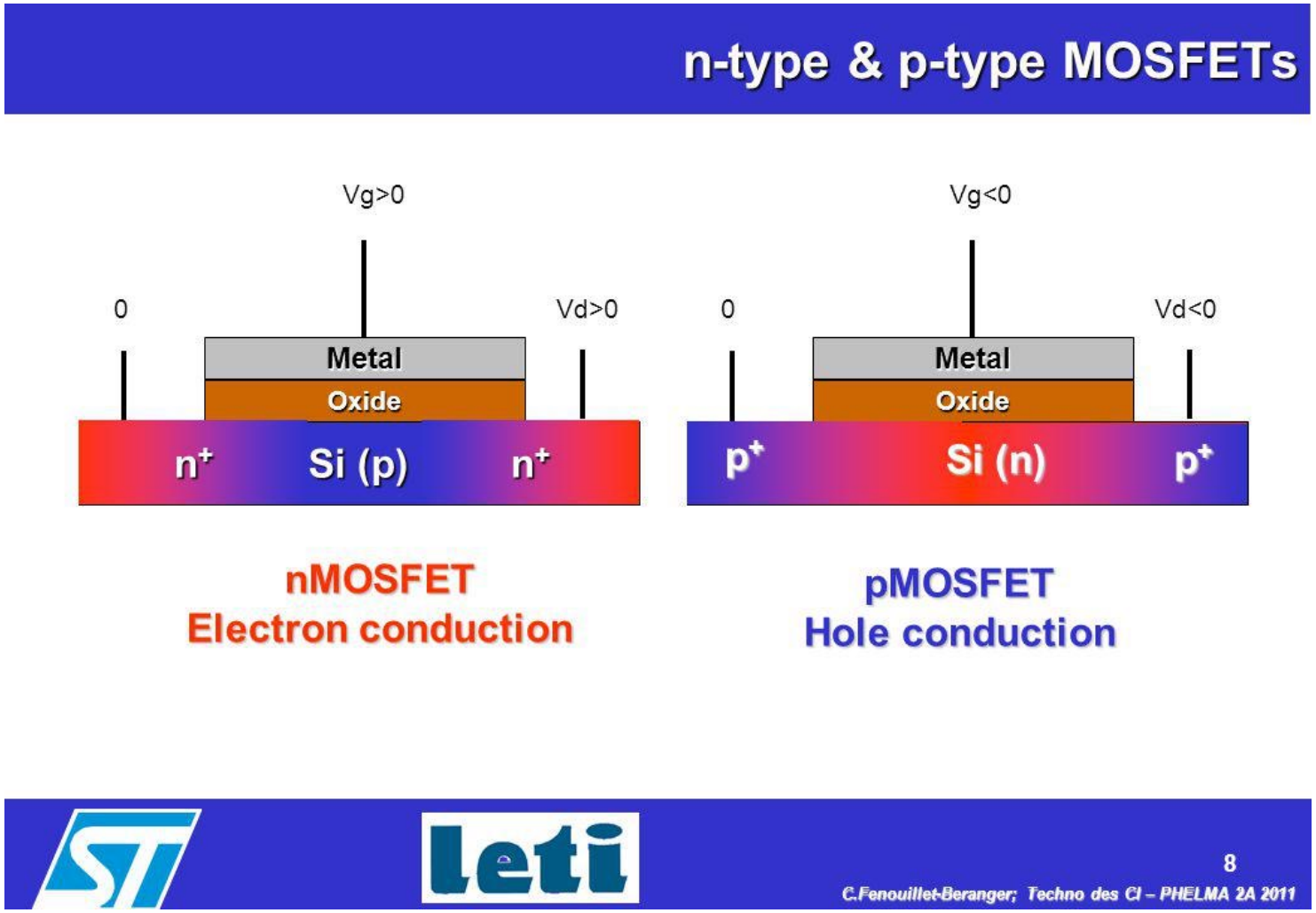
MOSFETS


Symbol
Vgate = GND
Vgate = Vdd
nFET
source
gate
drain
source
GND
Open
drain
source
Vdd
Closed
drain
pFET
source
gate
drain
source
GND
Closed
drain
source
Vdd
Open
drain

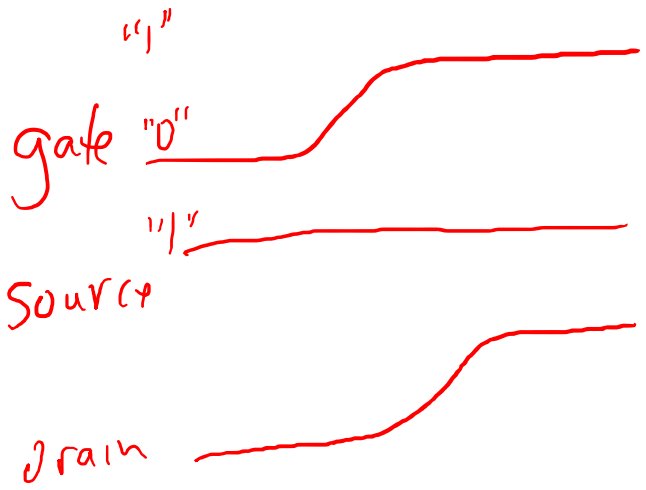
MOSFETS

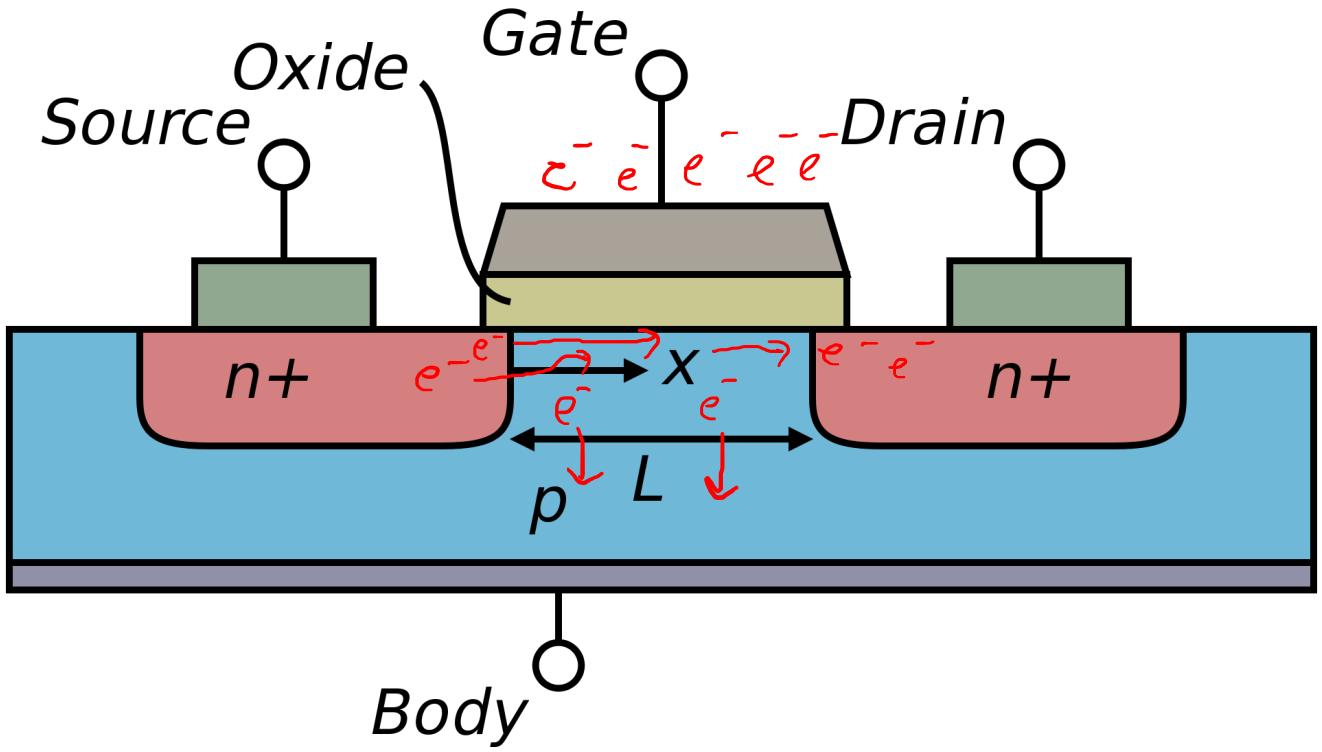


Correction: nFET vs. pFET



FET Delay

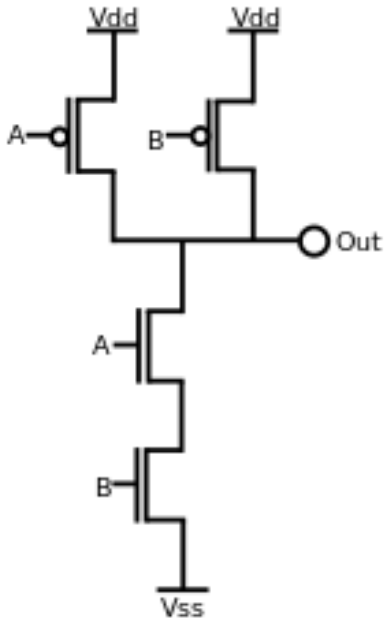


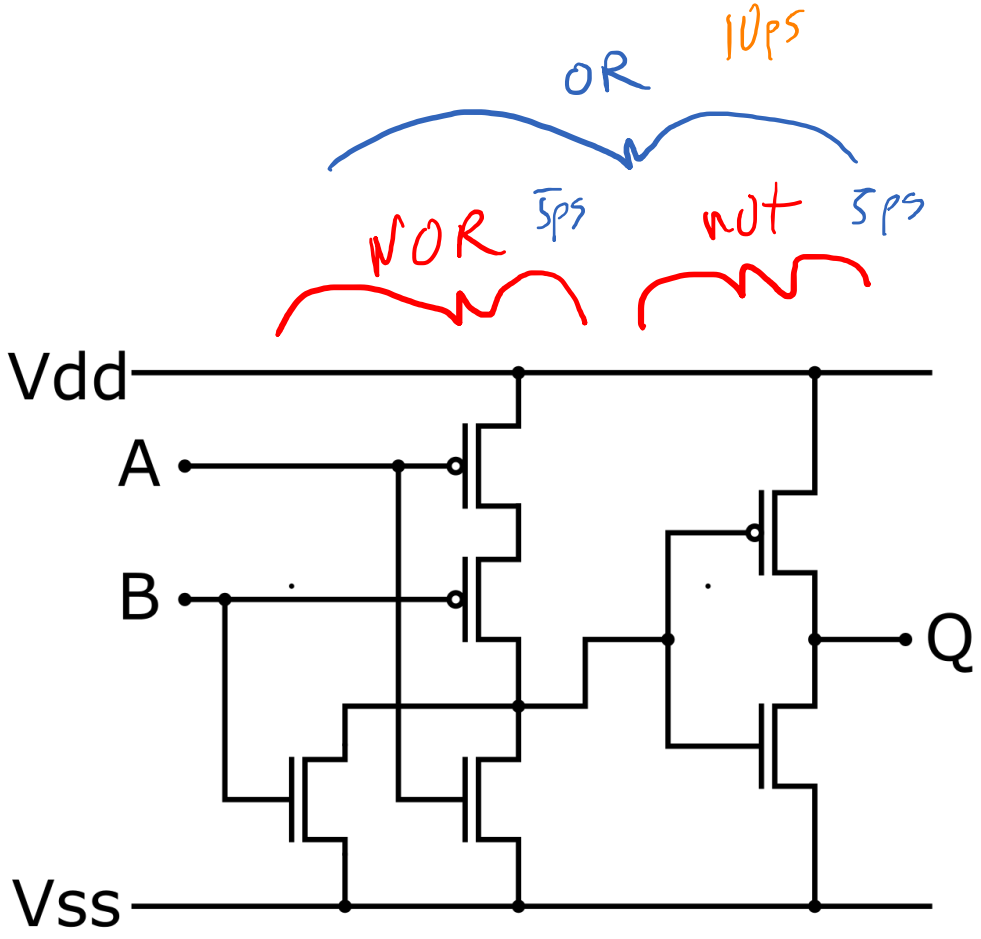


Gate Timing

- Assume 5ps / MOSFET

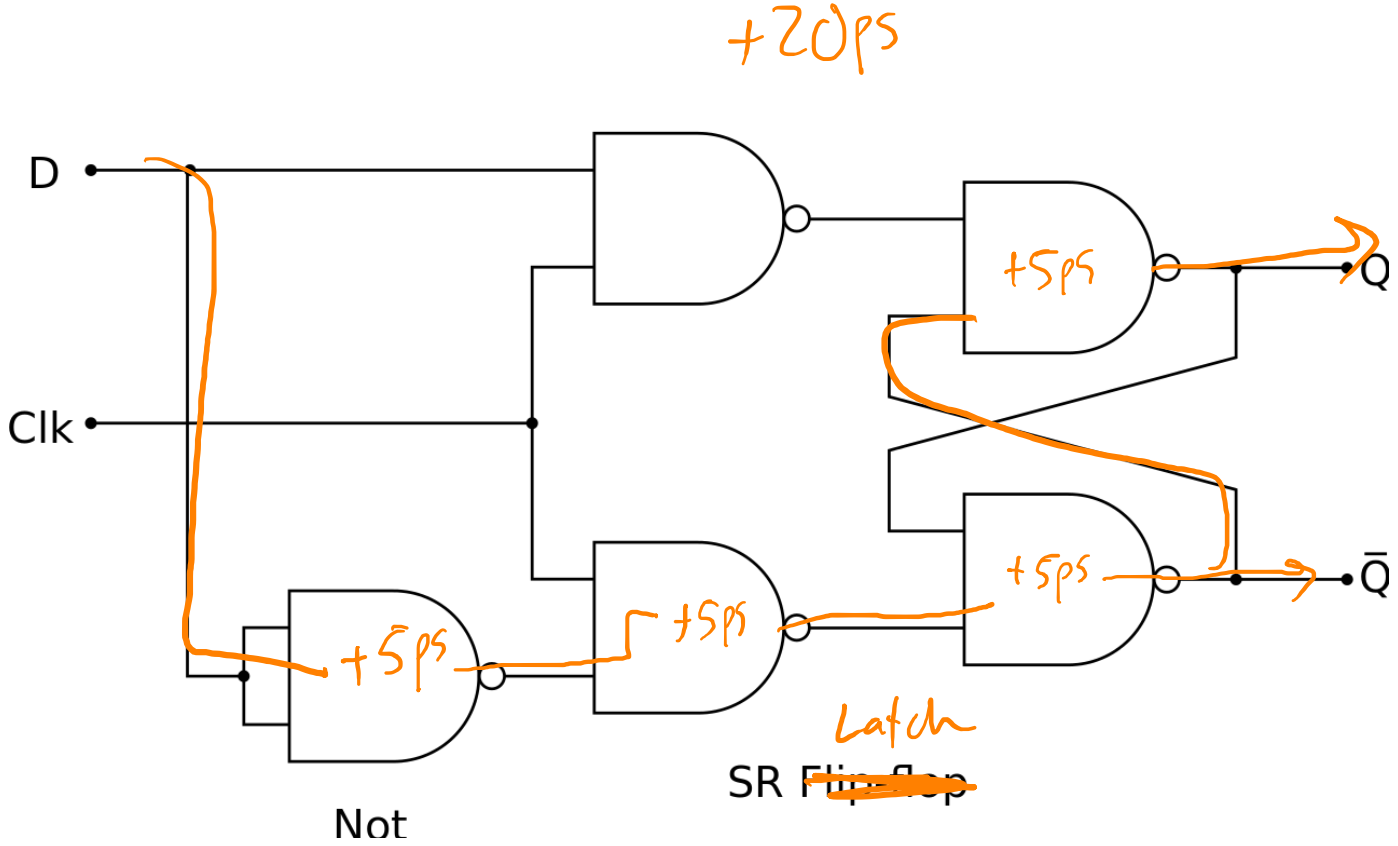
NAND = 5ps



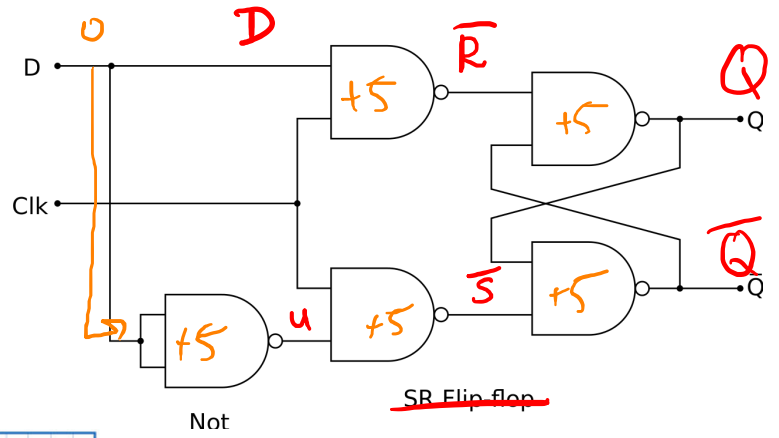


Flip-Flop Timing

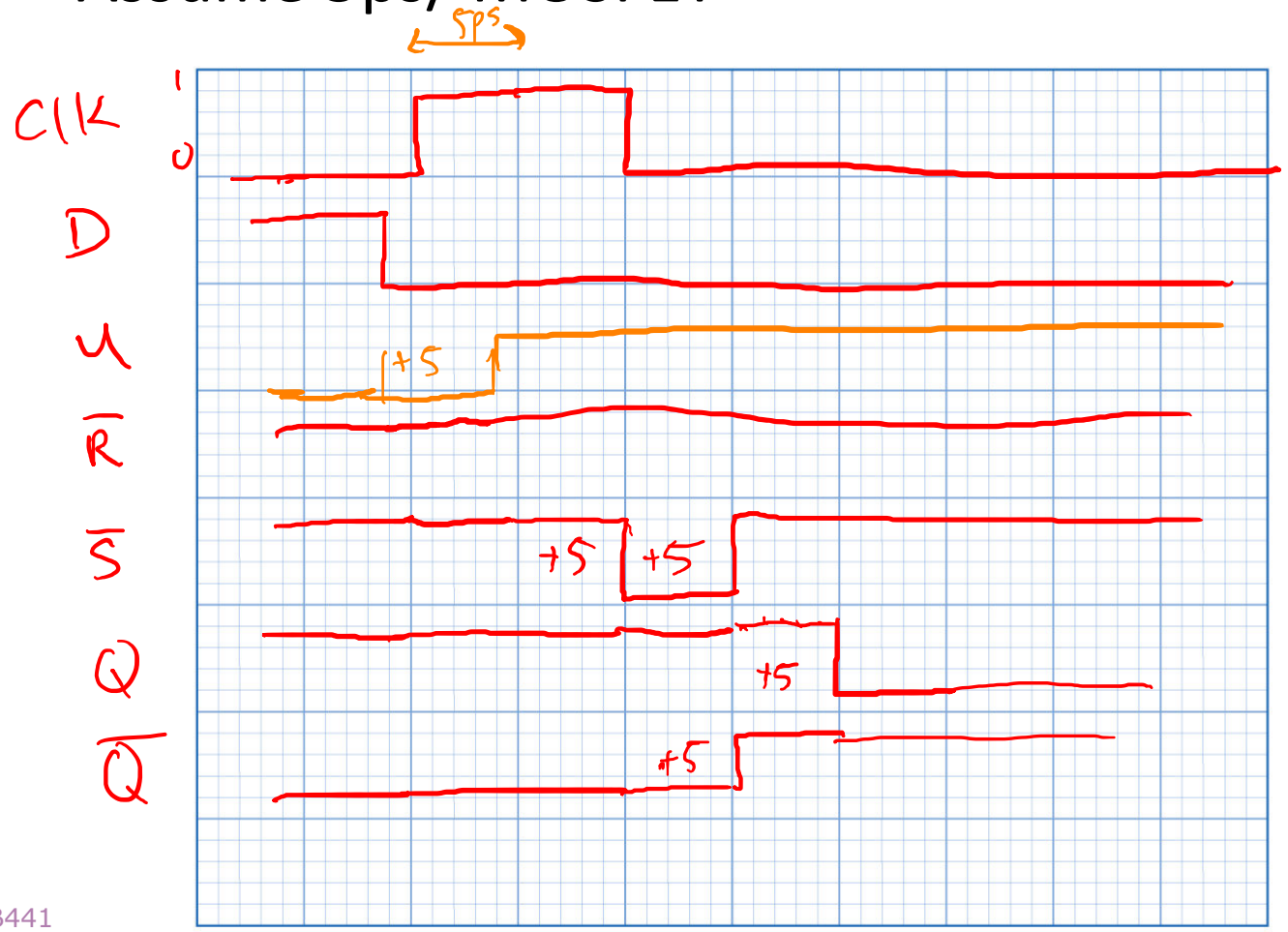
- Assume 5ps/ MOSFET



Setup Time Problems

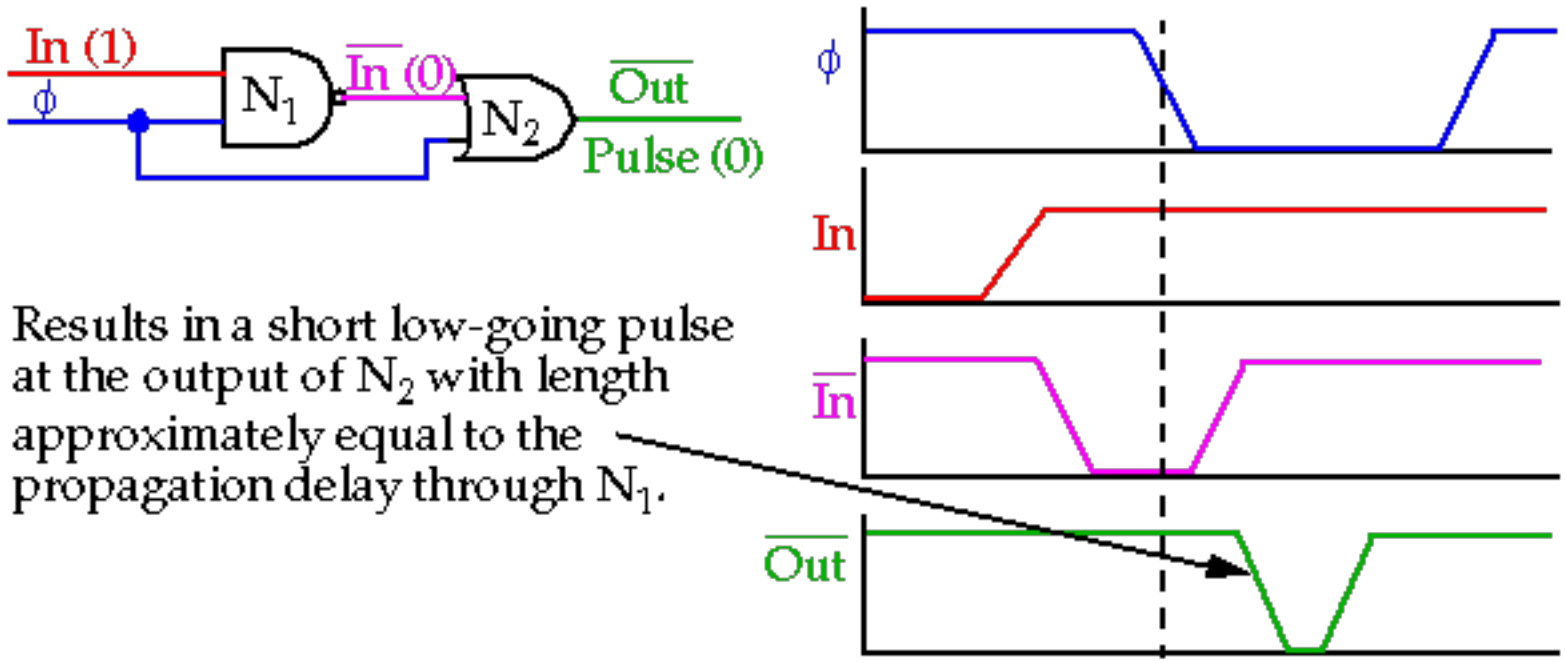


- Assume 5ps/ MOSFET



screwed this up redo next time...

Glitch

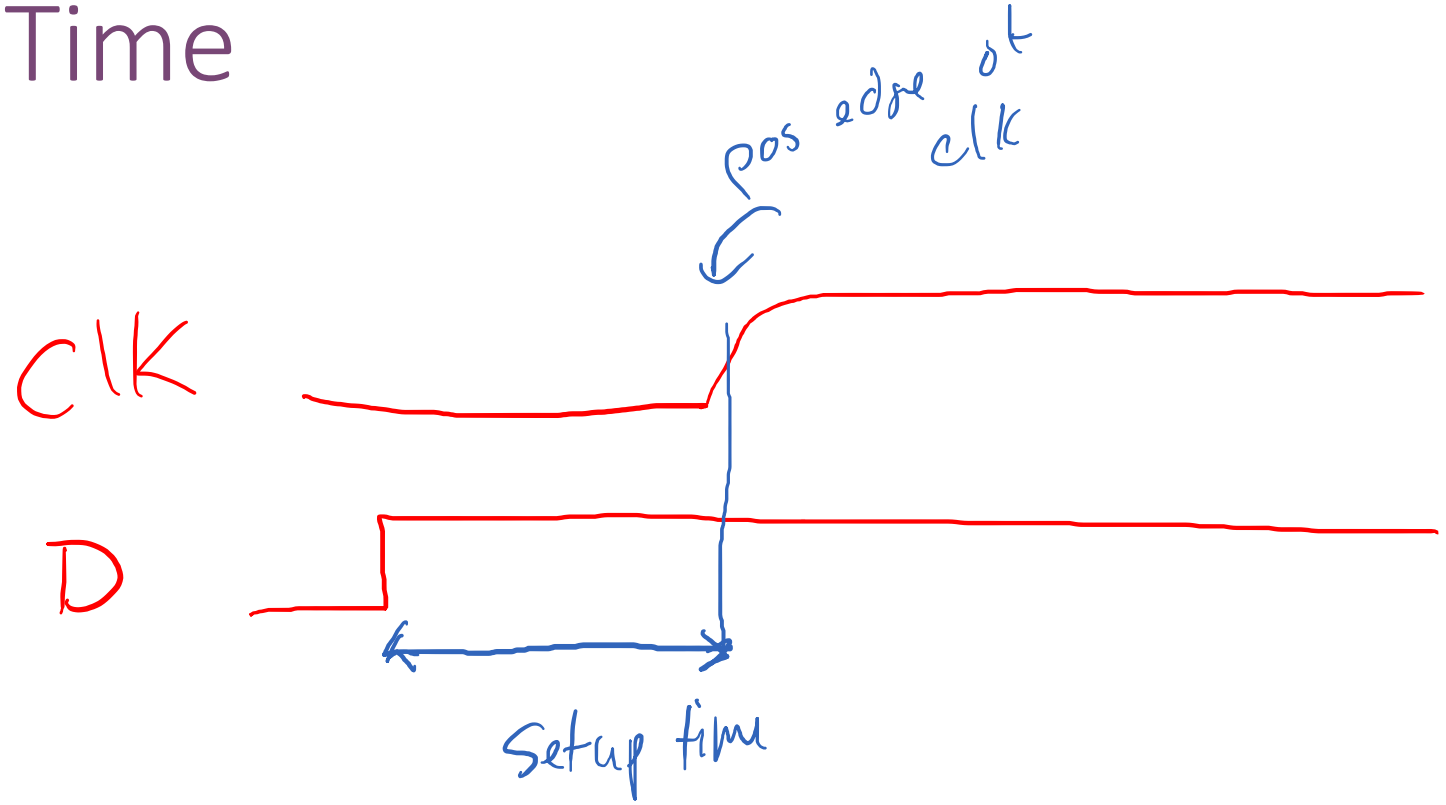

In (1)
ϕ
N1
In (0)
N2
Out
Pulse (0)
ϕ
In
In
Out
Results in a short low-going pulse at the output of N2 with length approximately equal to the propagation delay through N1.

Setup and Hold Time

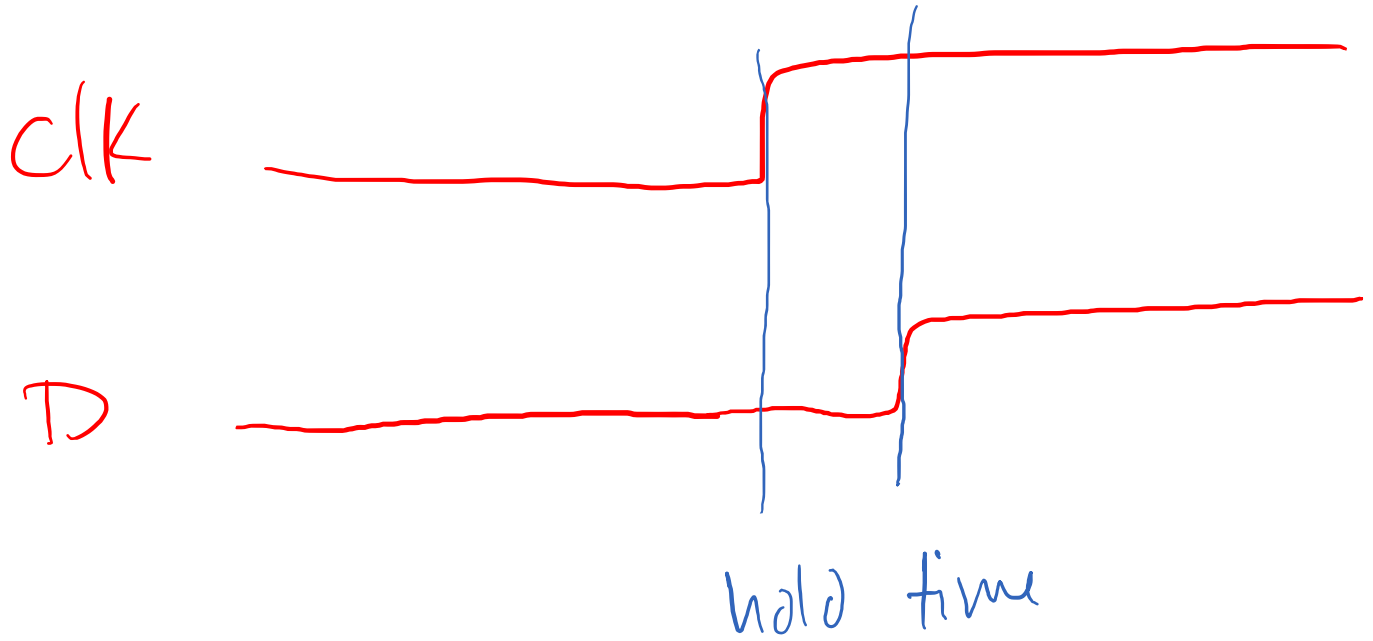
- **Setup Time**: minimum time the inputs to a flip-flop **must** be stable **before** the clock edge

- **Hold Time:** minimum time the inputs to a flip-flop **must** be stable **after** the clock edge

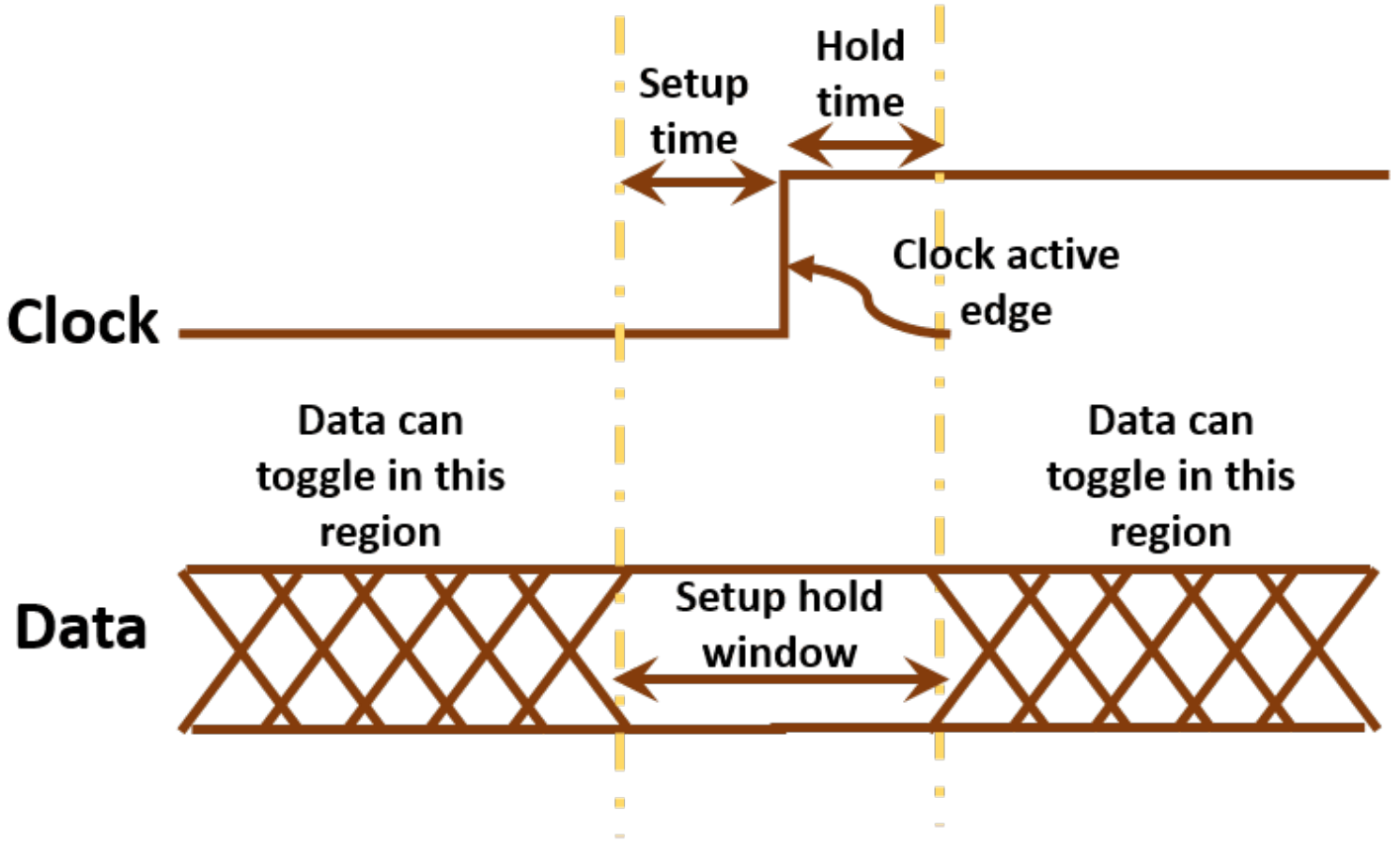
Setup Time



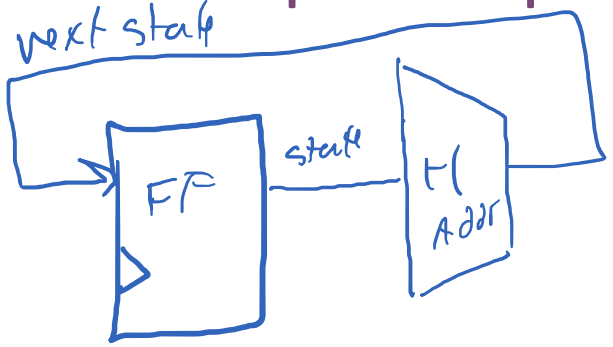
Hold Time

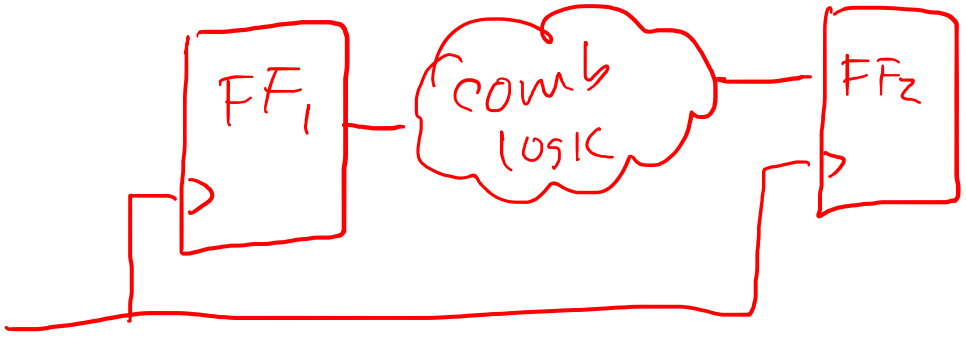


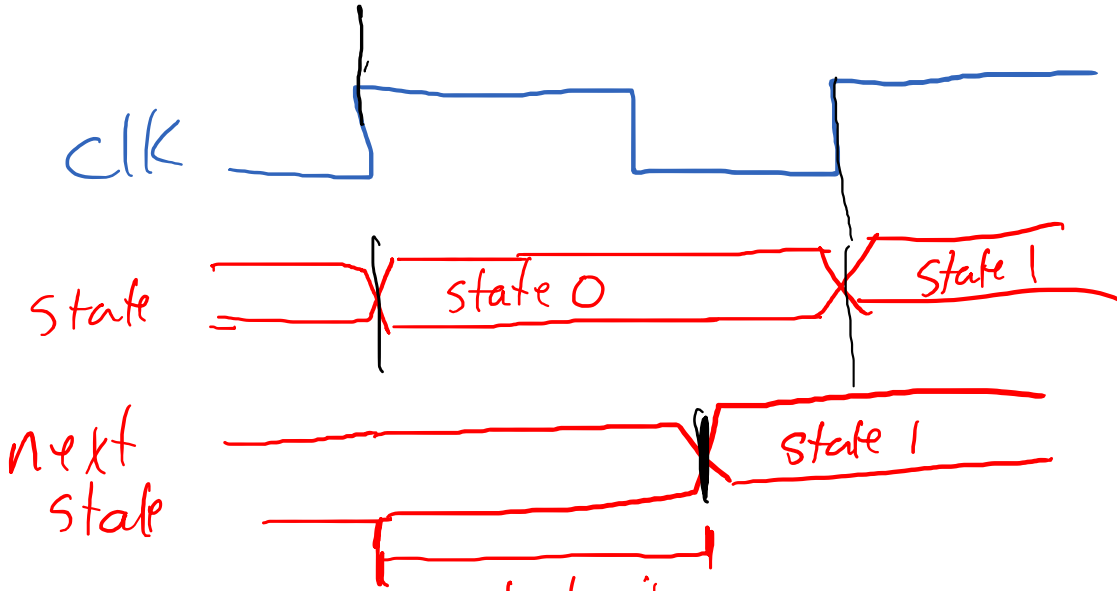
Setup/Hold Time

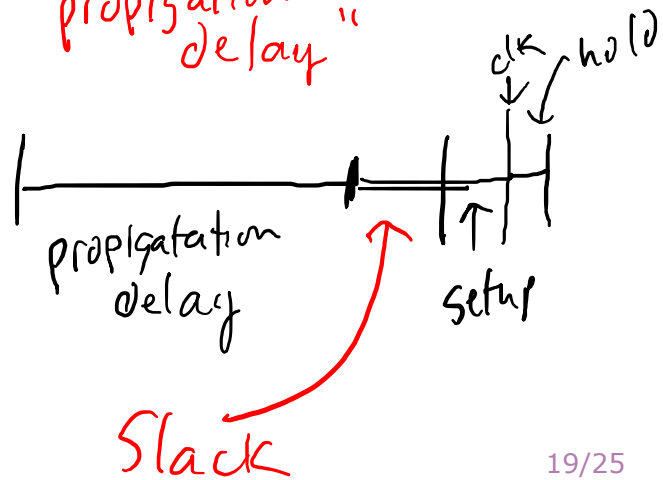


Inter Flip-Flop Timing









Inter Flip-Flop Timing

Register to register timing:

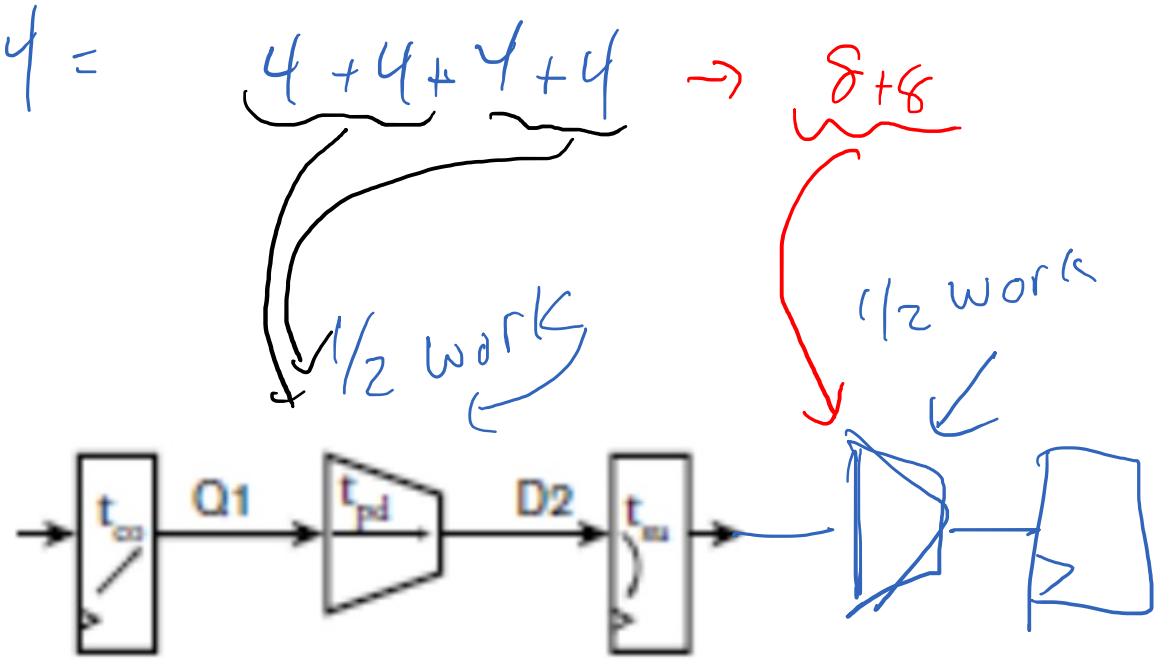
- output of a register *Q1*
- some combinational circuit
- input to the next register *D2*

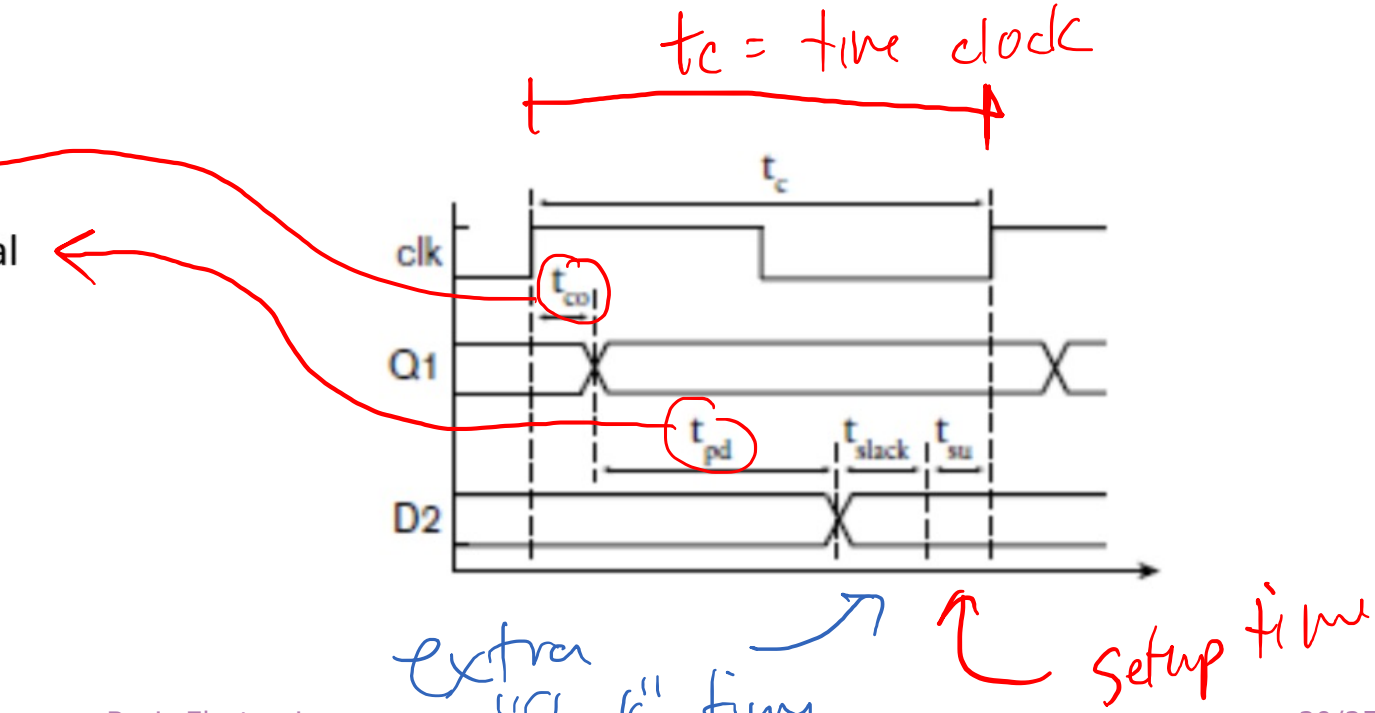
Delays:

- t_{co} , clock to output delay,
- t_{pd} , propagation delay in combinational circuit
- t_c , clock period

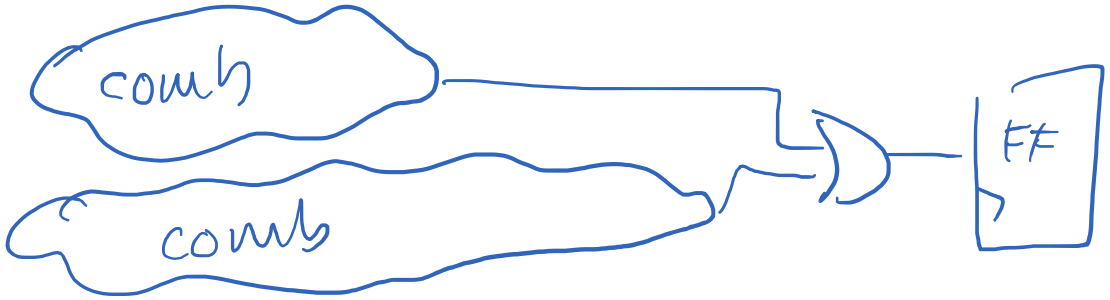
Timing requirement:

$$t_{co} + t_{pd} + t_{su} < t_c$$



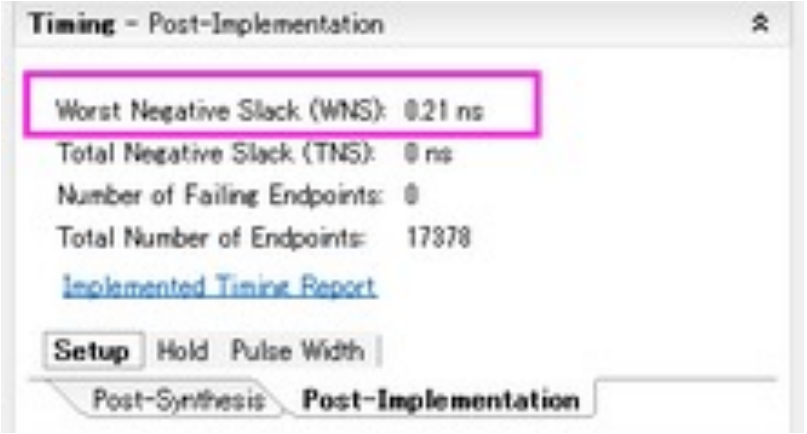


Slack



- Extra time between combinational propagation delay and setup time
- (Time between stable input and next clock edge)

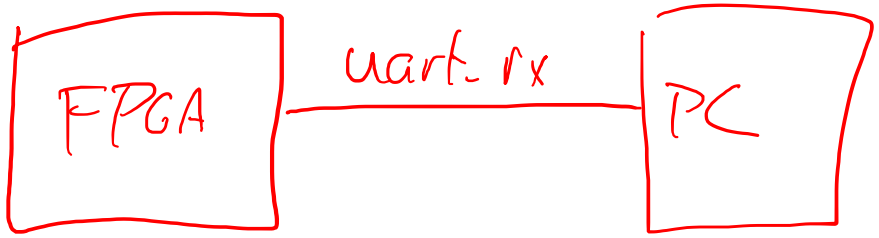
- Vivado:
  - WNS: Worst-case Negative Slack
  - TNS: True Negative Slack

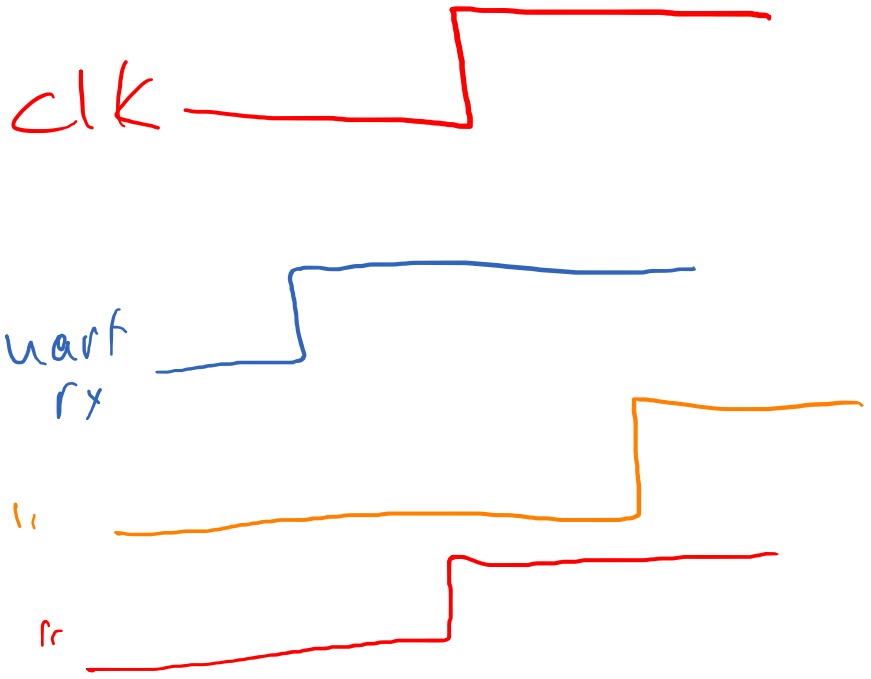


- If this number is <0, your circuit will (probably) not work

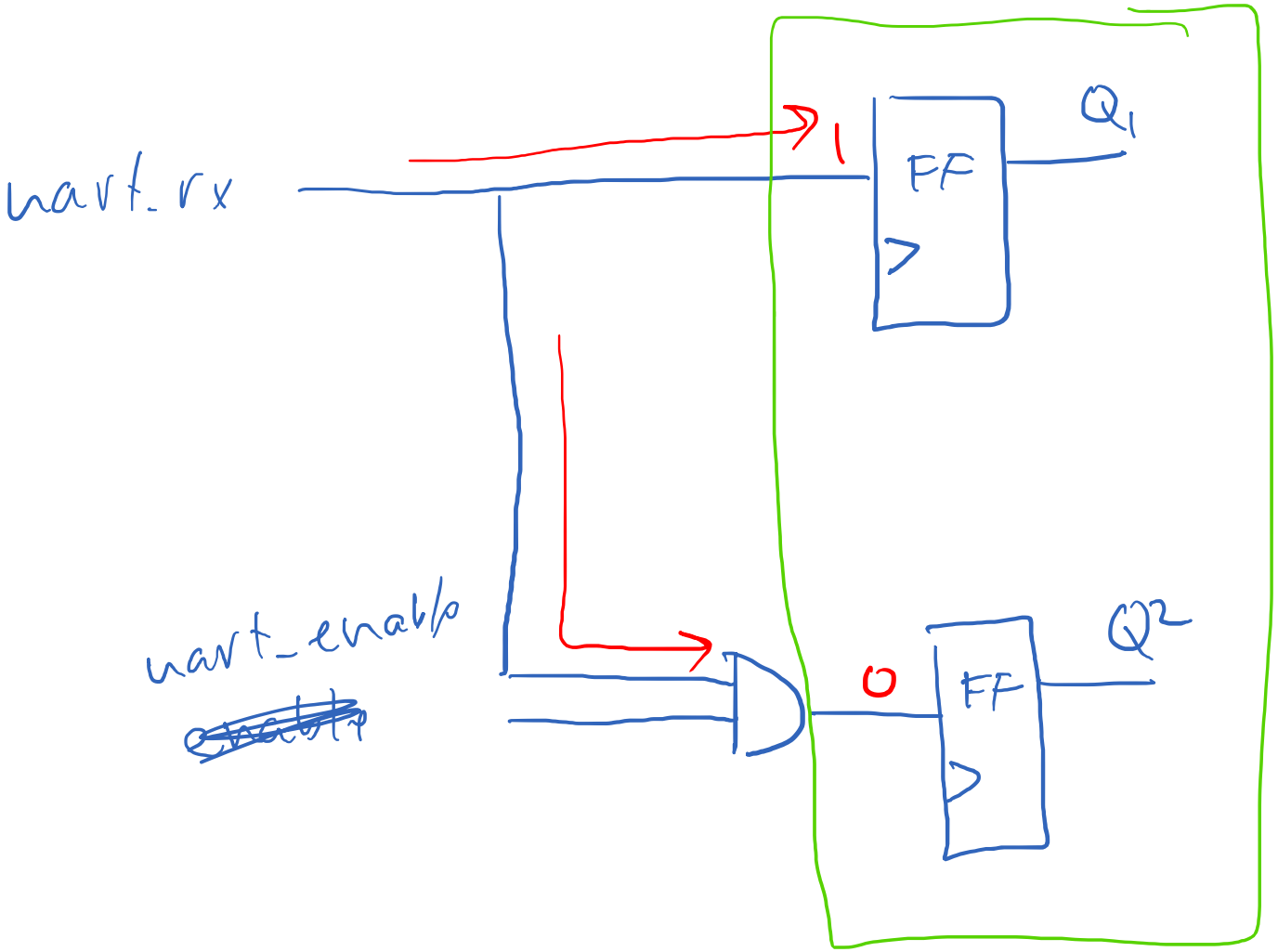
Setup/Hold Times on External Signals

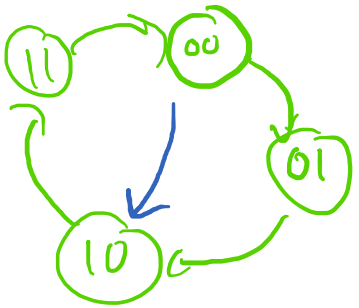
- What if I don’t know when my signal will arrive?

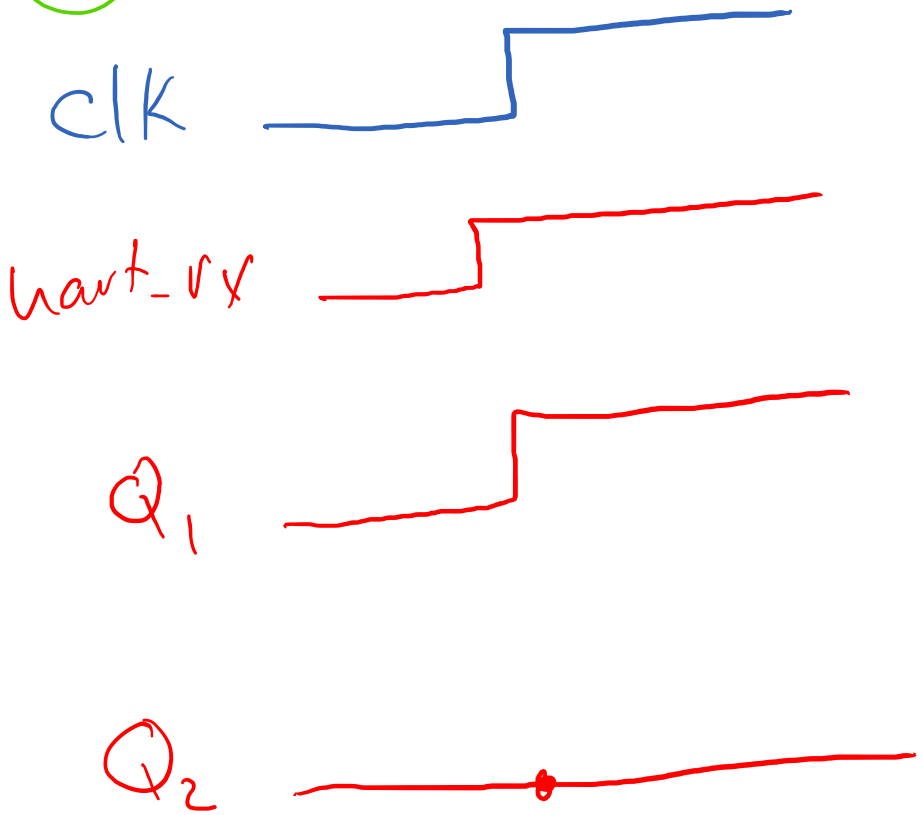




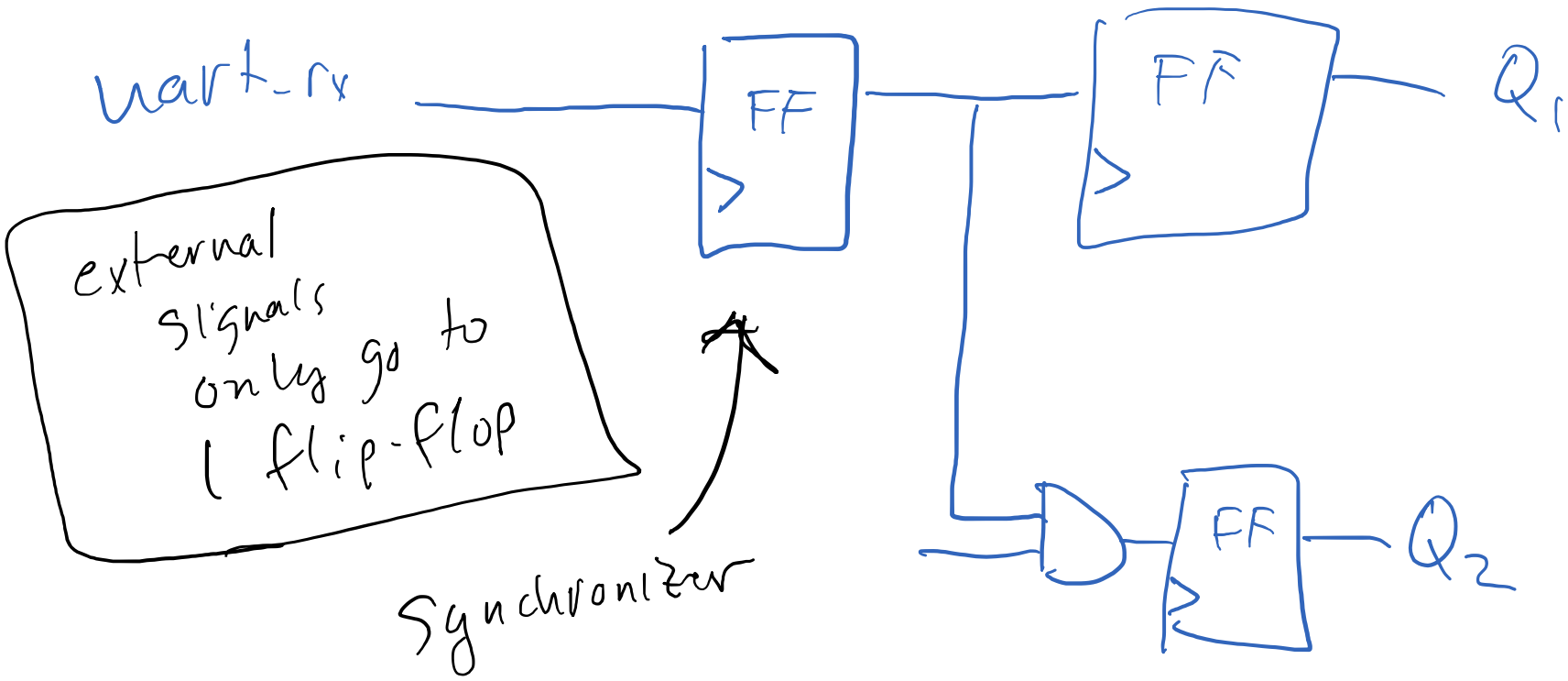
Out-of-Synchronization



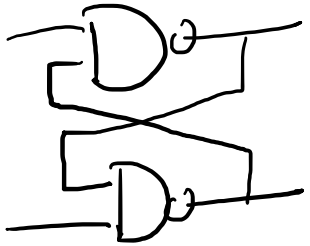


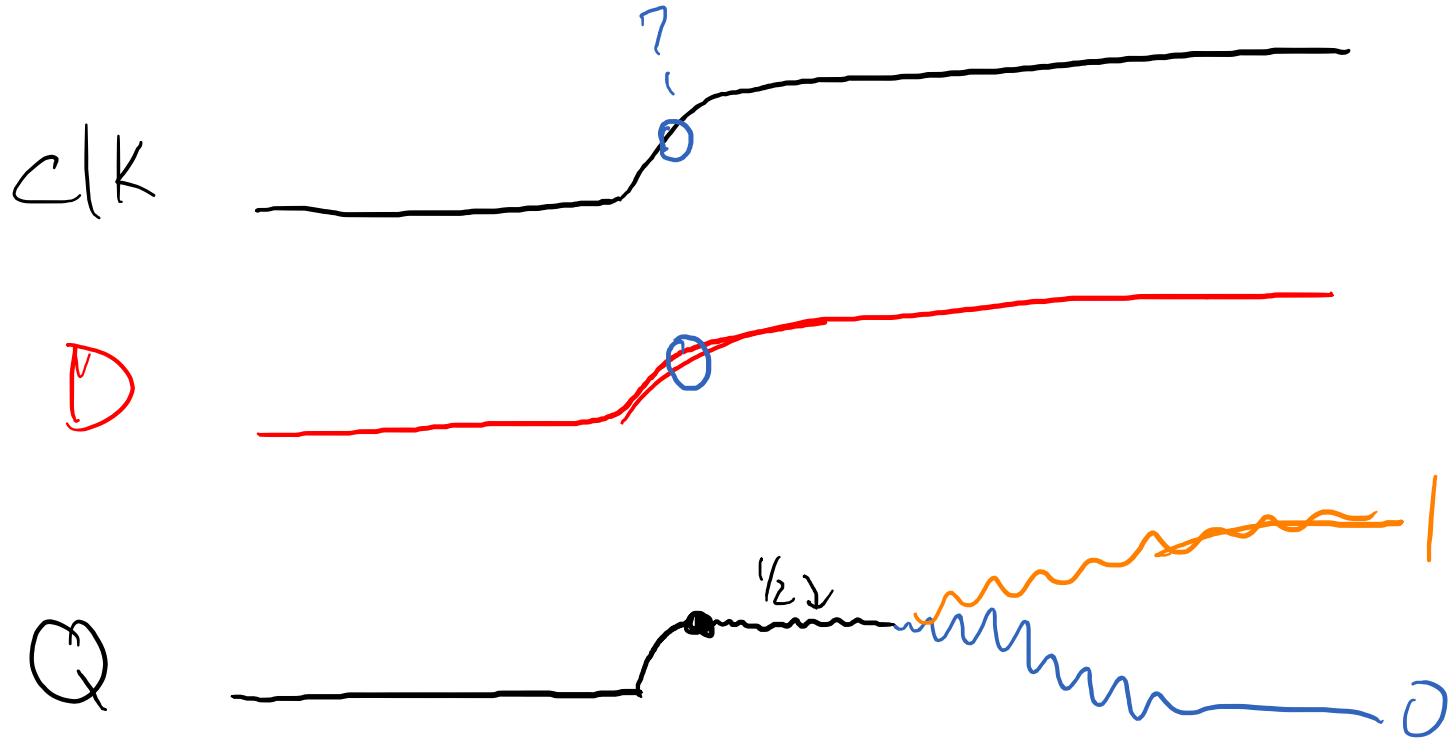


Synchronizers



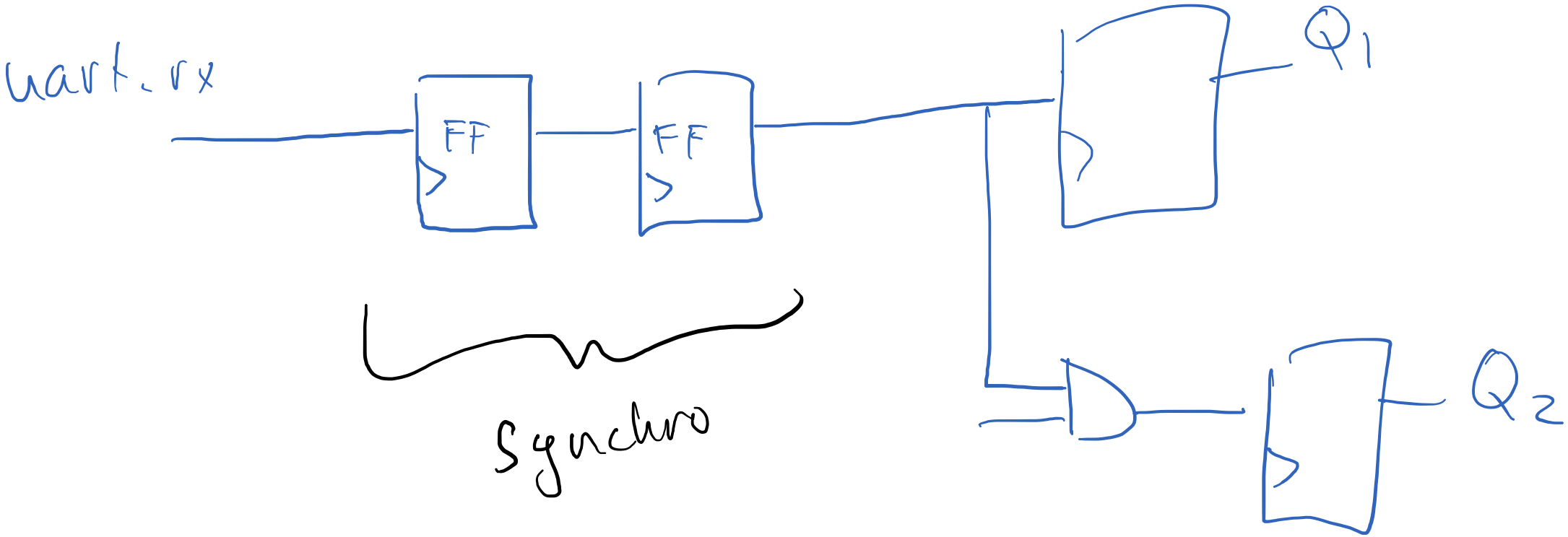
Metastability





metastability: not 0, not 1 ... it's 1/2

Synchronizers for Metastability



Next Time

- Binary Multiplication
- Pipelining