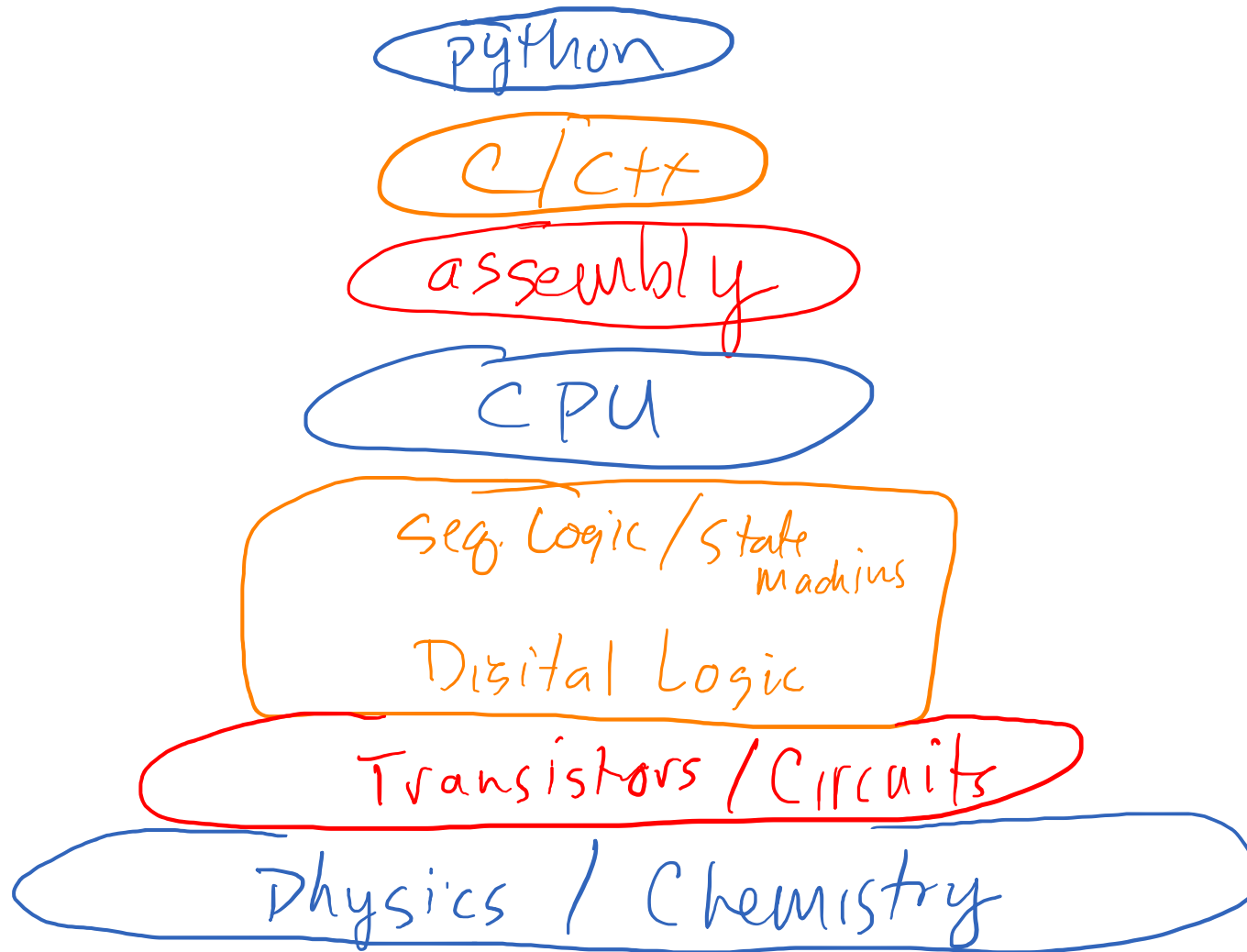


# CMOS

→ make sure  
you start a  
testbench w/  
 $rst = 1$  for a "few"  
clock cycles.

Andrew Lukefahr  
Indiana University - Bloomington

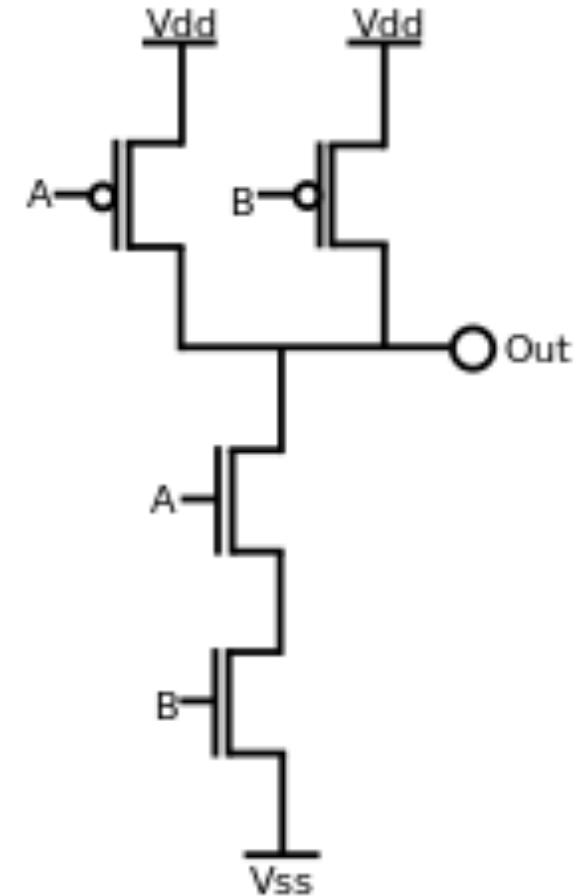
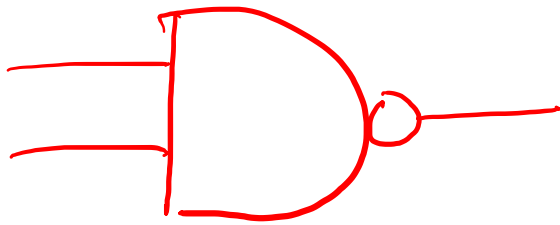
# The Compute Stack



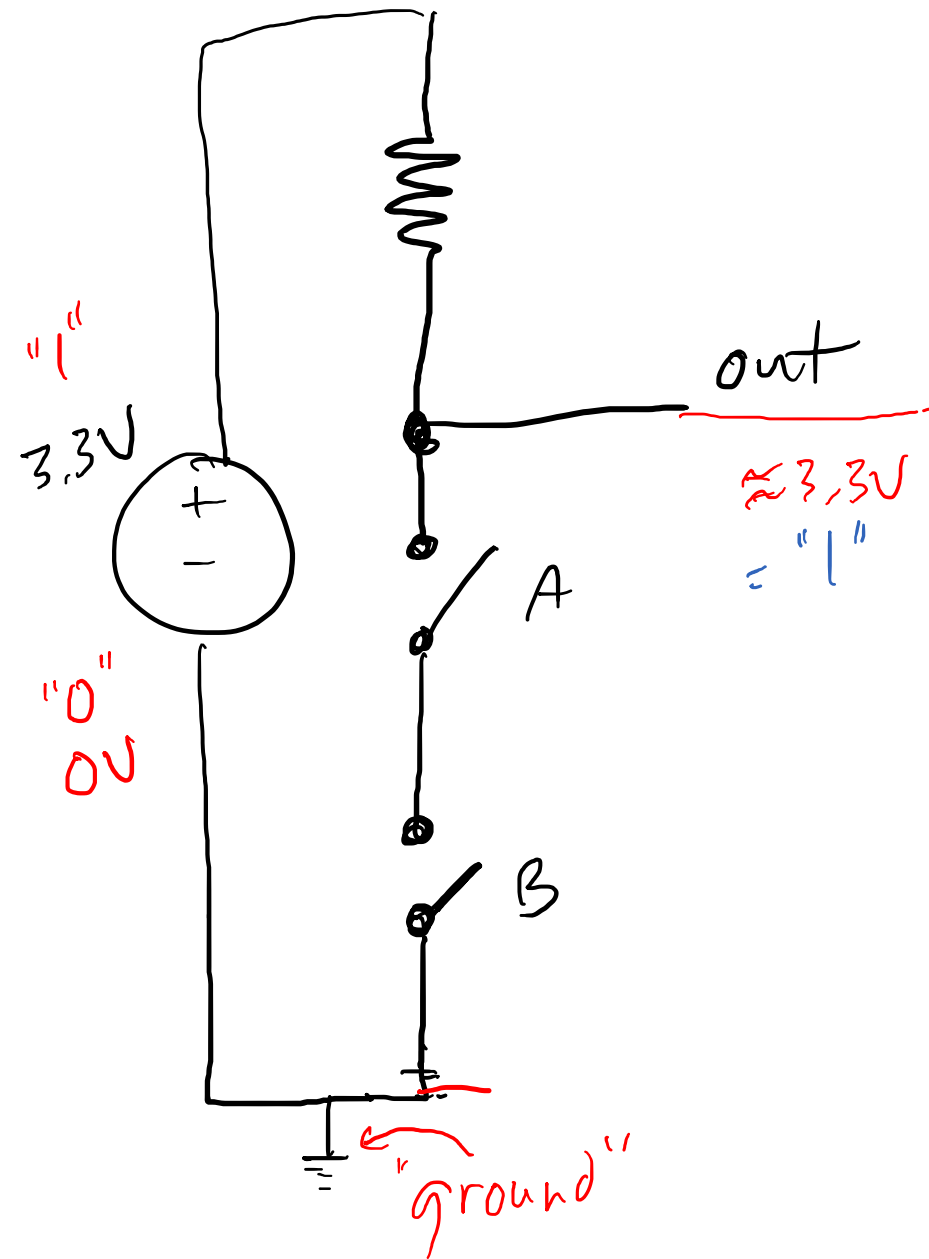
} dive

# All logic is NAND

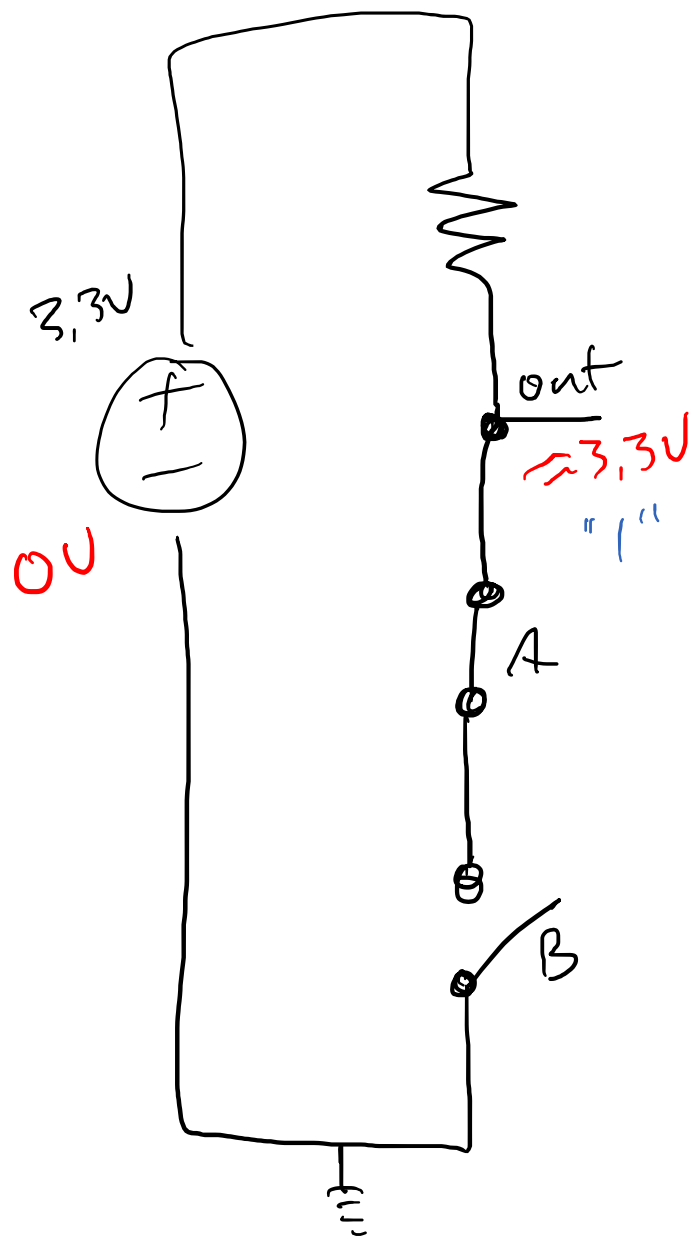
- It's not magic, it's an electronic circuit



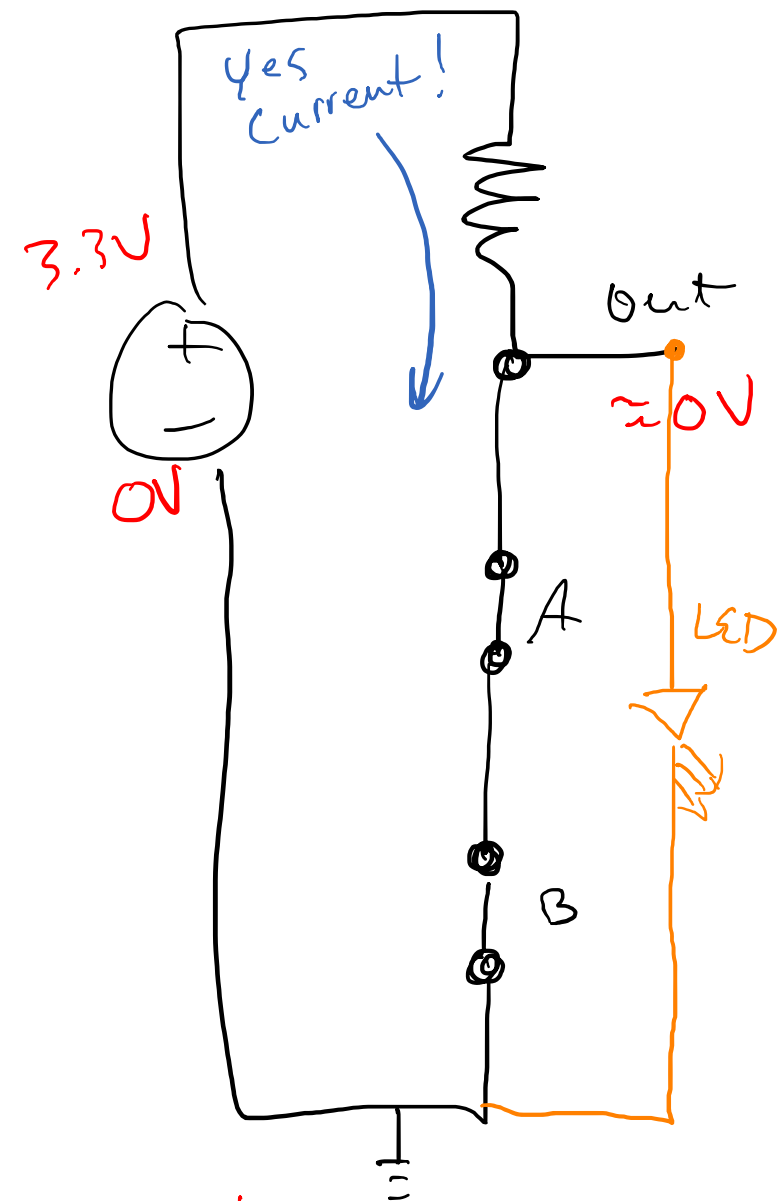
no current



no current



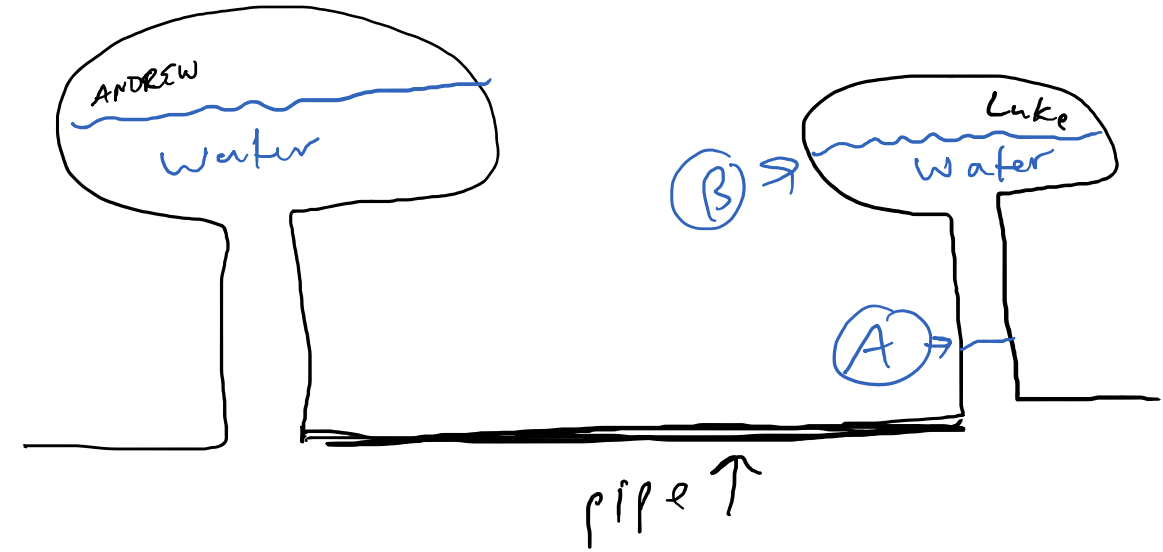
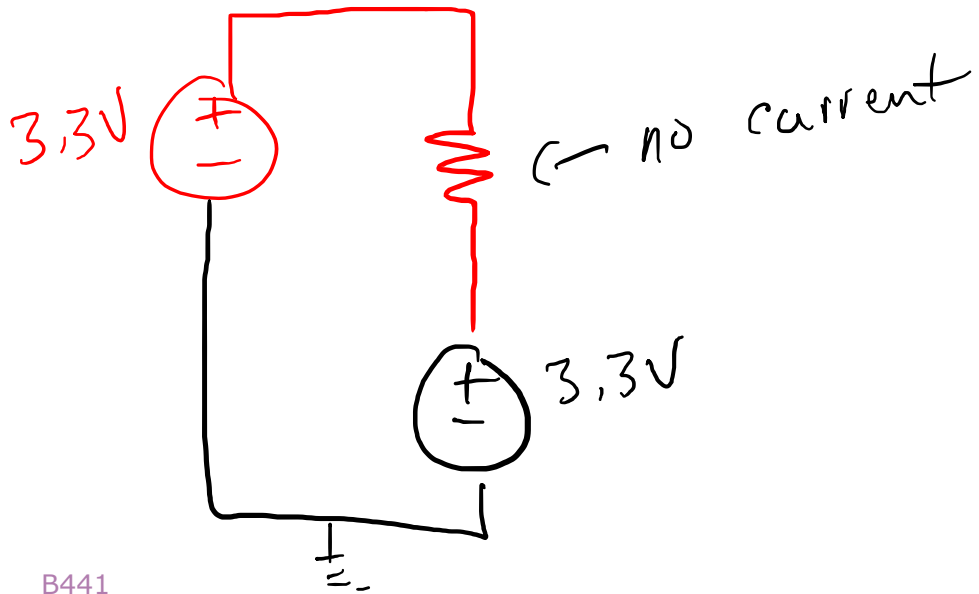
NAND



Stopped here

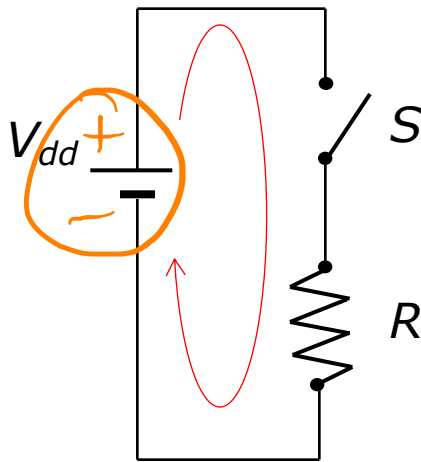
# Voltage Drop

- $V = IR$
- Voltage = Current \* Resistance
- What happens if current (i) == 0?

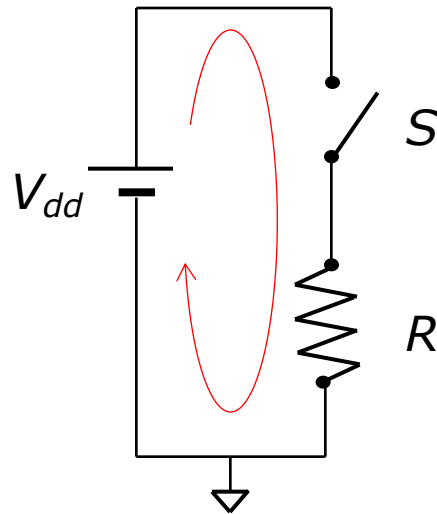


When water levels are equal → no flow through pipe

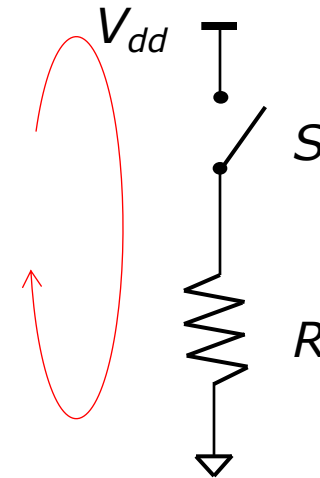
# Simplified Electronic Circuit



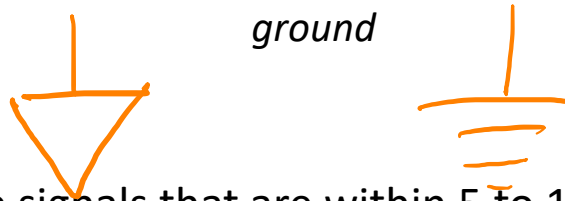
Circuit



Circuit with  
ground

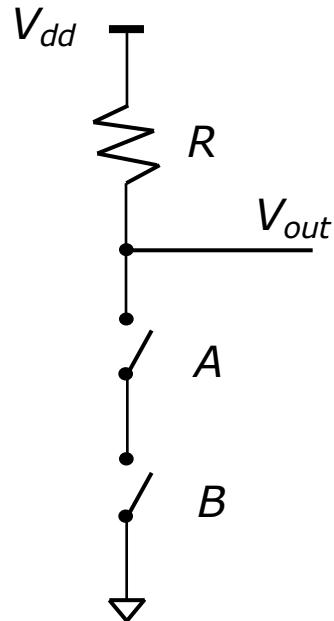


Shorthand  
notation



Most electronic circuits use signals that are within 5 to 10 volts of ground; in recent years, circuit signals are within 1 to 5 volts of ground.

# NAND



A	B	$V_{out}$
open	open	high
open	closed	high
closed	open	high
closed	closed	low

Convention:

Open: 0

Closed: 1

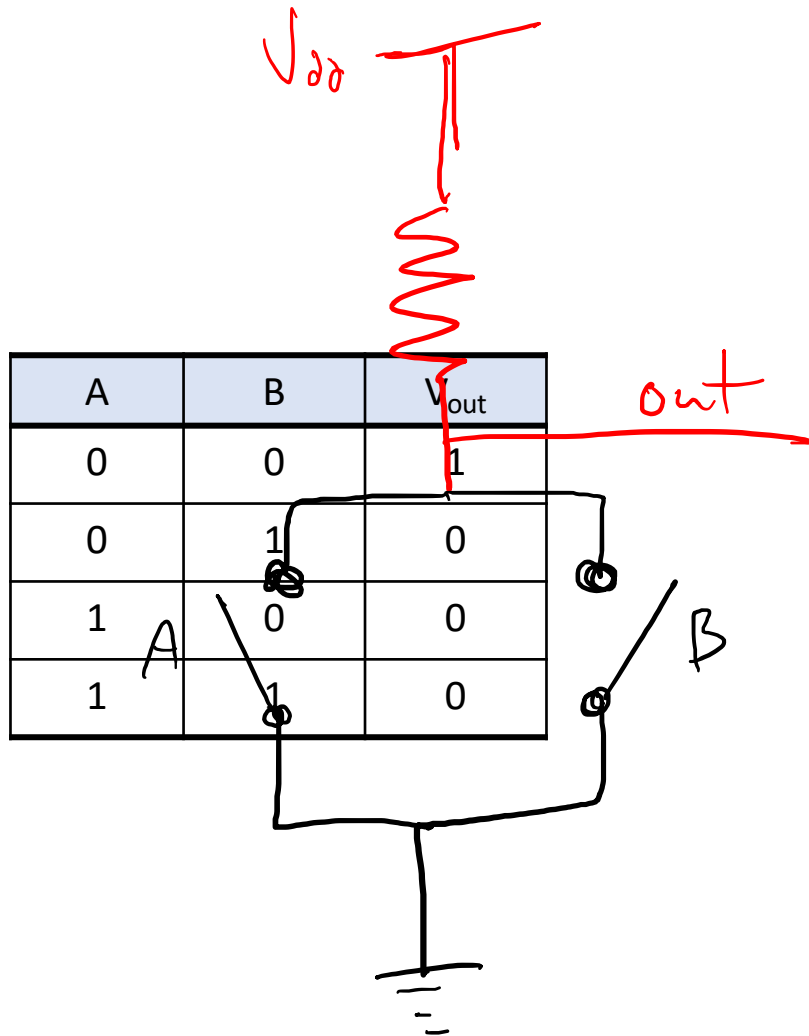
A	B	$V_{out}$
0	0	1
0	1	1
1	0	1
1	1	0

Low voltage: 0

High voltage: 1

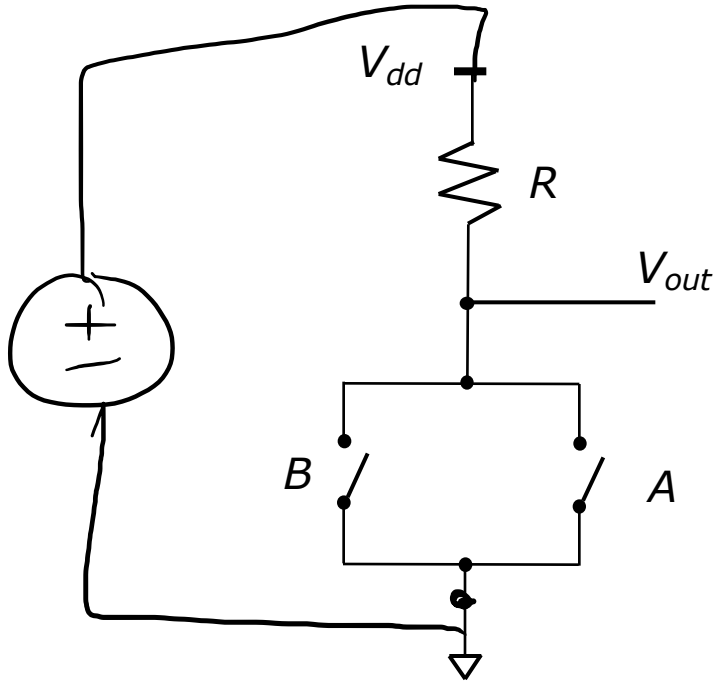
This circuit does not implement *AND*, rather it implements inverted *AND*, *NOT-AND*, or *NAND* logic operation!

# NOR





Drop the LED from the OR circuit and take the voltage from the resistor as the output:

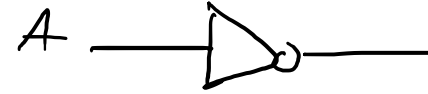


A	B	$V_{out}$
open	open	HV
open	closed	LV
closed	open	LV
closed	closed	LV

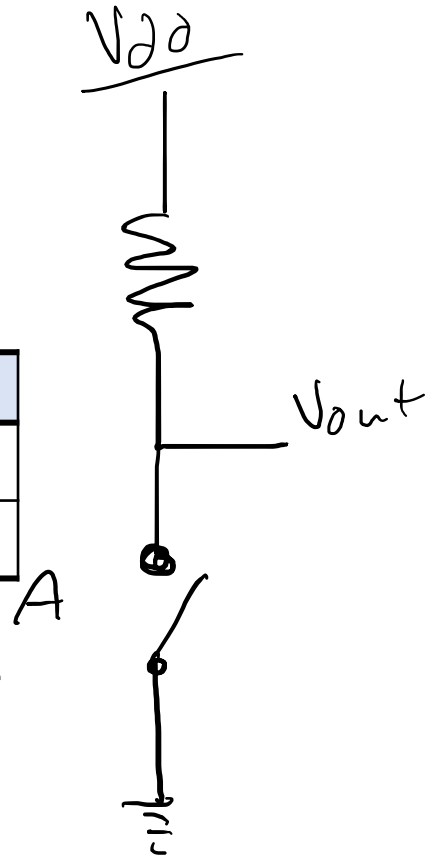
A	B	$V_{out}$
0	0	1
0	1	0
1	0	0
1	1	0

This circuit does not implement *OR*, rather it implements inverted *OR*, *NOT-OR*, or *NOR* logic operation!

# NOT

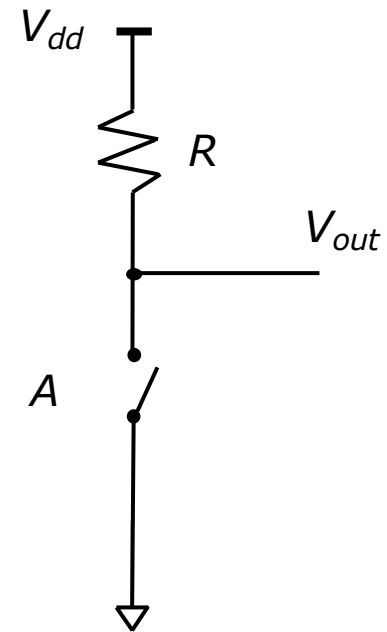


A	$V_{out}$
0	1
1	0

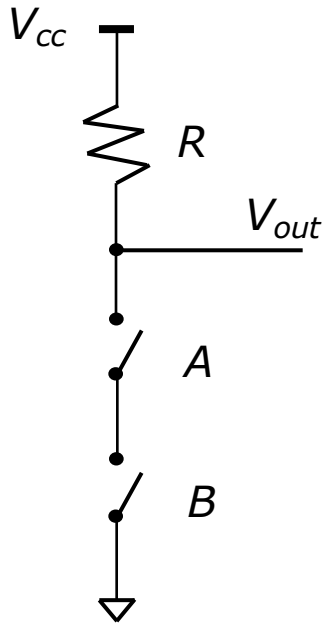


# NOT

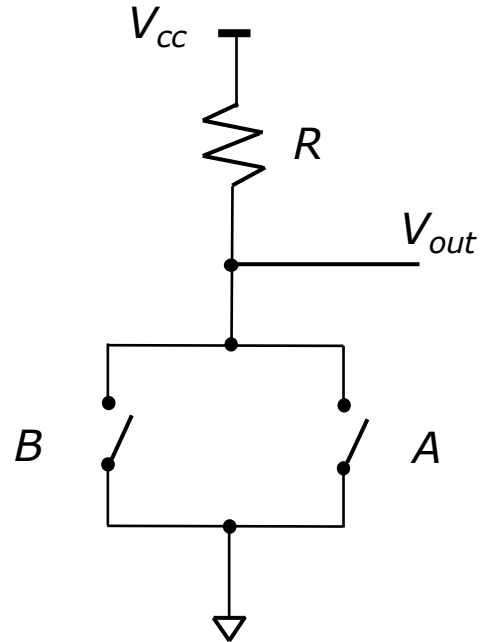
A	$V_{out}$
0	1
1	0



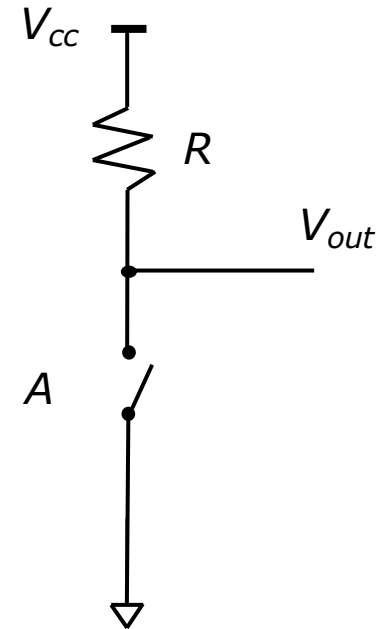
# What circuit is this?



NAND



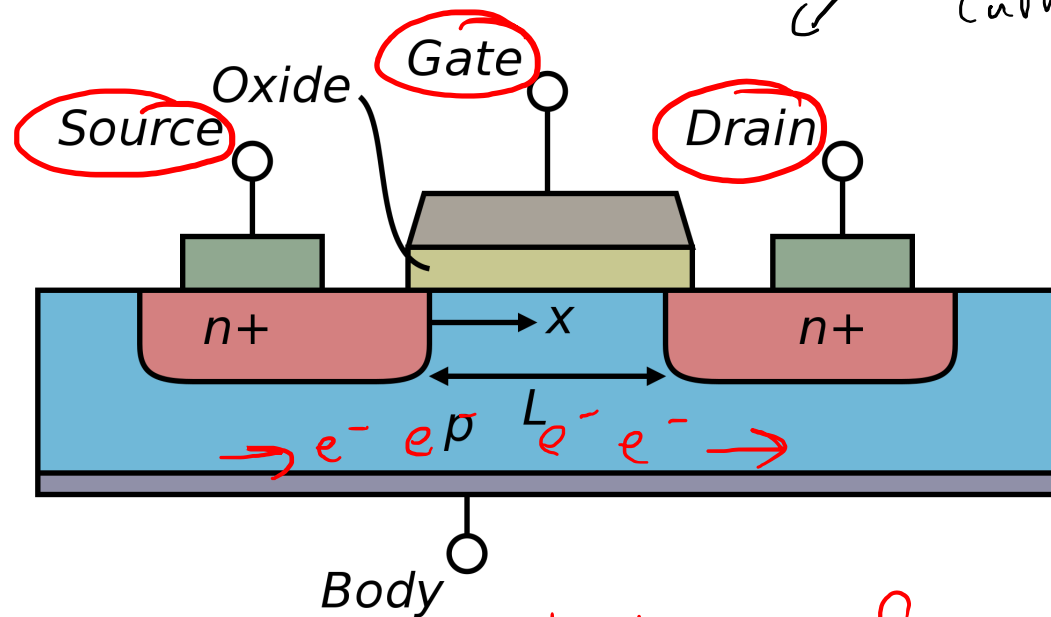
NOR



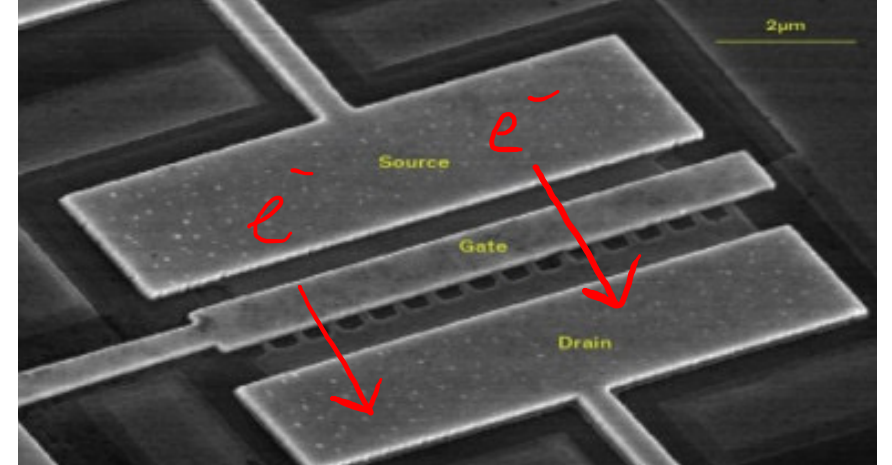
NOT

# MOSFETS → electronic switch

- Metal Oxide Semiconductor Field Effect Transistors ← name not on exam!
- MOSFETs (or just FETs)



electrons flows  
"current" flows  
source → drain  
drain → source

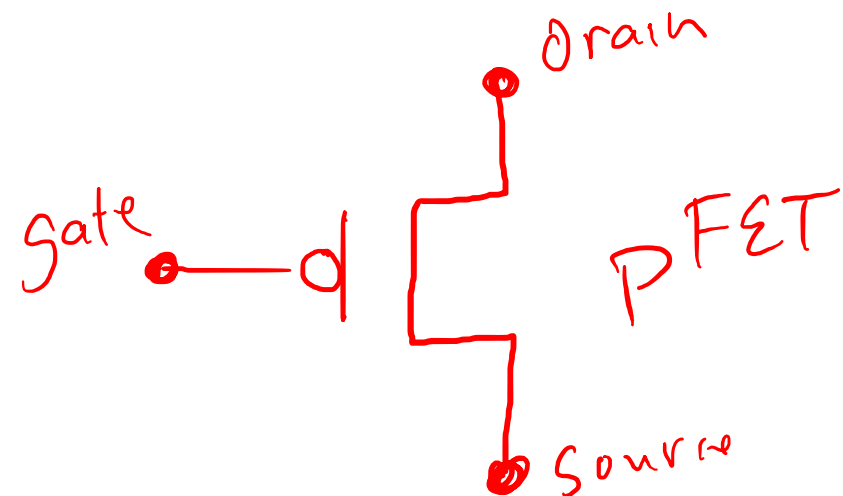
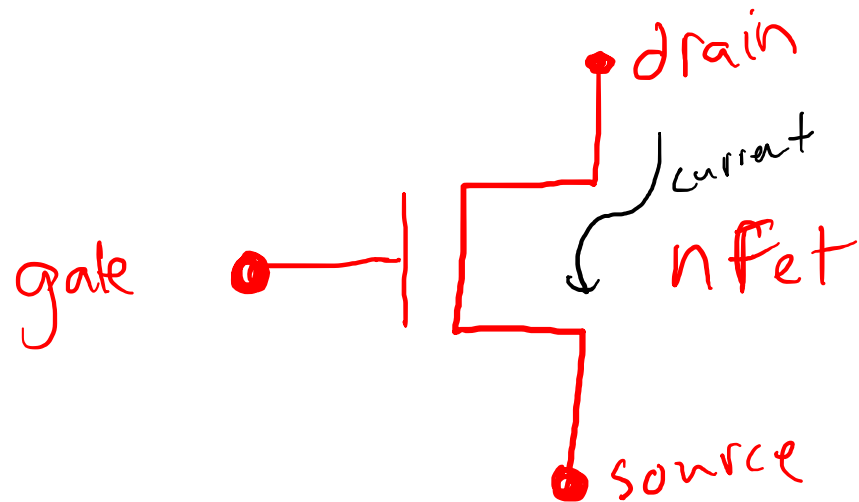


electrons flow from if

source to drain  
gate is "on"

# MOSFETS

- Two types of MOSFETs
  - N-Type (nFET)
  - P-Type (pFET)
- Behavior is exactly the opposite of each other



Digital electronic circuits are built from electronic switches that are called transistors instead of the mechanical switches and resistors.

The basic concept is the same—the switches (*transistors*) are arranged so that they can be turned on or off by signals carrying either LV or HV.

The transistor switches used in modern digital circuits are called “Metal Oxide Semiconductor Field Effect Transistors”, or *MOSFETs*(or just *FETs*).

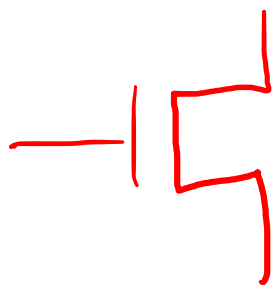
FETs are three terminal devices that can conduct current between two terminals (the source and the drain) when a third terminal (the gate) is driven by an appropriate logic signal.



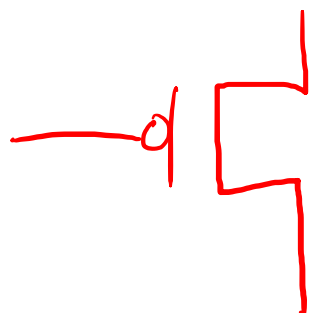
# MOSFETS

FET

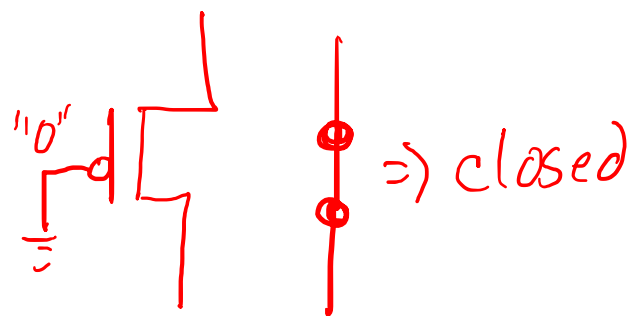
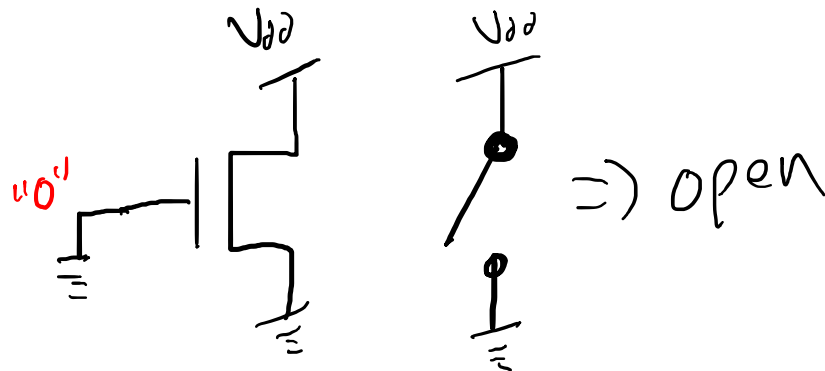
n FET



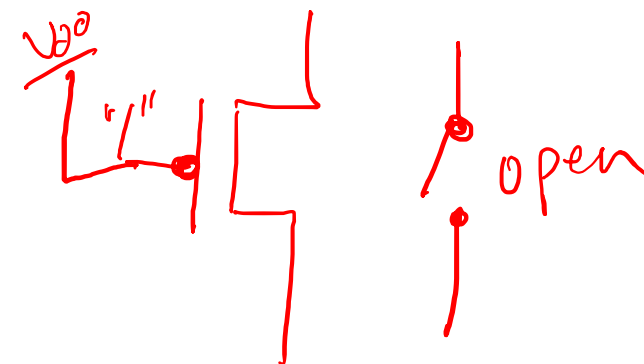
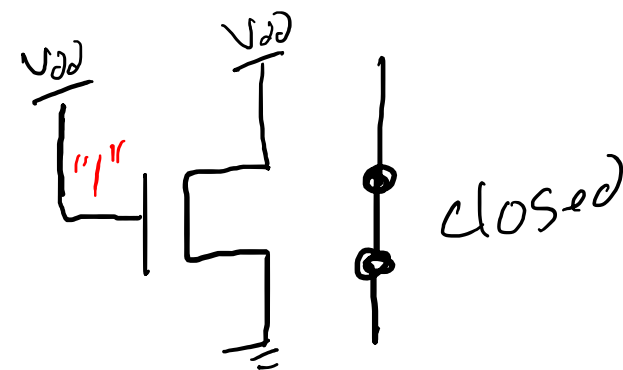
p FET



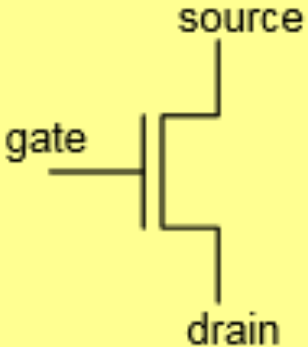
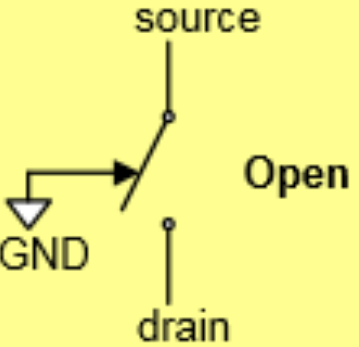
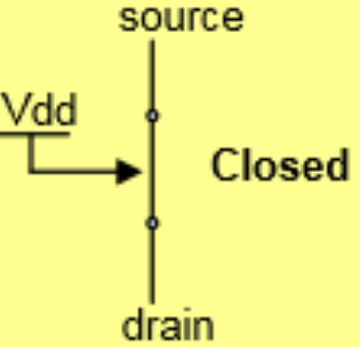
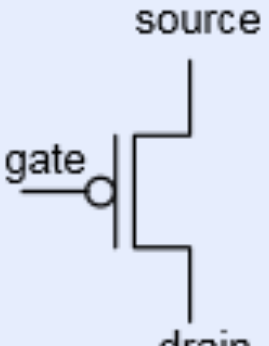
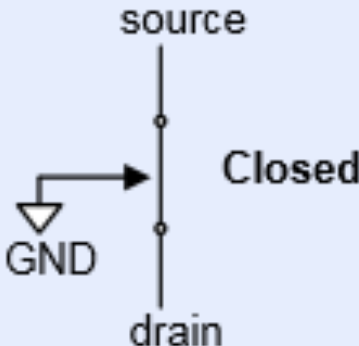
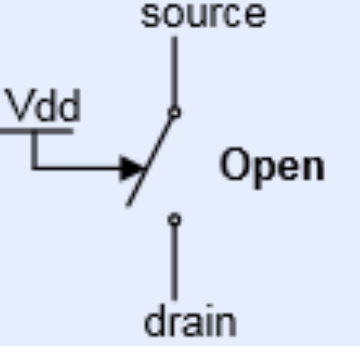
GND



VDD





	Symbol	$V_{gate} = GND$	$V_{gate} = V_{dd}$
<b>nFET</b>			
<b>pFET</b>			

## Switching Mode

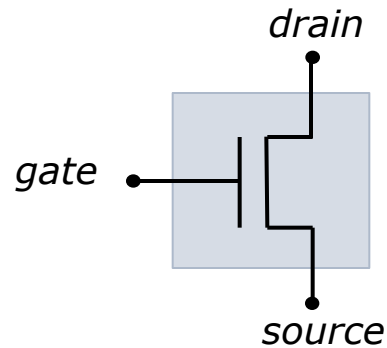
nFET is turned ON by high gate voltage.

pFET is turned ON by low gate voltage.

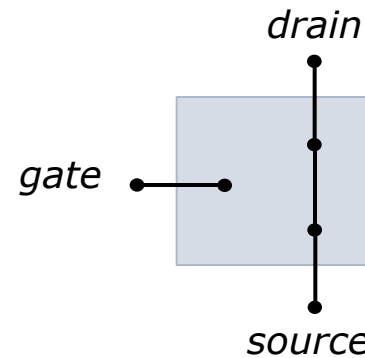
Gate	nFET	pFET
HV	ON	OFF
LV	OFF	ON

Equivalent circuits:

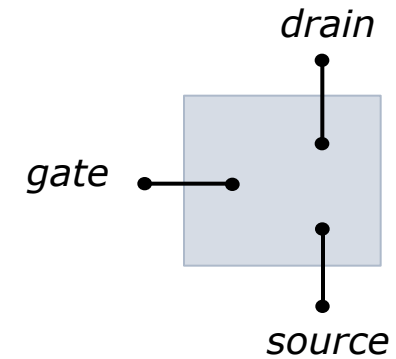
MOS FET:



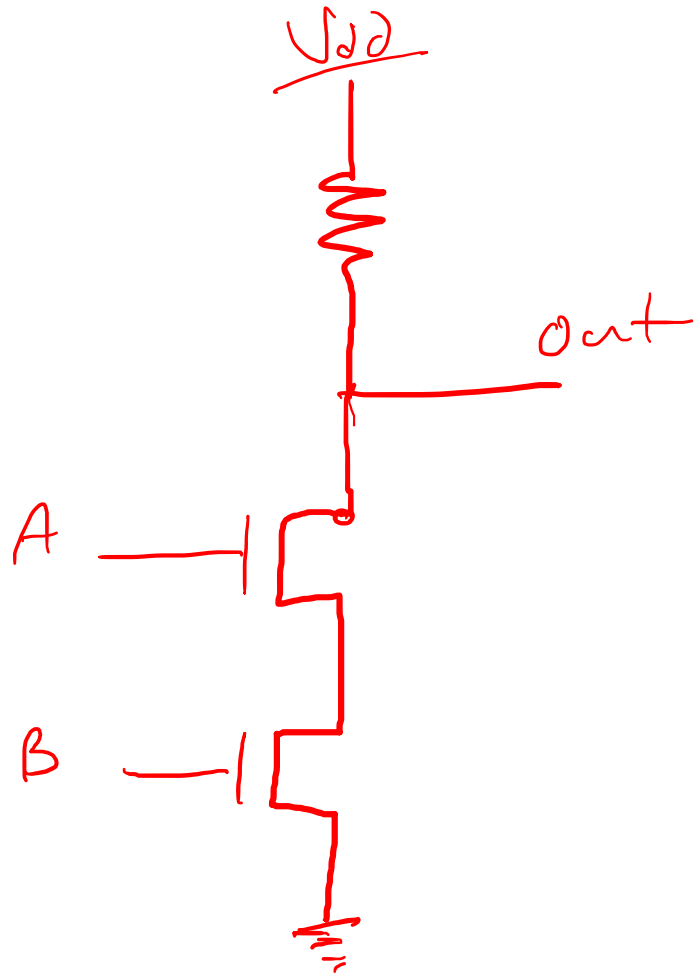
MOS FET is ON:



MOS FET is OFF:



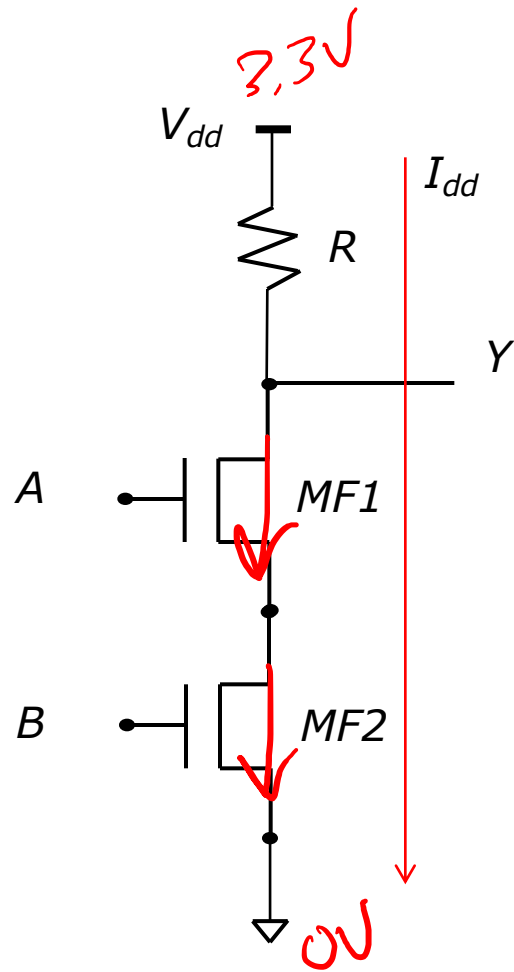
# NAND with nFETs



nFet =  
"1" → closed  
"0" → open

<u>A</u>	<u>B</u>	<u>Out</u>
0 <sub>pen</sub>	0 <sub>pen</sub>	1
0 <sub>pen</sub>	1	1
1	0 <sub>pen</sub>	1
1	1	0

## Analysis of nFET Based NAND Gate



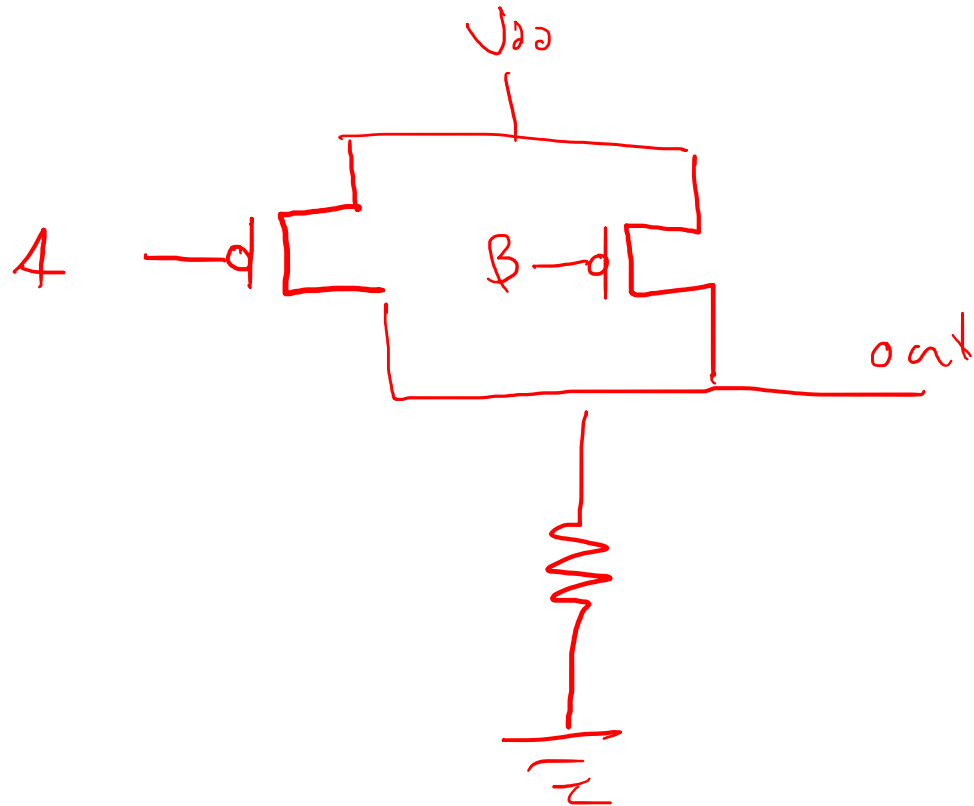
A	B	MF1	MF2	I	Y
LV	LV	off	off	0	HV
LV	HV	off	on	0	HV
HV	LV	on	off	0	HV
HV	HV	on	on	$V_{dd}/R$	LV

If we interpret HV as logic 1, and LV as logic 0, then we have the truth table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

This is inverted AND gate, or NAND gate!

# NAND with pMOS



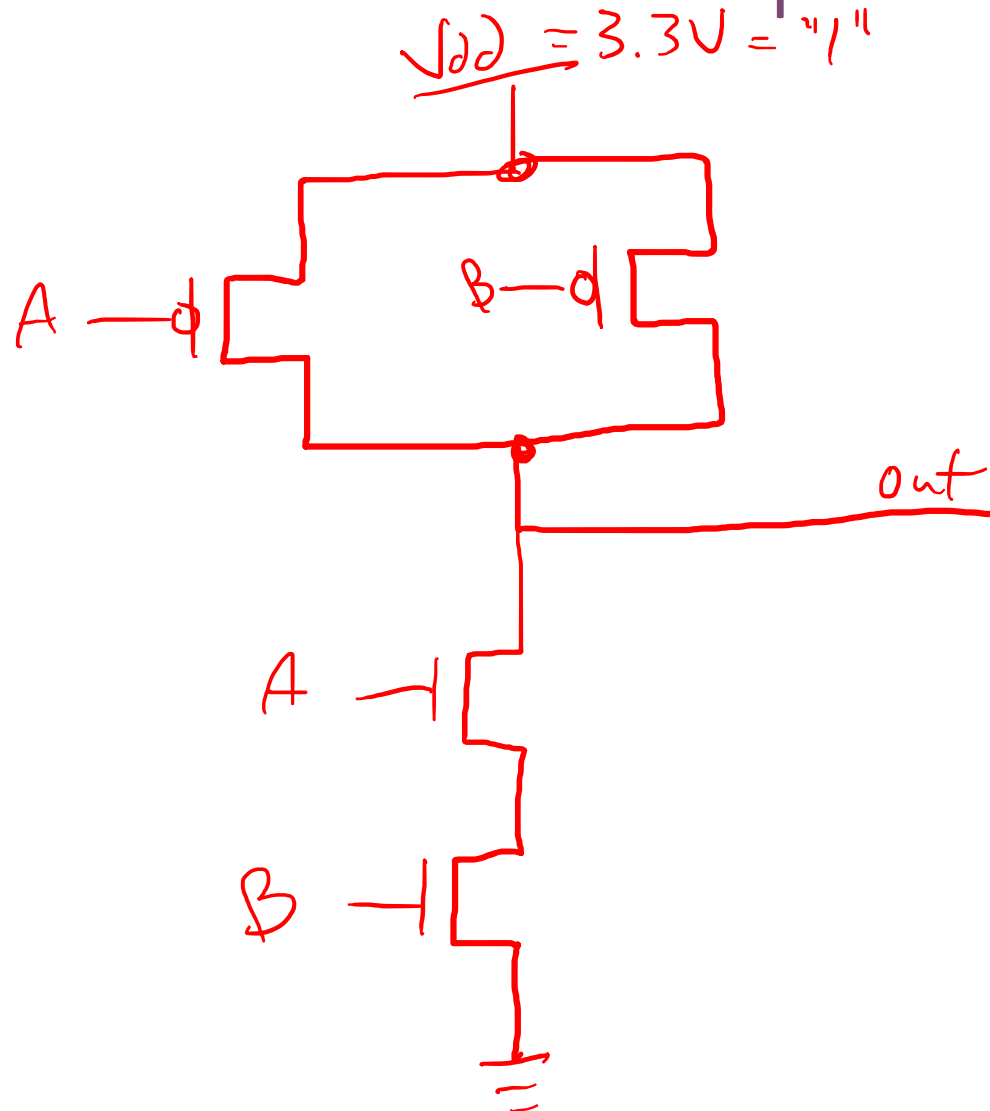
pMOS

0 = closed

1 = open

<u>A</u>	<u>B</u>	<u>out</u>
0	0	1
0	1	1
1	0	1
1	1	0

# NAND with Complimentary MOS (CMOS)



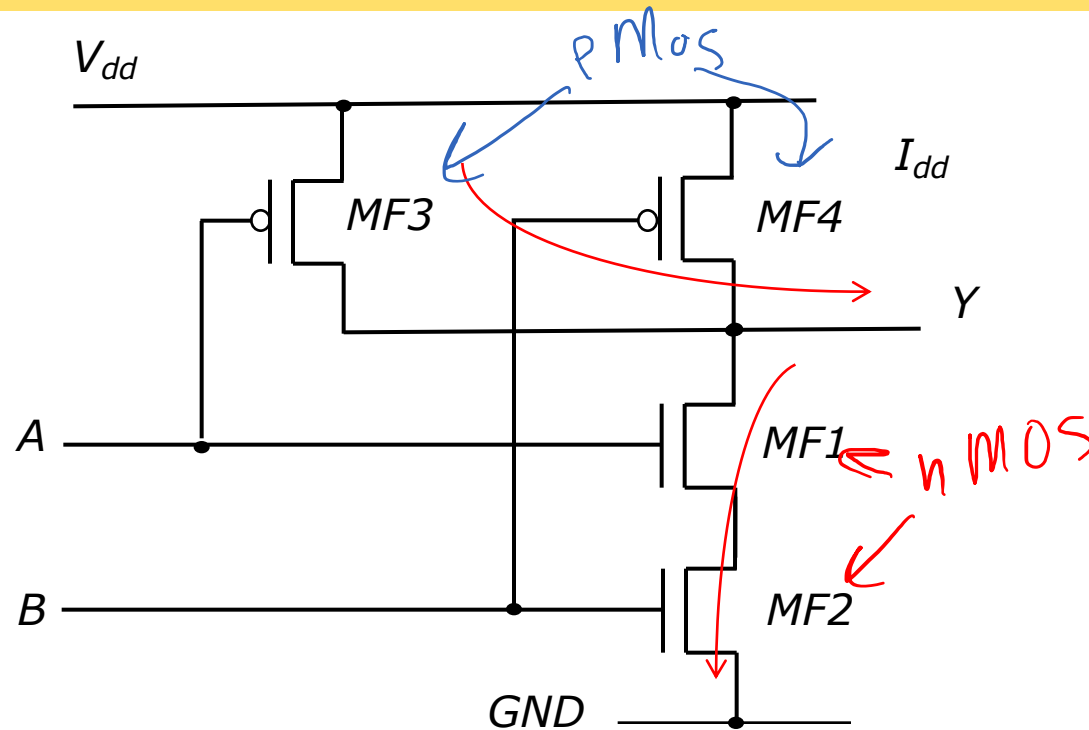
n Mos  
0  $\Rightarrow$  open  
1  $\Rightarrow$  closed

p Mos  
0  $\Rightarrow$  closed  
1  $\Rightarrow$  open

<u>A</u>	<u>B</u>
0	0
0	1
1	0
1	1

<u>out</u>
1
1
1
0

## CMOS NAND Gate



Both nFET and pFET transistors are used to implement the gate.

Advantage: no current from V<sub>dd</sub> to GND in either state, thus extremely low power dissipation.

A	B	MF1	MF2	MF3	MF4	I	Y
LV	LV	off	off	on	on	0	HV
LV	HV	off	on	on	off	0	HV
HV	LV	on	off	off	on	0	HV
HV	HV	on	on	off	off	0	LV

Because there is no current in either state, the CMOS gates have extremely low power dissipation.

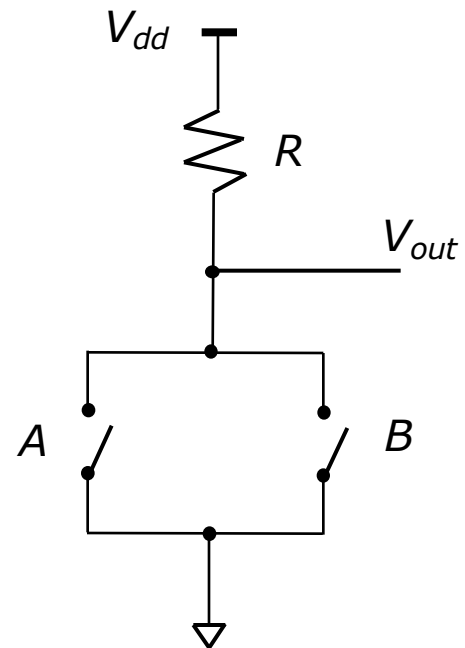
Dissipation is due to following effects:

- When the output switches from one logic level to another, there is a short period of time when all output transistors are ON, and the current flows from  $V_{dd}$  to GND.
- Gates have some parasitic capacitance, and during the switching of output from one voltage level to another, the output has to charge and discharge gates that are connected to the output.

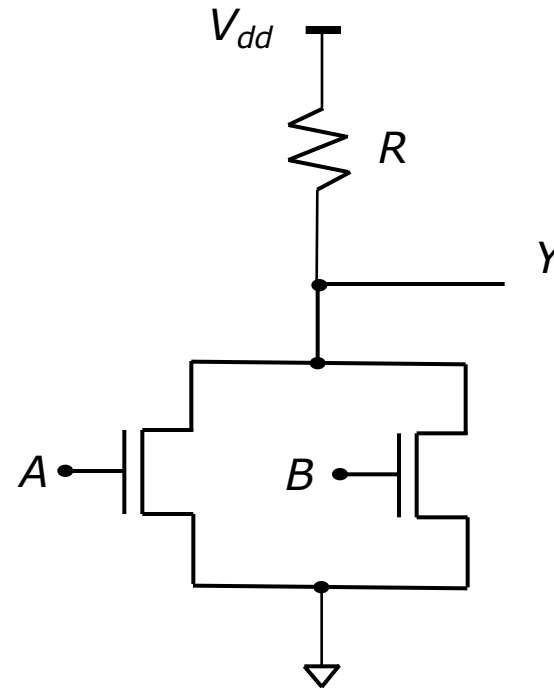
As the working frequency of CMOS gates increase, so will the power dissipation.



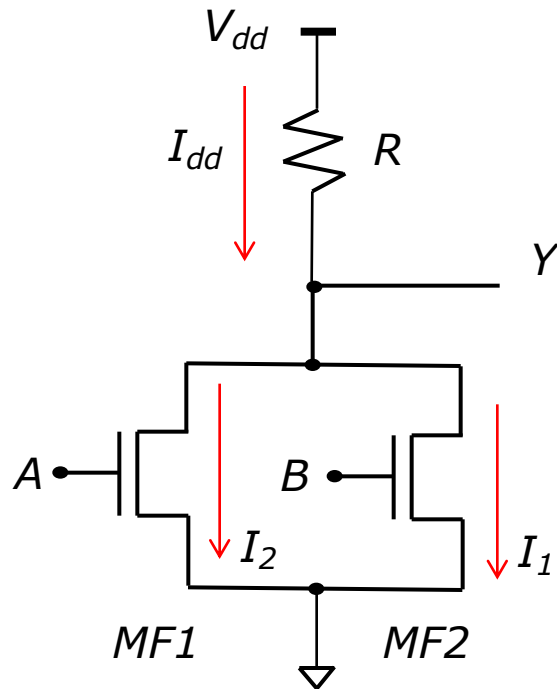
Mechanical:



Switches implemented by nFETs:



## Analysis of nFET Based NOR Gate



A	B	MF1	MF2	I	Y
LV	LV	off	off	0	HV
LV	HV	off	on	0	LV
HV	LV	on	off	0	LV
HV	HV	on	on	$V_{dd}/R$	LV

If we interpret HV as logic 1, and LV as logic 0, then we have the truth table:

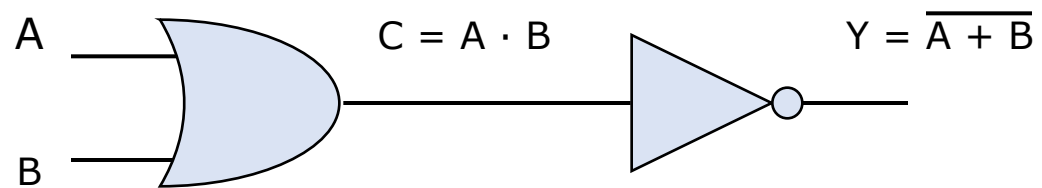
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

This is inverted OR gate, or NOR gate.

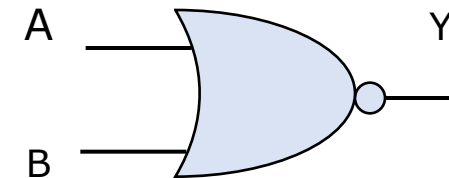
Truth table of a NOR gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

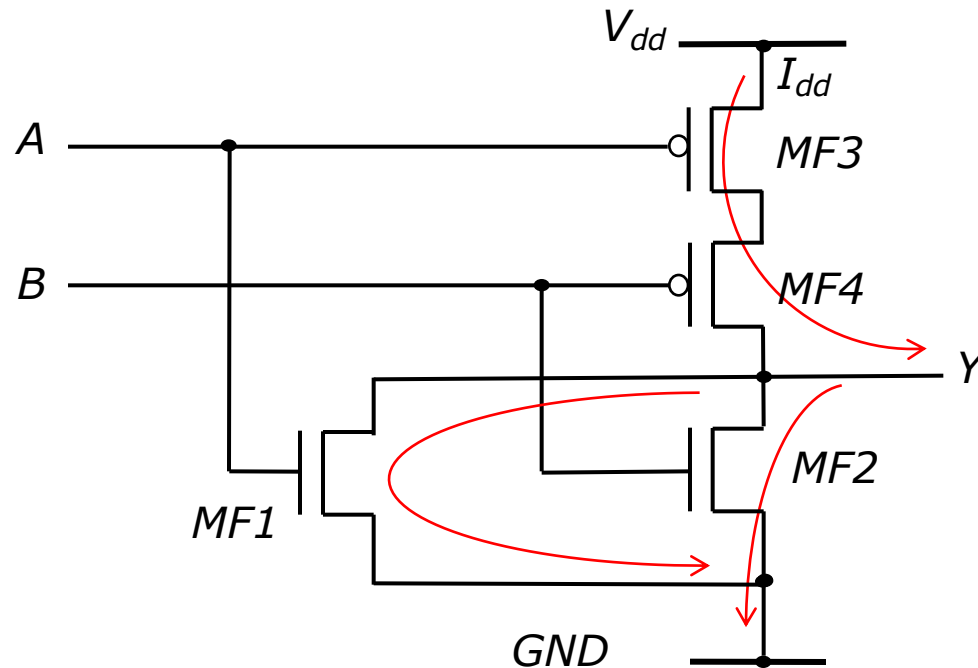
NOR gate is OR followed by NOT gate:



Graphical symbol of NOR gate:



## CMOS NOR Gate

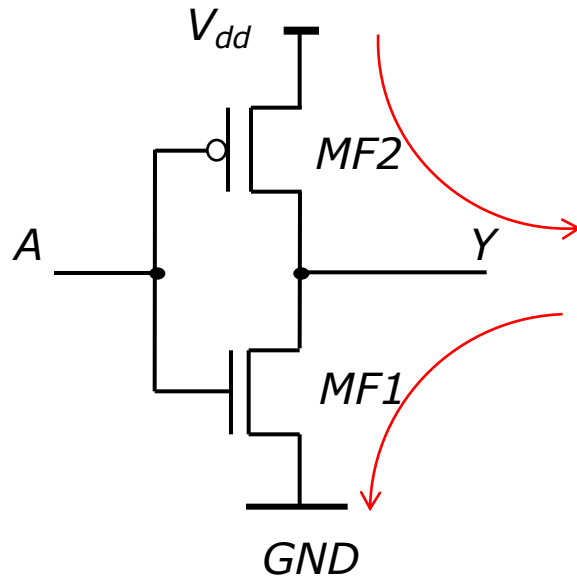


Both *nFET* and *pFET* transistors are used to implement the gate.

Advantage: no current from  $V_{dd}$  to *GND* in either state, thus extremely low power dissipation.

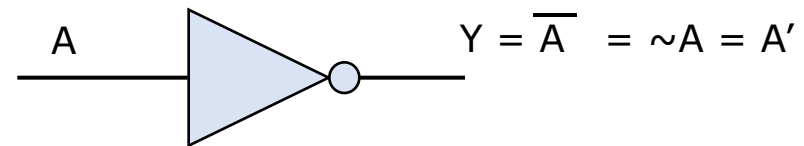
A	B	MF1	MF2	MF3	MF4	I	Y
LV	LV	off	off	on	on	0	HV
LV	HV	off	on	on	off	0	LV
HV	LV	on	off	off	on	0	LV
HV	HV	on	on	off	off	0	LV

CMOS inverter:



A	MF1	MF2	$I_{dd}$	Y
LV	off	on	0	HV
HV	on	off	0	LV

A	Y
0	1
1	0



# CMOS XOR?

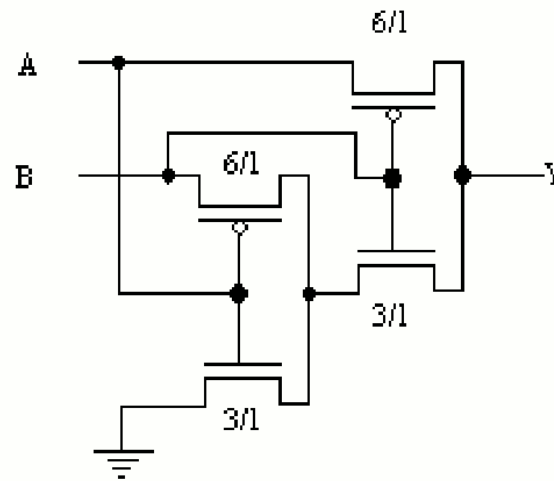
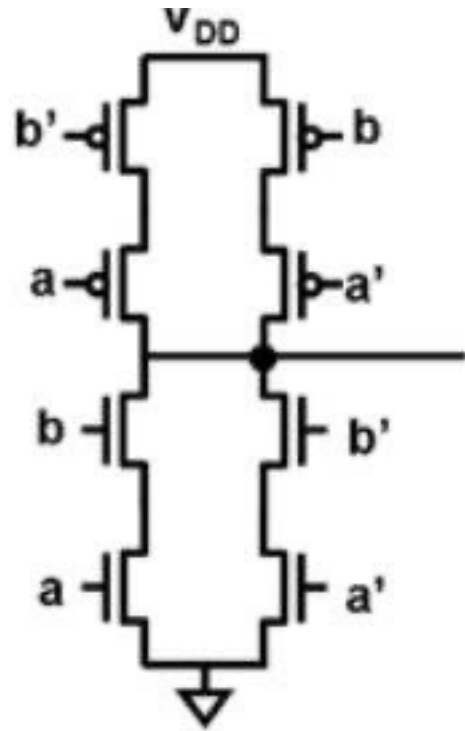


Fig. 1(c)

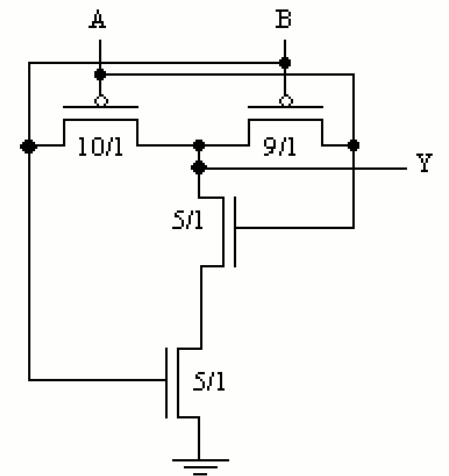


Fig. 1(d)

Fig. 1 Previous designs of XOR gates found in literature

# How a MOSFET works

- Yea, I'm not going to pretend I'm better than this guy...
- <https://www.youtube.com/watch?v=lcrBqCFLHIY>

Closer to physical reality:

- [@0.45](https://www.youtube.com/watch?v=tz62t-q_KEc)
- Add FinFETs
- [https://www.youtube.com/watch?v=TXxw1kdF5\\_Q](https://www.youtube.com/watch?v=TXxw1kdF5_Q)