University of Oslo
Department of Informatics

IN5180
Analog Microelectronics Design

Lab 2

UiO :

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1 Task 1: Design of a two stage operational amplifier

1.1 Specification and agenda

The goal of this task is to design an operational amplifier (opamp) with given specifications:

- Supply voltage (VDD) = 1.2 V
- External ideal reference current source 30 μA
- Differential to single ended gain above > 100 V/V
- Unity gain frequency (UGF) > 10 MHz
- Phase margin (PM) > 65 degrees
- Common Source Rejection Ratio (CMRR) > 40 dB
- Power Supply Rejection Ratio (PSRR) > 50 dB

The design into has been split to 2 parts: the differential stage and the common source (CS) stage. Each stage is designed separately maximizing amplification and keeping bandwidth above 10 MHz. After that we are going to tune the output voltage of the differential stage to the operational point of the CS stage. The next step is to find a proper compensation elements to satisfy PM requirements. Then, the CMRR and PSRR are studied with final tuning of the opamp circuit.

1.2 General consideration for the design

We have chosen an opamp design with the p-channel input stage since in this case the second stage has an n-channel input transistor which maximize the transconductance of the second stage and, hence, high frequency performance [1]. The length of all transistors are equal to 130 nm as double minimum length of the the TSMC65 process [2]. The width of each MOSFET is split to several fingers for a compact layout with proper performance.

We decided to use a capacitive load of 5 pF because it is close to expected capacitance of the membrane which is a dominant load for the opamp.

The main current mirror used for driving the circuit is shown in Fig. 1. We choose a total width of 1μm for the diode-connected pFET as adequate value convenient for calculation.

Our initial plan was to utilize the $\frac{g_m}{I_D}$ approach to estimate geometry for the amplifying transistors in both differential and CS stages. However, we received inadequate values for the widths of the MOSFET and decided to rely on the hand calculation (the square law model) complimented by the Cadence simulation.

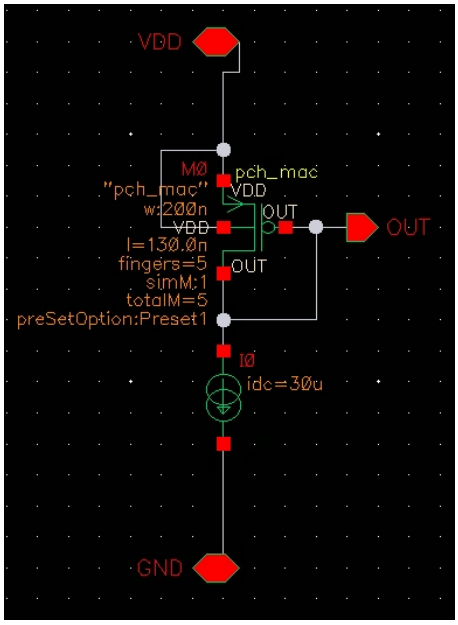


Figure 1

A few equations to be noted [1, 3]:

$$A_v = g_m r_{out}, \tag{1}$$

where A_v is a voltage gain of an CS amplifier, r_{out} is an output resistance, g_m is a transconductance of the amplifying MOSFET.

$$r_{ds} = \frac{L}{(\lambda L) I_D} \tag{2}$$

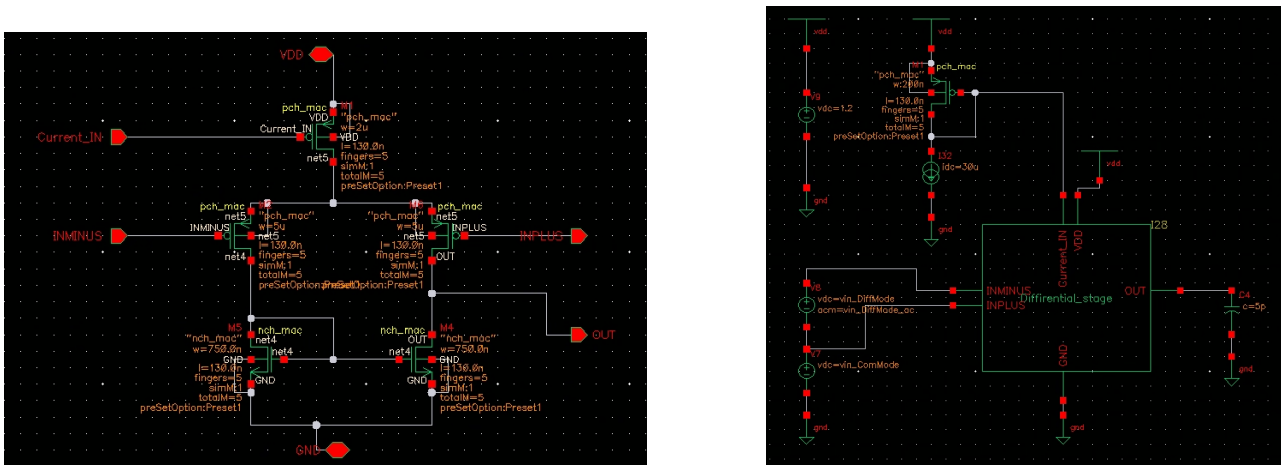
where r_{ds} is a drain to source resistance, λ is a output impedance constant, L is a channel length, I_D is a drain-to-source current, and (λL) - is a process parameter (0.1 and 0.15 μm/V for NMOS and PMOS, respectively, in the 45nm-process)

The square law model:

$$g_m = \sqrt{2\mu C_{ox}(\frac{W}{L})I_D}, \tag{3}$$

where μ is a carrier mobility, C_{ox} is a oxide layer capacitance, W is a width and L is the length of the channel.

1.3 Differential stage



(a) Schematics of the differential stage

(b) Testbench

Figure 2: Differential stage and its testbench

The differential stage with p-channel input transistors is shown in Fig. 2a. Transistor M1 acts as a current source, M2 and M6 is an amplifying MOSFETs, while M4 and M5 is a current mirror in the differential stage.

If we take a look on Eqs. (1), (2), (3) we can notice that the lower current is associated with higher gain. However, the UGF can be estimated as $UGF = \frac{g_m}{2\pi C_L}$, meaning that the higher current supply is necessary for a proper high frequency behaviour. Thus, we select W(M1) as 10 times of M0 in Fig. 1 to supply 300 μA.

The testbench for the differential stage is shown in Fig. 2b. The voltage source V7 is a common-mode input voltage, while V8 is responsible for the differential signal. The branch of the current-mirror common for both differential and CS stages is presented by transistor M1 and current source I32 similar to Fig. 1. The voltage source V9 provides is a power supply for the circuit, 5 pF capacitor is chosen as load.

We can estimate the required width of the amplifying transistors M2 and M6 using the square root model. The output resistance is equal to $(r_{ds6}||r_{ds4})$ and the differential gain of the differential pair can be determined similar to Eq. (1) as:

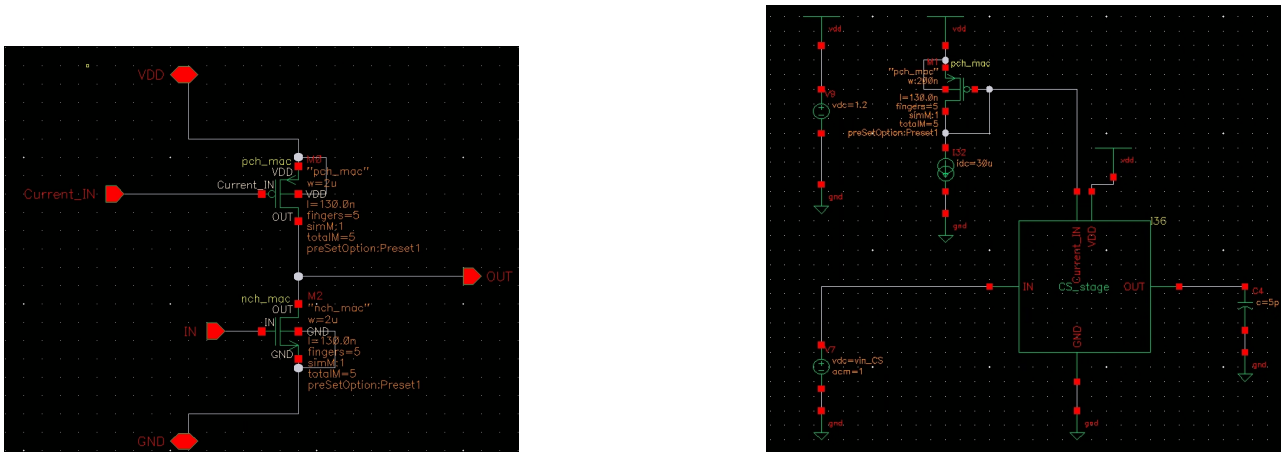
$$A_{v1} = g_{m1}(r_{ds2}||r_{ds4}) \tag{4}$$

The resistance of the MOSFET in saturation can be roughly found using Eq. (4) with I_d is equal to 300/2=150 μA. Therefore, $(r_{ds6}||r_{ds4}) \approx 3500$ Ohm and, if we'd like to obtain gain of A_v =20 V/V, the transconductance should be $g_{m6} = A_v/(r_{ds6}||r_{ds4}) \approx 5.7$ mS. The overdrive voltage can be expressed as $V_{eff} = \frac{2I_{D1}/g_{m1}}{2} \approx 0.05$ V and $W = \frac{2I_{D1}L}{\mu_n C_{ox} V_{eff}} \approx 11$ μm. Upon Cadence simulation, we correct the total widths W(M6) and W(M2) to 25 μm to obtain a proper voltage gain. The widths of M4 and M5 were optimized to get a output DC voltage optimal for the next CS stage and are discussed in Sec. 1.5.

A suitable DC common mode voltage V_{cm} is chosen using Parametric Analysis in Cadence when V_{cm} varies from 300 to 900 mV with an increment of 10 mV while AC-analysis is performed for each step. It revealed

that the optimal for our circuit value of V_{cm} is 480 mV because it gives a maximum UFG about 20 MHz and relatively high gain about 17 V/V.

1.4 Common-source stage



(a) Schematics of the common-source stage

(b) Testbench

Figure 3: Common-source stage and its testbench

The schematics of the CS stage is shown in Fig. 3a. Transistor M0 is a current source with a total width of 10 μm to supply about 300 μA of current to transistor M2. The latter is responsible for the amplification in the CS stage.

When we began to design this stage, we planed to refer to $\frac{g_m}{I_D}$ method. However, the values we got for W_2 were above 700μm, which is not considered to be adequate. Thus, we abandoned this method and turned back to square law model. Similar to hand calculation in 1.3, the optimum value for W_2 is found to be 4.5 μm for a expected voltage gain of 20. The testbench for the CS stage is very similar to that for the differential stage and is shown in Fig. 3b. Varying input DC voltage on the voltage supply V7, we can get a voltage gain on the output. However, we should take into account that while the amplification is higher in sub-threshold region, the bandwidth is higher in saturation. In addition to that, we can avoid some unpredictable behavior of the circuit keeping all the transistors saturated. Because of these considerations, the final width W_2 was chosen to be 10 μm. In this case, the operation point for M2 is above threshold voltage (V_{th} =525 mV) and equal to 570 mV. The final gain for this stage is 14.5 V/V and UGF is 66 MHz.

1.5 Two stage opamp. Stability and compensation

Firstly, we are going to combine both stages together and optimize the output DC voltage from the differential part to coincide with operational point of the CS stage. As discussed in the previous sub-chapter, the operational point for the CS stage is 570 mV. We found that the most efficient way to get this value on the output of the differential stage is to optimize the widths of transistors M4 and M5 in the current mirror in Fig. 2a. As it shown in Fig. 2a, the desired values for total widths $W4$ and $W5$ is 3.75 μm.

The total gain and UGF are presented in Fig. 4. The total gain is about 210 V/V (46.44 dB) and UGF is close to 500 MHz without a compensation circuit. That is a good result well above the required specs in Ch. 1.2. The especial attention was paid to verify that all the transistors operate in saturation with selected operation point and MOSFET parameters.

Now let us build a compensation circuit to get a desired stability and Phase Margin. The whole opamp with a compensation circuit is shown in Fig. 5. The compensation circuit consists of R_c and C_c in a feedback loop between input and output of the CS stage. The testbench to perform stability test ("*stb*"-analysis in Cadence)

is shown in Fig. 6. The opamp there is in voltage follower configuration with a probe IPRB0 breaking the feedback loop.

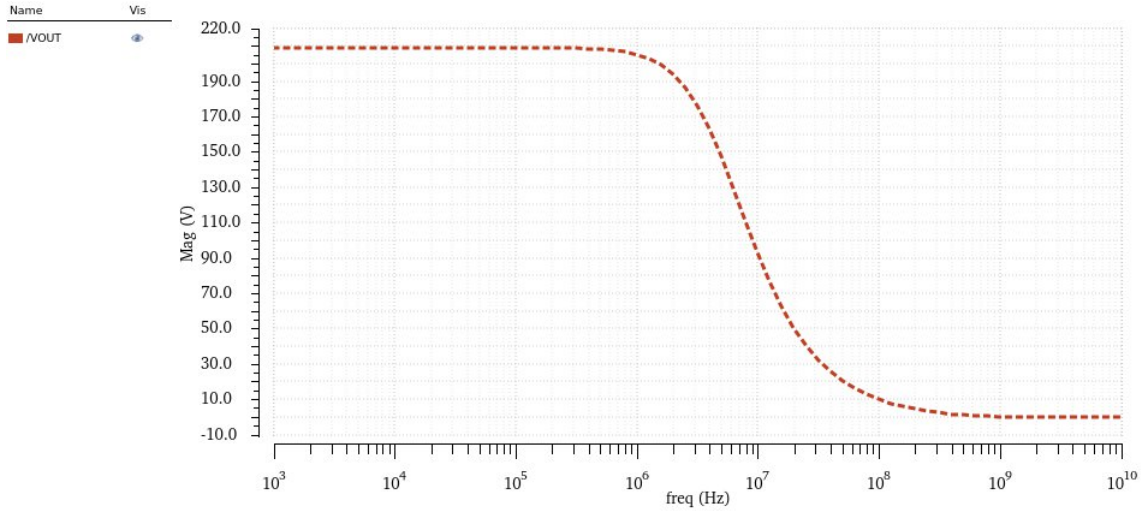


Figure 4: AC-analysis of the two stage opamp without compensation.

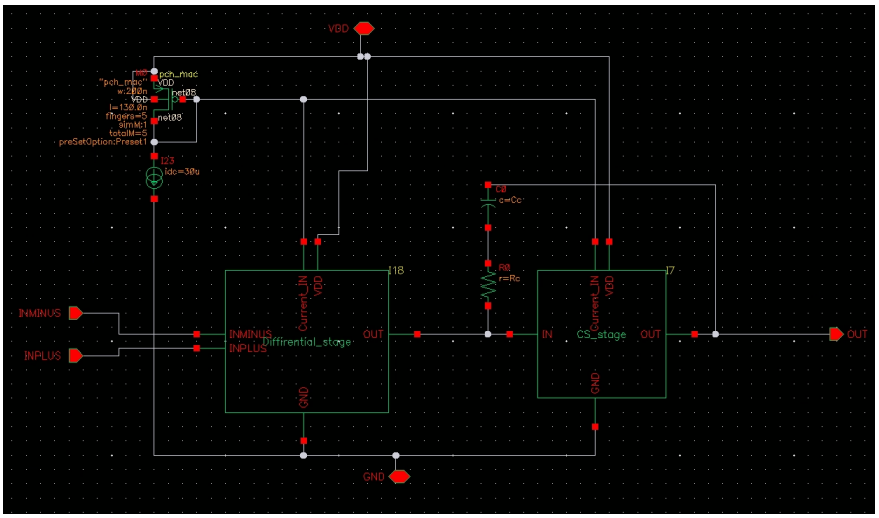


Figure 5: Schematics of the two stage opamp with the compensation circuit consisting of R_c and C_c

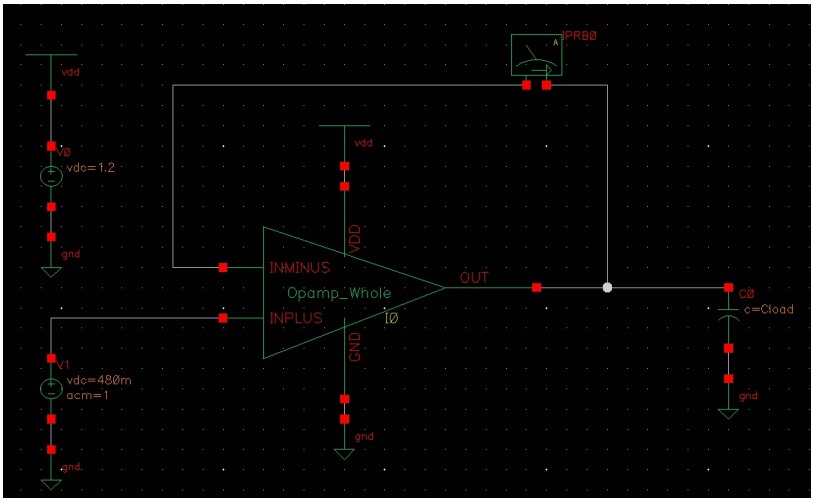


Figure 6: The two stage opamp with compensation circuit in voltage follower configuraion.

As a starting point, we plot the Bode plot for our opamp without compensation as shown in Fig. 7a. Despite the superior bandwidth of 608 MHz, we can see that PM is only 30.8°. We can distinguish two poles with frequencies about 5 MHz and 1 GHz and one zero giving phase growth above 10 GHz (LHPZ). We are going to utilize a procedure discussed in the lectures to split poles to get suitable PM [3]. The first pole will get much lower frequency while the second one will go below 0 dB to eliminate its contribution the amplifier performance. However, there is a trade-off between the stability and the bandwidth of the opamp.

The procedure for capacitive compensation is presented below.

1. First, the resistor is set to 0 Ohm and we tune only C_c. Starting with $C_C^{'} = (\beta \frac{g_{m1}}{g_{m7}})C_L$ setting unit gain frequency close to second pole. $g_{m7} = 1.16$mS (from the cadence simulation) $g_{m1} = 2.225$mS (from the cadence simulation) $\beta = 1$ (voltage follower configuration) C_L =5 pF
2. By simulating in cadence, find frequency with -125°phase shift (called $A^{'}$), this is the unit gain frequency ω_t target.
3. Choose new C_C such that ω_t is unit-gain frequency of L(s)
   - $C_C = C_C^{'} A^{'}$ phase margin
   - Simulate for several times.

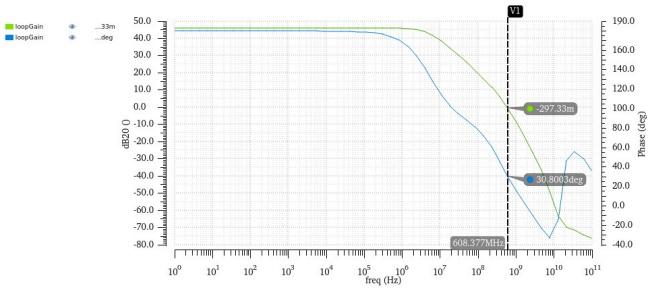
   The following values are obtained:
   - $C_{c1} = 0.52 C_L = 2.6$ pF, $w_{t1} = 31$ MHz, A_1 =1.73 V/V
   - $C_{c2} = C_{c1} \times A_1 = 4.498$ pF, $w_{t2} = 24.5$ MHz, $A_2 = 1.43$ V/V
   - $C_{c3} = C_{c2} \times A_2 = 6.43$ pF, $w_{t3} = 20$ MHz, $A_3 = 1.25$ V/V
   - $C_{c4} = C_{c3} \times A_3 = 8.04$ pF, $w_{t4} = 17.35$ MHz, $A_4 = 1.184$ V/V
   - $C_{c5} = C_{c4} \times A_4 = 9.52$ pF, $w_{t5} = 16$ MHz, $A_5 = 1.117$ V/V
   - $C_{c6} = C_{c5} \times A_5 = 10.63$ pF, $w_{t6} = 15.3$ MHz, $A_6 = 1.08$ V/V
   - $C_{c7} = C_{c6} \times A_6 = 11.5$ pF, $w_{t7} = 13.95$ MHz, $A_1 = 1.0$ V/V and it is a final value for C_c

The result of the capacitive compensation is shown in Fig. 7b. We can observe that capacitive compensation allowed achieving PM about 60°. However, we had to pay by much lower UGF equal to 13.5 MHz. The specs requires PM above 65°. One of the possible way to get higher PM is an introduction of a resistor (labelled as R_c) in the compensation circuit. The common procedure for that is listed below:

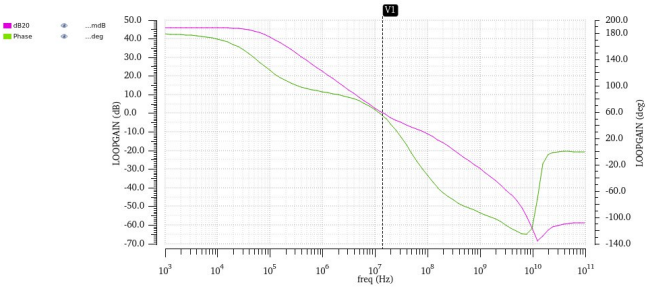
1. Choose $R_C = \frac{1}{1.7\omega_t C_C}$ giving phase margin of 85°(+30°) leaving 5° for variations.
2. Replace R_C with transistor $R_C = \frac{1}{\mu_n C_{ox}(\frac{W}{L} V_{eff})}$.

We have tried to use formula above to find R_c. However, we obtained a quite high resistance of 3.6 kOhm which disturbed the phase of the opamp significantly. To avoid it, we decided to perform stability test using Parametric Analysis in Cadence sweeping R_c from 0 to 1000 Ohm and choosing appropriate value. The best-fitting R_c is found to be 600 Ohm. The Bode plot for the opamp with capacitive-resistive compensation is shown in Fig. 7c. After the final compensation the PM is about 90°. The UGF is not affected by the resistive compensation and still equal to 13 MHz. The resulted PM is well above the required 65° from specs. We estimated in Cadence that the designed opamp can drive much higher capacitive load with acceptable PM. Only $C_L = 20$ pF can decrease PM to 65°.

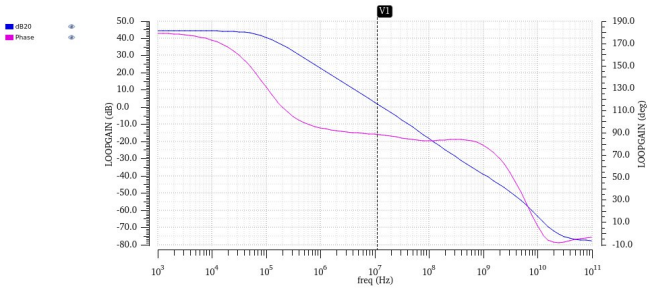
The next task in this lab is to develop comparator. The easiest way to do that is to make a cascade of opamps. However, the bandwidth of comparator BW_{tot} is significantly lower than that of single opamp BW and defined as $BW_{tot} = BW\sqrt{2^{1/N} - 1}$, where N is a total number of opamps in the cascade. Hence, it is beneficial to sacrifice some PM to get a higher BW of the opamp. To do that, we decided to reduce C_c and increase R_c. In addition to higher BW we also save an area occupied by the capacitor. The final Bode plot of opamp with the updated compensation is shown in Fig. 7d. In this configuration, the UGF is 45 MHz and the PM is 76° which is also above the required specification of 65°.



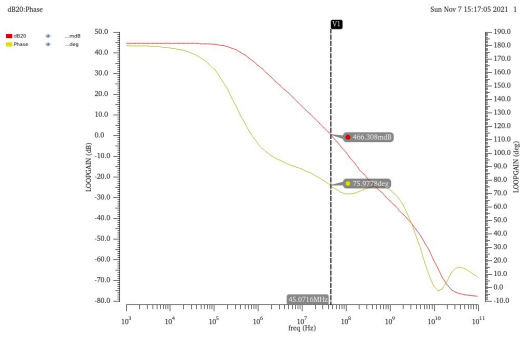
(a) Bode plot of the opamp without compensation: gain in dB (green line), phase (blue line).



(b) Bode plot of the opamp with C_c=11.5 pF



(c) Bode plot of the opamp with C_c=11.5 pF, $R_c = 600$ Ohm



(d) Bode plot of the opamp with C_c=3 pF, R_c = 800 Ohm

Figure 7: Bode plot of the opamp at different stages of compensation

1.6 Common mode and power supply and rejection ratios

The common mode rejection ratio (CMRR) is a parameter defined as a ratio of differential-mode gain to the common-mode gain: CMRR illustrates an ability of the opamp to reject common mode signals: CMRR $= 20\log_{10}\frac{A_d}{A_{CM}}$. The power supply rejection ratio is a similar term defined as a ratio of differential-mode gain to the gain of power supply voltage variation PSRR $= 20\log_{10}\frac{A_d}{A_{vdd}}$.

To study CMRR and PSRR, we build a testbench shown in Fig. 8. Then, we perform "xf"-analysis in Cadence to investigate an impact of each voltage supply on the output voltage for our opamp. We use two separated voltage sources for VDD and GND to distinguish their PSRR. To optimize PSRR and CMRR, we decided to vary the DC operational point V_{cm}. In this case we sacrifice a bit of gain, but it helps to improve CMRR and PSRR. The results are presentted in Fig. 9. CMRR improved from 41 dB to 48 dB, PSRR(vdd) increase from 42 dB to 53 dB, while PSRR(gnd) drops from 50 dB to 47 dB. We also sacrificed only 2 dB in differential gain (from A_{diff} =46 dB for $V_{cm} = 480$mV to A_{diff} =44 dB for $V_{cm} = 350$mV).

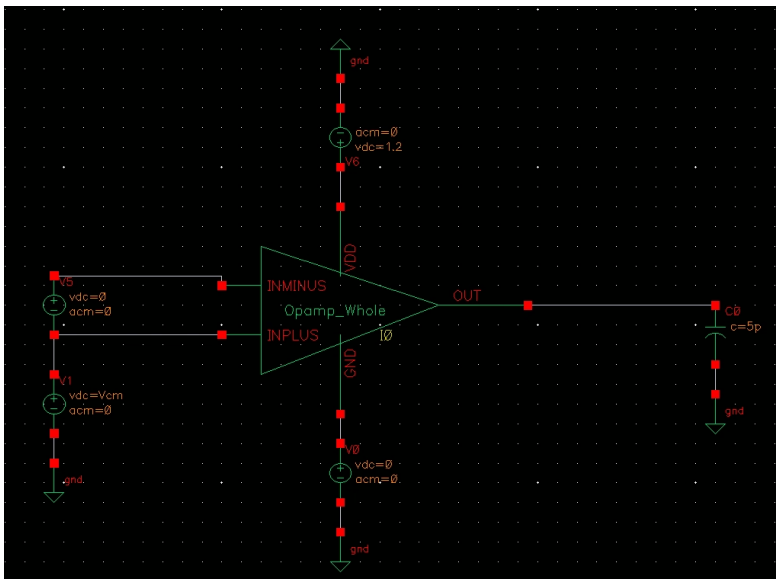


Figure 8: Testbench for CMRR- and PSRR-analysis

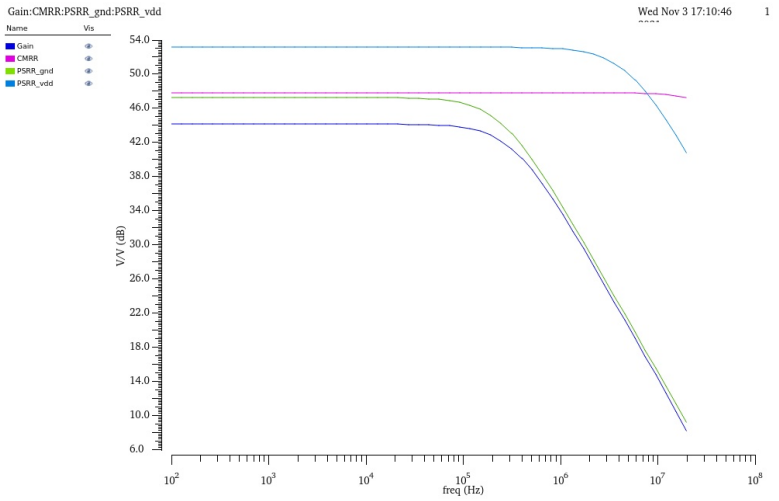
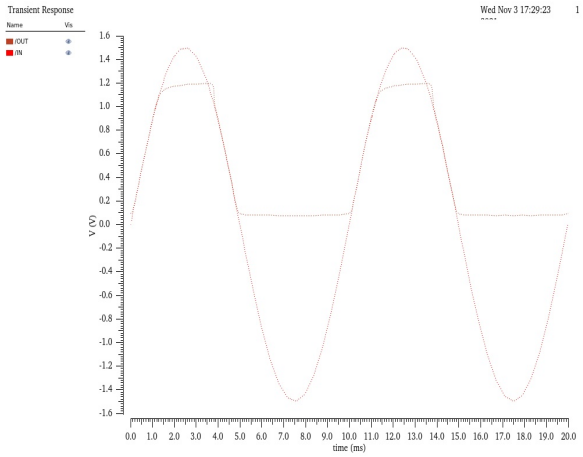


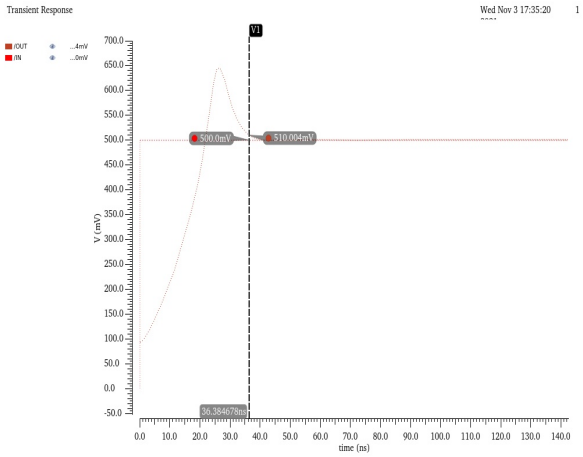
Figure 9: Gain, CMRR and PSRR for the opamp.

1.7 Slew rate, Output Swing, Settling time and Power Consumption of the opamp

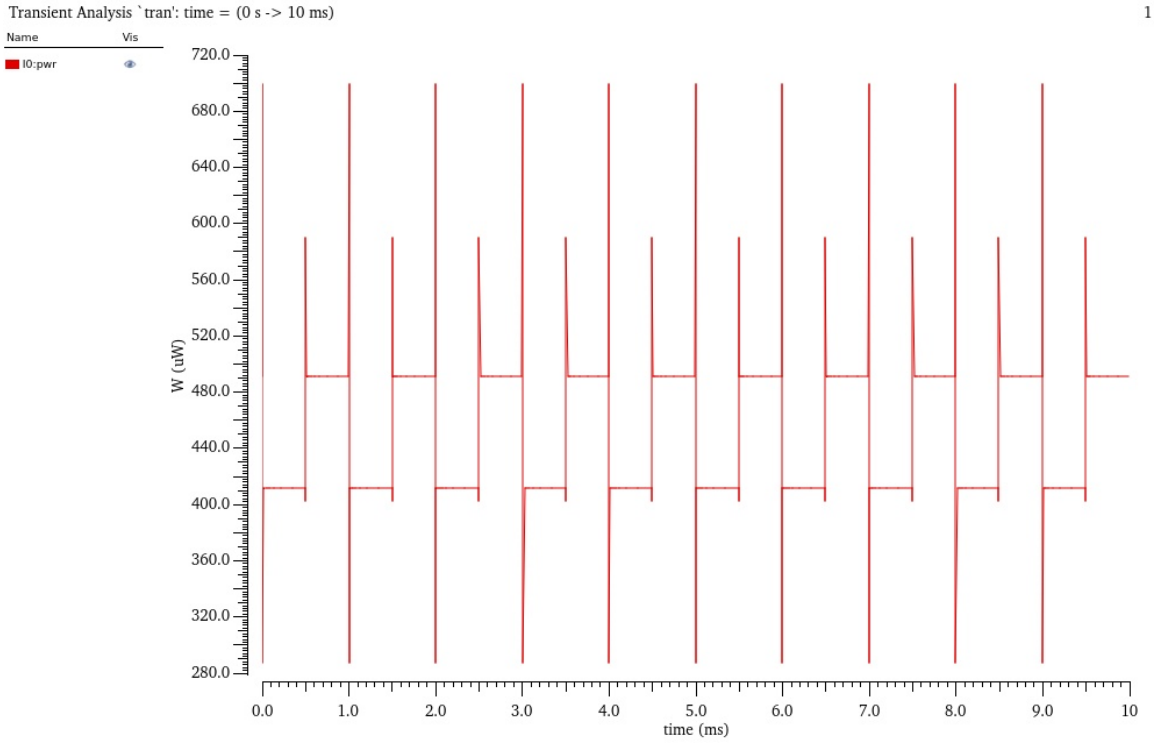
We performed a transient analysis of the opamp in the voltage follower configuration to study output swing, slew rate and settling time. The results are shown in Fig. 10. While we keep V_{dd} at 1.2 V we applied an input voltage above V_{dd} to study maximum output voltage. The latter is fount to be almost equal to 1.2 V (see Fig. 10a). The response of the voltage follower to step function is shown in Fig. 10b. There is a 30% overshoot for the output voltage but it stabilizes during 36 ns (margin 2% of the final value) which is fast enough for our goal in next task. The slew rate is about 28 V/μS which is also a satisfying result. The power consumption in case of the pulsed input voltage is demonstrated in Fig. 10c.



(a) Output swing



(b) Settling time and slew rate



(c) Power consumption

Figure 10: Transient analysis of the opamp

1.8 The final specs for the designed opamp

- Supply voltage (VDD) = 1.2 V
- External ideal reference current source 30 μA
- Differential to single ended gain above 161 V/V (44.145 dB)
- Unity gain frequency (UGF)= 45 MHz
- Phase margin (PM)= 75° for C_L = 5pF
- CMRR= 47.8 dB
- PSRR = 53.2 dB for VDD; PSRR = 47.2 dB for GND
- Slew Rate 28 V/μs
- Settling time 36 ns for 500 mV input step

The gain of the opamp should be high enough to provide a required sensitivity for the neural model. PM is important for stability during driving capacitive load of membrane. The opamp is intended to be used in the comparator design and should be fast enough to deal with μs-pulses. Slew rate, BW, and settling time reflects the speed of the opamp.

1.9 The layout, DRC and LVS reports for the 2-stage opamp

In this section, we are going to present the layout and its relevant checks, the DRC and LVS reports (to be enclosed in the appendix). Eight MOSFET are placed in the left part of the layout while resistor *rnondwo* and huge capacitor *crtmom* are on the right. The capacitor occupies most of the silicon area. Thus, even a capacitor of 3 pF requires a lot of space on the chip.

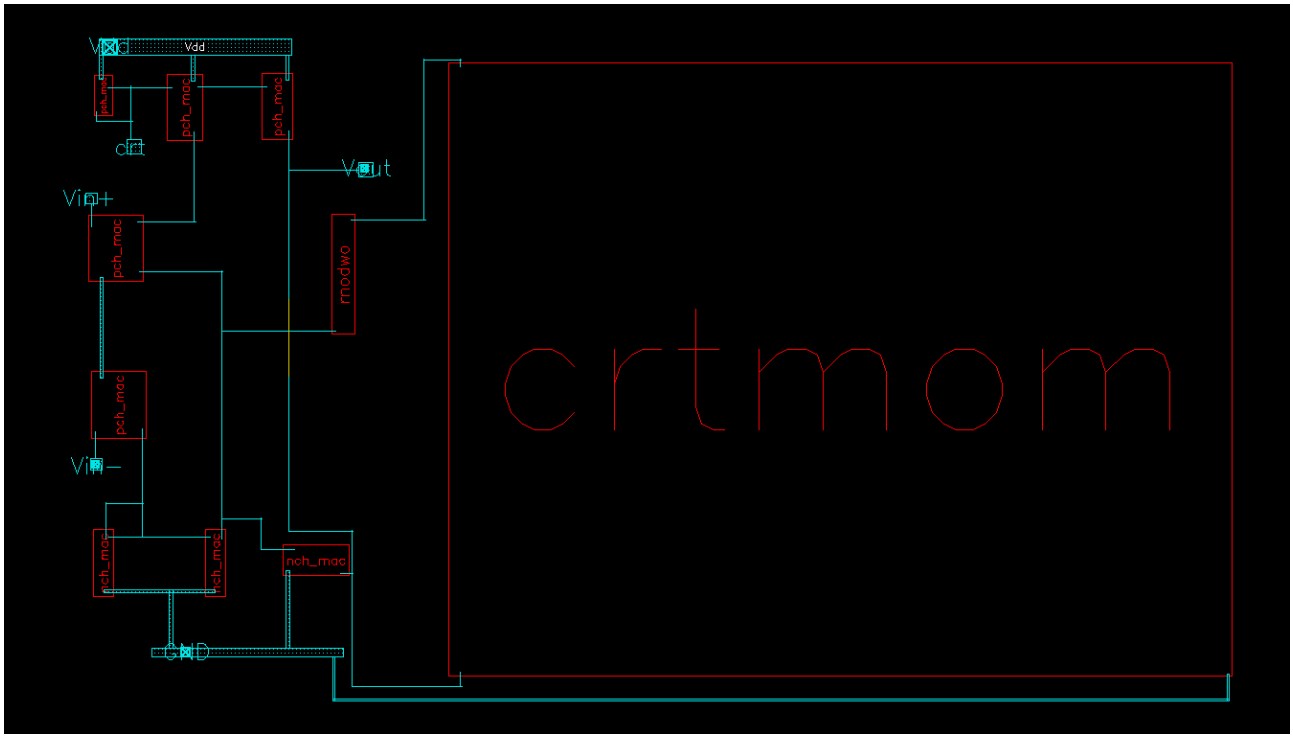


Figure 11: Layout view for 2 stage opamp, including both differential and common source stages.

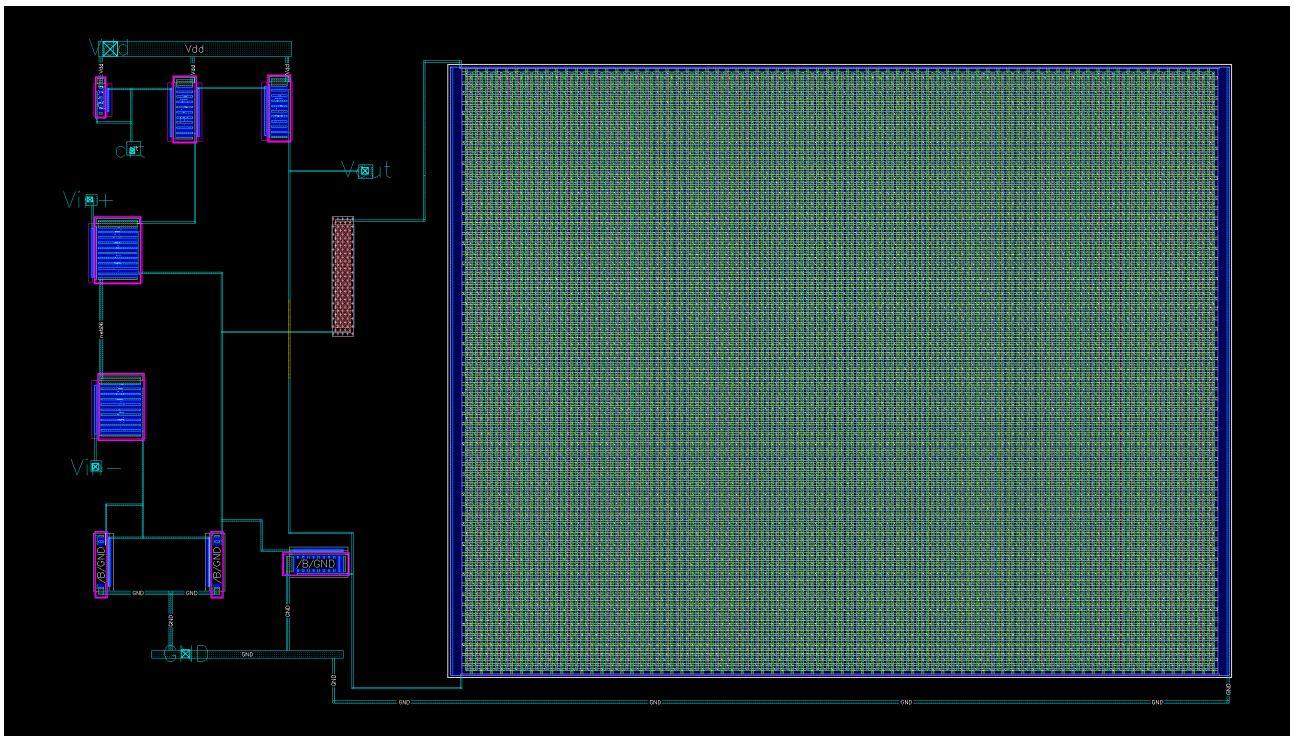


Figure 12: Layout view for 2 stage opamp, including both differential and common source stages.

2 Task 2: Design of comparator

We have chosen to develop a comparator based on the opamp from the previous task. We considered two possible schematics: a clocked opamp-based comparator and a regular opamp-based circuit.

2.1 The clocked comparator

The clocked comparator schematics is shown in Fig. 13. The circuit is based on the schematics from Fig.10.11 in Ref. [1]. This design helps to dimish the input offset. The main clock ϕ_2 connects the input to the cascade of opamps during the comparison phase when both opamps are in open loop configuration. The clocks ϕ_1, ϕ_1, ϕ_{11}, ϕ_{111} are activated during the reset phase when the input voltage is disconnected and both opamps are in voltage follower configuration with input connected to the ground via capacitor. These clocks have a different durations to eliminate the charge-injection effects. The timing of all clocks are shown in Fig. 14a.

The output voltage $OUT2$ from this comparator is shown in Fig. 14b together with the main clock $phi2$. During first 1 ms the input voltage V_{in} is 500 nV lower than the reference voltage and the $OUT2$ is about 0 during the clock comparison phase (when $phi2 = 1.2$ V). Between the clock cycle time the output voltage $OUT2$ demonstrates some pattern but this signal is not "recorded" since $phi2 = 0$ V. During next 1 ms V_{in} is 500 nV higher then the reference voltage and the $OUT2 = 1.2$ V during the comparison phase meaning than device has a sensitivity about 500 nV. Between the clock cycle time the output voltage has the same pattern which is again not recorded. This clocked design has a bit higher sensitivity that the the regular opamp-based circuit but has a lower operational speed (the clock period is 10 μs). In general, the clock period can be decrease but the procedure is complicated because of difficulty of tuning four different clocks. Thus, we have chosen to continue with a regular opamp-based circuit.

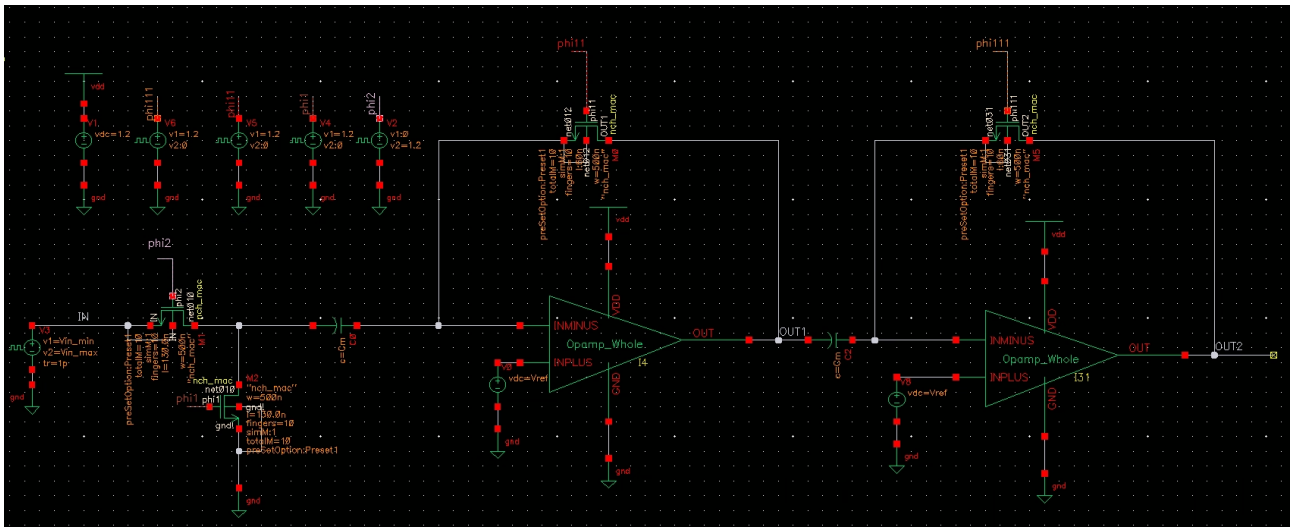
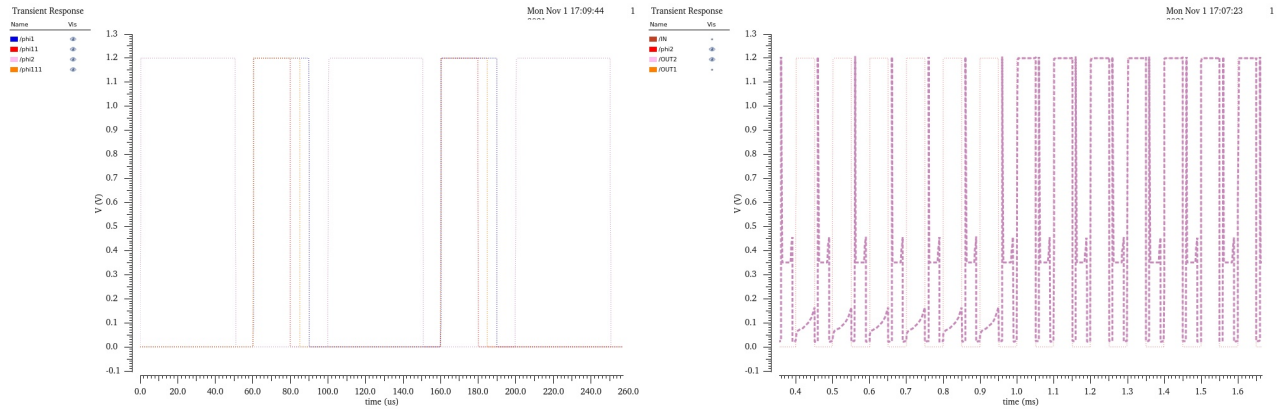


Figure 13: Clocked comparator with two opamps



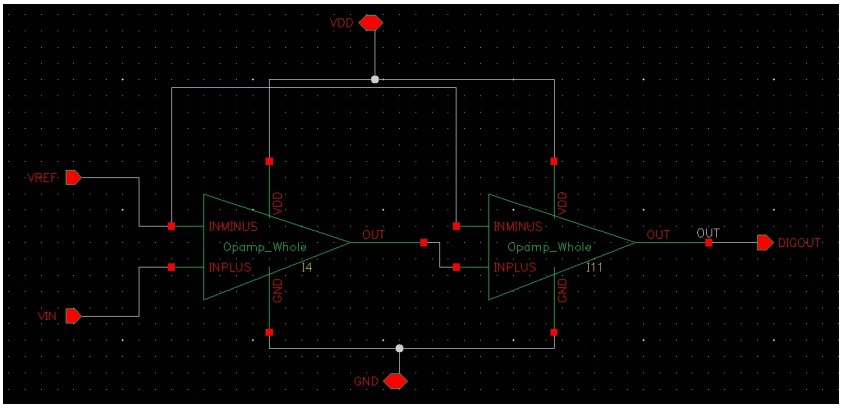
(a) Illustration of all clocks used in the design

(b) Output voltage $OUT2$ and the main clock $phi2$.

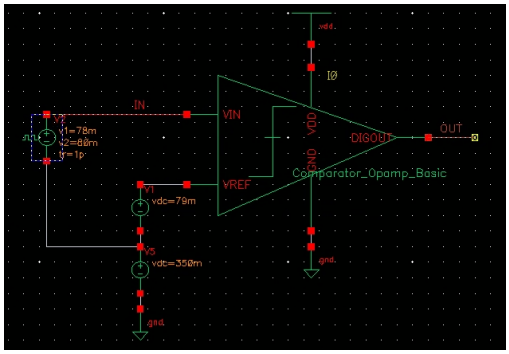
Figure 14: Results for the clocked comparator.

2.2 The non-clocked opamp-based comparator

The easier approach is just to connect two opamps in cascade as shown in Fig. 15a. We should take into account that both inputs should be also connected to common mode voltage of 350 mV (operation point for our opamp). This circuit simply amplifies the difference between inputs up to maximum output voltage 1.2 V if $VIN > VREF$ or to 0 V if $VIN < VREF$. The testbench for this comparator is presented in Fig. 15b. The sensitivity of this schematics is below 1 mV meaning that the device distinguishes 1 mV-difference between VIN and $VREF$ as shown in transient analysis in Fig. 16. The input voltage is a pulses from 78 to 80 mV while the reference voltage is 79 mV with a period of 3 ms. The speed is good enough to record pulses with period of 1μs . These specifications is enough for application with the neural model in Task 3.



(a) Basic comparator based on two opamps



(b) Testbench for the basic comparator

Figure 15: Basic comparator and its testbench.

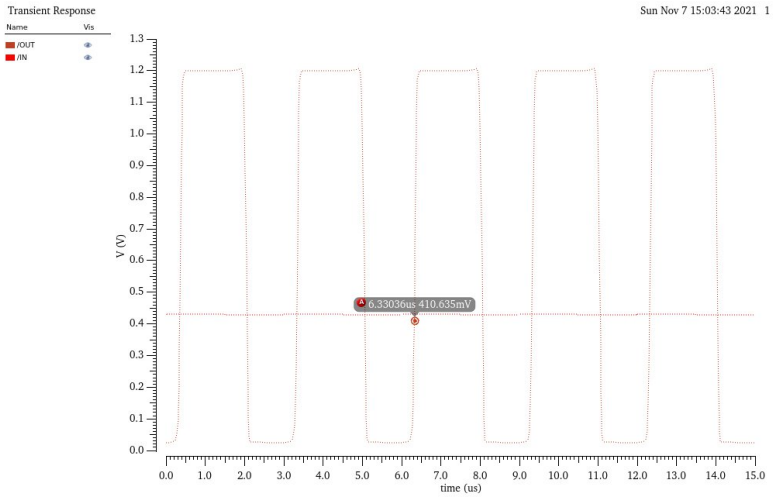


Figure 16: The performance of basic comparator circuit

The power consumption of the designed comparator is comparable with the consumption of two opamp. As it shown in Fig. 17, it is up to 900 mW.

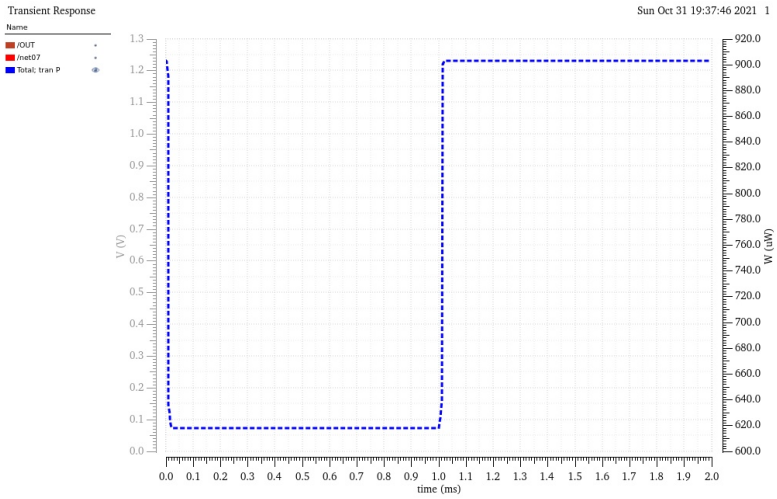
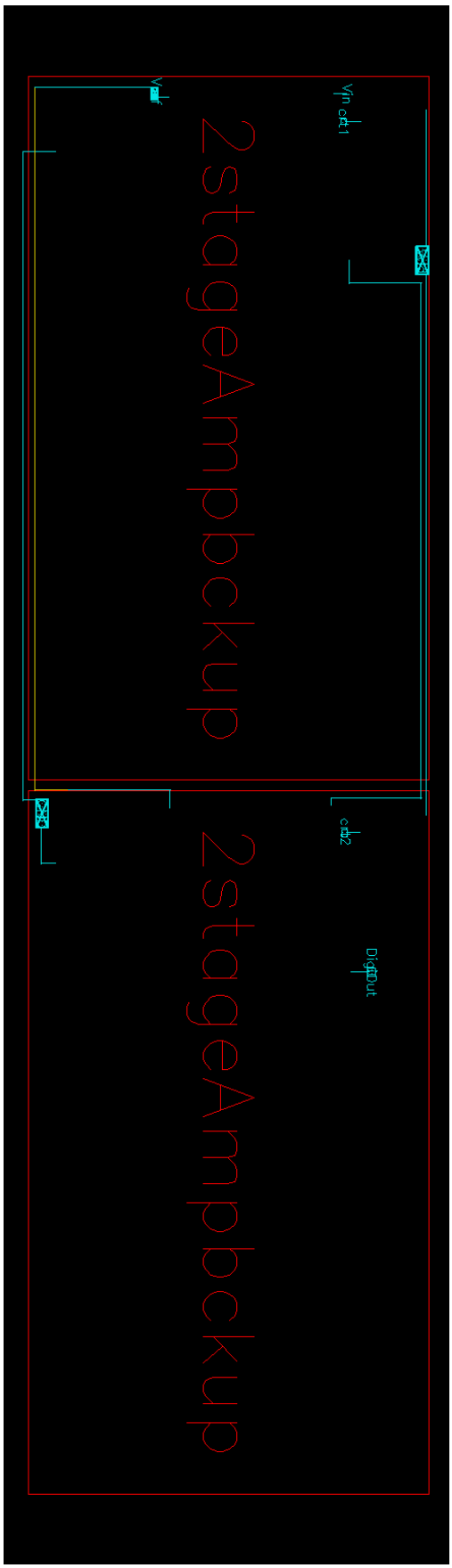


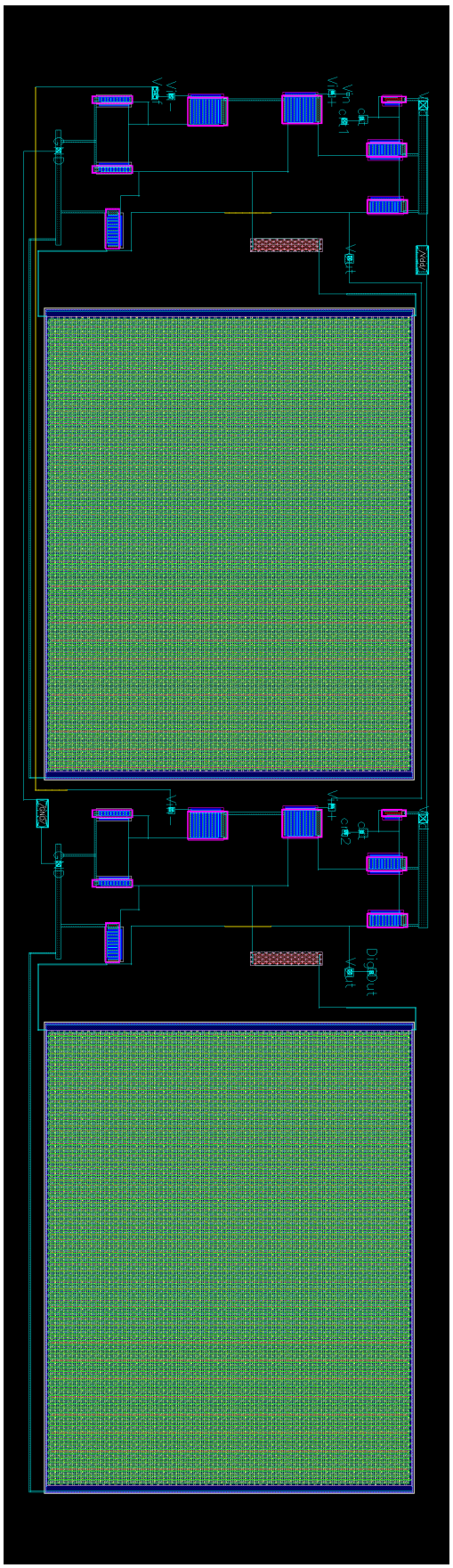
Figure 17: Power concumption of the comparator

2.3 The layout, DRC and LVS reports for the non-clocked comparator.

In this section, we are going to present the layout and its relevant checks, the DRC and LVS reports (to be enclosed in the appendix). The design of non-clocked comparator is just two opamp connected in series and it is reflected in its layout.



(a) Layout connection view for comparator.



(b) Layout detail view for comparator.

Figure 18: Layout for the comparator

3 Task 3: The neural model

In this task we are going to implement the neural model the opamp and the comparator we designed in the previous chapters.

3.1 The design and schematic

The schematics of Integrate and Fire Neuron is based on the circuit from Ref. [4] The circuit is shown in Fig. 19. Two pulsed current sources mimick the neural stimulus from two synapses. The opamp is connected in integrating configuration with the membrane capacitance of 5 pF. The comparator fire the spike and short the loop of opamp via nFET $M0$. The reference voltage is 80 mV while the common mode voltage is 350 mV for both comparator and opamp. It means that the comparator should send the High signal as soon as voltage on IN-terminal exceeds 430 mV.

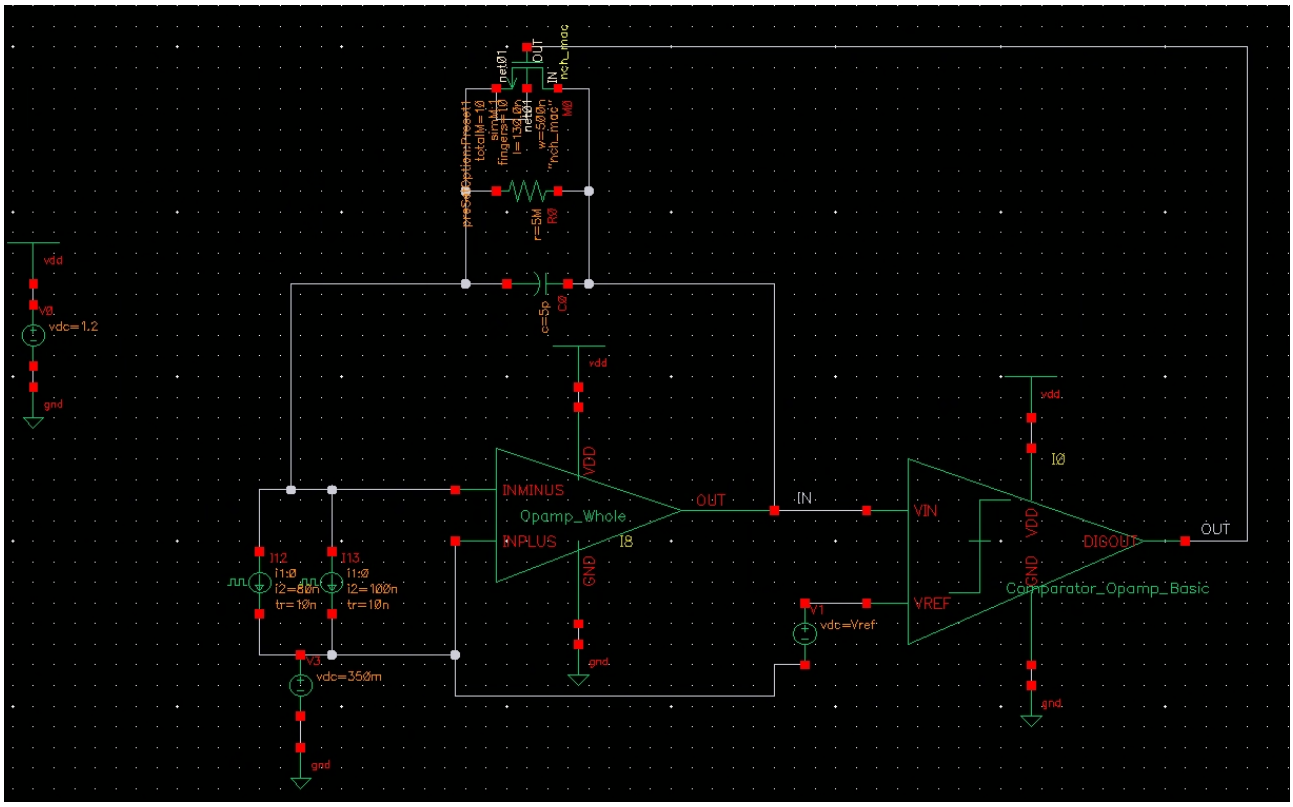


Figure 19: Neural model with integrate and fire function.

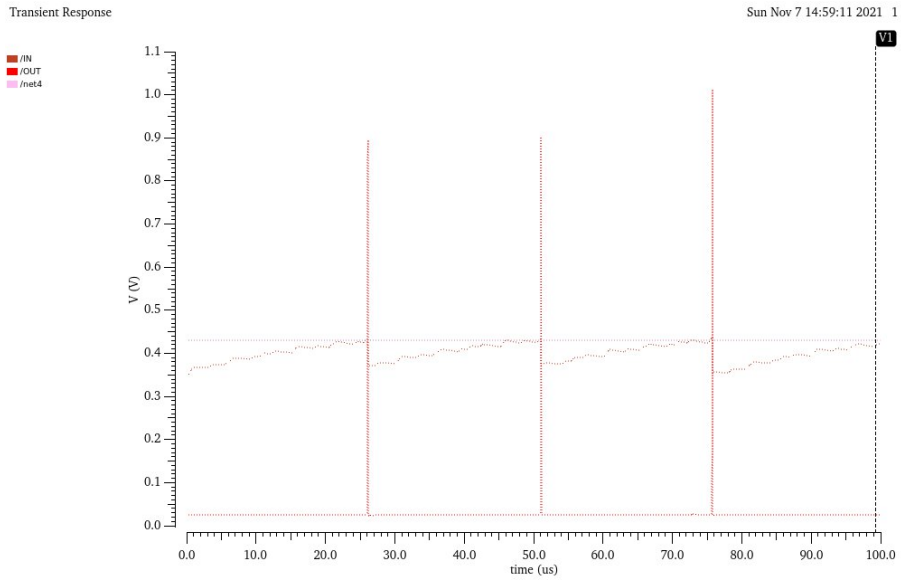


Figure 20: Neural model with integrate and fire function.

The results of the transient simulation is shown in Fig. 20. We can see that the schematics works exactly as we expected. Every pulse from the current sources are integrated by the opamp that manifests as steps on the OUT graph. As soon as integrated signal on terminal IN reaches 430 mV (the reference voltage on the comparator, $/net4$ in Fig. 20) the spike from the comparator resets voltage back to the common mode value of 350 mV.

3.2 The layout, DRC and LVS reports for the neural model (excluding spike generation)

In this section, we are going to present the layout and its relevant checks, the DRC and LVS reports (to be enclosed in the appendix). The design of the neural model is a connection of the 2-stage OpAmp and the comparator.

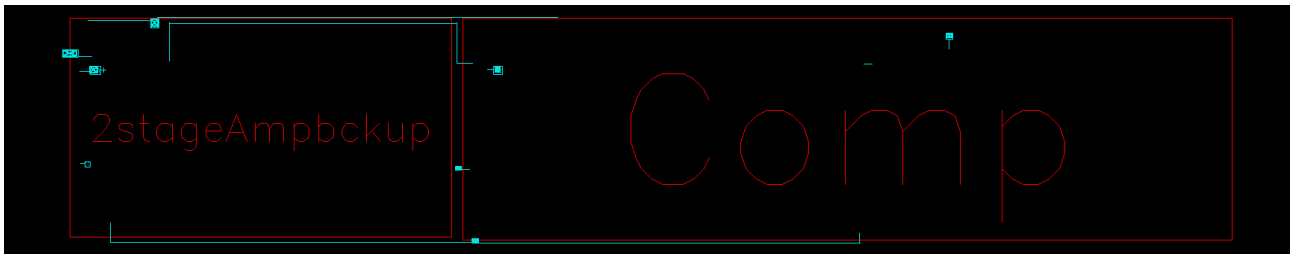


Figure 21: Layout connection view for the neural model.

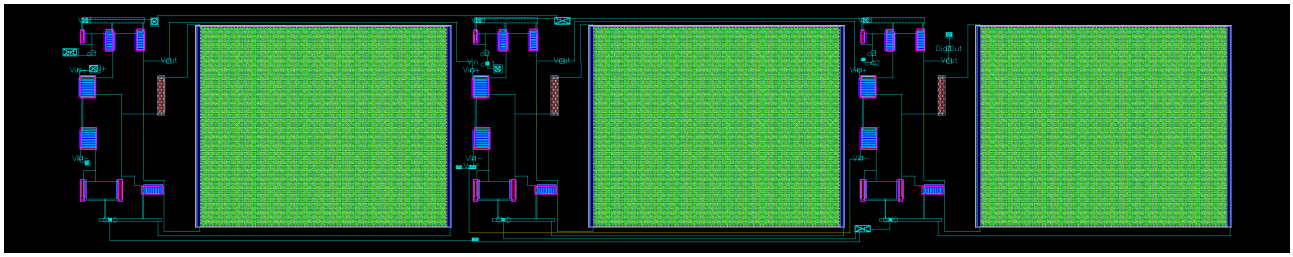


Figure 22: Layout detail view for the neural model.

References

[1] Tony Ch. Carusone, David A. Johns, Kenneth W. Martin, *Analog Integrated Circuit Design*. Wiley, Inc., Inc., Printed in the USA, 2012.

[2] Taiwan Semiconductor Manufacturing Co,
`https://europractice-ic.com/mpw-prototyping/asics/tsmc/`
`https://www.tsmc.com/english/dedicatedFoundry/technology`

[3] Kristian Gjertsen Kjelgård *Lecture notes in IN5180 - Analog Microelectronics Design*. University of Oslo, 2021.

[4] Bibhu Datta Sahoo, *Ring oscillator based sub-1V leaky integrate-and-fire neuron circuit*. Scientific Reports 7, 2017.

4 Appendix

4.1 Workload distribution

Task distribution		
Tasks	Kun Zhu	Illia Ilia Kolevatov
Differential stage	Secondary	✓Main
Common-source stage	✓Main	Secondary
Compensation	Secondary	✓Main
Comparator	Secondary	✓Main
Neuron spike circuit		✓Main
Layout	✓Main	
DRC report	✓Main	
LVS report	✓Main	

4.2 The DRC results

For the DRC checks, the following rules are excluded:

- Density checks.
- DOD*
- DPO*
- DM*
- ESD*
- PO.R8

The DRC report start from the next line.

```
Neuron 1000
NET_AREA_RATIO_RDBS
0 0 35 Nov 12 15:40:12 2021
M1.DN.6.M1.density 0
M1.DN.6.M2.density 0
M2.DN.6.M2.density 0
M1.DN.6.M3.density 0
M2.DN.6.M3.density 0
M3.DN.6.M3.density 0
M2.DN.6.M4.density 0
M3.DN.6.M4.density 0
M4.DN.6.M4.density 0
M3.DN.6.M5.density 0
M4.DN.6.M5.density 0
M5.DN.6.M5.density 0
M4.DN.6.M6.density 0
M5.DN.6.M6.density 0
M5.DN.6.M7.density 0
MOM.A.1.rep 0
MOM.A.2.rep 0
IND.DN.1L.M1.density 0
```

```
IND.DN.1H.M1.density 0
IND.DN.1L.M2.density 0
IND.DN.1H.M2.density 0
IND.DN.1L.M3.density 0
IND.DN.1H.M3.density 0
IND.DN.1L.M4.density 0
IND.DN.1H.M4.density 0
IND.DN.1L.M5.density 0
IND.DN.1H.M5.density 0
IND.DN.1L.M6.density 0
IND.DN.1H.M6.density 0
IND.DN.1L.M7.density 0
IND.DN.1H.M7.density 0
IND.DN.1L.M8.density 0
IND.DN.1H.M8.density 0
IND.DN.1L.M9.density 0
IND.DN.1H.M9.density 0
```

4.3 The DRC summary

```
==================================================================================
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Fri Nov 12 15:40:10 2021
Calibre Version:           v2020.4_15.9    Thu Oct 1 15:09:27 PDT 2020
Rule File Pathname:        /uio/hume/student-u52/kunzh/cadence617_tsmc65rf_oa/_calibre.drc_
Rule File Title:
Layout System:             GDS
Layout Path(s):            Neuron.calibre.db
Layout Primary Cell:       Neuron
Current Directory:         /uio/hume/student-u52/kunzh/cadence617_tsmc65rf_oa
User Name:                 kunzh
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      Neuron.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       Neuron.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = YES  SKEW = YES  ANGLED = NO  OFFGRID = YES
                           NONSIMPLE POLYGON = YES  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         ALL TEXT
Layers:                    MEMORY-BASED
Keep Empty Checks:         NO
----------------------------------------------------------------------------------
--- RUNTIME WARNINGS
---
Cell name parameter   for INSIDE CELL operation not located.
Cell name parameter   for NOT INSIDE CELL operation not located.
Cell name parameter   for INSIDE CELL operation not located.
Cell name parameter   for NOT INSIDE CELL operation not located.
Cell name parameter   for INSIDE CELL operation not located.
Cell name parameter   for NOT INSIDE CELL operation not located.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
PROJECTING constraint only supported with PARALLEL ONLY - setting PARALLEL ONLY.
----------------------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER FWCUi ................ TOTAL Original Geometry Count = 0   (0)
LAYER FWALi ................ TOTAL Original Geometry Count = 0   (0)
```

```
LAYER SRAMDMY_5 ..... TOTAL Original Geometry Count = 0   (0)
LAYER SRAMDMY_4 ..... TOTAL Original Geometry Count = 0   (0)
LAYER M8_NEW ........ TOTAL Original Geometry Count = 0   (0)
LAYER DUM8_NEW ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM8_OLD ... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM8_NEW ... TOTAL Original Geometry Count = 0   (0)
LAYER M9_NEW ........ TOTAL Original Geometry Count = 0   (0)
LAYER DUM9_NEW ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM9_OLD ... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM9_NEW ... TOTAL Original Geometry Count = 0   (0)
LAYER VIA7_NEW ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV7_OLD ... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV7_NEW ... TOTAL Original Geometry Count = 0   (0)
LAYER VIA8_NEW ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV8_OLD ... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV8_NEW ... TOTAL Original Geometry Count = 0   (0)
LAYER VIA9_NEW ...... TOTAL Original Geometry Count = 0   (0)
LAYER DOD ........... TOTAL Original Geometry Count = 0   (0)
LAYER ODi ........... TOTAL Original Geometry Count = 111 (348)
LAYER DPO ........... TOTAL Original Geometry Count = 0   (0)
LAYER POi ........... TOTAL Original Geometry Count = 279 (960)
LAYER DUM1 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M1i ........... TOTAL Original Geometry Count = 466 (1372)
LAYER DUM2 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M2i ........... TOTAL Original Geometry Count = 134 (409)
LAYER DUM3 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M3i ........... TOTAL Original Geometry Count = 159 (486)
LAYER DUM4 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M4i ........... TOTAL Original Geometry Count = 129 (396)
LAYER DUM5 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M5i ........... TOTAL Original Geometry Count = 159 (486)
LAYER DUM6 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M6i ........... TOTAL Original Geometry Count = 129 (396)
LAYER DUM7 .......... TOTAL Original Geometry Count = 0   (0)
LAYER M7i ........... TOTAL Original Geometry Count = 159 (486)
LAYER SRAMDMY ....... TOTAL Original Geometry Count = 0   (0)
LAYER DNWi .......... TOTAL Original Geometry Count = 0   (0)
LAYER NWi ........... TOTAL Original Geometry Count = 5   (18)
LAYER OD_18i ........ TOTAL Original Geometry Count = 0   (0)
LAYER OD_25i ........ TOTAL Original Geometry Count = 0   (0)
LAYER OD_33i ........ TOTAL Original Geometry Count = 0   (0)
LAYER OD_DECAP ...... TOTAL Original Geometry Count = 0   (0)
LAYER PPi ........... TOTAL Original Geometry Count = 12  (42)
LAYER NPi ........... TOTAL Original Geometry Count = 12  (39)
LAYER CBi ........... TOTAL Original Geometry Count = 0   (0)
LAYER CB2i .......... TOTAL Original Geometry Count = 0   (0)
LAYER RPOi .......... TOTAL Original Geometry Count = 1   (3)
LAYER NT_Ni ......... TOTAL Original Geometry Count = 0   (0)
LAYER POFUSE ........ TOTAL Original Geometry Count = 0   (0)
```

```
LAYER FUSELINK ..... TOTAL Original Geometry Count = 0   (0)
LAYER PMi ..... TOTAL Original Geometry Count = 0   (0)
LAYER PM1i ..... TOTAL Original Geometry Count = 0   (0)
LAYER PM2i ..... TOTAL Original Geometry Count = 0   (0)
LAYER VTH_Ni ..... TOTAL Original Geometry Count = 0   (0)
LAYER VTH_Pi ..... TOTAL Original Geometry Count = 0   (0)
LAYER VTL_Ni ..... TOTAL Original Geometry Count = 0   (0)
LAYER VTL_Pi ..... TOTAL Original Geometry Count = 0   (0)
LAYER UHVT_Ni ..... TOTAL Original Geometry Count = 0   (0)
LAYER UHVT_Pi ..... TOTAL Original Geometry Count = 0   (0)
LAYER CBDi ..... TOTAL Original Geometry Count = 0   (0)
LAYER UBMi ..... TOTAL Original Geometry Count = 0   (0)
LAYER RH ..... TOTAL Original Geometry Count = 1   (3)
LAYER ESD3 ..... TOTAL Original Geometry Count = 0   (0)
LAYER VARi ..... TOTAL Original Geometry Count = 0   (0)
LAYER APi ..... TOTAL Original Geometry Count = 0   (0)
LAYER Cu_PPIi ..... TOTAL Original Geometry Count = 0   (0)
LAYER CBMi ..... TOTAL Original Geometry Count = 0   (0)
LAYER CTMi ..... TOTAL Original Geometry Count = 0   (0)
LAYER RVi ..... TOTAL Original Geometry Count = 0   (0)
LAYER DCOi ..... TOTAL Original Geometry Count = 0   (0)
LAYER HVD_P ..... TOTAL Original Geometry Count = 0   (0)
LAYER HVD_N_nw ..... TOTAL Original Geometry Count = 0   (0)
LAYER BJTDMY ..... TOTAL Original Geometry Count = 0   (0)
LAYER LMARK ..... TOTAL Original Geometry Count = 0   (0)
LAYER SRM ..... TOTAL Original Geometry Count = 0   (0)
LAYER TCDDMY ..... TOTAL Original Geometry Count = 0   (0)
LAYER SRAMDMY_1 ..... TOTAL Original Geometry Count = 0   (0)
LAYER OD1Ti ..... TOTAL Original Geometry Count = 0   (0)
LAYER CLDDi ..... TOTAL Original Geometry Count = 0   (0)
LAYER CROWNi ..... TOTAL Original Geometry Count = 0   (0)
LAYER P3i ..... TOTAL Original Geometry Count = 0   (0)
LAYER SNCTi ..... TOTAL Original Geometry Count = 0   (0)
LAYER LUPWDMY ..... TOTAL Original Geometry Count = 0   (0)
LAYER VDDDMY ..... TOTAL Original Geometry Count = 0   (0)
LAYER VSSDMY ..... TOTAL Original Geometry Count = 0   (0)
LAYER M1_real ..... TOTAL Original Geometry Count = 466 (1372)
LAYER DM1_O ..... TOTAL Original Geometry Count = 0   (0)
LAYER M2_real ..... TOTAL Original Geometry Count = 134 (409)
LAYER DM2_O ..... TOTAL Original Geometry Count = 0   (0)
LAYER M3_real ..... TOTAL Original Geometry Count = 159 (486)
LAYER DM3_O ..... TOTAL Original Geometry Count = 0   (0)
LAYER M4_real ..... TOTAL Original Geometry Count = 129 (396)
LAYER DM4_O ..... TOTAL Original Geometry Count = 0   (0)
LAYER M5_real ..... TOTAL Original Geometry Count = 159 (486)
LAYER DM5_O ..... TOTAL Original Geometry Count = 0   (0)
LAYER M6_real ..... TOTAL Original Geometry Count = 129 (396)
LAYER DM6_O ..... TOTAL Original Geometry Count = 0   (0)
LAYER M7_real ..... TOTAL Original Geometry Count = 159 (486)
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LAYER DUM8_OLD ...........  TOTAL Original Geometry Count = 0   (0)
LAYER M9_OLD .............  TOTAL Original Geometry Count = 0   (0)
LAYER DUM9_OLD ...........  TOTAL Original Geometry Count = 0   (0)
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LAYER NCap_NTNi ..........  TOTAL Original Geometry Count = 0   (0)
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LAYER VIA2i ..............  TOTAL Original Geometry Count = 374 (2244)
LAYER VIA3i ..............  TOTAL Original Geometry Count = 376 (2256)
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LAYER NWDMY ..............  TOTAL Original Geometry Count = 0   (0)
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LAYER CSRDMY .............  TOTAL Original Geometry Count = 0   (0)
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LAYER INDDMY_COIL ........  TOTAL Original Geometry Count = 0   (0)
LAYER IND_CTAP ...........  TOTAL Original Geometry Count = 0   (0)
LAYER DIODMY .............  TOTAL Original Geometry Count = 0   (0)
LAYER RRuleAnalog ........  TOTAL Original Geometry Count = 0   (0)
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LAYER SBDDMY .............  TOTAL Original Geometry Count = 0   (0)
```

```
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LAYER CTMDMY_20 ..... TOTAL Original Geometry Count = 0   (0)
LAYER CDUDMY ........ TOTAL Original Geometry Count = 0   (0)
LAYER CO_PUSH ....... TOTAL Original Geometry Count = 0   (0)
LAYER RTMOMDMY ...... TOTAL Original Geometry Count = 1   (3)
LAYER VIA7_OLD ...... TOTAL Original Geometry Count = 0   (0)
LAYER VIA8_OLD ...... TOTAL Original Geometry Count = 0   (0)
LAYER VIA9_OLD ...... TOTAL Original Geometry Count = 0   (0)
LAYER RAM1TDMY ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEM1 ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEM2 ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEM3 ...... TOTAL Original Geometry Count = 0   (0)
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LAYER NOTUSEM6 ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEM7 ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEM8 ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEM9 ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEOD ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOTUSEPO ...... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM1 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM2 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM3 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM4 ....... TOTAL Original Geometry Count = 0   (0)
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LAYER NOUSEM6 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEM7 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV1 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV2 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV3 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV4 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV5 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NOUSEV6 ....... TOTAL Original Geometry Count = 0   (0)
LAYER NWi_OTHERS .... TOTAL Original Geometry Count = 0   (0)
LAYER ODi_OTHERS .... TOTAL Original Geometry Count = 0   (0)
LAYER ODi_SRAM ...... TOTAL Original Geometry Count = 0   (0)
LAYER ODi_RFDRAIN ... TOTAL Original Geometry Count = 0   (0)
LAYER POi_OTHERS .... TOTAL Original Geometry Count = 0   (0)
LAYER POi_SRAM ...... TOTAL Original Geometry Count = 0   (0)
LAYER COi_OTHERS .... TOTAL Original Geometry Count = 0   (0)
LAYER COi_SRAM ...... TOTAL Original Geometry Count = 0   (0)
LAYER MOMDMY_ALL .... TOTAL Original Geometry Count = 8   (24)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK G.1:UBMi ..................... TOTAL Result Count = 0 (0)
RULECHECK G.1:CBDi ..................... TOTAL Result Count = 0 (0)
RULECHECK G.1:CB2i ..................... TOTAL Result Count = 0 (0)
```

```
RULECHECK G.1:PMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:PM2i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:Cu_PPIi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DNWi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:NWi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD_18i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD_25i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD25_33 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD25_18 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD_33i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD_DECAP ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:PPi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:NPi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CBi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:RPOi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:NT_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:NCap_NTNi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:FWALi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:FWCUi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:POFUSE ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:FUSELINK ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:PM1i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SEALRINGi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VTH_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VTH_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VTL_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VTL_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:UHVT_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:UHVT_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:RH ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:ESD3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VARi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:APi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CBMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CTMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:RVi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DCOi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:HVD_P ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:HVD_N_nw ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:BJTDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:NWDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:RPDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:PMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SDI ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:ESD1DMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:ESD2DMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SRM ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CDUDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:TCDDMY ..... TOTAL Result Count = 0 (0)
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RULECHECK G.1:LOGO ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:INDDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CTMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CTMDMY_10 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CTMDMY_15 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CTMDMY_20 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_1 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_2 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_4 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_5 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_6 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_7 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_8 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_9 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:MOMDMY_AP ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:RTMOMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:RFDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:WBDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DIODMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SRAMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SRAMDMY_4 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SRAMDMY_5 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SRAMDMY_1 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:OD1Ti ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CLDDi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:CROWNi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:P3i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:SNCTi ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:LUPWDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VDDDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:VSSDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M1i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M1_real ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM1_O ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM1 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M2i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M2_real ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM2_O ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM2 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M3i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M3_real ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM3_O ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M4i ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M4_real ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM4_O ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM4 ..... TOTAL Result Count = 0 (0)
RULECHECK G.1:M5i ..... TOTAL Result Count = 0 (0)
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RULECHECK G.1:M5_real ..................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM5_O ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM5 ........................ TOTAL Result Count = 0 (0)
RULECHECK G.1:M6i ......................... TOTAL Result Count = 0 (0)
RULECHECK G.1:M6_real ..................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM6_O ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM6 ........................ TOTAL Result Count = 0 (0)
RULECHECK G.1:M7i ......................... TOTAL Result Count = 0 (0)
RULECHECK G.1:M7_real ..................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DM7_O ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM7 ........................ TOTAL Result Count = 0 (0)
RULECHECK G.1:M8_OLD ...................... TOTAL Result Count = 0 (0)
RULECHECK G.1:M8_NEW ...................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM8_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM8_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:M9_OLD ...................... TOTAL Result Count = 0 (0)
RULECHECK G.1:M9_NEW ...................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM9_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DUM9_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA1i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA2i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA3i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA4i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA5i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA6i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA7_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA7_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA8_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA8_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA9_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:VIA9_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.1:ODi ......................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DOD ......................... TOTAL Result Count = 0 (0)
RULECHECK G.1:DPO ......................... TOTAL Result Count = 0 (0)
RULECHECK G.1:mVTLi ....................... TOTAL Result Count = 0 (0)
RULECHECK G.1:CO .......................... TOTAL Result Count = 0 (0)
RULECHECK G.1:PO .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DNWi ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:NWi ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD_18i ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD_25i ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD25_33 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD25_18 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD_33i ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD_DECAP .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:PPi ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:NPi ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:COi ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:CO_PUSH ..................... TOTAL Result Count = 0 (0)
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RULECHECK G.2:CBi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CB2i ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:RPOi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:NT_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:NCap_NTNi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:FWALi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:FWCUi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:POFUSE ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:FUSELINK ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:PMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:PM1i ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:PM2i ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:SEALRINGi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:VTH_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:VTH_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:VTL_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:VTL_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:UHVT_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:UHVT_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CBDi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:UBMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:RH ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:ESD3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:VARi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:APi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:Cu_PPIi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CBMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CTMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:RVi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:DCOi ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:HVD_P ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:HVD_N_nw ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:BJTDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:NWDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:RPDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:PMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:SDI ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:ESD1DMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:ESD2DMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:SRM ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CDUDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:TCDDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:LOGO ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:INDDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CTMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CTMDMY_10 ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CTMDMY_15 ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:CTMDMY_20 ..... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_1 ..... TOTAL Result Count = 0 (0)
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RULECHECK G.2:MOMDMY_2 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_3 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_4 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_5 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_6 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_7 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_8 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_9 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:MOMDMY_AP .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:RTMOMDMY ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:RFDMY ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:WBDMY ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:DIODMY ....................... TOTAL Result Count = 0 (0)
RULECHECK G.2:SRAMDMY ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:SRAMDMY_4 .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:SRAMDMY_5 .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:SRAMDMY_1 .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:RAM1TDMY ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:OD1Ti ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:CLDDi ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:CROWNi ....................... TOTAL Result Count = 0 (0)
RULECHECK G.2:P3i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:SNCTi ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:LUPWDMY ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VDDDMY ....................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VSSDMY ....................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M1i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M1_real ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DM1_O ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM1 ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M2i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M2_real ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DM2_O ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM2 ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M3i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M3_real ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DM3_O ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM3 ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M4i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M4_real ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DM4_O ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM4 ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M5i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M5_real ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DM5_O ........................ TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM5 ......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M6i .......................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M6_real ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DM6_O ........................ TOTAL Result Count = 0 (0)
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RULECHECK G.2:DUM6 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M7i ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M7_real .................. TOTAL Result Count = 0 (0)
RULECHECK G.2:DM7_O .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM7 ..................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M8_OLD ................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M8_NEW ................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM8_OLD ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM8_NEW ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:M9_OLD ................... TOTAL Result Count = 0 (0)
RULECHECK G.2:M9_NEW ................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM9_OLD ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:DUM9_NEW ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA1i .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA2i .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA3i .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA4i .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA5i .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA6i .................... TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA7_OLD ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA7_NEW ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA8_OLD ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA8_NEW ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA9_OLD ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:VIA9_NEW ................. TOTAL Result Count = 0 (0)
RULECHECK G.2:ODi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DOD ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:POi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:DPO ...................... TOTAL Result Count = 0 (0)
RULECHECK G.2:mVTLi .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DNWi ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:NWi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:OD_18i ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:OD_25i ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:OD25_33 .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:OD25_18 .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:OD_33i ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:OD_DECAP ................. TOTAL Result Count = 0 (0)
RULECHECK G.3:PPi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:NPi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:COi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:CO_PUSH .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:CBi ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:RPOi ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:NT_Ni .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:NCap_NTNi ................ TOTAL Result Count = 0 (0)
RULECHECK G.3:FWALi .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:FWCUi .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:POFUSE ................... TOTAL Result Count = 0 (0)
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RULECHECK G.3:FUSELINK ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:SEALRINGi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VTH_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VTH_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VTL_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VTL_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:UHVT_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:UHVT_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:RH ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:ESD3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VARi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:APi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CBMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CTMi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:RVi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:DCOi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:HVD_P ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:HVD_N_nw ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:BJTDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:NWDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:RPDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:SDI ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:ESD1DMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:ESD2DMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:SRM ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CDUDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:TCDDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:LOGO ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:INDDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CTMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CTMDMY_10 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CTMDMY_15 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:CTMDMY_20 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_1 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_2 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_4 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_5 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_6 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_7 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_8 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_9 ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:MOMDMY_AP ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:RTMOMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:RFDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:WBDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:DIODMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:SRAMDMY ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:SRAMDMY_4 ..... TOTAL Result Count = 0 (0)
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RULECHECK G.3:SRAMDMY_5 ................. TOTAL Result Count = 0 (0)
RULECHECK G.3:SRAMDMY_1 ................. TOTAL Result Count = 0 (0)
RULECHECK G.3:RAM1TDMY .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:OD1Ti ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:CLDDi ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:CROWNi .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:P3i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:SNCTi ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:LUPWDMY ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:VDDDMY .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:VSSDMY .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M1i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M1_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM1_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM1 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M2i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M2_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM2_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM2 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M3i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M3_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM3_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM3 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M4i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M4_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM4_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM4 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M5i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M5_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM5_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM5 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M6i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M6_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM6_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM6 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M7i ....................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M7_real ................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DM7_O ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM7 ...................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M8_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M8_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM8_OLD .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM8_NEW .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:M9_OLD .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:M9_NEW .................... TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM9_OLD .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:DUM9_NEW .................. TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA1i ..................... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA2i ..................... TOTAL Result Count = 0 (0)
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RULECHECK G.3:VIA3i ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA4i ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA5i ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA6i ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA7_OLD ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA7_NEW ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA8_OLD ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA8_NEW ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA9_OLD ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:VIA9_NEW ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:ODi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:DOD ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:POi ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:DPO ..... TOTAL Result Count = 0 (0)
RULECHECK G.3:mVTLi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:ODi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:POi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:VTH_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:VTH_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:VTL_Ni ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:VTL_Pi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:PPi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:NPi ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M1i ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M2i ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M3i ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M4i ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M5i ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M6i ..... TOTAL Result Count = 0 (0)
RULECHECK G.4:M7i ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM1 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM2 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM3 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM4 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM5 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM6 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM7 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM8 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEM9 ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEOD ..... TOTAL Result Count = 0 (0)
RULECHECK G.5:NOTUSEPO ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M1 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M2 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M3 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M4 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M5 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M6 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M7 ..... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.M8 ..... TOTAL Result Count = 0 (0)
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RULECHECK USER_GUIDE.M9 ................. TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA1 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA2 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA3 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA4 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA5 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA6 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA7 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.VIA8 ............... TOTAL Result Count = 0 (0)
RULECHECK USER_GUIDE.2 .................. TOTAL Result Count = 0 (0)
RULECHECK NW_DATATYPE:WARNING1 .......... TOTAL Result Count = 0 (0)
RULECHECK OD_DATATYPE:WARNING1 .......... TOTAL Result Count = 0 (0)
RULECHECK OD_DATATYPE:WARNING2 .......... TOTAL Result Count = 0 (0)
RULECHECK OD_DATATYPE:WARNING3 .......... TOTAL Result Count = 0 (0)
RULECHECK PO_DATATYPE:WARNING1 .......... TOTAL Result Count = 0 (0)
RULECHECK PO_DATATYPE:WARNING2 .......... TOTAL Result Count = 0 (0)
RULECHECK CO_DATATYPE:WARNING1 .......... TOTAL Result Count = 0 (0)
RULECHECK CO_DATATYPE:WARNING2 .......... TOTAL Result Count = 0 (0)
RULECHECK NW.W.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.2 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.3 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.4 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.5 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.6 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.S.7 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.EN.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK NW.EN.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK NW.EN.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK NW.A.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.A.2 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.A.3 ........................ TOTAL Result Count = 0 (0)
RULECHECK NW.A.4 ........................ TOTAL Result Count = 0 (0)
RULECHECK NWROD.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.EN.1 .................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.EN.2 .................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.O.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.O.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.R.4 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.R.5 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.R.6 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.R.7 ..................... TOTAL Result Count = 0 (0)
RULECHECK NWRSTI.EN.1 ................... TOTAL Result Count = 0 (0)
RULECHECK NWRSTI.EN.2 ................... TOTAL Result Count = 0 (0)
RULECHECK NWRSTI.EX.1 ................... TOTAL Result Count = 0 (0)
RULECHECK NWRSTI.O.1 .................... TOTAL Result Count = 0 (0)
RULECHECK NT_N.W.1 ...................... TOTAL Result Count = 0 (0)
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RULECHECK NT_N.W.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.W.2.2 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.W.4 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.W.5 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.A.3 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.A.4 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.R.2 ..... TOTAL Result Count = 0 (0)
RULECHECK NT_N.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK DNW.R.5 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.W.4 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.S.3.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.L.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.L.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD.R.1 ..... NOT EXECUTED
RULECHECK DOD.W.1 ..... NOT EXECUTED
RULECHECK DOD.S.1 ..... NOT EXECUTED
RULECHECK DOD.S.2 ..... NOT EXECUTED
RULECHECK DOD.S.3 ..... NOT EXECUTED
RULECHECK DOD.S.5 ..... NOT EXECUTED
RULECHECK DOD.S.6 ..... NOT EXECUTED
RULECHECK DOD.S.7 ..... NOT EXECUTED
RULECHECK DOD.S.7.1 ..... NOT EXECUTED
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RULECHECK DOD.S.8 ..... NOT EXECUTED
RULECHECK DOD.S.9 ..... NOT EXECUTED
RULECHECK DOD.S.10 ..... NOT EXECUTED
RULECHECK DOD.EN.1 ..... NOT EXECUTED
RULECHECK DOD.EN.2 ..... NOT EXECUTED
RULECHECK OD.DN.1:L ..... NOT EXECUTED
RULECHECK OD.DN.1:H ..... NOT EXECUTED
RULECHECK OD.DN.2:L ..... NOT EXECUTED
RULECHECK OD.DN.2:H_IO ..... NOT EXECUTED
RULECHECK OD.DN.2:H_CORE ..... NOT EXECUTED
RULECHECK OD.DN.3:L ..... NOT EXECUTED
RULECHECK OD.DN.3:H_IO ..... NOT EXECUTED
RULECHECK OD.DN.3:H_CORE ..... NOT EXECUTED
RULECHECK DOD.R.1 ..... NOT EXECUTED
RULECHECK DOD.R.3 ..... NOT EXECUTED
RULECHECK OD2.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.6 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.S.7 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.EX.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.EX.3 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD2.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD25_33.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD25_33.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK OD25_33.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD25_18.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK OD25_18.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.W.4 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.W.5 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.4.1 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.6 ..... TOTAL Result Count = 0 (0)
RULECHECK PO.S.7 ..... TOTAL Result Count = 0 (0)
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RULECHECK PO.S.9 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.S.10 .................... TOTAL Result Count = 0 (0)
RULECHECK PO.S.15 .................... NOT EXECUTED
RULECHECK PO.S.16 .................... TOTAL Result Count = 0 (0)
RULECHECK PO.EX.1 .................... TOTAL Result Count = 0 (0)
RULECHECK PO.EX.2 .................... TOTAL Result Count = 0 (0)
RULECHECK PO.EX.3 .................... TOTAL Result Count = 0 (0)
RULECHECK PO.L.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.A.1.1 ................... TOTAL Result Count = 0 (0)
RULECHECK PO.A.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.DN.1:L .................. NOT EXECUTED
RULECHECK PO.DN.1:H .................. NOT EXECUTED
RULECHECK PO.DN.2 .................... NOT EXECUTED
RULECHECK PO.DN.3 .................... NOT EXECUTED
RULECHECK PO.R.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.R.4 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.R.6 ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.R.8 ..................... NOT EXECUTED
RULECHECK DPO.W.1 .................... NOT EXECUTED
RULECHECK DPO.S.1 .................... NOT EXECUTED
RULECHECK DPO.S.2 .................... NOT EXECUTED
RULECHECK DPO.S.3 .................... NOT EXECUTED
RULECHECK DPO.S.5 .................... NOT EXECUTED
RULECHECK DPO.S.6 .................... NOT EXECUTED
RULECHECK DPO.S.6.1 .................. NOT EXECUTED
RULECHECK DPO.S.8 .................... NOT EXECUTED
RULECHECK DPO.S.9 .................... NOT EXECUTED
RULECHECK DPO.EN.1 ................... NOT EXECUTED
RULECHECK DPO.R.1 .................... NOT EXECUTED
RULECHECK DPO.R.3 .................... NOT EXECUTED
RULECHECK DTCD.W.1 ................... TOTAL Result Count = 0 (0)
RULECHECK DTCD.R.1 ................... TOTAL Result Count = 0 (0)
RULECHECK DTCD.R.2 ................... TOTAL Result Count = 0 (0)
RULECHECK DTCD.R.3 ................... TOTAL Result Count = 0 (0)
RULECHECK VTH_N.W.1 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_N.S.1 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_N.S.2__VTH_N.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VTH_N.S.3 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_N.EN.1__VTH_N.EN.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VTH_N.A.1 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_N.A.2 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_N.R.1 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_N.R.2 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_P.W.1 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_P.S.1 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_P.S.2__VTH_P.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VTH_P.S.3 .................. TOTAL Result Count = 0 (0)
RULECHECK VTH_P.EN.1__VTH_P.EN.2 ..... TOTAL Result Count = 0 (0)
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RULECHECK VTH_P.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTH_P.A.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTH_P.R.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTH_P.R.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.S.2__VTL_N.S.2.1 ........ TOTAL Result Count = 0 (0)
RULECHECK VTL_N.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.EN.1__VTL_N.EN.2 ........ TOTAL Result Count = 0 (0)
RULECHECK VTL_N.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.A.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.R.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_N.R.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.S.2__VTL_P.S.2.1 ........ TOTAL Result Count = 0 (0)
RULECHECK VTL_P.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.EN.1__VTL_P.EN.2 ........ TOTAL Result Count = 0 (0)
RULECHECK VTL_P.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.A.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.R.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VTL_P.R.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK mVTL.EN.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK mVTL.S.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK mVTL.R.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK PP.W.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.S.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.S.2 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.S.4 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.S.5 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.S.6 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.S.7 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.EN.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK PP.EX.1 ....................... NOT EXECUTED
RULECHECK PP.EX.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK PP.EX.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK PP.EX.4 ....................... TOTAL Result Count = 0 (0)
RULECHECK PP.O.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.A.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.A.2 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.A.3 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.R.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK PP.R.2 ........................ TOTAL Result Count = 0 (0)
RULECHECK NP.W.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK NP.S.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK NP.S.2 ........................ TOTAL Result Count = 0 (0)
RULECHECK NP.S.4 ........................ TOTAL Result Count = 0 (0)
RULECHECK NP.S.5 ........................ TOTAL Result Count = 0 (0)
RULECHECK NP.S.6 ........................ TOTAL Result Count = 0 (0)
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RULECHECK NP.S.7 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.EX.2 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.EX.3 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.EX.4 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.A.3 ..... TOTAL Result Count = 0 (0)
RULECHECK NP.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK LDN.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK LDN.EX.1:DCO ..... TOTAL Result Count = 0 (0)
RULECHECK LDN.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK LDP.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK LDP.EX.1:DCO ..... TOTAL Result Count = 0 (0)
RULECHECK LDP.O.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VT.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VT.EX.2 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.EX.1.1 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.EX.2 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK RPO.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK RES.8 ..... TOTAL Result Count = 0 (0)
RULECHECK RES.10 ..... TOTAL Result Count = 0 (0)
RULECHECK RES.11 ..... TOTAL Result Count = 0 (0)
RULECHECK RES.21 ..... TOTAL Result Count = 0 (0)
RULECHECK RES.22 ..... TOTAL Result Count = 0 (0)
RULECHECK RES.12g ..... TOTAL Result Count = 0 (0)
RULECHECK RES.13g ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.W.4 ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.R.2 ..... NOT EXECUTED
RULECHECK VAR.R.3 ..... NOT EXECUTED
RULECHECK VAR.R.4 ..... TOTAL Result Count = 0 (0)
RULECHECK VAR.R.5 ..... NOT EXECUTED
RULECHECK HVD_N.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.S.1 ..... TOTAL Result Count = 0 (0)
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RULECHECK HVD_N.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.S.6 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.L.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.R.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.R.4 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_N.R.6 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.L.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.R.2 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.R.4 ..... TOTAL Result Count = 0 (0)
RULECHECK HVD_P.R.6 ..... TOTAL Result Count = 0 (0)
RULECHECK GR.R.1 ..... TOTAL Result Count = 0 (0)
RULECHECK GR.R.7__GR.R.8 ..... TOTAL Result Count = 0 (0)
RULECHECK GR.R.10__GR.R.11 ..... TOTAL Result Count = 0 (0)
RULECHECK GR.R.13 ..... TOTAL Result Count = 0 (0)
RULECHECK GR.R.14 ..... TOTAL Result Count = 0 (0)
RULECHECK BV.W.1g ..... TOTAL Result Count = 0 (0)
RULECHECK BV.W.2g ..... TOTAL Result Count = 0 (0)
RULECHECK BV.R.1g ..... TOTAL Result Count = 0 (0)
RULECHECK CO.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.2.2 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK CO.S.5 ..... TOTAL Result Count = 0 (0)
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RULECHECK CO.S.6 ..................... NOT EXECUTED
RULECHECK CO.EN.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK CO.EN.1.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK CO.EN.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK CO.EN.3__CO.EN.4 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.W.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.W.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.2.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.4 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.5 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.S.6 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.EN.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.EN.2__M1.EN.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.EN.4 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.A.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK M1.DN.1 ..................... NOT EXECUTED
RULECHECK M1.DN.1.1 ..................... NOT EXECUTED
RULECHECK M1.DN.2 ..................... NOT EXECUTED
RULECHECK M1.DN.4 ..................... NOT EXECUTED
RULECHECK VIA1.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA1.W.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA1.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA1.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA1.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA1.EN.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA1.EN.2__VIA1.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.2__VIA1.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.4:M1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.4:M2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.5:M1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.5:M2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.6:M1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.6:M2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA1.R.11 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.EN.1 ..... TOTAL Result Count = 0 (0)
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RULECHECK M2.EN.2__M2.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.S.6 ..... TOTAL Result Count = 0 (0)
RULECHECK M2.DN.1 ..... NOT EXECUTED
RULECHECK M2.DN.1.1 ..... NOT EXECUTED
RULECHECK M2.DN.2 ..... NOT EXECUTED
RULECHECK M2.DN.4 ..... NOT EXECUTED
RULECHECK VIA2.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.EN.2__VIA2.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.2__VIA2.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.4:M2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.4:M3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.5:M2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.5:M3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.6:M2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.6:M3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA2.R.11 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.EN.2__M3.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.S.6 ..... TOTAL Result Count = 0 (0)
RULECHECK M3.DN.1 ..... NOT EXECUTED
RULECHECK M3.DN.1.1 ..... NOT EXECUTED
RULECHECK M3.DN.2 ..... NOT EXECUTED
RULECHECK M3.DN.4 ..... NOT EXECUTED
RULECHECK M1.DN.5 ..... NOT EXECUTED
RULECHECK M1.DN.6 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.EN.1 ..... TOTAL Result Count = 0 (0)
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RULECHECK VIA3.EN.2__VIA3.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.2__VIA3.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.4:M3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.4:M4 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.5:M3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.5:M4 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.6:M3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.6:M4 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA3.R.11 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.2.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.5 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.EN.2__M4.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.A.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.A.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.S.6 ..... TOTAL Result Count = 0 (0)
RULECHECK M4.DN.1 ..... NOT EXECUTED
RULECHECK M4.DN.1.1 ..... NOT EXECUTED
RULECHECK M4.DN.2 ..... NOT EXECUTED
RULECHECK M4.DN.4 ..... NOT EXECUTED
RULECHECK M2.DN.5 ..... NOT EXECUTED
RULECHECK M2.DN.6 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.S.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.EN.2__VIA4.EN.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.2__VIA4.R.3 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.4:M4 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.4:M5 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.5:M4 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.5:M5 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.6:M4 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.6:M5 ..... TOTAL Result Count = 0 (0)
RULECHECK VIA4.R.11 ..... TOTAL Result Count = 0 (0)
RULECHECK M5.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M5.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK M5.W.3 ..... TOTAL Result Count = 0 (0)
RULECHECK M5.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK M5.S.2 ..... TOTAL Result Count = 0 (0)
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RULECHECK M5.S.2.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M5.S.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK M5.S.4 ....................... TOTAL Result Count = 0 (0)
RULECHECK M5.S.5 ....................... TOTAL Result Count = 0 (0)
RULECHECK M5.EN.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK M5.EN.2__M5.EN.3 ............. TOTAL Result Count = 0 (0)
RULECHECK M5.A.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M5.A.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M5.S.6 ....................... TOTAL Result Count = 0 (0)
RULECHECK M5.DN.1 ...................... NOT EXECUTED
RULECHECK M5.DN.1.1 .................... NOT EXECUTED
RULECHECK M5.DN.2 ...................... NOT EXECUTED
RULECHECK M5.DN.4 ...................... NOT EXECUTED
RULECHECK M3.DN.5 ...................... NOT EXECUTED
RULECHECK M3.DN.6 ...................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.W.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.EN.1 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA5.EN.2__VIA5.EN.3 ......... TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.2__VIA5.R.3 ........... TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.4:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.4:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.5:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.5:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.6:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.6:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA5.R.11 .................... TOTAL Result Count = 0 (0)
RULECHECK M6.W.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.W.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.W.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.2.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.4 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.5 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.EN.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK M6.EN.2__M6.EN.3 ............. TOTAL Result Count = 0 (0)
RULECHECK M6.A.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.A.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.S.6 ....................... TOTAL Result Count = 0 (0)
RULECHECK M6.DN.1 ...................... NOT EXECUTED
RULECHECK M6.DN.1.1 .................... NOT EXECUTED
RULECHECK M6.DN.2 ...................... NOT EXECUTED
RULECHECK M6.DN.4 ...................... NOT EXECUTED
RULECHECK M4.DN.5 ...................... NOT EXECUTED
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RULECHECK M4.DN.6 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.W.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.EN.1 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA6.EN.2__VIA6.EN.3 ......... TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.2__VIA6.R.3 ........... TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.4:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.4:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.5:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.5:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.6:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.6:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA6.R.11 .................... TOTAL Result Count = 0 (0)
RULECHECK M7.W.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.W.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.W.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.2.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.4 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.5 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.EN.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK M7.EN.2__M7.EN.3 ............. TOTAL Result Count = 0 (0)
RULECHECK M7.A.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.A.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.S.6 ....................... TOTAL Result Count = 0 (0)
RULECHECK M7.DN.1 ...................... NOT EXECUTED
RULECHECK M7.DN.1.1 .................... NOT EXECUTED
RULECHECK M7.DN.2 ...................... NOT EXECUTED
RULECHECK M7.DN.4 ...................... NOT EXECUTED
RULECHECK M5.DN.5 ...................... NOT EXECUTED
RULECHECK M5.DN.6 ...................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.W.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.EN.1 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.EN.2 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.R.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.R.3:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA7.R.3:M8 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA7.EN.3 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.EN.4 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.S.3 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.S.4 ..................... TOTAL Result Count = 0 (0)
```

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RULECHECK VIA7.S.5 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA7.R.7 ..................... TOTAL Result Count = 0 (0)
RULECHECK M8.W.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.W.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.S.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.S.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.S.3 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.EN.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK M8.EN.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK M8.A.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.A.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.DN.1 ...................... NOT EXECUTED
RULECHECK M8.DN.1.1 .................... NOT EXECUTED
RULECHECK M8.DN.2 ...................... NOT EXECUTED
RULECHECK M8.DN.4 ...................... NOT EXECUTED
RULECHECK M8.EN.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK M8.DN.5:L .................... NOT EXECUTED
RULECHECK M8.DN.5:H .................... NOT EXECUTED
RULECHECK M8.W.4 ....................... TOTAL Result Count = 0 (0)
RULECHECK M8.S.4 ....................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.W.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.EN.5 .................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.R.8 ..................... TOTAL Result Count = 0 (0)
RULECHECK VIA8.R.3:M8 .................. TOTAL Result Count = 0 (0)
RULECHECK VIA8.R.3:M9 .................. TOTAL Result Count = 0 (0)
RULECHECK M9.W.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M9.W.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M9.S.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M9.EN.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK M9.A.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK M9.A.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK M9.DN.1:L .................... NOT EXECUTED
RULECHECK M9.DN.1:H .................... NOT EXECUTED
RULECHECK M9.DN.2:L .................... NOT EXECUTED
RULECHECK M9.DN.2:H .................... NOT EXECUTED
RULECHECK CTM.W.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CTM.W.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK CTM.S.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CTM.EN.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK CTM.R.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CBM.W.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CBM.W.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK CBM.S.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CBM.S.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK CBM.S.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK CBM.EN.2 ..................... TOTAL Result Count = 0 (0)
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RULECHECK CBM.R.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK MOM.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M1 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M2 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M3 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M4 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.2:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M1 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M2 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M3 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M4 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.3:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK MOM.S.4:VIA1 ................ TOTAL Result Count = 0 (0)
RULECHECK MOM.S.4:VIA2 ................ TOTAL Result Count = 0 (0)
RULECHECK MOM.S.4:VIA3 ................ TOTAL Result Count = 0 (0)
RULECHECK MOM.S.4:VIA4 ................ TOTAL Result Count = 0 (0)
RULECHECK MOM.S.4:VIA5 ................ TOTAL Result Count = 0 (0)
RULECHECK MOM.S.4:VIA6 ................ TOTAL Result Count = 0 (0)
RULECHECK MOM.A.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.2:M2 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.W.2:M3 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.W.2:M4 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.W.2:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.W.2:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.W.2:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.W.3:M8 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.2:M2 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.2:M3 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.2:M4 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.2:M5 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.2:M6 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.2:M7 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.3:M8 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M1 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M1 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M2 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M2 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M3 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M3 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M4 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M4 .................. TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M5 .................. TOTAL Result Count = 0 (0)
```

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RULECHECK IND.S.5:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.4:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.S.5:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M1 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M3 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M4 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.4:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.6:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.6:M9 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.W.7 ........................ TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M1 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M2 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M3 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M4 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M5 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M6 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M7 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M8 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.DN.1:M9 .................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M1 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M3 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M4 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.8:M9 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK IND.R.2__IND.R.3:VIA7 ......... TOTAL Result Count = 0 (0)
RULECHECK IND.R.2__IND.R.3:VIA8 ......... TOTAL Result Count = 0 (0)
RULECHECK IND.R.4 ........................ TOTAL Result Count = 0 (0)
RULECHECK IND.R.13 ....................... TOTAL Result Count = 0 (0)
RULECHECK IND.R.6 ........................ TOTAL Result Count = 0 (0)
RULECHECK IND.DN.6 ....................... NOT EXECUTED
RULECHECK IND.DN.9 ....................... NOT EXECUTED
RULECHECK IND.DN.7:M1 .................... NOT EXECUTED
RULECHECK IND.DN.7:M2 .................... NOT EXECUTED
RULECHECK IND.DN.7:M3 .................... NOT EXECUTED
RULECHECK IND.DN.7:M4 .................... NOT EXECUTED
RULECHECK IND.DN.7:M5 .................... NOT EXECUTED
RULECHECK IND.DN.7:M6 .................... NOT EXECUTED
```

```
RULECHECK IND.DN.7:M7 ..................... NOT EXECUTED
RULECHECK IND.DN.7:M8 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M1 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M2 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M3 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M4 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M5 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M6 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M7 ..................... NOT EXECUTED
RULECHECK IND.DN.8:M8 ..................... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M1 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M1 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M2 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M2 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M3 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M3 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M4 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M4 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M5 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M5 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M6 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M6 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M7 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M7 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M8 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M8 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:L_M9 ............... NOT EXECUTED
RULECHECK IND_MD.DN.11:H_M9 ............... NOT EXECUTED
RULECHECK IND_MD.DN.10:M1 ................. NOT EXECUTED
RULECHECK IND_MD.DN.10:M2 ................. NOT EXECUTED
RULECHECK IND_MD.DN.10:M3 ................. NOT EXECUTED
RULECHECK IND_MD.DN.10:M4 ................. NOT EXECUTED
RULECHECK IND_MD.DN.10:M5 ................. NOT EXECUTED
RULECHECK IND_MD.DN.10:M6 ................. NOT EXECUTED
RULECHECK IND_MD.R.17:VIA1 ................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.17:VIA2 ................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.17:VIA3 ................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.17:VIA4 ................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.17:VIA5 ................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.17:VIA6 ................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.2:M2 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.2:M3 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.2:M4 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.2:M5 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.2:M6 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.2:M7 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.3:M8 ................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.4:M1 ................... TOTAL Result Count = 0 (0)
```

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RULECHECK IND_MD.W.4:M2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.4:M3 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.4:M4 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.4:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.4:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.4:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.W.7 ........................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.2:M2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.2:M3 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.2:M4 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.2:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.2:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.2:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.3:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M1 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M1 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M2 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M3 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M3 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M4 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M4 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M5 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M6 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M7 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.4:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.S.5:M8 ..................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.2__IND_MD.R.3:VIA7 ... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.2__IND_MD.R.3:VIA8 ... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M1 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M2 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M3 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M4 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M5 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M6 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M7 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M8 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.R.13:M9 .................... TOTAL Result Count = 0 (0)
RULECHECK IND_MD.DN.6 ....................... NOT EXECUTED
RULECHECK IND_MD.DN.9 ....................... NOT EXECUTED
RULECHECK IND_MD.DN.7:M1 .................... NOT EXECUTED
RULECHECK IND_MD.DN.7:M2 .................... NOT EXECUTED
RULECHECK IND_MD.DN.7:M3 .................... NOT EXECUTED
RULECHECK IND_MD.DN.7:M4 .................... NOT EXECUTED
RULECHECK IND_MD.DN.7:M5 .................... NOT EXECUTED
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RULECHECK IND_MD.DN.7:M6 ..... NOT EXECUTED
RULECHECK IND_MD.DN.7:M7 ..... NOT EXECUTED
RULECHECK IND_MD.DN.7:M8 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M1 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M2 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M3 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M4 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M5 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M6 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M7 ..... NOT EXECUTED
RULECHECK IND_MD.DN.8:M8 ..... NOT EXECUTED
RULECHECK CSR.R.1:DNWi ..... NOT EXECUTED
RULECHECK CSR.R.1:NWi ..... NOT EXECUTED
RULECHECK CSR.R.1:OD_18i ..... NOT EXECUTED
RULECHECK CSR.R.1:OD_25i ..... NOT EXECUTED
RULECHECK CSR.R.1:OD25_33 ..... NOT EXECUTED
RULECHECK CSR.R.1:OD25_18 ..... NOT EXECUTED
RULECHECK CSR.R.1:OD_33i ..... NOT EXECUTED
RULECHECK CSR.R.1:OD_DECAP ..... NOT EXECUTED
RULECHECK CSR.R.1:PPi ..... NOT EXECUTED
RULECHECK CSR.R.1:NPi ..... NOT EXECUTED
RULECHECK CSR.R.1:COi ..... NOT EXECUTED
RULECHECK CSR.R.1:CO_PUSH ..... NOT EXECUTED
RULECHECK CSR.R.1:CBi ..... NOT EXECUTED
RULECHECK CSR.R.1:CB2i ..... NOT EXECUTED
RULECHECK CSR.R.1:RPOi ..... NOT EXECUTED
RULECHECK CSR.R.1:NT_Ni ..... NOT EXECUTED
RULECHECK CSR.R.1:NCap_NTNi ..... NOT EXECUTED
RULECHECK CSR.R.1:FWALi ..... NOT EXECUTED
RULECHECK CSR.R.1:FWCUi ..... NOT EXECUTED
RULECHECK CSR.R.1:POFUSE ..... NOT EXECUTED
RULECHECK CSR.R.1:FUSELINK ..... NOT EXECUTED
RULECHECK CSR.R.1:PMi ..... NOT EXECUTED
RULECHECK CSR.R.1:PM1i ..... NOT EXECUTED
RULECHECK CSR.R.1:PM2i ..... NOT EXECUTED
RULECHECK CSR.R.1:SEALRINGi ..... NOT EXECUTED
RULECHECK CSR.R.1:VTH_Ni ..... NOT EXECUTED
RULECHECK CSR.R.1:VTH_Pi ..... NOT EXECUTED
RULECHECK CSR.R.1:VTL_Ni ..... NOT EXECUTED
RULECHECK CSR.R.1:VTL_Pi ..... NOT EXECUTED
RULECHECK CSR.R.1:UHVT_Ni ..... NOT EXECUTED
RULECHECK CSR.R.1:UHVT_Pi ..... NOT EXECUTED
RULECHECK CSR.R.1:CBDi ..... NOT EXECUTED
RULECHECK CSR.R.1:UBMi ..... NOT EXECUTED
RULECHECK CSR.R.1:RH ..... NOT EXECUTED
RULECHECK CSR.R.1:ESD3 ..... NOT EXECUTED
RULECHECK CSR.R.1:VARi ..... NOT EXECUTED
RULECHECK CSR.R.1:APi ..... NOT EXECUTED
RULECHECK CSR.R.1:Cu_PPIi ..... NOT EXECUTED
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RULECHECK CSR.R.1:CBMi ..................... NOT EXECUTED
RULECHECK CSR.R.1:CTMi ..................... NOT EXECUTED
RULECHECK CSR.R.1:RVi ...................... NOT EXECUTED
RULECHECK CSR.R.1:DCOi ..................... NOT EXECUTED
RULECHECK CSR.R.1:HVD_P .................... NOT EXECUTED
RULECHECK CSR.R.1:HVD_N_nw ................. NOT EXECUTED
RULECHECK CSR.R.1:BJTDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:NWDMY .................... NOT EXECUTED
RULECHECK CSR.R.1:RPDMY .................... NOT EXECUTED
RULECHECK CSR.R.1:PMDMY .................... NOT EXECUTED
RULECHECK CSR.R.1:SDI ...................... NOT EXECUTED
RULECHECK CSR.R.1:ESD1DMY .................. NOT EXECUTED
RULECHECK CSR.R.1:ESD2DMY .................. NOT EXECUTED
RULECHECK CSR.R.1:LMARK .................... NOT EXECUTED
RULECHECK CSR.R.1:SRM ...................... NOT EXECUTED
RULECHECK CSR.R.1:CSRDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:CDUDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:TCDDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:LOGO ..................... NOT EXECUTED
RULECHECK CSR.R.1:INDDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:CTMDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:CTMDMY_10 ................ NOT EXECUTED
RULECHECK CSR.R.1:CTMDMY_15 ................ NOT EXECUTED
RULECHECK CSR.R.1:CTMDMY_20 ................ NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_1 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_2 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_3 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_4 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_5 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_6 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_7 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_8 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_9 ................. NOT EXECUTED
RULECHECK CSR.R.1:MOMDMY_AP ................ NOT EXECUTED
RULECHECK CSR.R.1:RTMOMDMY ................. NOT EXECUTED
RULECHECK CSR.R.1:RFDMY .................... NOT EXECUTED
RULECHECK CSR.R.1:WBDMY .................... NOT EXECUTED
RULECHECK CSR.R.1:DIODMY ................... NOT EXECUTED
RULECHECK CSR.R.1:SRAMDMY ................... NOT EXECUTED
RULECHECK CSR.R.1:SRAMDMY_4 ................ NOT EXECUTED
RULECHECK CSR.R.1:SRAMDMY_5 ................ NOT EXECUTED
RULECHECK CSR.R.1:SRAMDMY_1 ................ NOT EXECUTED
RULECHECK CSR.R.1:RAM1TDMY .................. NOT EXECUTED
RULECHECK CSR.R.1:OD1Ti ..................... NOT EXECUTED
RULECHECK CSR.R.1:CLDDi ..................... NOT EXECUTED
RULECHECK CSR.R.1:CROWNi .................... NOT EXECUTED
RULECHECK CSR.R.1:P3i ....................... NOT EXECUTED
RULECHECK CSR.R.1:SNCTi ..................... NOT EXECUTED
RULECHECK CSR.R.1:LUPWDMY ................... NOT EXECUTED
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RULECHECK CSR.R.1:VDDDMY ..... NOT EXECUTED
RULECHECK CSR.R.1:VSSDMY ..... NOT EXECUTED
RULECHECK CSR.R.1:M1i ..... NOT EXECUTED
RULECHECK CSR.R.1:M1_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM1_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM1 ..... NOT EXECUTED
RULECHECK CSR.R.1:M2i ..... NOT EXECUTED
RULECHECK CSR.R.1:M2_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM2_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM2 ..... NOT EXECUTED
RULECHECK CSR.R.1:M3i ..... NOT EXECUTED
RULECHECK CSR.R.1:M3_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM3_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM3 ..... NOT EXECUTED
RULECHECK CSR.R.1:M4i ..... NOT EXECUTED
RULECHECK CSR.R.1:M4_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM4_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM4 ..... NOT EXECUTED
RULECHECK CSR.R.1:M5i ..... NOT EXECUTED
RULECHECK CSR.R.1:M5_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM5_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM5 ..... NOT EXECUTED
RULECHECK CSR.R.1:M6i ..... NOT EXECUTED
RULECHECK CSR.R.1:M6_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM6_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM6 ..... NOT EXECUTED
RULECHECK CSR.R.1:M7i ..... NOT EXECUTED
RULECHECK CSR.R.1:M7_real ..... NOT EXECUTED
RULECHECK CSR.R.1:DM7_O ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM7 ..... NOT EXECUTED
RULECHECK CSR.R.1:M8_OLD ..... NOT EXECUTED
RULECHECK CSR.R.1:M8_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM8_OLD ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM8_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:M9_OLD ..... NOT EXECUTED
RULECHECK CSR.R.1:M9_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM9_OLD ..... NOT EXECUTED
RULECHECK CSR.R.1:DUM9_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA1i ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA2i ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA3i ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA4i ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA5i ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA6i ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA7_OLD ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA7_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA8_OLD ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA8_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:VIA9_OLD ..... NOT EXECUTED
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RULECHECK CSR.R.1:VIA9_NEW ..... NOT EXECUTED
RULECHECK CSR.R.1:ODi ..... NOT EXECUTED
RULECHECK CSR.R.1:DOD ..... NOT EXECUTED
RULECHECK CSR.R.1:POi ..... NOT EXECUTED
RULECHECK CSR.R.1:DPO ..... NOT EXECUTED
RULECHECK CSR.R.1:mVTLi ..... NOT EXECUTED
RULECHECK CSR.R.1:INDDMY_COIL ..... NOT EXECUTED
RULECHECK CSR.R.1:INDDMY_MD ..... NOT EXECUTED
RULECHECK CSR.R.1:INDDMY_HD ..... NOT EXECUTED
RULECHECK CSR.R.2:A ..... NOT EXECUTED
RULECHECK CSR.R.2:B ..... NOT EXECUTED
RULECHECK CSR.R.2:C ..... NOT EXECUTED
RULECHECK CSR.R.2:D ..... NOT EXECUTED
RULECHECK CSR.R.2:E ..... NOT EXECUTED
RULECHECK CSR.R.2:F ..... NOT EXECUTED
RULECHECK CSR.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.2 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.S.4 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.4 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.R.3:CO ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA1 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA2 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA3 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA4 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA5 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA6 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA7 ..... NOT EXECUTED
RULECHECK CSR.R.3:VIA8 ..... NOT EXECUTED
RULECHECK CSR.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.W.2 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.L.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.5.1 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M1i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M2i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M3i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M4i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M5i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M6i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M7i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M8i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:M9i ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.6.1:APi ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA1 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA2 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA3 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA4 ..... TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA5 ..... TOTAL Result Count = 0 (0)
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RULECHECK CSR.EN.7:VIA6 ................. TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA7 ................. TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.7:VIA8 ................. TOTAL Result Count = 0 (0)
RULECHECK CSR.EN.8 ..................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M1 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M2 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M3 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M4 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M5 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M6 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M7 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M8 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:M9 .................... TOTAL Result Count = 0 (0)
RULECHECK SR.S.1:AP .................... TOTAL Result Count = 0 (0)
RULECHECK SR.AP:WARNING ................ TOTAL Result Count = 0 (0)
RULECHECK SR.CB2:WARNING ............... TOTAL Result Count = 0 (0)
RULECHECK SR.CB:WARNING ................ TOTAL Result Count = 0 (0)
RULECHECK SR.CBD_RV:WARNING ............ TOTAL Result Count = 0 (0)
RULECHECK SR.UBM:WARNING ............... TOTAL Result Count = 0 (0)
RULECHECK SR.CO_VIA:WARNING ............ TOTAL Result Count = 0 (0)
RULECHECK SR.R.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK SR.EN.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CDU.R.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK CDU.R.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK CDU:WARNING1 ................. TOTAL Result Count = 0 (0)
RULECHECK CDU:WARNING2 ................. TOTAL Result Count = 0 (0)
RULECHECK DM1.W.1 ...................... NOT EXECUTED
RULECHECK DM1.W.2 ...................... NOT EXECUTED
RULECHECK DM1.S.1 ...................... NOT EXECUTED
RULECHECK DM1.S.2 ...................... NOT EXECUTED
RULECHECK DM1.S.3 ...................... NOT EXECUTED
RULECHECK DM1.S.3.1 .................... NOT EXECUTED
RULECHECK DM1.S.4 ...................... NOT EXECUTED
RULECHECK DM1.S.5 ...................... NOT EXECUTED
RULECHECK DM1.S.5.1 .................... NOT EXECUTED
RULECHECK DM1.S.7 ...................... NOT EXECUTED
RULECHECK DM1.S.8 ...................... NOT EXECUTED
RULECHECK DM1.S.10 ..................... NOT EXECUTED
RULECHECK DM1.EN.1 ..................... NOT EXECUTED
RULECHECK DM1.A.1 ...................... NOT EXECUTED
RULECHECK DM1.A.2 ...................... NOT EXECUTED
RULECHECK DM1.R.1 ...................... NOT EXECUTED
RULECHECK DM1.R.3 ...................... NOT EXECUTED
RULECHECK DM1_O.R.1 .................... NOT EXECUTED
RULECHECK DM2.W.1 ...................... NOT EXECUTED
RULECHECK DM2.W.2 ...................... NOT EXECUTED
RULECHECK DM2.S.1 ...................... NOT EXECUTED
RULECHECK DM2.S.2 ...................... NOT EXECUTED
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RULECHECK DM2.S.3 ..... NOT EXECUTED
RULECHECK DM2.S.3.1 ..... NOT EXECUTED
RULECHECK DM2.S.4 ..... NOT EXECUTED
RULECHECK DM2.S.5 ..... NOT EXECUTED
RULECHECK DM2.S.5.1 ..... NOT EXECUTED
RULECHECK DM2.S.7 ..... NOT EXECUTED
RULECHECK DM2.S.8 ..... NOT EXECUTED
RULECHECK DM2.S.10 ..... NOT EXECUTED
RULECHECK DM2.EN.1 ..... NOT EXECUTED
RULECHECK DM2.A.1 ..... NOT EXECUTED
RULECHECK DM2.A.2 ..... NOT EXECUTED
RULECHECK DM2.R.1 ..... NOT EXECUTED
RULECHECK DM2.R.3 ..... NOT EXECUTED
RULECHECK DM2_O.R.1 ..... NOT EXECUTED
RULECHECK DM3.W.1 ..... NOT EXECUTED
RULECHECK DM3.W.2 ..... NOT EXECUTED
RULECHECK DM3.S.1 ..... NOT EXECUTED
RULECHECK DM3.S.2 ..... NOT EXECUTED
RULECHECK DM3.S.3 ..... NOT EXECUTED
RULECHECK DM3.S.3.1 ..... NOT EXECUTED
RULECHECK DM3.S.4 ..... NOT EXECUTED
RULECHECK DM3.S.5 ..... NOT EXECUTED
RULECHECK DM3.S.5.1 ..... NOT EXECUTED
RULECHECK DM3.S.7 ..... NOT EXECUTED
RULECHECK DM3.S.8 ..... NOT EXECUTED
RULECHECK DM3.S.10 ..... NOT EXECUTED
RULECHECK DM3.EN.1 ..... NOT EXECUTED
RULECHECK DM3.A.1 ..... NOT EXECUTED
RULECHECK DM3.A.2 ..... NOT EXECUTED
RULECHECK DM3.R.1 ..... NOT EXECUTED
RULECHECK DM3.R.3 ..... NOT EXECUTED
RULECHECK DM3_O.R.1 ..... NOT EXECUTED
RULECHECK DM4.W.1 ..... NOT EXECUTED
RULECHECK DM4.W.2 ..... NOT EXECUTED
RULECHECK DM4.S.1 ..... NOT EXECUTED
RULECHECK DM4.S.2 ..... NOT EXECUTED
RULECHECK DM4.S.3 ..... NOT EXECUTED
RULECHECK DM4.S.3.1 ..... NOT EXECUTED
RULECHECK DM4.S.4 ..... NOT EXECUTED
RULECHECK DM4.S.5 ..... NOT EXECUTED
RULECHECK DM4.S.5.1 ..... NOT EXECUTED
RULECHECK DM4.S.7 ..... NOT EXECUTED
RULECHECK DM4.S.8 ..... NOT EXECUTED
RULECHECK DM4.S.10 ..... NOT EXECUTED
RULECHECK DM4.EN.1 ..... NOT EXECUTED
RULECHECK DM4.A.1 ..... NOT EXECUTED
RULECHECK DM4.A.2 ..... NOT EXECUTED
RULECHECK DM4.R.1 ..... NOT EXECUTED
RULECHECK DM4.R.3 ..... NOT EXECUTED
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RULECHECK DM4_O.R.1 ..... NOT EXECUTED
RULECHECK DM5.W.1 ..... NOT EXECUTED
RULECHECK DM5.W.2 ..... NOT EXECUTED
RULECHECK DM5.S.1 ..... NOT EXECUTED
RULECHECK DM5.S.2 ..... NOT EXECUTED
RULECHECK DM5.S.3 ..... NOT EXECUTED
RULECHECK DM5.S.3.1 ..... NOT EXECUTED
RULECHECK DM5.S.4 ..... NOT EXECUTED
RULECHECK DM5.S.5 ..... NOT EXECUTED
RULECHECK DM5.S.5.1 ..... NOT EXECUTED
RULECHECK DM5.S.7 ..... NOT EXECUTED
RULECHECK DM5.S.8 ..... NOT EXECUTED
RULECHECK DM5.S.10 ..... NOT EXECUTED
RULECHECK DM5.EN.1 ..... NOT EXECUTED
RULECHECK DM5.A.1 ..... NOT EXECUTED
RULECHECK DM5.A.2 ..... NOT EXECUTED
RULECHECK DM5.R.1 ..... NOT EXECUTED
RULECHECK DM5.R.3 ..... NOT EXECUTED
RULECHECK DM5_O.R.1 ..... NOT EXECUTED
RULECHECK DM6.W.1 ..... NOT EXECUTED
RULECHECK DM6.W.2 ..... NOT EXECUTED
RULECHECK DM6.S.1 ..... NOT EXECUTED
RULECHECK DM6.S.2 ..... NOT EXECUTED
RULECHECK DM6.S.3 ..... NOT EXECUTED
RULECHECK DM6.S.3.1 ..... NOT EXECUTED
RULECHECK DM6.S.4 ..... NOT EXECUTED
RULECHECK DM6.S.5 ..... NOT EXECUTED
RULECHECK DM6.S.5.1 ..... NOT EXECUTED
RULECHECK DM6.S.7 ..... NOT EXECUTED
RULECHECK DM6.S.8 ..... NOT EXECUTED
RULECHECK DM6.S.10 ..... NOT EXECUTED
RULECHECK DM6.EN.1 ..... NOT EXECUTED
RULECHECK DM6.A.1 ..... NOT EXECUTED
RULECHECK DM6.A.2 ..... NOT EXECUTED
RULECHECK DM6.R.1 ..... NOT EXECUTED
RULECHECK DM6.R.3 ..... NOT EXECUTED
RULECHECK DM6_O.R.1 ..... NOT EXECUTED
RULECHECK DM7.W.1 ..... NOT EXECUTED
RULECHECK DM7.W.2 ..... NOT EXECUTED
RULECHECK DM7.S.1 ..... NOT EXECUTED
RULECHECK DM7.S.2 ..... NOT EXECUTED
RULECHECK DM7.S.3 ..... NOT EXECUTED
RULECHECK DM7.S.3.1 ..... NOT EXECUTED
RULECHECK DM7.S.4 ..... NOT EXECUTED
RULECHECK DM7.S.5 ..... NOT EXECUTED
RULECHECK DM7.S.5.1 ..... NOT EXECUTED
RULECHECK DM7.S.7 ..... NOT EXECUTED
RULECHECK DM7.S.8 ..... NOT EXECUTED
RULECHECK DM7.S.9 ..... NOT EXECUTED
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RULECHECK DM7.S.10 ..... NOT EXECUTED
RULECHECK DM7.EN.1 ..... NOT EXECUTED
RULECHECK DM7.A.1 ..... NOT EXECUTED
RULECHECK DM7.A.2 ..... NOT EXECUTED
RULECHECK DM7.R.1 ..... NOT EXECUTED
RULECHECK DM7.R.3 ..... NOT EXECUTED
RULECHECK DM7_O.R.1 ..... NOT EXECUTED
RULECHECK DM8.W.1 ..... NOT EXECUTED
RULECHECK DM8.W.2 ..... NOT EXECUTED
RULECHECK DM8.S.1 ..... NOT EXECUTED
RULECHECK DM8.S.2 ..... NOT EXECUTED
RULECHECK DM8.S.3 ..... NOT EXECUTED
RULECHECK DM8.S.4 ..... NOT EXECUTED
RULECHECK DM8.S.5 ..... NOT EXECUTED
RULECHECK DM8.S.5.1 ..... NOT EXECUTED
RULECHECK DM8.S.7 ..... NOT EXECUTED
RULECHECK DM8.S.8 ..... NOT EXECUTED
RULECHECK DM8.EN.1 ..... NOT EXECUTED
RULECHECK DM8.A.1 ..... NOT EXECUTED
RULECHECK DM8.A.2 ..... NOT EXECUTED
RULECHECK DM8.R.1 ..... NOT EXECUTED
RULECHECK DM8.R.3 ..... NOT EXECUTED
RULECHECK DM9.W.1 ..... NOT EXECUTED
RULECHECK DM9.W.2 ..... NOT EXECUTED
RULECHECK DM9.S.1 ..... NOT EXECUTED
RULECHECK DM9.S.2 ..... NOT EXECUTED
RULECHECK DM9.S.3 ..... NOT EXECUTED
RULECHECK DM9.S.4 ..... NOT EXECUTED
RULECHECK DM9.S.5 ..... NOT EXECUTED
RULECHECK DM9.S.5.1 ..... NOT EXECUTED
RULECHECK DM9.S.7 ..... NOT EXECUTED
RULECHECK DM9.S.8 ..... NOT EXECUTED
RULECHECK DM9.EN.1 ..... NOT EXECUTED
RULECHECK DM9.A.1 ..... NOT EXECUTED
RULECHECK DM9.A.2 ..... NOT EXECUTED
RULECHECK DM9.R.1 ..... NOT EXECUTED
RULECHECK DM9.R.3 ..... NOT EXECUTED
RULECHECK RV.W.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK RV.S.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK RV.S.3.WB ..... TOTAL Result Count = 0 (0)
RULECHECK RV.EN.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK RV.R.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.W.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.W.2.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.S.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.S.2.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.S.3.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.EN.1.WB ..... TOTAL Result Count = 0 (0)
RULECHECK AP.EN.2.WB ..... TOTAL Result Count = 0 (0)
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RULECHECK AP.DN.1:L ..................... NOT EXECUTED
RULECHECK AP.DN.1:H ..................... NOT EXECUTED
RULECHECK FUSE_WARN.1 ................... TOTAL Result Count = 0 (0)
RULECHECK FUSE_WARN.2 ................... TOTAL Result Count = 0 (0)
RULECHECK FUSE_WARN.3 ................... TOTAL Result Count = 0 (0)
RULECHECK FU.L.1.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK FU.S.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK LW.W.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK LW.L.1 ........................ TOTAL Result Count = 0 (0)
RULECHECK LW.EN.1 ....................... TOTAL Result Count = 0 (0)
RULECHECK LW.EN.2 ....................... TOTAL Result Count = 0 (0)
RULECHECK LOGO.S.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK LOGO.O.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK LUP.1g ........................ TOTAL Result Count = 0 (0)
RULECHECK LUP.2g ........................ TOTAL Result Count = 0 (0)
RULECHECK LUP.3.1.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.1.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.2.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.2.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.3.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.3.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.4.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.4.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.5.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.3.5.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.4g ........................ TOTAL Result Count = 0 (0)
RULECHECK LUP.5.1.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.1.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.2.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.2.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.3.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.3.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.4.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.4.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.5.1g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.5.5.2g .................... TOTAL Result Count = 0 (0)
RULECHECK LUP.6 ......................... TOTAL Result Count = 0 (0)
RULECHECK ESD.WARN.1 .................... NOT EXECUTED
RULECHECK ESD.WARN.2 .................... NOT EXECUTED
RULECHECK ESD.1g ........................ NOT EXECUTED
RULECHECK ESD.3g ........................ NOT EXECUTED
RULECHECK ESD.4g ........................ NOT EXECUTED
RULECHECK ESD.5g ........................ NOT EXECUTED
RULECHECK ESD.6g ........................ NOT EXECUTED
RULECHECK ESD.7g ........................ NOT EXECUTED
RULECHECK ESD.12g ....................... NOT EXECUTED
RULECHECK ESD.16g ....................... NOT EXECUTED
RULECHECK ESD.17g ....................... NOT EXECUTED
RULECHECK ESD.18g ....................... NOT EXECUTED
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RULECHECK ESD.19g ..... NOT EXECUTED
RULECHECK ESD.20g ..... NOT EXECUTED
RULECHECK ESD.21g ..... NOT EXECUTED
RULECHECK ESD.22g ..... NOT EXECUTED
RULECHECK ESD.23g ..... NOT EXECUTED
RULECHECK ESD.27g ..... NOT EXECUTED
RULECHECK ESD.28g ..... NOT EXECUTED
RULECHECK ESD.30g ..... NOT EXECUTED
RULECHECK ESD.32g ..... NOT EXECUTED
RULECHECK ESD.33g ..... NOT EXECUTED
RULECHECK ESD.34g ..... NOT EXECUTED
RULECHECK ESD.37g ..... NOT EXECUTED
RULECHECK ESD.47g ..... NOT EXECUTED
RULECHECK ESD.48g ..... NOT EXECUTED
RULECHECK ESD.49g ..... NOT EXECUTED
RULECHECK ESD.50g ..... NOT EXECUTED
RULECHECK ESD.51g ..... NOT EXECUTED
RULECHECK ESD.52g ..... NOT EXECUTED
RULECHECK ESD.55g ..... NOT EXECUTED
RULECHECK ESD.56g ..... NOT EXECUTED
RULECHECK ESD.57g ..... NOT EXECUTED
RULECHECK ESD.58g ..... NOT EXECUTED
RULECHECK ESD.59g ..... NOT EXECUTED
RULECHECK ESD.60g ..... NOT EXECUTED
RULECHECK ESD.61g ..... NOT EXECUTED
RULECHECK ESD.62g ..... NOT EXECUTED
RULECHECK ESD.63g ..... NOT EXECUTED
RULECHECK ESD.64g ..... NOT EXECUTED
RULECHECK ESD.65g ..... NOT EXECUTED
RULECHECK ESD.66g ..... NOT EXECUTED
RULECHECK ESD.72g ..... NOT EXECUTED
RULECHECK ESDIMP.W.1 ..... NOT EXECUTED
RULECHECK ESDIMP.S.1 ..... NOT EXECUTED
RULECHECK ESDIMP.S.2 ..... NOT EXECUTED
RULECHECK ESDIMP.EN.1 ..... NOT EXECUTED
RULECHECK ESDIMP.A.1 ..... NOT EXECUTED
RULECHECK ESDIMP.A.2 ..... NOT EXECUTED
RULECHECK ESDIMP.R.1 ..... NOT EXECUTED
RULECHECK ESDIMP.EN.1:R ..... NOT EXECUTED
RULECHECK SRAM.W.1 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.S.1 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.S.2 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.EN.1 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.EX.1 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.O.1 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.R.12 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.R.13 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.R.15 ..... TOTAL Result Count = 0 (0)
RULECHECK SRAM.R.17 ..... TOTAL Result Count = 0 (0)
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RULECHECK SRAM.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK NW.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK OD.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK PO.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK NP.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK PP.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK CO.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK M1.S.1:SRM_SRAMDMY ........... TOTAL Result Count = 0 (0)
RULECHECK VIA1.S.1:SRM_SRAMDMY ......... TOTAL Result Count = 0 (0)
RULECHECK WLD.R.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK WLD.R.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK WLD.R.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK WLD.R.6 ...................... TOTAL Result Count = 0 (0)
RULECHECK WLD.R.7 ...................... TOTAL Result Count = 0 (0)
RULECHECK PO.S.14m ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.EN.1m ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.EN.2m ..................... TOTAL Result Count = 0 (0)
RULECHECK PO.EN.3m ..................... TOTAL Result Count = 0 (0)
RULECHECK BJT.R.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK BJT.R.8 ...................... TOTAL Result Count = 0 (0)
RULECHECK RES.2m:OD .................... TOTAL Result Count = 0 (0)
RULECHECK RES.2m:PO .................... TOTAL Result Count = 0 (0)
RULECHECK NWROD.R.1m ................... TOTAL Result Count = 0 (0)
RULECHECK NWRSTI.R.1m .................. TOTAL Result Count = 0 (0)
RULECHECK SBD.W.1__SBD.W.1.1 ........... TOTAL Result Count = 0 (0)
RULECHECK SBD.W.2__SBD.W.2.1 ........... TOTAL Result Count = 0 (0)
RULECHECK SBD.W.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.W.4 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.S.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.E.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.E.1.1 .................... TOTAL Result Count = 0 (0)
RULECHECK SBD.E.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.E.2.1 .................... TOTAL Result Count = 0 (0)
RULECHECK SBD.E.2.2 .................... TOTAL Result Count = 0 (0)
RULECHECK SBD.E.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.O.1 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.R.2 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.R.3 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.R.4 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.R.5 ...................... TOTAL Result Count = 0 (0)
RULECHECK SBD.R.6 ...................... TOTAL Result Count = 0 (0)
RULECHECK _VAR.R.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK _VAR.R.5 ..................... TOTAL Result Count = 0 (0)
RULECHECK VAR.R.6 ...................... TOTAL Result Count = 0 (0)
RULECHECK VAR.R.7 ...................... TOTAL Result Count = 0 (0)
RULECHECK VAR.R.8 ...................... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
```

```
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                   1
TOTAL REAL Time:                  1
TOTAL Original Layer Geometries: 5976 (25347)
TOTAL DRC RuleChecks Executed:   1293
TOTAL DRC Results Generated:     0 (0)
```

4.4 The LVS report

```
##################################################
##                                              ##
##        C A L I B R E   S Y S T E M           ##
##                                              ##
##            L V S   R E P O R T               ##
##                                              ##
##################################################
```

```
REPORT FILE NAME:         Neuron.lvs.report
LAYOUT NAME:              /uio/hume/student-u52/kunzh/cadence617_tsmc65rf_oa/Neuron.sp ('Neuron')
SOURCE NAME:              /uio/hume/student-u52/kunzh/cadence617_tsmc65rf_oa/Neuron.src.net ('Neuron')
RULE FILE:                /uio/hume/student-u52/kunzh/cadence617_tsmc65rf_oa/_calibre.lvs_
CREATION TIME:            Wed Nov 10 19:33:13 2021
CURRENT DIRECTORY:        /uio/hume/student-u52/kunzh/cadence617_tsmc65rf_oa
USER NAME:                kunzh
CALIBRE VERSION:          v2020.4_15.9    Thu Oct 1 15:09:27 PDT 2020
```

OVERALL COMPARISON RESULTS

```
      #       ###################       _   _
     #        #                 #       *   *
  #   #       #     CORRECT     #         |
   # #        #                 #       \___/
    #         ###################
```

```
*********************************************************************************************************
                                  CELL  SUMMARY
*********************************************************************************************************

  Result         Layout                      Source
  -----------    -----------                 --------------
  CORRECT        Neuron                      Neuron
```

```
*********************************************************************************************************
                                  LVS PARAMETERS
*********************************************************************************************************

o LVS Setup:

   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                          "AHVDD" "AHVDDB" "AHVDDG" "AHVDDR" "AHVDDWELL" "AVDD" "AVDDB" "AVDDB
                                           G" "AVDDG" "AVDDR"
                                           "AVDWELL" "DHVDD" "DVDD" "HVDDWELL" "TACVDD" "TAVD33" "TAVD33PST" "T
                                           AVDD" "TAVDDPST"
                                           "TVDD" "VD33" "VDD" "VDD5V" "VDDESD" "VDDG" "VDDM" "VDDPST" "VDDSA"
```

```
                                    "VDWELL"
LVS GROUND NAME                     "AGND" "AHVSS" "AHVSSB" "AHVSSG" "AHVSSR" "AHVSSUB" "AVSS" "AVSSB" "
                                    AVSSBG" "AVSSG"
                                    "AVSSR" "AVSSUB" "DHVSS" "DVSS" "GND" "HVSSUB" "TAVSS" "TAVSSPST" "T
                                    VSS" "VS33" "VSS"
                                    "VSSESD" "VSSG" "VSSM" "VSSPST" "VSSUB"
LVS CELL SUPPLY                     NO
LVS RECOGNIZE GATES                 ALL
// LVS HCELL REPORT
LVS IGNORE PORTS                    NO
LVS CHECK PORT NAMES                YES
LVS IGNORE TRIVIAL NAMED PORTS      NO
LVS BUILTIN DEVICE PIN SWAP         YES
LVS ALL CAPACITOR PINS SWAPPABLE    YES
LVS DISCARD PINS BY DEVICE          NO
LVS SOFT SUBSTRATE PINS             NO
LVS INJECT LOGIC                    YES
LVS EXPAND UNBALANCED CELLS         YES
LVS FLATTEN INSIDE CELL             NO
LVS EXPAND SEED PROMOTIONS          NO
LVS PRESERVE PARAMETERIZED CELLS    NO
LVS GLOBALS ARE PORTS               YES
LVS REVERSE WL                      NO
LVS SPICE PREFER PINS               YES
LVS SPICE SLASH IS SPACE            YES
LVS SPICE ALLOW FLOATING PINS       YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS    NO
LVS SPICE CONDITIONAL LDD           NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS NO
// LVS SPICE EXCLUDE CELL SOURCE
// LVS SPICE EXCLUDE CELL LAYOUT
LVS SPICE IMPLIED MOS AREA          NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS          NO
LVS SPICE REDEFINE PARAM            NO
LVS SPICE REPLICATE DEVICES         NO
LVS SPICE SCALE X PARAMETERS        NO
LVS SPICE STRICT WL                 NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                 NO
LVS EXACT SUBTYPES                  NO
LAYOUT CASE                         NO
SOURCE CASE                         NO
LVS COMPARE CASE                    NO
LVS COMPARE CASE STRICT             NO
LVS DOWNCASE DEVICE                 NO
LVS REPORT MAXIMUM                  50
LVS PROPERTY RESOLUTION MAXIMUM     65536
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                    YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE
// LVS IGNORE DEVICE PIN
// LVS PREFER NETS FILTER SOURCE
// LVS PREFER NETS FILTER LAYOUT
LVS PREFER PORT NETS                NO
LVS EXPAND ON ERROR                 NO
```

```
// Device Type Map

LVS DEVICE TYPE                         RESISTOR "rm1" "rm10" "rm2" "rm3" "rm4" "rm5" "rm6" "rm7" "rm8" "rm9
                                                 " "rnodl" "rnodl_m"
                                                 "rnods" "rnods_m" "rnodwo" "rnodwo_m" "rnpolyl" "rnpolyl_m"
                                                 "rnpolys"
                                                 "rnpolys_m" "rnpolywo" "rnpolywo_m" "rnwod" "rnwod_m" "rnws
                                                 ti" "rnwsti_m"
                                                 "rpodl" "rpodl_m" "rpods" "rpods_m" "rpodwo" "rpodwo_m" "rp
                                                 polyl" "rppolyl_m"
                                                 "rppolyl_rf" "rppolyl_rf_rdk" "rppolys" "rppolys_m" "rppoly
                                                 s_rf"
                                                 "rppolys_rf_rdk" "rppolywo" "rppolywo_m" "rppolywo_rf" "rpp
                                                 olywo_rf_rdk"
                                                 [ POS=PLUS NEG=MINUS ]  SOURCE LAYOUT

// Reduction

LVS REDUCE SERIES MOS                   NO
LVS REDUCE PARALLEL MOS                 YES
LVS REDUCE SEMI SERIES MOS              NO
LVS REDUCE SPLIT GATES                  NO
LVS REDUCE PARALLEL BIPOLAR             YES
LVS REDUCE SERIES CAPACITORS            YES
LVS REDUCE PARALLEL CAPACITORS          YES
LVS REDUCE SERIES RESISTORS             YES
LVS REDUCE PARALLEL RESISTORS           YES
LVS REDUCE PARALLEL DIODES              YES

LVS REDUCE  rnwsti_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnwsti_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnwod_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnwod_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rpodwo_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rpodwo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnodwo_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnodwo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rpodl_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rpodl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnodl_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnodl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rpods_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rpods_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnods_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnods_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rppolys_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rppolys_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnpolys_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnpolys_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rppolyl_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rppolyl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnpolyl_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnpolyl_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rppolywo_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rppolywo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rnpolywo_m  PARALLEL [ TOLERANCE lr 0 ]
LVS REDUCE  rnpolywo_m  SERIES PLUS MINUS [ TOLERANCE wr 0 ]
LVS REDUCE  rppolyl_rf  PARALLEL NO
LVS REDUCE  rppolyl_rf  SERIES PLUS MINUS NO
LVS REDUCE  rppolyl_rf_rdk  PARALLEL NO
```

```
LVS REDUCE  rppolyl_rf_rdk  SERIES PLUS MINUS NO
LVS REDUCE  rppolys_rf  PARALLEL NO
LVS REDUCE  rppolys_rf  SERIES PLUS MINUS NO
LVS REDUCE  rppolys_rf_rdk  PARALLEL NO
LVS REDUCE  rppolys_rf_rdk  SERIES PLUS MINUS NO
LVS REDUCE  rppolywo_rf  PARALLEL NO
LVS REDUCE  rppolywo_rf  SERIES PLUS MINUS NO
LVS REDUCE  rppolywo_rf_rdk  PARALLEL NO
LVS REDUCE  rppolywo_rf_rdk  SERIES PLUS MINUS NO
LVS REDUCTION PRIORITY                PARALLEL

LVS SHORT EQUIVALENT NODES            NO

// Filter

LVS FILTER  D(pnwdio)  OPEN LAYOUT

// Trace Property

TRACE PROPERTY  lddp(pch_hv25_spw)  l l 0
TRACE PROPERTY  lddp(pch_hv25_spw)  w w 0
TRACE PROPERTY  lddn(nch_hv25_snw)  l l 0
TRACE PROPERTY  lddn(nch_hv25_snw)  w w 0
TRACE PROPERTY  mn(nch)  l l 0
TRACE PROPERTY  mn(nch)  w w 0
TRACE PROPERTY  mn(nch_18)  l l 0
TRACE PROPERTY  mn(nch_18)  w w 0
TRACE PROPERTY  mn(nch_18_dnw)  l l 0
TRACE PROPERTY  mn(nch_18_dnw)  w w 0
TRACE PROPERTY  mn(nch_25)  l l 0
TRACE PROPERTY  mn(nch_25)  w w 0
TRACE PROPERTY  mn(nch_25_dnw)  l l 0
TRACE PROPERTY  mn(nch_25_dnw)  w w 0
TRACE PROPERTY  mn(nch_25_dnwod)  l l 0
TRACE PROPERTY  mn(nch_25_dnwod)  w w 0
TRACE PROPERTY  mn(nch_25_dnwud)  l l 0
TRACE PROPERTY  mn(nch_25_dnwud)  w w 0
TRACE PROPERTY  mn(nch_25od)  l l 0
TRACE PROPERTY  mn(nch_25od)  w w 0
TRACE PROPERTY  mn(nch_25od28)  l l 0
TRACE PROPERTY  mn(nch_25od28)  w w 0
TRACE PROPERTY  mn(nch_25od28_dnw)  l l 0
TRACE PROPERTY  mn(nch_25od28_dnw)  w w 0
TRACE PROPERTY  mn(nch_25ud)  l l 0
TRACE PROPERTY  mn(nch_25ud)  w w 0
TRACE PROPERTY  mn(nch_33)  l l 0
TRACE PROPERTY  mn(nch_33)  w w 0
TRACE PROPERTY  mn(nch_33_dnw)  l l 0
TRACE PROPERTY  mn(nch_33_dnw)  w w 0
TRACE PROPERTY  mn(nch_dnw)  l l 0
TRACE PROPERTY  mn(nch_dnw)  w w 0
TRACE PROPERTY  mn(nch_dnw_1tr)  l l 0
TRACE PROPERTY  mn(nch_dnw_1tr)  w w 0
TRACE PROPERTY  mn(nch_dnw_w)  l l 0
TRACE PROPERTY  mn(nch_dnw_w)  w w 0
TRACE PROPERTY  mn(nch_dnw_w_lvt)  l l 0
TRACE PROPERTY  mn(nch_dnw_w_lvt)  w w 0
TRACE PROPERTY  mn(nch_esd18)  l l 0
TRACE PROPERTY  mn(nch_esd18)  w w 0
TRACE PROPERTY  mn(nch_esd18_dnw)  l l 0
TRACE PROPERTY  mn(nch_esd18_dnw)  w w 0
```

```
TRACE PROPERTY  mn(nch_hvt)  l l 0
TRACE PROPERTY  mn(nch_hvt)  w w 0
TRACE PROPERTY  mn(nch_hvt_dnw)  l l 0
TRACE PROPERTY  mn(nch_hvt_dnw)  w w 0
TRACE PROPERTY  mn(nch_lpg)  l l 0
TRACE PROPERTY  mn(nch_lpg)  w w 0
TRACE PROPERTY  mn(nch_lpghvt)  l l 0
TRACE PROPERTY  mn(nch_lpghvt)  w w 0
TRACE PROPERTY  mn(nch_lpgna)  l l 0
TRACE PROPERTY  mn(nch_lpgna)  w w 0
TRACE PROPERTY  mn(nch_lvt)  l l 0
TRACE PROPERTY  mn(nch_lvt)  w w 0
TRACE PROPERTY  mn(nch_lvt_dnw)  l l 0
TRACE PROPERTY  mn(nch_lvt_dnw)  w w 0
TRACE PROPERTY  mn(nch_mlvt)  l l 0
TRACE PROPERTY  mn(nch_mlvt)  w w 0
TRACE PROPERTY  mn(nch_mlvt_dnw)  l l 0
TRACE PROPERTY  mn(nch_mlvt_dnw)  w w 0
TRACE PROPERTY  mn(nch_na)  l l 0
TRACE PROPERTY  mn(nch_na)  w w 0
TRACE PROPERTY  mn(nch_na18)  l l 0
TRACE PROPERTY  mn(nch_na18)  w w 0
TRACE PROPERTY  mn(nch_na25)  l l 0
TRACE PROPERTY  mn(nch_na25)  w w 0
TRACE PROPERTY  mn(nch_na25od)  l l 0
TRACE PROPERTY  mn(nch_na25od)  w w 0
TRACE PROPERTY  mn(nch_na25ud)  l l 0
TRACE PROPERTY  mn(nch_na25ud)  w w 0
TRACE PROPERTY  mn(nch_na33)  l l 0
TRACE PROPERTY  mn(nch_na33)  w w 0
TRACE PROPERTY  mn(nch_timer)  l l 0
TRACE PROPERTY  mn(nch_timer)  w w 0
TRACE PROPERTY  mn(nch_uhvt)  l l 0
TRACE PROPERTY  mn(nch_uhvt)  w w 0
TRACE PROPERTY  mn(nch_uhvt_dnw)  l l 0
TRACE PROPERTY  mn(nch_uhvt_dnw)  w w 0
TRACE PROPERTY  mn(nch_ulvt)  l l 0
TRACE PROPERTY  mn(nch_ulvt)  w w 0
TRACE PROPERTY  mn(nch_ulvt_dnw)  l l 0
TRACE PROPERTY  mn(nch_ulvt_dnw)  w w 0
TRACE PROPERTY  mn(nch_w)  l l 0
TRACE PROPERTY  mn(nch_w)  w w 0
TRACE PROPERTY  mn(nch_w_lvt)  l l 0
TRACE PROPERTY  mn(nch_w_lvt)  w w 0
TRACE PROPERTY  mn(nchpd_dphcsr)  l l 0
TRACE PROPERTY  mn(nchpd_dphcsr)  w w 0
TRACE PROPERTY  mn(nchpd_dpsr)  l l 0
TRACE PROPERTY  mn(nchpd_dpsr)  w w 0
TRACE PROPERTY  mn(nchpd_hvtdphcsr)  l l 0
TRACE PROPERTY  mn(nchpd_hvtdphcsr)  w w 0
TRACE PROPERTY  mn(nchpd_hvtdpsr)  l l 0
TRACE PROPERTY  mn(nchpd_hvtdpsr)  w w 0
TRACE PROPERTY  mn(nchpd_hvtsr)  l l 0
TRACE PROPERTY  mn(nchpd_hvtsr)  w w 0
TRACE PROPERTY  mn(nchpd_lpgdpsr)  l l 0
TRACE PROPERTY  mn(nchpd_lpgdpsr)  w w 0
TRACE PROPERTY  mn(nchpd_lpgsr)  l l 0
TRACE PROPERTY  mn(nchpd_lpgsr)  w w 0
TRACE PROPERTY  mn(nchpd_lpgtpsr)  l l 0
TRACE PROPERTY  mn(nchpd_lpgtpsr)  w w 0
TRACE PROPERTY  mn(nchpd_sr)  l l 0
```

```
TRACE PROPERTY  mn(nchpd_sr)  w w 0
TRACE PROPERTY  mn(nchpd_ulpdpsr)  l l 0
TRACE PROPERTY  mn(nchpd_ulpdpsr)  w w 0
TRACE PROPERTY  mn(nchpd_ulpsr)  l l 0
TRACE PROPERTY  mn(nchpd_ulpsr)  w w 0
TRACE PROPERTY  mn(nchpd_wisr)  l l 0
TRACE PROPERTY  mn(nchpd_wisr)  w w 0
TRACE PROPERTY  mn(nchpd_wosr)  l l 0
TRACE PROPERTY  mn(nchpd_wosr)  w w 0
TRACE PROPERTY  mn(nchpg_dphcsr)  l l 0
TRACE PROPERTY  mn(nchpg_dphcsr)  w w 0
TRACE PROPERTY  mn(nchpg_dpsr)  l l 0
TRACE PROPERTY  mn(nchpg_dpsr)  w w 0
TRACE PROPERTY  mn(nchpg_hvtdphcsr)  l l 0
TRACE PROPERTY  mn(nchpg_hvtdphcsr)  w w 0
TRACE PROPERTY  mn(nchpg_hvtdpsr)  l l 0
TRACE PROPERTY  mn(nchpg_hvtdpsr)  w w 0
TRACE PROPERTY  mn(nchpg_hvtsr)  l l 0
TRACE PROPERTY  mn(nchpg_hvtsr)  w w 0
TRACE PROPERTY  mn(nchpg_lpgdpsr)  l l 0
TRACE PROPERTY  mn(nchpg_lpgdpsr)  w w 0
TRACE PROPERTY  mn(nchpg_lpgsr)  l l 0
TRACE PROPERTY  mn(nchpg_lpgsr)  w w 0
TRACE PROPERTY  mn(nchpg_lpgtpsr)  l l 0
TRACE PROPERTY  mn(nchpg_lpgtpsr)  w w 0
TRACE PROPERTY  mn(nchpg_sr)  l l 0
TRACE PROPERTY  mn(nchpg_sr)  w w 0
TRACE PROPERTY  mn(nchpg_ulpdpsr)  l l 0
TRACE PROPERTY  mn(nchpg_ulpdpsr)  w w 0
TRACE PROPERTY  mn(nchpg_ulpsr)  l l 0
TRACE PROPERTY  mn(nchpg_ulpsr)  w w 0
TRACE PROPERTY  mn(nchpg_wisr)  l l 0
TRACE PROPERTY  mn(nchpg_wisr)  w w 0
TRACE PROPERTY  mn(nchpg_wosr)  l l 0
TRACE PROPERTY  mn(nchpg_wosr)  w w 0
TRACE PROPERTY  mp(pch)  l l 0
TRACE PROPERTY  mp(pch)  w w 0
TRACE PROPERTY  mp(pch_18)  l l 0
TRACE PROPERTY  mp(pch_18)  w w 0
TRACE PROPERTY  mp(pch_25)  l l 0
TRACE PROPERTY  mp(pch_25)  w w 0
TRACE PROPERTY  mp(pch_25od)  l l 0
TRACE PROPERTY  mp(pch_25od)  w w 0
TRACE PROPERTY  mp(pch_25od28)  l l 0
TRACE PROPERTY  mp(pch_25od28)  w w 0
TRACE PROPERTY  mp(pch_25ud)  l l 0
TRACE PROPERTY  mp(pch_25ud)  w w 0
TRACE PROPERTY  mp(pch_33)  l l 0
TRACE PROPERTY  mp(pch_33)  w w 0
TRACE PROPERTY  mp(pch_edc)  l l 0
TRACE PROPERTY  mp(pch_edc)  w w 0
TRACE PROPERTY  mp(pch_hvt)  l l 0
TRACE PROPERTY  mp(pch_hvt)  w w 0
TRACE PROPERTY  mp(pch_lpg)  l l 0
TRACE PROPERTY  mp(pch_lpg)  w w 0
TRACE PROPERTY  mp(pch_lpghvt)  l l 0
TRACE PROPERTY  mp(pch_lpghvt)  w w 0
TRACE PROPERTY  mp(pch_lvt)  l l 0
TRACE PROPERTY  mp(pch_lvt)  w w 0
TRACE PROPERTY  mp(pch_mlvt)  l l 0
TRACE PROPERTY  mp(pch_mlvt)  w w 0
```

```
TRACE PROPERTY  mp(pch_timer)  l l 0
TRACE PROPERTY  mp(pch_timer)  w w 0
TRACE PROPERTY  mp(pch_uhvt)  l l 0
TRACE PROPERTY  mp(pch_uhvt)  w w 0
TRACE PROPERTY  mp(pch_ulvt)  l l 0
TRACE PROPERTY  mp(pch_ulvt)  w w 0
TRACE PROPERTY  mp(pch_w)  l l 0
TRACE PROPERTY  mp(pch_w)  w w 0
TRACE PROPERTY  mp(pch_w_lvt)  l l 0
TRACE PROPERTY  mp(pch_w_lvt)  w w 0
TRACE PROPERTY  mp(pchpu_dphcsr)  l l 0
TRACE PROPERTY  mp(pchpu_dphcsr)  w w 0
TRACE PROPERTY  mp(pchpu_dpsr)  l l 0
TRACE PROPERTY  mp(pchpu_dpsr)  w w 0
TRACE PROPERTY  mp(pchpu_hvtdphcsr)  l l 0
TRACE PROPERTY  mp(pchpu_hvtdphcsr)  w w 0
TRACE PROPERTY  mp(pchpu_hvtdpsr)  l l 0
TRACE PROPERTY  mp(pchpu_hvtdpsr)  w w 0
TRACE PROPERTY  mp(pchpu_hvtsr)  l l 0
TRACE PROPERTY  mp(pchpu_hvtsr)  w w 0
TRACE PROPERTY  mp(pchpu_lpgdpsr)  l l 0
TRACE PROPERTY  mp(pchpu_lpgdpsr)  w w 0
TRACE PROPERTY  mp(pchpu_lpgsr)  l l 0
TRACE PROPERTY  mp(pchpu_lpgsr)  w w 0
TRACE PROPERTY  mp(pchpu_lpgtpsr)  l l 0
TRACE PROPERTY  mp(pchpu_lpgtpsr)  w w 0
TRACE PROPERTY  mp(pchpu_sr)  l l 0
TRACE PROPERTY  mp(pchpu_sr)  w w 0
TRACE PROPERTY  mp(pchpu_ulpdpsr)  l l 0
TRACE PROPERTY  mp(pchpu_ulpdpsr)  w w 0
TRACE PROPERTY  mp(pchpu_ulpsr)  l l 0
TRACE PROPERTY  mp(pchpu_ulpsr)  w w 0
TRACE PROPERTY  mp(pchpu_wisr)  l l 0
TRACE PROPERTY  mp(pchpu_wisr)  w w 0
TRACE PROPERTY  mp(pchpu_wosr)  l l 0
TRACE PROPERTY  mp(pchpu_wosr)  w w 0
TRACE PROPERTY  q(npn10)  a a 0
TRACE PROPERTY  q(npn10_s)  a a 0
TRACE PROPERTY  q(npn2)  a a 0
TRACE PROPERTY  q(npn2_s)  a a 0
TRACE PROPERTY  q(npn5)  a a 0
TRACE PROPERTY  q(npn5_s)  a a 0
TRACE PROPERTY  q(pnp10)  a a 0
TRACE PROPERTY  q(pnp10_s)  a a 0
TRACE PROPERTY  q(pnp2)  a a 0
TRACE PROPERTY  q(pnp2_s)  a a 0
TRACE PROPERTY  q(pnp5)  a a 0
TRACE PROPERTY  q(pnp5_s)  a a 0
TRACE PROPERTY  d(ndio)  a a 0
TRACE PROPERTY  d(ndio_18)  a a 0
TRACE PROPERTY  d(ndio_25)  a a 0
TRACE PROPERTY  d(ndio_25od)  a a 0
TRACE PROPERTY  d(ndio_25od28)  a a 0
TRACE PROPERTY  d(ndio_25ud)  a a 0
TRACE PROPERTY  d(ndio_33)  a a 0
TRACE PROPERTY  d(ndio_esd)  a a 0
TRACE PROPERTY  d(ndio_hvt)  a a 0
TRACE PROPERTY  d(ndio_lpg)  a a 0
TRACE PROPERTY  d(ndio_lpghvt)  a a 0
TRACE PROPERTY  d(ndio_lpgna)  a a 0
TRACE PROPERTY  d(ndio_lvt)  a a 0
```

```
TRACE PROPERTY  d(ndio_mlvt)  a a 0
TRACE PROPERTY  d(ndio_na)  a a 0
TRACE PROPERTY  d(ndio_na18)  a a 0
TRACE PROPERTY  d(ndio_na25)  a a 0
TRACE PROPERTY  d(ndio_na25od)  a a 0
TRACE PROPERTY  d(ndio_na25ud)  a a 0
TRACE PROPERTY  d(ndio_na33)  a a 0
TRACE PROPERTY  d(ndio_uhvt)  a a 0
TRACE PROPERTY  d(ndio_w)  a a 0
TRACE PROPERTY  d(nwdio)  a a 0
TRACE PROPERTY  d(nwdio_18)  a a 0
TRACE PROPERTY  d(nwdio_25)  a a 0
TRACE PROPERTY  d(nwdio_33)  a a 0
TRACE PROPERTY  d(pdio)  a a 0
TRACE PROPERTY  d(pdio_18)  a a 0
TRACE PROPERTY  d(pdio_25)  a a 0
TRACE PROPERTY  d(pdio_25od)  a a 0
TRACE PROPERTY  d(pdio_25od28)  a a 0
TRACE PROPERTY  d(pdio_25ud)  a a 0
TRACE PROPERTY  d(pdio_33)  a a 0
TRACE PROPERTY  d(pdio_hvt)  a a 0
TRACE PROPERTY  d(pdio_lpg)  a a 0
TRACE PROPERTY  d(pdio_lpghvt)  a a 0
TRACE PROPERTY  d(pdio_lvt)  a a 0
TRACE PROPERTY  d(pdio_mlvt)  a a 0
TRACE PROPERTY  d(pdio_uhvt)  a a 0
TRACE PROPERTY  d(pdio_w)  a a 0
TRACE PROPERTY  crtmom_rf  nv nv 0
TRACE PROPERTY  crtmom_rf  nh nh 0
TRACE PROPERTY  crtmom_rf  s s 0
TRACE PROPERTY  crtmom_rf  w w 0
TRACE PROPERTY  crtmom_rf  stm stm 0
TRACE PROPERTY  crtmom_rf  spm spm 0
TRACE PROPERTY  crtmom_rf_rdk  nv nv 0
TRACE PROPERTY  crtmom_rf_rdk  nh nh 0
TRACE PROPERTY  crtmom_rf_rdk  s s 0
TRACE PROPERTY  crtmom_rf_rdk  w w 0
TRACE PROPERTY  crtmom_rf_rdk  stm stm 0
TRACE PROPERTY  crtmom_rf_rdk  spm spm 0
TRACE PROPERTY  crtmom  nv nv 0
TRACE PROPERTY  crtmom  nh nh 0
TRACE PROPERTY  crtmom  s s 0
TRACE PROPERTY  crtmom  w w 0
TRACE PROPERTY  crtmom  stm stm 0
TRACE PROPERTY  crtmom  spm spm 0
TRACE PROPERTY  crtmom_2t  nv nv 0
TRACE PROPERTY  crtmom_2t  nh nh 0
TRACE PROPERTY  crtmom_2t  s s 0
TRACE PROPERTY  crtmom_2t  w w 0
TRACE PROPERTY  crtmom_2t  stm stm 0
TRACE PROPERTY  crtmom_2t  spm spm 0
TRACE PROPERTY  crtmom_mx  nv nv 0
TRACE PROPERTY  crtmom_mx  nh nh 0
TRACE PROPERTY  crtmom_mx  s s 0
TRACE PROPERTY  crtmom_mx  w w 0
TRACE PROPERTY  crtmom_mx  stm stm 0
TRACE PROPERTY  crtmom_mx  spm spm 0
TRACE PROPERTY  crtmom_mx  mf mf 0
TRACE PROPERTY  fmom  nr nr 0
TRACE PROPERTY  fmom  lr lr 0
TRACE PROPERTY  fmom  s s 0
```

```
TRACE PROPERTY  fmom  w w 0
TRACE PROPERTY  fmom  stm stm 0
TRACE PROPERTY  fmom  spm spm 0
TRACE PROPERTY  fmom_mx  nr nr 0
TRACE PROPERTY  fmom_mx  lr lr 0
TRACE PROPERTY  fmom_mx  s s 0
TRACE PROPERTY  fmom_mx  w w 0
TRACE PROPERTY  fmom_mx  stm stm 0
TRACE PROPERTY  fmom_mx  spm spm 0
TRACE PROPERTY  fmom_mx  mf mf 0
TRACE PROPERTY  lincap  lr lr 0
TRACE PROPERTY  lincap  wr wr 0
TRACE PROPERTY  lincap  mr mr 0
TRACE PROPERTY  lincap_25  lr lr 0
TRACE PROPERTY  lincap_25  wr wr 0
TRACE PROPERTY  lincap_25  mr mr 0
TRACE PROPERTY  lincap_rf  lr lr 0
TRACE PROPERTY  lincap_rf  wr wr 0
TRACE PROPERTY  lincap_rf  br br 0
TRACE PROPERTY  lincap_rf  gr gr 0
TRACE PROPERTY  lincap_rf_25  lr lr 0
TRACE PROPERTY  lincap_rf_25  wr wr 0
TRACE PROPERTY  lincap_rf_25  br br 0
TRACE PROPERTY  lincap_rf_25  gr gr 0
TRACE PROPERTY  lowcpad_d15  lt lt 0
TRACE PROPERTY  lowcpad_d15  wt wt 0
TRACE PROPERTY  lowcpad_d15  lay lay 0
TRACE PROPERTY  lowcpad_d23  lt lt 0
TRACE PROPERTY  lowcpad_d23  wt wt 0
TRACE PROPERTY  lowcpad_d23  lay lay 0
TRACE PROPERTY  mimcap_sin  lt lt 0
TRACE PROPERTY  mimcap_sin  wt wt 0
TRACE PROPERTY  mimcap_sin  mimflag mimflag 0
TRACE PROPERTY  mimcap_sin_3t  lt lt 0
TRACE PROPERTY  mimcap_sin_3t  wt wt 0
TRACE PROPERTY  mimcap_sin_3t  lay lay 0
TRACE PROPERTY  mimcap_sin_3t  mimflag mimflag 0
TRACE PROPERTY  mimcap_um_sin_rf  lt lt 0
TRACE PROPERTY  mimcap_um_sin_rf  wt wt 0
TRACE PROPERTY  mimcap_um_sin_rf  mimflag mimflag 0
TRACE PROPERTY  mimcap_woum_sin_rf  lt lt 0
TRACE PROPERTY  mimcap_woum_sin_rf  wt wt 0
TRACE PROPERTY  mimcap_woum_sin_rf  lay lay 0
TRACE PROPERTY  mimcap_woum_sin_rf  mimflag mimflag 0
TRACE PROPERTY  moscap_rf  lr lr 0
TRACE PROPERTY  moscap_rf  wr wr 0
TRACE PROPERTY  moscap_rf  br br 0
TRACE PROPERTY  moscap_rf  gr gr 0
TRACE PROPERTY  moscap_rf18  lr lr 0
TRACE PROPERTY  moscap_rf18  wr wr 0
TRACE PROPERTY  moscap_rf18  br br 0
TRACE PROPERTY  moscap_rf18  gr gr 0
TRACE PROPERTY  moscap_rf18_nw  lr lr 0
TRACE PROPERTY  moscap_rf18_nw  wr wr 0
TRACE PROPERTY  moscap_rf18_nw  br br 0
TRACE PROPERTY  moscap_rf18_nw  gr gr 0
TRACE PROPERTY  moscap_rf25  lr lr 0
TRACE PROPERTY  moscap_rf25  wr wr 0
TRACE PROPERTY  moscap_rf25  br br 0
TRACE PROPERTY  moscap_rf25  gr gr 0
TRACE PROPERTY  moscap_rf25_nw  lr lr 0
```

```
TRACE PROPERTY  moscap_rf25_nw  wr wr 0
TRACE PROPERTY  moscap_rf25_nw  br br 0
TRACE PROPERTY  moscap_rf25_nw  gr gr 0
TRACE PROPERTY  moscap_rf33  lr lr 0
TRACE PROPERTY  moscap_rf33  wr wr 0
TRACE PROPERTY  moscap_rf33  br br 0
TRACE PROPERTY  moscap_rf33  gr gr 0
TRACE PROPERTY  moscap_rf33_nw  lr lr 0
TRACE PROPERTY  moscap_rf33_nw  wr wr 0
TRACE PROPERTY  moscap_rf33_nw  br br 0
TRACE PROPERTY  moscap_rf33_nw  gr gr 0
TRACE PROPERTY  moscap_rf_hvt  lr lr 0
TRACE PROPERTY  moscap_rf_hvt  wr wr 0
TRACE PROPERTY  moscap_rf_hvt  br br 0
TRACE PROPERTY  moscap_rf_hvt  gr gr 0
TRACE PROPERTY  moscap_rf_hvt_nw  lr lr 0
TRACE PROPERTY  moscap_rf_hvt_nw  wr wr 0
TRACE PROPERTY  moscap_rf_hvt_nw  br br 0
TRACE PROPERTY  moscap_rf_hvt_nw  gr gr 0
TRACE PROPERTY  moscap_rf_nw  lr lr 0
TRACE PROPERTY  moscap_rf_nw  wr wr 0
TRACE PROPERTY  moscap_rf_nw  br br 0
TRACE PROPERTY  moscap_rf_nw  gr gr 0
TRACE PROPERTY  moscap_rf_rdk  lr lr 0
TRACE PROPERTY  moscap_rf_rdk  wr wr 0
TRACE PROPERTY  moscap_rf_rdk  br br 0
TRACE PROPERTY  moscap_rf_rdk  gr gr 0
TRACE PROPERTY  ndio_hia_rf  al al 0
TRACE PROPERTY  ndio_hia_rf  aw aw 0
TRACE PROPERTY  nmos_rf  wr wr 0
TRACE PROPERTY  nmos_rf  lr lr 0
TRACE PROPERTY  nmos_rf  nr nr 0
TRACE PROPERTY  nmos_rf_18  wr wr 0
TRACE PROPERTY  nmos_rf_18  lr lr 0
TRACE PROPERTY  nmos_rf_18  nr nr 0
TRACE PROPERTY  nmos_rf_18_6t  wr wr 0
TRACE PROPERTY  nmos_rf_18_6t  lr lr 0
TRACE PROPERTY  nmos_rf_18_6t  nr nr 0
TRACE PROPERTY  nmos_rf_18_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_18_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_18_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_25  wr wr 0
TRACE PROPERTY  nmos_rf_25  lr lr 0
TRACE PROPERTY  nmos_rf_25  nr nr 0
TRACE PROPERTY  nmos_rf_25_6t  wr wr 0
TRACE PROPERTY  nmos_rf_25_6t  lr lr 0
TRACE PROPERTY  nmos_rf_25_6t  nr nr 0
TRACE PROPERTY  nmos_rf_25_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_25_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_25_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_25_nodnwod  wr wr 0
TRACE PROPERTY  nmos_rf_25_nodnwod  lr lr 0
TRACE PROPERTY  nmos_rf_25_nodnwod  nr nr 0
TRACE PROPERTY  nmos_rf_25_nodnwud  wr wr 0
TRACE PROPERTY  nmos_rf_25_nodnwud  lr lr 0
TRACE PROPERTY  nmos_rf_25_nodnwud  nr nr 0
TRACE PROPERTY  nmos_rf_25od  wr wr 0
TRACE PROPERTY  nmos_rf_25od  lr lr 0
TRACE PROPERTY  nmos_rf_25od  nr nr 0
TRACE PROPERTY  nmos_rf_25od33_6t  wr wr 0
TRACE PROPERTY  nmos_rf_25od33_6t  lr lr 0
```

```
TRACE PROPERTY  nmos_rf_25od33_6t  nr nr 0
TRACE PROPERTY  nmos_rf_25ud  wr wr 0
TRACE PROPERTY  nmos_rf_25ud  lr lr 0
TRACE PROPERTY  nmos_rf_25ud  nr nr 0
TRACE PROPERTY  nmos_rf_25ud18_6t  wr wr 0
TRACE PROPERTY  nmos_rf_25ud18_6t  lr lr 0
TRACE PROPERTY  nmos_rf_25ud18_6t  nr nr 0
TRACE PROPERTY  nmos_rf_33  wr wr 0
TRACE PROPERTY  nmos_rf_33  lr lr 0
TRACE PROPERTY  nmos_rf_33  nr nr 0
TRACE PROPERTY  nmos_rf_33_6t  wr wr 0
TRACE PROPERTY  nmos_rf_33_6t  lr lr 0
TRACE PROPERTY  nmos_rf_33_6t  nr nr 0
TRACE PROPERTY  nmos_rf_33_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_33_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_33_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_6t  wr wr 0
TRACE PROPERTY  nmos_rf_6t  lr lr 0
TRACE PROPERTY  nmos_rf_6t  nr nr 0
TRACE PROPERTY  nmos_rf_cas_nw  wr wr 0
TRACE PROPERTY  nmos_rf_cas_nw  lr lr 0
TRACE PROPERTY  nmos_rf_cas_nw  nr nr 0
TRACE PROPERTY  nmos_rf_cas_nw  wrr wrr 0
TRACE PROPERTY  nmos_rf_cas_nw  lrr lrr 0
TRACE PROPERTY  nmos_rf_cas_nw  nrr nrr 0
TRACE PROPERTY  nmos_rf_cross_nw  wr wr 0
TRACE PROPERTY  nmos_rf_cross_nw  lr lr 0
TRACE PROPERTY  nmos_rf_cross_nw  nr nr 0
TRACE PROPERTY  nmos_rf_diff_nw  wr wr 0
TRACE PROPERTY  nmos_rf_diff_nw  lr lr 0
TRACE PROPERTY  nmos_rf_diff_nw  nr nr 0
TRACE PROPERTY  nmos_rf_hvt  wr wr 0
TRACE PROPERTY  nmos_rf_hvt  lr lr 0
TRACE PROPERTY  nmos_rf_hvt  nr nr 0
TRACE PROPERTY  nmos_rf_hvt_6t  wr wr 0
TRACE PROPERTY  nmos_rf_hvt_6t  lr lr 0
TRACE PROPERTY  nmos_rf_hvt_6t  nr nr 0
TRACE PROPERTY  nmos_rf_hvt_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_hvt_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_hvt_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_lvt  wr wr 0
TRACE PROPERTY  nmos_rf_lvt  lr lr 0
TRACE PROPERTY  nmos_rf_lvt  nr nr 0
TRACE PROPERTY  nmos_rf_lvt_6t  wr wr 0
TRACE PROPERTY  nmos_rf_lvt_6t  lr lr 0
TRACE PROPERTY  nmos_rf_lvt_6t  nr nr 0
TRACE PROPERTY  nmos_rf_lvt_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_lvt_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_lvt_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_mlvt  wr wr 0
TRACE PROPERTY  nmos_rf_mlvt  lr lr 0
TRACE PROPERTY  nmos_rf_mlvt  nr nr 0
TRACE PROPERTY  nmos_rf_mlvt_6t  wr wr 0
TRACE PROPERTY  nmos_rf_mlvt_6t  lr lr 0
TRACE PROPERTY  nmos_rf_mlvt_6t  nr nr 0
TRACE PROPERTY  nmos_rf_mlvt_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_mlvt_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_mlvt_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_na18  wr wr 0
TRACE PROPERTY  nmos_rf_na18  lr lr 0
TRACE PROPERTY  nmos_rf_na18  nr nr 0
```

```
TRACE PROPERTY  nmos_rf_nodnw  wr wr 0
TRACE PROPERTY  nmos_rf_nodnw  lr lr 0
TRACE PROPERTY  nmos_rf_nodnw  nr nr 0
TRACE PROPERTY  nmos_rf_rdk  wr wr 0
TRACE PROPERTY  nmos_rf_rdk  lr lr 0
TRACE PROPERTY  nmos_rf_rdk  nr nr 0
TRACE PROPERTY  nmoscap  wr wr 0
TRACE PROPERTY  nmoscap  lr lr 0
TRACE PROPERTY  nmoscap_18  wr wr 0
TRACE PROPERTY  nmoscap_18  lr lr 0
TRACE PROPERTY  nmoscap_25  wr wr 0
TRACE PROPERTY  nmoscap_25  lr lr 0
TRACE PROPERTY  nmoscap_33  wr wr 0
TRACE PROPERTY  nmoscap_33  lr lr 0
TRACE PROPERTY  nmoscap_lpg  wr wr 0
TRACE PROPERTY  nmoscap_lpg  lr lr 0
TRACE PROPERTY  pdio_hia_rf  al al 0
TRACE PROPERTY  pdio_hia_rf  aw aw 0
TRACE PROPERTY  pmos_rf  wr wr 0
TRACE PROPERTY  pmos_rf  lr lr 0
TRACE PROPERTY  pmos_rf  nr nr 0
TRACE PROPERTY  pmos_rf_18  wr wr 0
TRACE PROPERTY  pmos_rf_18  lr lr 0
TRACE PROPERTY  pmos_rf_18  nr nr 0
TRACE PROPERTY  pmos_rf_18_5t  wr wr 0
TRACE PROPERTY  pmos_rf_18_5t  lr lr 0
TRACE PROPERTY  pmos_rf_18_5t  nr nr 0
TRACE PROPERTY  pmos_rf_18_nw  wr wr 0
TRACE PROPERTY  pmos_rf_18_nw  lr lr 0
TRACE PROPERTY  pmos_rf_18_nw  nr nr 0
TRACE PROPERTY  pmos_rf_18_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_18_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_18_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_25  wr wr 0
TRACE PROPERTY  pmos_rf_25  lr lr 0
TRACE PROPERTY  pmos_rf_25  nr nr 0
TRACE PROPERTY  pmos_rf_25_5t  wr wr 0
TRACE PROPERTY  pmos_rf_25_5t  lr lr 0
TRACE PROPERTY  pmos_rf_25_5t  nr nr 0
TRACE PROPERTY  pmos_rf_25_nw  wr wr 0
TRACE PROPERTY  pmos_rf_25_nw  lr lr 0
TRACE PROPERTY  pmos_rf_25_nw  nr nr 0
TRACE PROPERTY  pmos_rf_25_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_25_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_25_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_25_nwod  wr wr 0
TRACE PROPERTY  pmos_rf_25_nwod  lr lr 0
TRACE PROPERTY  pmos_rf_25_nwod  nr nr 0
TRACE PROPERTY  pmos_rf_25_nwud  wr wr 0
TRACE PROPERTY  pmos_rf_25_nwud  lr lr 0
TRACE PROPERTY  pmos_rf_25_nwud  nr nr 0
TRACE PROPERTY  pmos_rf_25od  wr wr 0
TRACE PROPERTY  pmos_rf_25od  lr lr 0
TRACE PROPERTY  pmos_rf_25od  nr nr 0
TRACE PROPERTY  pmos_rf_25od33_5t  wr wr 0
TRACE PROPERTY  pmos_rf_25od33_5t  lr lr 0
TRACE PROPERTY  pmos_rf_25od33_5t  nr nr 0
TRACE PROPERTY  pmos_rf_25od33_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_25od33_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_25od33_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_25ud  wr wr 0
```

```
TRACE PROPERTY  pmos_rf_25ud  lr lr 0
TRACE PROPERTY  pmos_rf_25ud  nr nr 0
TRACE PROPERTY  pmos_rf_25ud18_5t  wr wr 0
TRACE PROPERTY  pmos_rf_25ud18_5t  lr lr 0
TRACE PROPERTY  pmos_rf_25ud18_5t  nr nr 0
TRACE PROPERTY  pmos_rf_25ud18_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_25ud18_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_25ud18_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_33  wr wr 0
TRACE PROPERTY  pmos_rf_33  lr lr 0
TRACE PROPERTY  pmos_rf_33  nr nr 0
TRACE PROPERTY  pmos_rf_33_5t  wr wr 0
TRACE PROPERTY  pmos_rf_33_5t  lr lr 0
TRACE PROPERTY  pmos_rf_33_5t  nr nr 0
TRACE PROPERTY  pmos_rf_33_nw  wr wr 0
TRACE PROPERTY  pmos_rf_33_nw  lr lr 0
TRACE PROPERTY  pmos_rf_33_nw  nr nr 0
TRACE PROPERTY  pmos_rf_33_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_33_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_33_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_5t  wr wr 0
TRACE PROPERTY  pmos_rf_5t  lr lr 0
TRACE PROPERTY  pmos_rf_5t  nr nr 0
TRACE PROPERTY  pmos_rf_hvt  wr wr 0
TRACE PROPERTY  pmos_rf_hvt  lr lr 0
TRACE PROPERTY  pmos_rf_hvt  nr nr 0
TRACE PROPERTY  pmos_rf_hvt_5t  wr wr 0
TRACE PROPERTY  pmos_rf_hvt_5t  lr lr 0
TRACE PROPERTY  pmos_rf_hvt_5t  nr nr 0
TRACE PROPERTY  pmos_rf_hvt_nw  wr wr 0
TRACE PROPERTY  pmos_rf_hvt_nw  lr lr 0
TRACE PROPERTY  pmos_rf_hvt_nw  nr nr 0
TRACE PROPERTY  pmos_rf_hvt_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_hvt_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_hvt_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_lvt  wr wr 0
TRACE PROPERTY  pmos_rf_lvt  lr lr 0
TRACE PROPERTY  pmos_rf_lvt  nr nr 0
TRACE PROPERTY  pmos_rf_lvt_5t  wr wr 0
TRACE PROPERTY  pmos_rf_lvt_5t  lr lr 0
TRACE PROPERTY  pmos_rf_lvt_5t  nr nr 0
TRACE PROPERTY  pmos_rf_lvt_nw  wr wr 0
TRACE PROPERTY  pmos_rf_lvt_nw  lr lr 0
TRACE PROPERTY  pmos_rf_lvt_nw  nr nr 0
TRACE PROPERTY  pmos_rf_lvt_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_lvt_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_lvt_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_mlvt  wr wr 0
TRACE PROPERTY  pmos_rf_mlvt  lr lr 0
TRACE PROPERTY  pmos_rf_mlvt  nr nr 0
TRACE PROPERTY  pmos_rf_mlvt_5t  wr wr 0
TRACE PROPERTY  pmos_rf_mlvt_5t  lr lr 0
TRACE PROPERTY  pmos_rf_mlvt_5t  nr nr 0
TRACE PROPERTY  pmos_rf_mlvt_nw  wr wr 0
TRACE PROPERTY  pmos_rf_mlvt_nw  lr lr 0
TRACE PROPERTY  pmos_rf_mlvt_nw  nr nr 0
TRACE PROPERTY  pmos_rf_mlvt_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_mlvt_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_mlvt_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_nw  wr wr 0
TRACE PROPERTY  pmos_rf_nw  lr lr 0
```

```
TRACE PROPERTY  pmos_rf_nw  nr nr 0
TRACE PROPERTY  pmos_rf_nw_5t  wr wr 0
TRACE PROPERTY  pmos_rf_nw_5t  lr lr 0
TRACE PROPERTY  pmos_rf_nw_5t  nr nr 0
TRACE PROPERTY  pmos_rf_rdk  wr wr 0
TRACE PROPERTY  pmos_rf_rdk  lr lr 0
TRACE PROPERTY  pmos_rf_rdk  nr nr 0
TRACE PROPERTY  pmoscap_rf  lr lr 0
TRACE PROPERTY  pmoscap_rf  wr wr 0
TRACE PROPERTY  pmoscap_rf  br br 0
TRACE PROPERTY  pmoscap_rf  gr gr 0
TRACE PROPERTY  pmoscap_rf18  lr lr 0
TRACE PROPERTY  pmoscap_rf18  wr wr 0
TRACE PROPERTY  pmoscap_rf18  br br 0
TRACE PROPERTY  pmoscap_rf18  gr gr 0
TRACE PROPERTY  pmoscap_rf25  lr lr 0
TRACE PROPERTY  pmoscap_rf25  wr wr 0
TRACE PROPERTY  pmoscap_rf25  br br 0
TRACE PROPERTY  pmoscap_rf25  gr gr 0
TRACE PROPERTY  probe1  a a 0
TRACE PROPERTY  probe1  pj pj 0
TRACE PROPERTY  probe2  a a 0
TRACE PROPERTY  probe2  pj pj 0
TRACE PROPERTY  probe3  a a 0
TRACE PROPERTY  probe3  pj pj 0
TRACE PROPERTY  probe4  a a 0
TRACE PROPERTY  probe4  pj pj 0
TRACE PROPERTY  probe5  a a 0
TRACE PROPERTY  probe5  pj pj 0
TRACE PROPERTY  probe6  a a 0
TRACE PROPERTY  probe6  pj pj 0
TRACE PROPERTY  probe7  a a 0
TRACE PROPERTY  probe7  pj pj 0
TRACE PROPERTY  rfesd_rf1  lay lay 0
TRACE PROPERTY  rfesd_rf2  lay lay 0
TRACE PROPERTY  rfesd_rf3  lay lay 0
TRACE PROPERTY  rfesd_rf4  lay lay 0
TRACE PROPERTY  rfesd_rf5  lay lay 0
TRACE PROPERTY  rfesd_rf6  lay lay 0
TRACE PROPERTY  rfesd_rf7  lay lay 0
TRACE PROPERTY  rfesd_rf8  lay lay 0
TRACE PROPERTY  rm1  w w 0
TRACE PROPERTY  rm1  l l 0
TRACE PROPERTY  rm10  w w 0
TRACE PROPERTY  rm10  l l 0
TRACE PROPERTY  rm2  w w 0
TRACE PROPERTY  rm2  l l 0
TRACE PROPERTY  rm3  w w 0
TRACE PROPERTY  rm3  l l 0
TRACE PROPERTY  rm4  w w 0
TRACE PROPERTY  rm4  l l 0
TRACE PROPERTY  rm5  w w 0
TRACE PROPERTY  rm5  l l 0
TRACE PROPERTY  rm6  w w 0
TRACE PROPERTY  rm6  l l 0
TRACE PROPERTY  rm7  w w 0
TRACE PROPERTY  rm7  l l 0
TRACE PROPERTY  rm8  w w 0
TRACE PROPERTY  rm8  l l 0
TRACE PROPERTY  rm9  w w 0
TRACE PROPERTY  rm9  l l 0
```

```
TRACE PROPERTY  rnodl  l l 0
TRACE PROPERTY  rnodl  w w 0
TRACE PROPERTY  rnodl_m  lr lr 0
TRACE PROPERTY  rnodl_m  wr wr 0
TRACE PROPERTY  rnods  l l 0
TRACE PROPERTY  rnods  w w 0
TRACE PROPERTY  rnods_m  lr lr 0
TRACE PROPERTY  rnods_m  wr wr 0
TRACE PROPERTY  rnodwo  l l 0
TRACE PROPERTY  rnodwo  w w 0
TRACE PROPERTY  rnodwo_m  lr lr 0
TRACE PROPERTY  rnodwo_m  wr wr 0
TRACE PROPERTY  rnpolyl  l l 0
TRACE PROPERTY  rnpolyl  w w 0
TRACE PROPERTY  rnpolyl_m  lr lr 0
TRACE PROPERTY  rnpolyl_m  wr wr 0
TRACE PROPERTY  rnpolys  l l 0
TRACE PROPERTY  rnpolys  w w 0
TRACE PROPERTY  rnpolys_m  lr lr 0
TRACE PROPERTY  rnpolys_m  wr wr 0
TRACE PROPERTY  rnpolywo  l l 0
TRACE PROPERTY  rnpolywo  w w 0
TRACE PROPERTY  rnpolywo_m  lr lr 0
TRACE PROPERTY  rnpolywo_m  wr wr 0
TRACE PROPERTY  rnwod  l l 0
TRACE PROPERTY  rnwod  w w 0
TRACE PROPERTY  rnwod_m  lr lr 0
TRACE PROPERTY  rnwod_m  wr wr 0
TRACE PROPERTY  rnwsti  l l 0
TRACE PROPERTY  rnwsti  w w 0
TRACE PROPERTY  rnwsti_m  lr lr 0
TRACE PROPERTY  rnwsti_m  wr wr 0
TRACE PROPERTY  rpodl  l l 0
TRACE PROPERTY  rpodl  w w 0
TRACE PROPERTY  rpodl_m  lr lr 0
TRACE PROPERTY  rpodl_m  wr wr 0
TRACE PROPERTY  rpods  l l 0
TRACE PROPERTY  rpods  w w 0
TRACE PROPERTY  rpods_m  lr lr 0
TRACE PROPERTY  rpods_m  wr wr 0
TRACE PROPERTY  rpodwo  l l 0
TRACE PROPERTY  rpodwo  w w 0
TRACE PROPERTY  rpodwo_m  lr lr 0
TRACE PROPERTY  rpodwo_m  wr wr 0
TRACE PROPERTY  rppolyl  l l 0
TRACE PROPERTY  rppolyl  w w 0
TRACE PROPERTY  rppolyl_m  lr lr 0
TRACE PROPERTY  rppolyl_m  wr wr 0
TRACE PROPERTY  rppolyl_rf  w w 0
TRACE PROPERTY  rppolyl_rf  l l 0
TRACE PROPERTY  rppolyl_rf_rdk  w w 0
TRACE PROPERTY  rppolyl_rf_rdk  l l 0
TRACE PROPERTY  rppolys  l l 0
TRACE PROPERTY  rppolys  w w 0
TRACE PROPERTY  rppolys_m  lr lr 0
TRACE PROPERTY  rppolys_m  wr wr 0
TRACE PROPERTY  rppolys_rf  w w 0
TRACE PROPERTY  rppolys_rf  l l 0
TRACE PROPERTY  rppolys_rf_rdk  w w 0
TRACE PROPERTY  rppolys_rf_rdk  l l 0
TRACE PROPERTY  rppolywo  l l 0
```

```
TRACE PROPERTY  rppolywo  w w 0
TRACE PROPERTY  rppolywo_m  lr lr 0
TRACE PROPERTY  rppolywo_m  wr wr 0
TRACE PROPERTY  rppolywo_rf  w w 0
TRACE PROPERTY  rppolywo_rf  l l 0
TRACE PROPERTY  rppolywo_rf_rdk  w w 0
TRACE PROPERTY  rppolywo_rf_rdk  l l 0
TRACE PROPERTY  sbd_rf  nf nf 0
TRACE PROPERTY  sbd_rf  w w 0
TRACE PROPERTY  sbd_rf  l l 0
TRACE PROPERTY  sbd_rf_nw  nf nf 0
TRACE PROPERTY  sbd_rf_nw  w w 0
TRACE PROPERTY  sbd_rf_nw  l l 0
TRACE PROPERTY  sline_gscpw_mu  l l 0
TRACE PROPERTY  sline_gscpw_mu  s s 0
TRACE PROPERTY  sline_gscpw_mu  w w 0
TRACE PROPERTY  sline_gscpw_mu  lay lay 0
TRACE PROPERTY  sline_ms_mu  l l 0
TRACE PROPERTY  sline_ms_mu  w w 0
TRACE PROPERTY  sline_ms_mu  lay lay 0
TRACE PROPERTY  spiral_std_mu_z  lay lay 0
TRACE PROPERTY  spiral_std_mu_z  w w 0.05
TRACE PROPERTY  spiral_std_mu_z  nr nr 0
TRACE PROPERTY  spiral_std_mu_z  rad rad 0
TRACE PROPERTY  spiral_std_mu_z  gdis gdis 0
TRACE PROPERTY  spiral_std_mu_z  spacing spacing 0
TRACE PROPERTY  spiral_std_mu_z_rdk  lay lay 0
TRACE PROPERTY  spiral_std_mu_z_rdk  w w 0.05
TRACE PROPERTY  spiral_std_mu_z_rdk  nr nr 0
TRACE PROPERTY  spiral_std_mu_z_rdk  rad rad 0
TRACE PROPERTY  spiral_std_mu_z_rdk  gdis gdis 0
TRACE PROPERTY  spiral_std_mu_z_rdk  spacing spacing 0
TRACE PROPERTY  spiral_sym_ct_mu_z  lay lay 0
TRACE PROPERTY  spiral_sym_ct_mu_z  w w 0.05
TRACE PROPERTY  spiral_sym_ct_mu_z  nr nr 0
TRACE PROPERTY  spiral_sym_ct_mu_z  rad rad 0
TRACE PROPERTY  spiral_sym_ct_mu_z  gdis gdis 0
TRACE PROPERTY  spiral_sym_ct_mu_z  spacing spacing 0
TRACE PROPERTY  spiral_sym_ct_mu_z_rdk  lay lay 0
TRACE PROPERTY  spiral_sym_ct_mu_z_rdk  w w 0.05
TRACE PROPERTY  spiral_sym_ct_mu_z_rdk  nr nr 0
TRACE PROPERTY  spiral_sym_ct_mu_z_rdk  rad rad 0
TRACE PROPERTY  spiral_sym_ct_mu_z_rdk  gdis gdis 0
TRACE PROPERTY  spiral_sym_ct_mu_z_rdk  spacing spacing 0
TRACE PROPERTY  spiral_sym_mu_z  lay lay 0
TRACE PROPERTY  spiral_sym_mu_z  w w 0.05
TRACE PROPERTY  spiral_sym_mu_z  nr nr 0
TRACE PROPERTY  spiral_sym_mu_z  rad rad 0
TRACE PROPERTY  spiral_sym_mu_z  gdis gdis 0
TRACE PROPERTY  spiral_sym_mu_z  spacing spacing 0
TRACE PROPERTY  spiral_sym_mu_z_rdk  lay lay 0
TRACE PROPERTY  spiral_sym_mu_z_rdk  w w 0.05
TRACE PROPERTY  spiral_sym_mu_z_rdk  nr nr 0
TRACE PROPERTY  spiral_sym_mu_z_rdk  rad rad 0
TRACE PROPERTY  spiral_sym_mu_z_rdk  gdis gdis 0
TRACE PROPERTY  spiral_sym_mu_z_rdk  spacing spacing 0
TRACE PROPERTY  xjvar  w w 0
TRACE PROPERTY  xjvar  l l 0
TRACE PROPERTY  xjvar  nr nr 0
TRACE PROPERTY  xjvar_nw  w w 0
TRACE PROPERTY  xjvar_nw  l l 0
```

```
   TRACE PROPERTY  xjvar_nw  nr nr 0


                  CELL COMPARISON RESULTS ( TOP LEVEL )


                       #       ###################       _   _
                     #         #                 #       *   *
                   #   #       #     CORRECT     #         |
                    # #        #                 #       \___/
                     #         ###################


LAYOUT CELL NAME:         Neuron
SOURCE CELL NAME:         Neuron

-------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

               Layout    Source         Component Type
               ------    ------         --------------
 Ports:             9         9

 Nets:             23        23

 Instances:        90         9    *    MN (4 pins)
                  135        15    *    MP (4 pins)
                    3         3         rnodwo (2 pins)
                    3         3         crtmom (3 pins)
               ------    ------
 Total Inst:      231        30


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

               Layout    Source         Component Type
               ------    ------         --------------
 Ports:             9         9

 Nets:             23        23

 Instances:         9         9         MN (4 pins)
                   15        15         MP (4 pins)
                    3         3         rnodwo (2 pins)
                    3         3         crtmom (3 pins)
               ------    ------
 Total Inst:       30        30


       * = Number of objects in layout different from number in source.


*************************************************************************************************************
                               INFORMATION AND WARNINGS
```

```
*****************************************************************************************************

                Matched     Matched     Unmatched     Unmatched     Component
                 Layout      Source        Layout        Source     Type
                -------     -------     ---------     ---------     ---------
   Ports:             9           9             0             0

   Nets:             23          23             0             0

   Instances:         9           9             0             0     MN(NCH)
                     15          15             0             0     MP(PCH)
                      3           3             0             0     rnodwo
                      3           3             0             0     crtmom
                -------     -------     ---------     ---------
   Total Inst:       30          30             0             0


o Statistics:

   225 layout mos transistors were reduced to 24.
     201 mos transistors were deleted by parallel reduction.


o Initial Correspondence Points:

   Ports:        VDD GND CRT VIN- VIN+ VREF CRT1 CRT2 VOUT


*****************************************************************************************************
                                        SUMMARY
*****************************************************************************************************

Total CPU Time:      0 sec
Total Elapsed Time:  1 sec
```