RAK439 SPI WiFi Module

Specification V1.0

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Content

1. Overview of the module

The RAK439 module is an ultra-low-power and low-cost Wi-Fi® module that fully supports mainstream encryption modes and the WAPI encryption mode, and supports the SPI of 802.11b/g/n. The interior of the module integrates a radio frequency base station, a balun, a radio frequency switch, a crystal oscillator and a power conversion circuit. The hardware design can be completed with only a few of peripheral circuits. An IPEX external antenna pedestal is arranged in the module, and antenna pins are led out from the module, so the design of an on-board antenna can be realized.

The RAK439module provides a mature master control drive API library, BSD-like socket operation and a platform initialized function library, so customers can easily integrate the modules to their own master control platform, which significantly shortens the evaluation period. The driver library also supports the operation ways of NOS and OS, so it is flexible to use.

2. Functional characteristics

2.1 Hardware interface

- Four-wire SPI interface, with the interface rate supporting 24Mbps at most
- The throughput of the module is up to 6Mbps

2.2 WiFi characteristics

- Meet the IEEE 802.11b/g/n criteria, support 802.11n uniflow, and provide high throughput rate
- Support the basic network mode (Station mode) and the routing mode (SoftAP)
- Support WPA/WPA2-PSK TKIP/AES, WAPI-PSK encryption mode.
- Support one-key network configuration, the WPS pattern, EasyConfig
- Support PMK quickly joining the network (time<1s)
- Support the 802.11 PS mode and the low power consumption mode

2.3 TCP/IP characteristics

- Support the TCP server and the TCP client side, and the UDP server and the UDP client side.
- Support 8 sockets at most, and support blocking and non-blocking operations
- Support the DHCP server and the DHCP client side
- Support the DNS client side

2.4 Other characteristics

- Provide driver libraries of various platforms, and the amount of resources occupied by these libraries Flash<40KB Ram<10KB.
- Power supply: 3.1~3.5V
- Operating temperature: -40~+85℃
- Moisture sensitivity level (MSL): 3
- Dimensions: 16.08mm x 14.08mm x 2.2mm

2.5 Application fields

- Medical equipment
- Industrial handsets
- Industrial automation and measurement
- WiFi cameras
- Toys and other Internet-based consumer electronics products

2.6 System block diagram

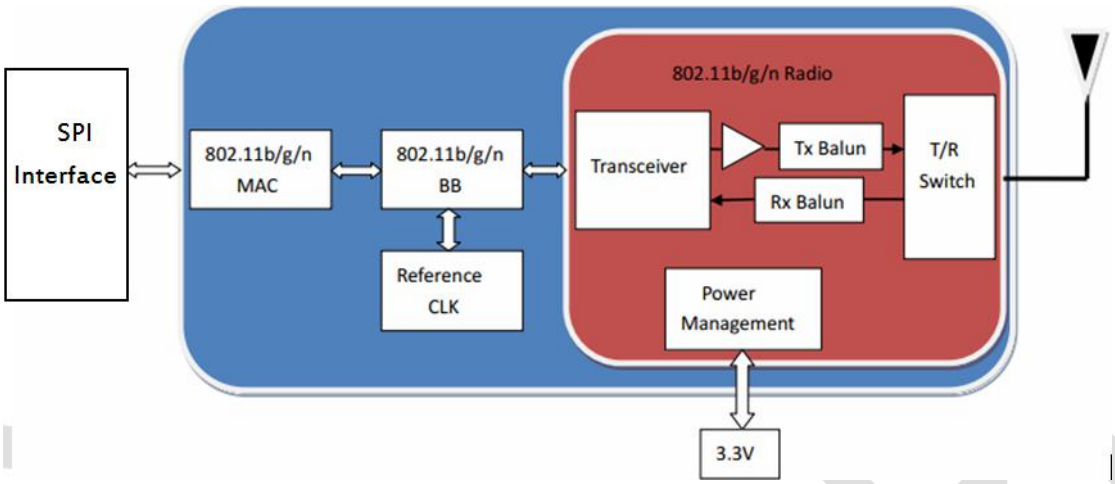

Figure 2-1 Block diagram of the module system

3 Hardware

3.1 Module view

The following figure shows the front view and the rear view of the module.

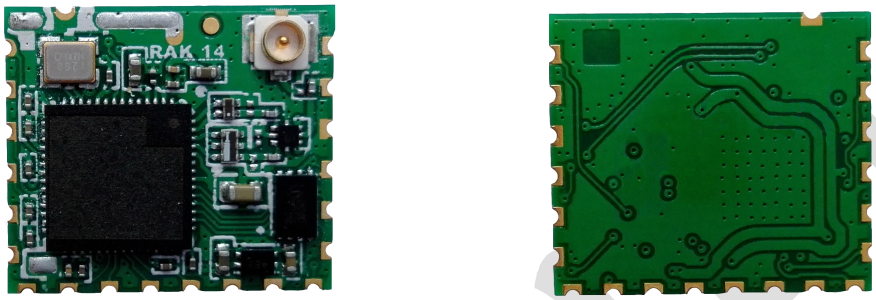

Figure 3-1 Module view

3.2 Definition of PIN

Table 3-1 Definition of PIN of the module

No.	Name	Type	Description
5	CHIP_PWD_L	I, PU	Reset pin of the module
6	GSPI_MOSI	I	SPI MOSI pin of the module
7	GSPI_CS	I	SPI CS (chip select) pin of the module
9	GSPI_INT	O	SPI INT interrupt output pin of the module
10	GSPI_MISO	O	SPI MISO pin of the module
11	GSPI_CLK	I	SPI CLK clock input pin of the module
12	1.8V	O	1.8V power output of the module
13	VDD3V3	P	3.3V power input of the module
19	RF_OUT	O	RF output pin, capable of being designed to be connected with the on-board antenna
20	MODE	I	Sets the chip working mode, and the SPI mode must be pulled down
18,21	GND	GND	GND
1,2,3,4,8，14,15,16,17	NC		NC

Remarks:

1. Indications of letters of pin types in Table 3-1: P: power. GND: ground; I: input; O: output; PU: pull upwards.

2. Pin 19 is the RF output pin which can be connected with the on-board antenna as per design. Please hang Pin 19 in the air when not using it.
3. NC pins are hung in the air.

3.3 PCB packaging diagram

The following figure 3-2 shows the recommended PCB packaging dimensions.

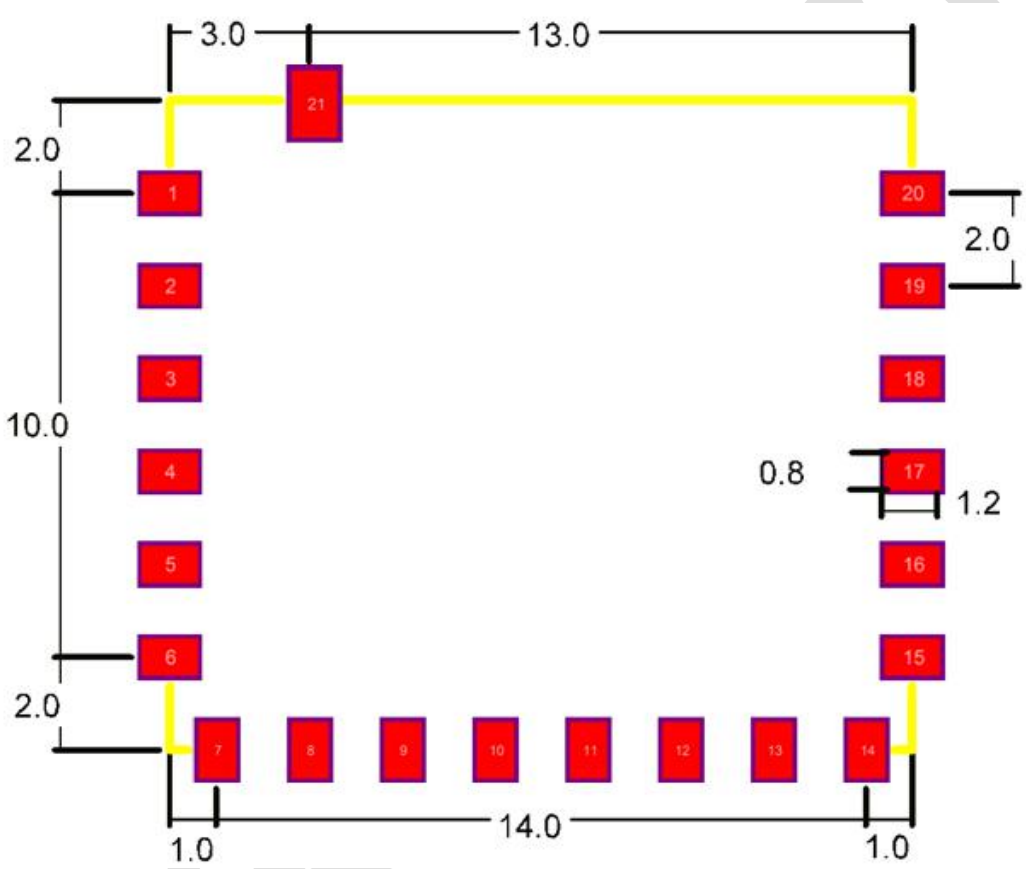

Figure 3-2 recommended PCB packaging

3.4 Typical circuit

Figure 3-3 shows the design for the typical circuit of the module. The design should pay attention to the precautions:

1. The power design of the WIFI module is important. The power should support the WIFI module to continuously receive and transmit current peak of 350ma at high WIFI rate and high RF output, and this value should be reserved with appropriate safety margin, which is generally recommended at 400-500ma.

2. Signal integrity of SPI communication lines should be considered, as distortion of the SPI Clock may lead to desynchrony in SPI communication and subsequent communication failure. Thus, the

following three elements need to be considered. Firstly, SPI lines should be equal at length. Secondly, if the module and the host are connected in a wired way, the number of ground wires should be increased as much as possible, but the length should be prevented from being too long. Thirdly, if the SPI clock line is connected with a resistor in series, the default value of the resistor is 33 Ω .

3. The reset line of the module should be connected with the IO port of the host, so the module can realize hardware reset from abnormality.

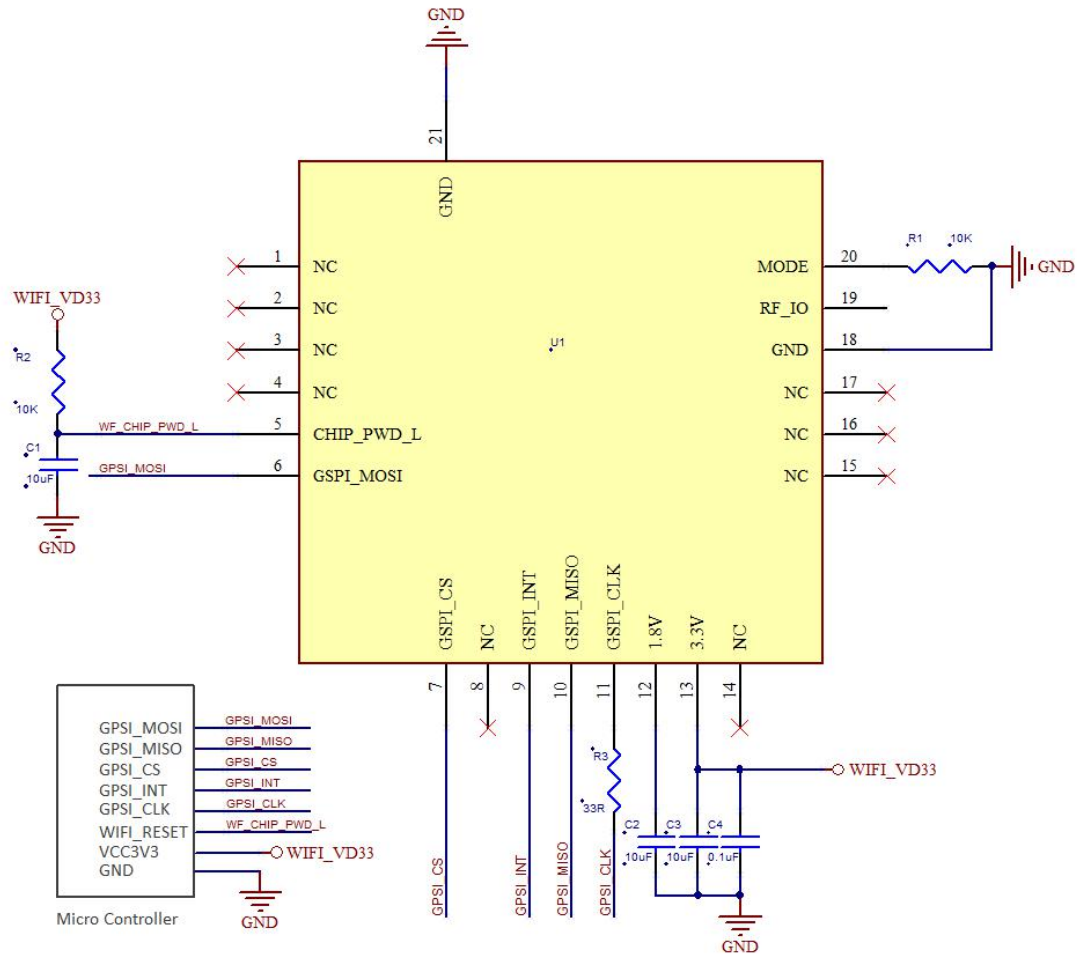

Figure 3-3 Design of typical circuit

4 Electrical characteristics

4.1 Absolute maximum

Table 4-1 lists the absolute maximum, and Table 4-2 lists the working conditions that RAK439 module recommends. The absolute maximum is a value, exceeding which any operation would cause damage to the devices, so it is not recommended to perform any operation above this maximum value or other values indicated in this document.

Table 4-1 Absolute maximum

Symbol	Parameter	Maximum change	Unit
VDD3V3	External 3.3V power	-0.3~4.0	V
3.3V IO VIH Max	Maximum input voltage of IO port during 3.3V IO power supply	VDD+0.3	V
VIH Min	Minimum input voltage of IO port during 3.3V IO power supply	-0.3	V
RFin	Maximum radio frequency input (based on 50Ω input)	+10	dBm
Tstore	Storage temperature	-45~+135	℃
ESD	Electrostatic discharge	2000	V

4.2 Recommended operating conditions

Table 4-2 Recommended operating conditions

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
VDD3V3	External 3.3V power	3.1	3.3	3.5	V
$T_{ambient}$	Environment temperature	-40		85	℃

4.3 DC electrical characteristics

Table 4-3 lists the general DC electrical characteristics under the recommended operating conditions (special instructions excluded).

Table 4-3 General DC electrical characteristics (3.3V I/O operation)

Symbol	Parameter		Condition	Minimum value	Typical value	Maximum value	Unit
V_{IH}	High-level input voltage			0.7xVDD			V
V_{IL}	Low-level input voltage					0.3xVDD	V
I_{IL}	Input leakage	No pull-up or pull-down	$0<V_{IN}<V_{DD}$ $0<V_{OUT}<V_{DD}$	0		-3	nA

	current	resistance					
		Pull up	$0<V_{IN}<V_{DD}$ $0<V_{OUT}<V_{DD}$	16		48	μA
		Pull down	$0<V_{IN}<V_{DD}$ $0<V_{OUT}<V_{DD}$	-14		-47	μA
V_{OH}	High-level output voltage		I_{OH}=-4mA	0.9xVDD			V
			I_{OH}=-12mA	0.9xVDD			V
V_{OL}	Low-level output voltage		I_{OH}=4mA			0.1xVDD	V
			I_{OH}=12mA			0.1xVDD	V

4.4 RF parameters

Table 4-4 lists the RF transmitting characteristics, and Table 4-5 lists the electrical characteristics of RF receiving sensitivity.

Table 4-4 RF transmitting characteristics

Symbol	Parameter	Condition	Typical value	Unit
F_{tx}	Carrier frequency range		2.4	GHz
P_{out}	Output power			
	802.11b	1Mbps	17	dBm
	802.11g	6Mbps	17	
	802.11n,HT20	MCS0	17	
	802.11g EVM	54Mbps	14	
	802.11n,HT20 EVM	MCS7	10	
A_{pl}	Accuracy of power balance loop		±1.5	dB

Table 4-5 RF receiving characteristics

Parameter		Test Conditions	Typical value	Unit
Receiving sensitivity	11b, 1Mbps		-97	dBm
	11b, 2 Mbps		-92	dBm
	11b, 5.5 Mbps		-90	dBm
	11b, 11 Mbps		-88	dBm
	11g, 9Mbps		-91	dBm
	11g, 18Mbps		-87	dBm

	11g, 36Mbps		-81	dBm
	11g, 54Mbps		-75	dBm
	11n, MCS1, 13Mbps		-89	dBm
	11n, MCS3, 26Mbps		-82	dBm
	11n, MCS5, 52Mbps		-75	dBm
	11n, MCS7, 65Mbps		-72	dBm
Maximum input signal	CH7	11g, 54Mbps	10	dBm
Adjacent channel rejection	6Mbps		37	dBc
	54Mbps		21	dBc
	MCS0		38	dBc
	MCS7		20	dBc

4.5 SPI interface timing

Figure 4-1 shows the 8bit mode of the SPI, and the SPI of the host needs to select the same polarity and phase as same as the SPI clock of the slave (module). As shown in the diagram, the SPI clock idle level is high, and the polarity is 1; data are received at the rising edge of the SPI clock (SPI_MOSI), and are sent at the falling edge of the SPI clock (SPI_MISO).

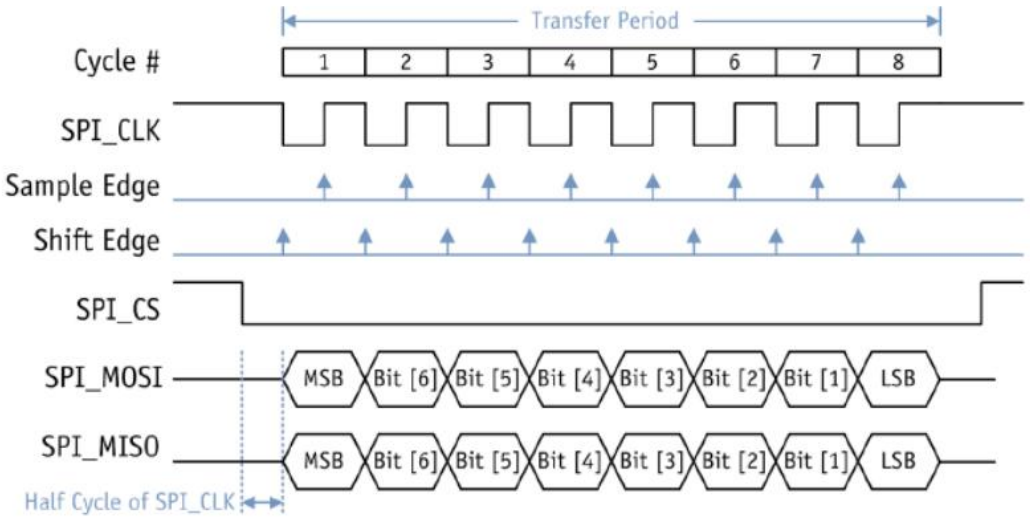

Figure 4-1 Operation timing sequence of SPI 8bit mode

4.6 Power on and reset timing sequence

Figure 4-2 is the power on and power off timing sequence diagram of the module; Figure 4-3 is

the reset timing sequence diagram; and Table 4-2 shows the value scope of the reset timing sequence parameters.

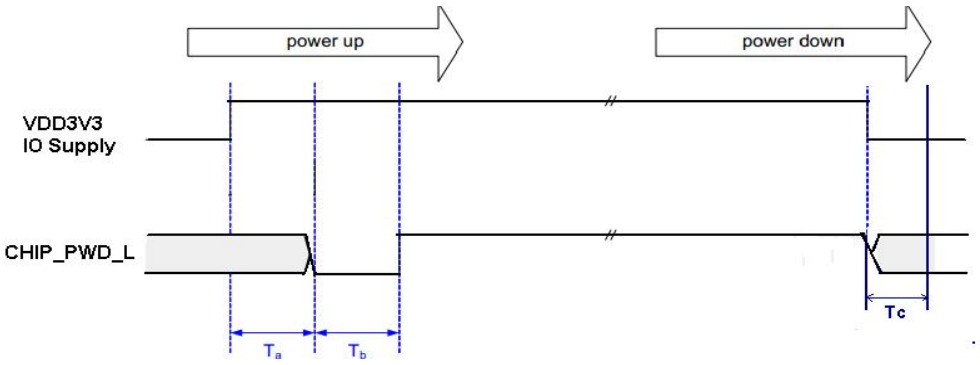

Figure 4-2 Power on/off timing sequence diagram

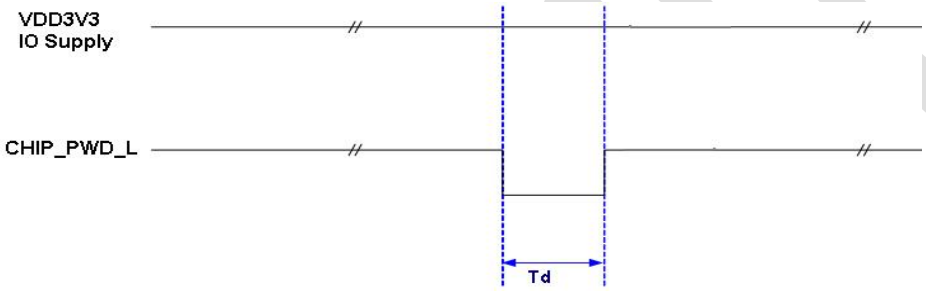

Figure 4-3 Reset timing sequence diagram

Table 4-2 Parameters of reset timing sequence diagram

Symbol	Description	Minimum value（μS）
Ta	Duration from VDD3V3 power on to taking effect of IO power supply	5
Tb	Duration from taking effect of VDD3V3 to reset completion	100
Tc	Duration from VDD3V3 outage to taking effect of reset	NA
Td	Reset pulse length	1000

5 Antenna design

5.1 External antenna

If the external antenna module has the IPEX antenna pedestal, the design will be simple.

5.2 On-board antenna

If the antenna leading-out module is selected, design for the on-board antenna will be needed. During design, it should be noted that a 50Ωresistor is needed between the leading-out pin and the antenna part. Besides, a clearance area should be reserved in the antenna part (referring to the specific design manual of antenna). The module should be put at four corners of the board as much as possible.

6 Power consumption management

Power consumption modes of the module are divided as follows:

Table 6-1 Power save mode

Working mode	Operating status	Power consumption
Power save mode	OFF	0.004mA
	Power Save	3mA
Continuous reception (max)	54Mbps(OFDM)	86mA
Continuous Transmission (max)	54Mbps(OFDM)	210mA

OFF state: this state is entered directly by pulling down the CHIP_PWD_L pin; sleep clock is disabled in this state, and no state is retained;

Power Save state: only the sleep clock works, the oscillator and crystal are disabled, any waking event will compulsively make transmission from this state to WAKE-UP state. It is mainly used for conducting DTIM together with the routers. The low-power-consumption mode is kept as waking at intervals is adopted.

7 Production guidance

Figure 7-1 shows the recommended reflow curve of production in the reflow soldering way.

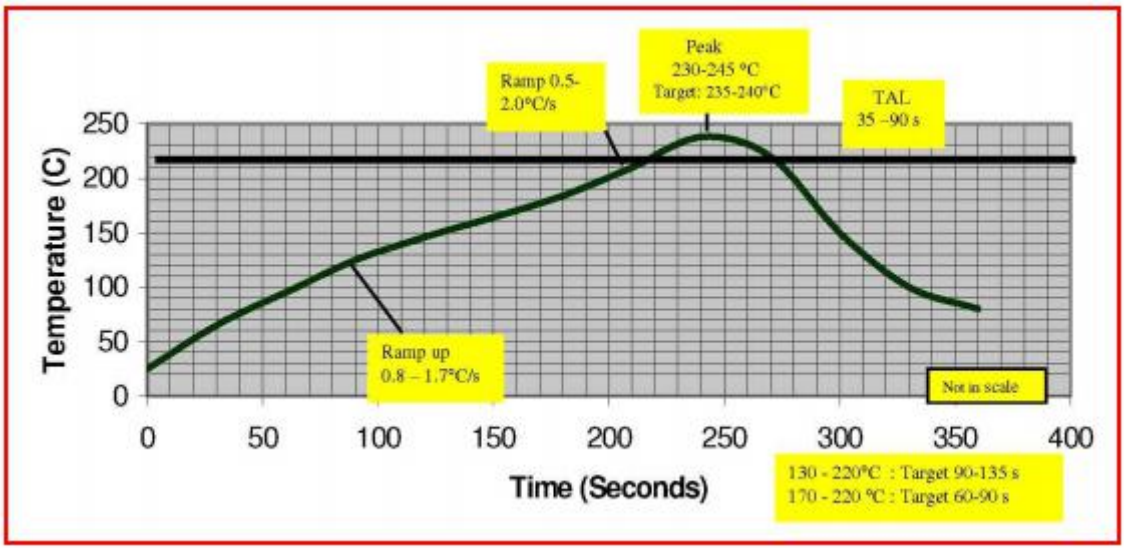

Figure 7-1 Recommended reflow soldering curve

Notes:

As shown in the above figure, it is based on the SAC305 lead-free tin paste (3% silver and 0.5% copper). Alpha OM-338 lead-free cleaning-free flux is recommended. This curve of the above figure is mainly used for guidance. The duration of the entire reflow process is subject to the number of thermal pads of the assembly board and the device intensity.

8 Order information

8.1 Product lines

Table 9-1 Product information

Products	Description	Single pallet package	Minimum package
RAK439BS-XXXX	External antenna	70pcs/tray	700pcs
RAK439CS-XXXX	RF-OUT	70pcs/tray	700pcs

8.2 Other information

Weight: 0.74g/pcs

Package: Pallet package, lead-free package

Version

Version	Author	Date	Content modification
V1.0		2015/03/20	Released