All the codes and results in this document are available in the Github repository.

While

Initial code:

```
export fn add1(reg u64 arg) -> reg u64
   {
      reg u64 z;
      reg bool temp;
      z = 0;
      temp = arg > 0;
      while(temp){
          z += 1;
          arg -= 1;
          temp = arg > 0;
      }
11
      return z;
12
  }
13
```

After adding #init_msf and #update_msf:

```
export
  fn add1 (reg u64 arg) -> (reg u64) {
    reg u64 msf;
    reg u64 z;
    reg bool temp;
    msf = #init_msf();
    z = 0;
    temp = arg > 0;
9
    while (temp) {
10
      msf = #update_msf(temp, msf);
      z = z + 1;
      arg = arg - 1;
13
      temp = arg > 0;
14
15
    msf = #update_msf((! temp), msf);
16
    return (z);
```

The generated assembly code:

```
.att_syntax
.text
```

```
.p2align 5
      .globl _add1
      .globl add1
   _add1:
  add1:
     movq $0, %rax
      cmpq $0, %rdi
9
      jmp
           Ladd1$1
  Ladd1$2:
11
     incq %rax
12
     addq $-1, %rdi
13
      cmpq $0, %rdi
14
  Ladd1$1:
      jnbe Ladd1$2
16
     ret
17
```

If

Input code:

```
fn double_64(reg u64 inp) -> reg u64
   {
2
       reg u64 dupl;
       dupl = 2 * inp;
       return dupl;
5
   }
6
   export fn add1(reg u64 arg) -> reg u64
9
       reg u64 z;
       reg bool temp;
11
       temp = arg > 0;
       if temp{
           z = double_64(arg);
       }
15
       else{
16
           z = double_64(arg);
17
           z = z + 1;
       }
19
       return z;
20
   }
21
```

after slh update msf:

```
fn double_64 (reg u64 msf.102, reg u64 inp.174) -> (reg u64, reg u64) {
reg u64 dupl.175;
```

```
3
     dupl.175 = (((64u) 2) *64u inp.174); /* u64 */
     return (msf.102, dupl.175);
   }
   export
   fn add1 (reg u64 arg.171) -> (reg u64) {
9
     reg u64 msf.102;
     reg u64 z.172;
     reg bool temp.173;
12
13
     msf.102 = \#init_msf();
14
     temp.173 = (arg.171 > u ((64u) 0));
     if temp.173 {
16
      msf.102 = #update_msf(temp.173, msf.102);
17
       (msf.102, z.172) = double_64(msf.102, arg.171);
18
     } else {
19
      msf.102 = #update_msf((! temp.173), msf.102);
20
       (msf.102, z.172) = double_64(msf.102, arg.171);
      z.172 = (z.172 +64u ((64u) 1));
     }
     return (z.172);
24
   }
25
   generated assembly code:
      .att_syntax
      .text
      .p2align 5
      .globl
             _add1
      .globl
              add1
   _add1:
   add1:
      movq %rsp, %rsi
      andq $-8, %rsp
9
      lfence
      movq $0, %rax
      cmpq $0, %rdi
12
      jnbe Ladd1$1
13
     movq $-1, %rcx
      cmovnbe %rcx, %rax
15
      call Ldouble_64$1
16
   Ladd1$4:
17
      incq %rax
18
           Ladd1$2
      jmp
19
   Ladd1$1:
     movq $-1, %rcx
```

```
22 cmovbe %rcx, %rax

23 call Ldouble_64$1

24 Ladd1$3:

25 Ladd1$2:

26 movq %rsi, %rsp

27 ret

28 Ldouble_64$1:

29 imulq $2, %rdi, %rax

30 ret
```

Function call inside while

```
initial code:
   fn double_64(reg u64 inp) -> reg u64
   {
       reg u64 dupl;
       dupl = 2 * inp;
       return dupl;
   export fn add1(reg u64 arg) -> reg u64
   {
       reg u64 z;
9
       reg bool temp;
       z = 0;
11
       temp = arg > 0;
       while(temp){
          z += 1;
14
          z = double_64(z);
          arg -= 1;
16
          temp = arg > 0;
       }
18
       return z;
19
   }
20
   after slh_gen:
   fn double_64 (reg u64 inp) -> (reg u64) {
     reg u64 dupl;
     dupl = (((64u) 2) *64u inp); /* u64 */
     return (dupl);
   }
6
   export
   fn add1 (reg u64 arg) -> (reg u64) {
```

```
reg u64 z;
10
     reg bool temp;
11
12
     z = ((64u) \ 0); /* u64 */
13
     temp = (arg >u ((64u) 0)); /* bool */
14
     while (temp) {
15
       z = (z +64u ((64u) 1)); /* u64 */
16
       z = double_64(z);
17
       arg = (arg -64u ((64u) 1)); /* u64 */
18
       temp = (arg >u ((64u) 0)); /* bool */
19
     }
20
     return (z);
21
22
  }
```