Politenico di Milano

Dipartimento Elettronica, Informazione e Bioingegneria

HEAPLab Project Report

Signals Timing

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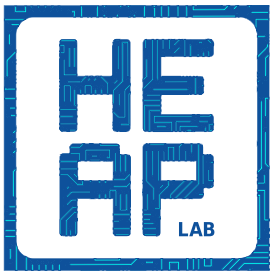
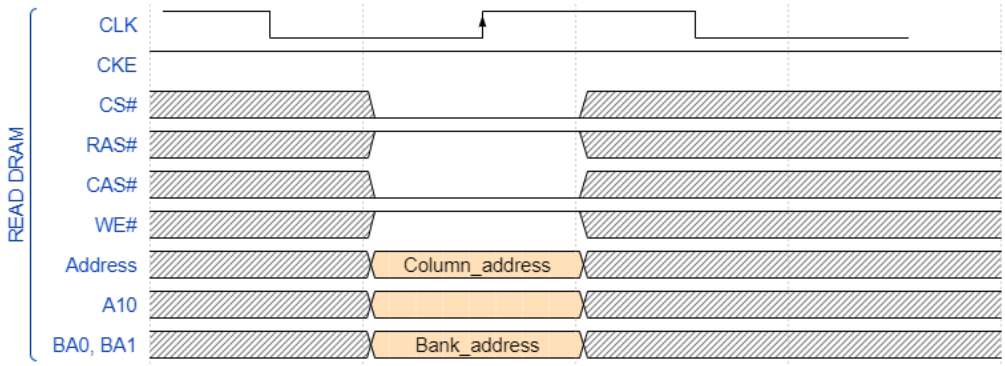
January 2, 2021

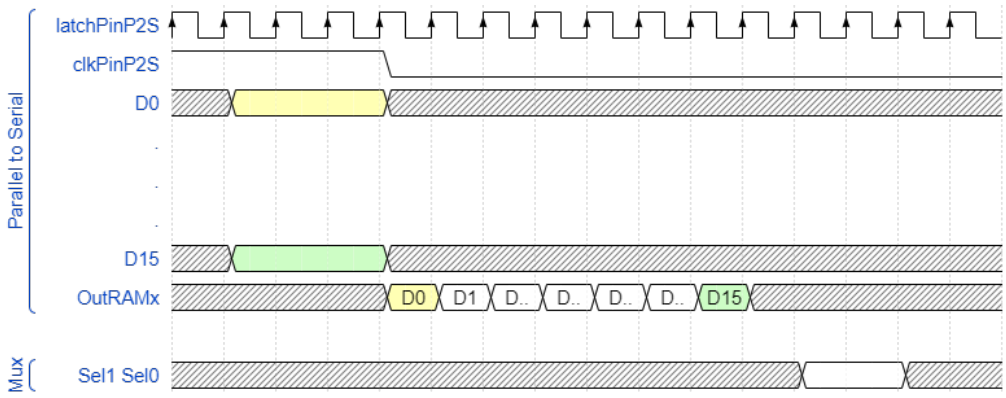


1 READ

1.1 DRAM

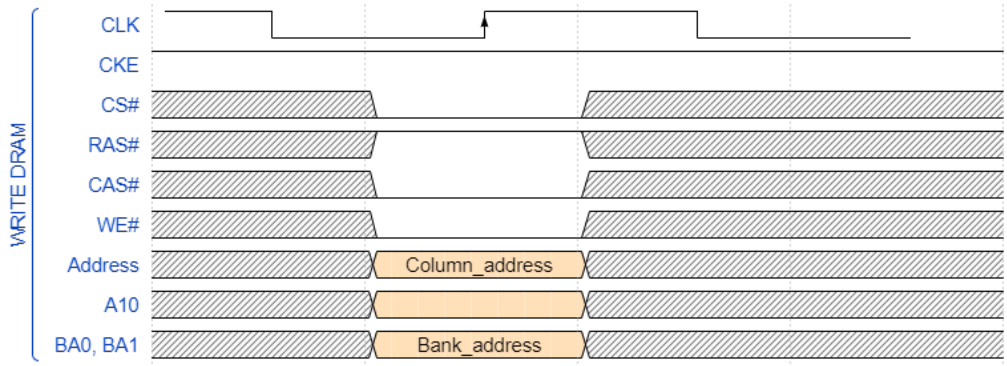


1.2 Shift Register Parallel to Serial



2 WRITE

2.1 DRAM



2.2 Shift RegisterSerial to Parallel