Politecnico di Torino

III Facoltà di Ingegneria

Implementation and optimization of FIR filter Integrated Systems Architecture

Master degree in Electrical Engineering

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November 20, 2021

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CHAPTER 1

Contents

The aim of this laboratory is to design a FIR filter with a cut-off frequency of 2Khz and a sampling frequency of 10 Khz. As first step, we described it using Matlab model with 2 sinusoidal signals at different frequencies. Then , we compare the results obtained with a fixed-point model described using C code. After that, we consider the THD of the C model with a constraint of not higher than -30db.

1.1 Filter design using Matlab

1.2 Fixed point C model

1.3 THD evaluation and final considerations

1.4 BASIC FIR VHDL

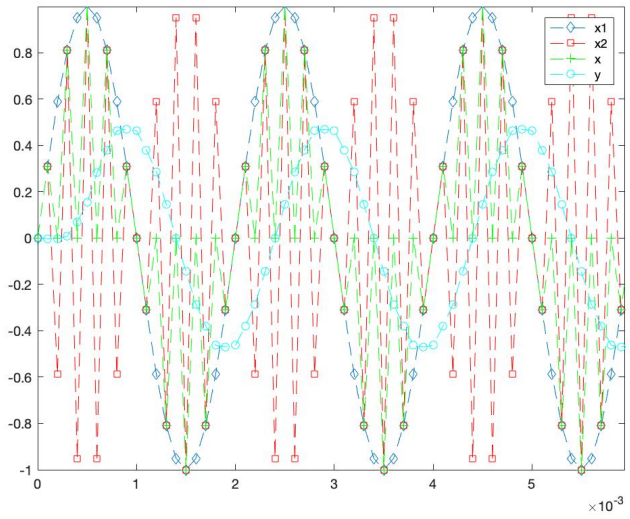
CHAPTER 2

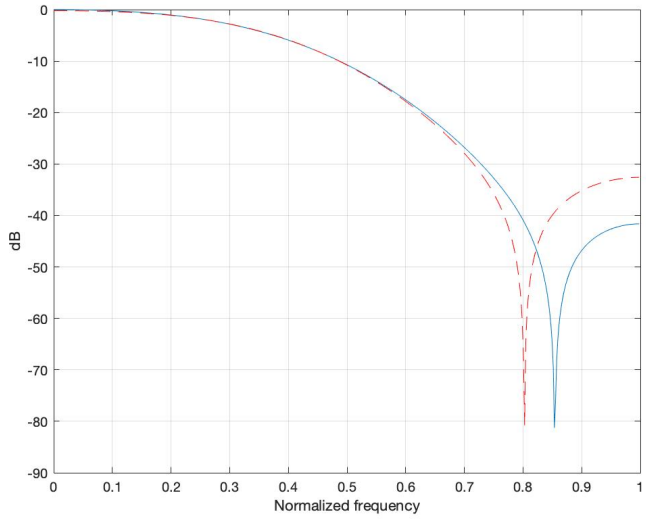
Reference model development

The aim of this laboratory is to design a FIR filter with a cut-off frequency of 2Khz and a sampling frequency of 10 Khz. As first step, we described it using Matlab model with 2 sinusoidal signals at different frequencies. Then , we compare the results obtained with a fixed-point model described using C code. After that, we consider the THD of the C model with a constraint of not higher than -30db.

2.1 1.1 Filter FIR using Matlab

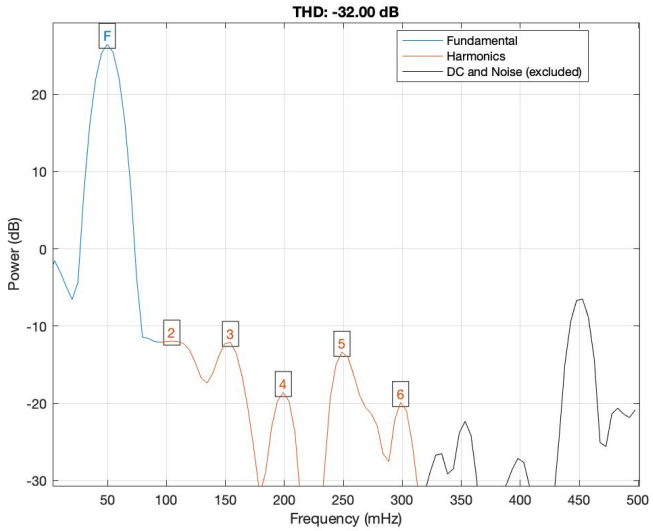
The first step was to compute then number of bits and the order, in our case we got number of bits equals to 8 and even for the order(initially our group was composed by 3 people but one dropped and kept worked as a 3 members group for the computation of the parameters). Using the file myfirdesign.m ,present in the Portale , we set the obtained parameters with the desired cut-off and sampling frequency . In this way we obtained the transfer function and the quantized function and we also get the coefficients to be used in the C model and by the myfilter.m.





Now using the 2 sinusoidal signals with the coefficients got previously , we can now behave correctly our filter FIR.

Then we save our results in an output file that will be compared later with the C model results.



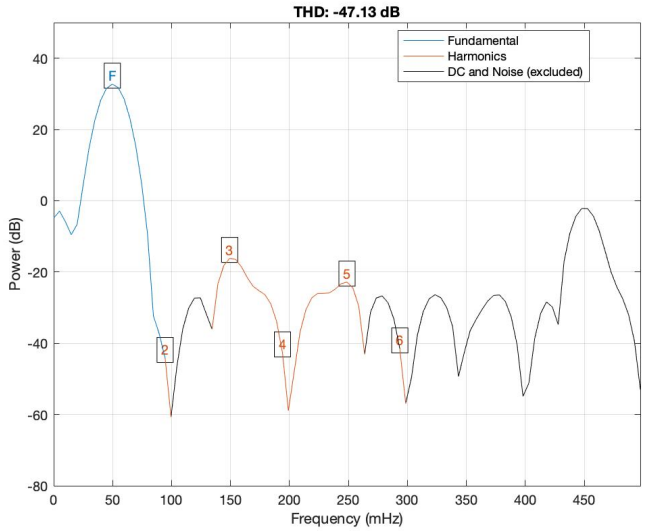
2.2 1.2 Fixed Model C model

In this section we will comment how the C model filter has been considered. All the parameters come from the matlab output. We implemented it by using the direct form using the formula present in the description of the laboratory file

The program , after reading the file samples.txt and set all the parameters, uses a 8bit-shift register after the multiplication among the variable and the related coefficient, and then calculate the results and save them in the output.txt file

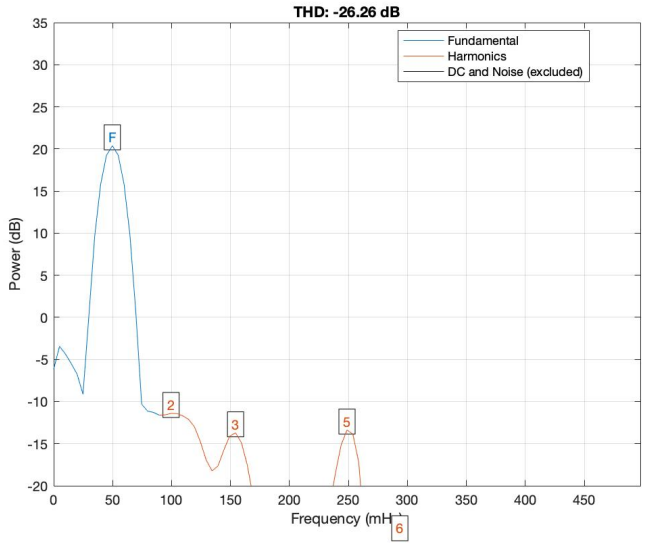
2.3 1.3 THD evaluation and final considerations

After running the C code and getting the output file , we go back to the Matlab because we evaluate the THD of our C model.



As you can see it has a value smaller than the constraint so it is ok.

Finally we tried to decrease the number of the bits used (wrt tthe Thd constraint) how it failed because using a 7 bit model we dont respect the limitation, therefore the fir will be implemented in VHDL with 8 bits dimension.



CHAPTER 3

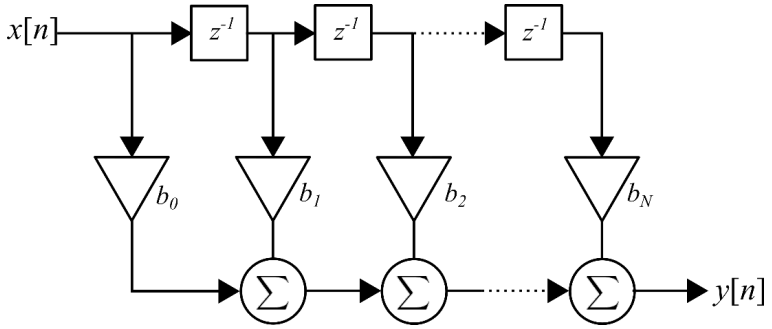
Basic FIR VHDL

3.1 VLSI

In this section we are going to implement a FIR model using VHDL , and then synthetised it and placed and routed and power estimation

3.2 implementation and architecture in vhdl

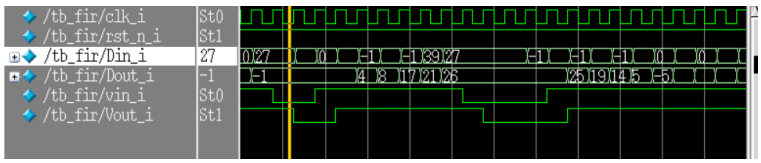
As used in the previous models , our VHDL filter will work on a 8 bit parallelism and will be of 8th grade.



The circuit accepts in input DIN(a sample per time) ,the 9 coefficients (H0.....H8), and the VIN (enable bit) , as output it has the result DOUT and the VOUT ('1' when data are ready to be sampled). Internally it s composed by different blocks :STAGE ,MULTIPLIER,ADDER,FD,REG. The component STAGE is used to compute the partial value of each coefficient , while MULTIPLIER and ADDER to compute the mathematics and the flip flop FD and the REG used to synchronize the values to be sampled in the right moment

3.3 Simulation

After implementing it , we have to pass to the next step: the simulation . In order to simulate it, we need a testbench that reads that samples.txt file and saves the results in the output.txt file . The testbench is composed by our FIR, clkgen.vhd, datasink.vhd and datamaker.vhd (the new files have been downloaded from the portale). clkgen.vhd creates the clock and establishes if the simulation is ended or not . datamaker.vhd reads the input file samples.txt datasink.vhd save the results in an output file



The vhdl model is equivalent to the C one because they have the same output files.

3.4 Synthesis

After creating the syn folder and the dcsetup file from the portale we can now start do the Synthesis . It has been created a script in order to do this step , As first step we have to compute the maximum frequency in order to get it we have to set the Period to zero and synthetize it . In this way , we can know estimate the maximum frequency and the related area . WE got a period of 2.56 ns . Combinational area: 2710.008005 Buf/Inv area: 119.966000 Noncombinational area: 438.368014 Total cell area: 3148.376020

After this step , we have to run the script again but using a period that is four time the minimum period .

Combinational area: 2557.324010 Buf/Inv area: 110.124001 Noncombinational area: 436.240014 Total cell area: 2993.564025

period of 10.24 ns

The script, finally, generates a .v and .sdc and .sdf and saved in the netlist folder.

3.5 switching activity based power consumption

In this section we will discuss about power consumption at frequency max over four . In the sim folder has been implemented a script named netlistsim that creates .vcd file to be saved in syn folder. in the saif folder there is a script to convert the .vcd file to a .saif file. Finally going back to the syn folder , there is script named laststep that reports the power information into a file (using the saif file)

Internal Switching Leakage Total Power Group Power Power Power Power (———————————————————————————— iopad 0.0000 0.0000 0.0000 0.0000 (0.00memory 0.0000 0.0000 0.0000 0.0000 (0.00blackbox 0.0000 0.0000 0.0000 0.0000 (0.00clocknetwork 0.0000 0.0000 0.0000 0.0000 (0.00register 0.0000 0.0000 0.0000 0.0000 (0.00sequential 61.3082 32.5404 7.2265e+03 101.0752 (11.27combinational 351.4474 376.4234 6.7847e+04 795.7197 (88.73———————————————————————————— Total 412.7556 uW 408.9639 uW 7.5074e+04 nW 896.7949 uW

3.6 PLACE AND ROUTE

In this section the topic will be place and route . First of all , we have to prepare the environment downloading designglobals and mmmcfile from the portale. after that we launch INNOVUS cadence to do the place and route . Following all the steps present in the description we finally got a fir.GateCount that includes area values.

Gate area 0.7980 um2 Level 0 Module myfir Gates= 3745 Cells= 1527 Area= 2988.5 um2

Last step we save the netlist (a verilog file) and firsdf used to compute the power .

3.7 Post place route power

In this section we will evaluate the power using Modelsim and Innovus Chasing the steps in the Document file we create a new script to be run by Modelsim and we got a power report. Whilst in Innovus using the .sdf file created before we can know estimate the power .

```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:        0.37781856            52.8577%
Total Switching Power:       0.27571636            38.5734%
Total Leakage Power:         0.06124930             8.5689%
Total Power:                 0.71478423
-----------------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                       0.06023     0.02764     0.00701     0.09488       13.27
Macro                                  0           0           0           0           0
IO                                     0           0           0           0           0
Combinational                    0.3176      0.2481     0.05424      0.6199       86.73
Clock (Combinational)                  0           0           0           0           0
Clock (Sequential)                     0           0           0           0           0
-----------------------------------------------------------------------------------------
Total                            0.3778      0.2757     0.06125      0.7148         100
-----------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
VDD                       1.1     0.3778      0.2757     0.06125      0.7148         100


-----------------------------------------------------------------------------------------
*       Power Distribution Summary:
*               Highest Average Power:  stages_7_add_add_18_U1_1 (FA_X1):         0.002597
*               Highest Leakage Power:           vout_2_out_1_reg (DFFR_X1):      8.621e-05
*               Total Cap:      8.69705e-12 F
*               Total instances in design:  1527
*               Total instances in design with no power:     0
*          Total instances in design with no activity:     0
*               Total Fillers and Decap:     0
```

CHAPTER 4

Advanced Fir

The goal of this step is to improve the performance of the Fir filter exploiting the 3 level - unfolding and the pipeline.

4.1 unfolding process

In order to exploit the unfolding we have to modify the architecture of the filter , using now 3 inputs as requested.

For this it has been computed analitically the expression of the 3 level unfolding :

$$y[3k] = B0x[3k] + B1x[3(k-1)+2] + B2x[3(k-1)+1] + B3x[3(k-1)] + B4x[3(k-2)+2] + \\ + B5[3(k-2)+1] + B6x[3(k-2)] + B7x[3(k-3)+2] + B8x[3(k-3)+1]$$

$$y[3k+1] = B0x[3k+1] + B1x[3k] + B2x[3(k-1)+2] + B3x[3(k-1)+1] + B4x[3(k-1)] + \\ + B5x[3(k-2)+2] + B6x[3(k-2)+1] + B7x[3(k-2)] + B8x[3(k-3)+2]$$

$$y[3k+2] = B0x[3k+2] + B1x[3k+1] + B2x[3k] + B3x[3(k-1)+2] + B4x[3(k-1)+1] + \\ + B5x[3(k-1)] + B6x[3(k-2)+2] + B7x[3(k-2)+1] + B8x[3(k-2)]$$

every addend is delayed to exploit the unfolding

4.2 Pipeline

This technique is used to improve the throughput reducing the longest path. The critical path is composed by 8 adders in a row plus a multiplication unity.

A first pipe level is added just after any multiplication , exploiting the feedforward cut-set rule .

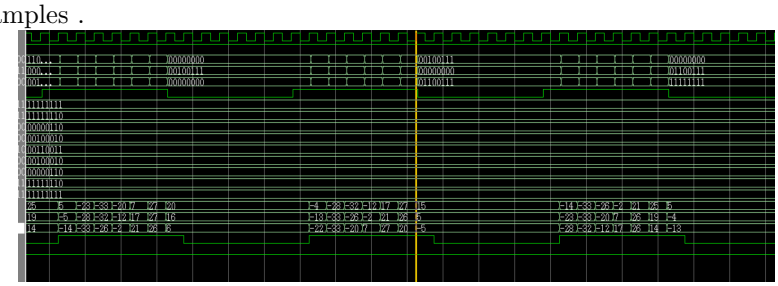
In this way , the longest path is decreased to the back-to-back 8 adders. After using , as suggested in the documentation , the Design Compiler we find out that there is a possible further improvement : adding a register between the the fourth and the fifth adders and adding a second level of pipe to the last 4 multiplications .

This lead to reduce the critical path to be the max among 4 adders , 1 mult, after a careful analysis it has found out that 1 mult is equal (more or less) , in a timing consideration, to 5 adders . So , the critical path is given by the multiplication unit.

4.3 Simulation

In order to implement the optimized filter in VHDL , it has been created 3 modules : STAGE1 ,SATGE2 ,STAGE3 . Each stage receives a triple of values and calculates an output : STAGE1 computes DOUT3N, STAGE2 computes DOUT3N+1, and finally STAGE3 DOUT3N+2.

Before and after the declaration of the three components there are registers to synchronize the samples .



a significant comparison to the standard Fir is that to complete the process, the basic needs more or less 2000 ns whilst the optimized one only 800ns.

4.4 Synthesis

In this section it will be considered the synthesis process . After setting the period to 0 , and running the script we find out that the minimum period is 1.41 ns . So the clock is faster than the one used in the standard one , but we have 2 drawbacks : the area and the power consumption increased .

Internal Switching Leakage Total Power Group Power Power Power Power (———————————————————————————— iopad 0.0000 0.0000 0.0000 0.0000 (0.00memory 0.0000 0.0000 0.0000 0.0000 (0.00blackbox 0.0000 0.0000 0.0000 0.0000 (0.00clocknetwork 0.0000 0.0000 0.0000 0.0000 (0.00register 0.0000 0.0000 0.0000 0.0000 (0.00sequential 344.2199 80.5487 4.1845e+04 466.6137 (21.25combinational 708.4887 804.2510 2.1686e+05 1.7296e+03 (78.75———————————————————————————— Total 1.0527e+03 uW 884.7997 uW 2.5871e+05 nW 2.1962e+03 uW

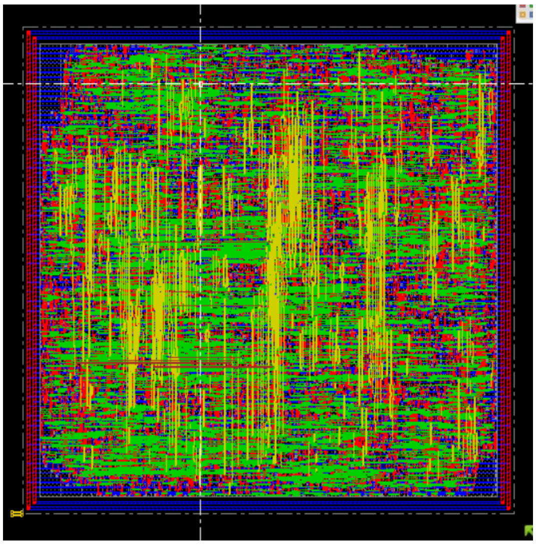
```
Number of ports:                         3192
Number of nets:                         11381
Number of cells:                         8017
Number of combinational cells:           7342
Number of sequential cells:               529
Number of macros/black boxes:               0
Number of buf/inv:                       1618
Number of references:                       9

Combinational area:               9690.912024
Buf/Inv area:                      932.862003
Noncombinational area:            2392.669913
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 12083.581937
```

4.5 Place and Route

In this section we repeat the same steps done in the basic fir place and route.



The data about area and power consumption are those :

Total Power ———————————————— Total Internal Power: 0.35132026 53.4937Total Switching Power: 0.24351373 37.0786Total Leakage Power: 0.06191630 9.4277Total Power: 0.65675029 ————————————————

Group Internal Switching Leakage Total Percentage Power Power Power Power (———————————————— Sequential 0.06212 0.02483 0.007773 0.09473 14.42 Macro 0 0 0 0 0 IO 0 0 0 0 0 Combinational 0.2892 0.2187 0.05414 0.562 85.58 Clock (Combinational) 0 0 0 0 0 Clock (Sequential) 0 0 0 0 0 ———————————————— Total 0.3513 0.2435 0.06192 0.6568 100 ————————————————

Rail Voltage Internal Switching Leakage Total Percentage Power Power Power Power (———————————————— VDD 1.1 0.3513 0.2435 0.06192 0.6568 100

———————————————— * Power Distribution Summary: * Highest Average Power: Add$_{7a}dd_18_U1_3(FA_X1) : 0.002697*HighestLeakagePower : Reg_in_reg_out_reg_{7(}DFFR_X1) : 8.621e{-}05*TotalCap : 8.43255e{-}12F*Totalinstancesindesign : 1523*Totalinstancesindesignwithnopower : 0*Totalinstancesindesignwithnoactivity : 0*TotalFillersandDecap : 0 -$

Gate area 0.7980 um$^2 Level0ModulemyfirGates = 13304Cells = 5474Area = 10616.9um^2$